Ordering number : ENA2160

LV8282PV

Bi-CMOS IC

CD/DVD-ROM/RW 4.5ch Driver

ON Semiconductor®

http://onsemi.com

Overview

LV8282PV is a system driver IC which incorporates driver circuits for CD/DVD player system on a single chip with 4 BTL type channels. It adopts 4 output and 5 control input method to use 4ch BTL for SLED and LOADING. When switched to LOADING mode, you can select a control reference voltage between IC internal voltage mode and external voltage (VREF input) mode. During LOADING operation, even if control reference voltage is not supplied, you can still operate the IC without any need for another supply voltage.
LV8282PV incorporates a pin to switch the operation of variable REG circuit independently. Therefore, this IC is suitable to use as regulator.
The dynamic range of this IC is wide with linear MOS technology.

Function

- Incorporated POWER AMP 4ch (BTL method 4ch)
- I_O MAX: 1A
- Incorporated level shift circuit (BTL method, incorporated in the entire 4ch)
- When BTL circuit of the 4th ch is in LOADING mode, you can select a control reference voltage between internal reference voltage mode and VREF (external voltage) mode.
- Incorporated variable regulator control circuit (which uses an external NPN-transistor. Voltage is set by an external resistor.)
- Incorporated ON/OFF switch function controllable independently by variable regulator
- Internal 5V regulator output pin
- Incorporated thermal shutdown protection circuit (TSD) (thermal shutdown protection signal output pin included)
- Incorporated charge pump

Specifications

Absolute Maximum Ratings at Ta = 25°C

Parameter	Symbol	Conditions	Ratings	Unit
Supply voltage	V_{CC} max		15.0	V
Output block supply voltage	VM max		15.0	V
Pre-drive voltage (gate voltage)	VG max	VG < VM+8.0V	21.0	V
Output current	I_O max1	1ch to 4ch	1.0	A
Allowable power dissipation 1	Pd max1	Independent IC	0.55	W
Allowable power dissipation 2	Pd max2	Mounted on a specified board *	1.65	W
Operating temperature range	Topr		-40 to +85	°C
Storage temperature	Tstg		-55 to +150	°C
Junction temperature	Tj max		+150	°C

* Mounted on a board : 76.1mm × 114.3mm × 1.6mm, glass epoxy board

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

Recommendation Operating Conditions at Ta = 25°C

Parameter	Symbol	Conditions	Ratings	Unit
Supply voltage 1	V_{CC}		5.5 to 13	V
Output block supply voltage 2	VM1, 2		5.5 to 13	V
Output current	I_O max2		0.8	A

Electrical Characteristics: circuit blocks shared in the system, at Ta = 25°C, V_{CC} = VM1 = VM2 = 8.0V VREF = 2.5V

Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
Quiescent current 1	$I_{CC}1$	Total current of V_{CC}+VM1+VM2		6.5	9.0	mA
Quiescent current 2	$I_{CC}2$	EN1, EN2 = L, SWREG = H Total current of V_{CC}+VM1+VM2		2.0	3.0	mA
Quiescent current 3	$I_{CC}3$	EN1, EN2 = L, SWREG = L Total current of V_{CC}+VM1+VM2	0		10	μA
VG pin						
Output voltage 1	VG1	VM1 = VM2 = 8V	VM+5.5	VM+8	VM+8.5	V
Overheat protection circuit						
Thermal shutdown temperature	TSD	Design target value	150		180	°C
Hysteresis width	ΔTSD	Design target value		25		°C
Signal output pin voltage	TSDO	Design target value: I_O = 0.5mA		0.2		V
EN 1, 2						
H level input voltage range	V_{ENH}		2.0		V_{CC}	V
L level input voltage range	V_{ENL}		0		0.6	V
Input current	I_{EN}	3.3V input	30	65	80	μA

BTL Block at (1 to 4ch) Ta = 25°C, V_{CC} = VM1 = VM2 = 8.0V VREF = 2.5V

Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
Drive block (BTL AMP)						
Reference voltage input range	VREFIN		1		3	V
V_{IN}						
Control input voltage range	V_{IN}		0		5	V
Output (V_O 1, 2, 3, 4+-)						
Output saturation voltage	VSAT	Total of saturation voltages of upper and lower output transistors at I_O = 0.2A (2.5Ω assumed for upper and lower transistors)		0.5	0.9	V
Offset voltage between outputs	VOFF	At load of 8Ω	-50		50	mV
Input-output voltage gain	VGAIN	At load of 8Ω	24.0	24.4	25.2	dB
Slew rate	SR	Design target value		1		V/μS
LOADING internal reference voltage	LVREF	LOADING mode (only 4ch)	1.55	1.65	1.75	V

Power Supply Block at Ta = 25°C, V_{CC} = VM1 = VM2 = 8.0V VREF = 2.5V

Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
5V Regulator block (REG 5)						
Output voltage	REG5	I_O = 0mA	4.8	5.0	5.3	V
Output current	IREGO				20	mA
Voltage to cancel the reduced-voltage protection voltage	LVSOFF		3.95	4.15	4.7	V
Voltage to enable the reduced-voltage protection	LVSON	All outputs OFF	3.4	3.6	3.85	V
External variable regulator control (REGO, FR)						
SWREG pin						
H level input voltage range	V_{SWH}	Variable REG block ON	2.0		V_{CC}	V
L level input voltage range	V_{SWL}	Variable REG block OFF	0		0.6	V
REGO						
Control output current	IREGO	SOUCE current	1.0	1.3	1.5	mA
Charge pump (CP, CPC, VG)						
Switching frequency 1	fcp	CPSW:0 to 0.9V	85	120	165	kHz
Switching frequency 2	fcp	CPSW:1.2 to 2.4V	110	145	190	kHz
Switching frequency 3	fcp	CPSW:2.7 to 3.9V	65	90	140	kHz
CPSW						
CPSW input voltage range	VCPSW		0		REG5	V
Charge pump stop voltage	CPSTOP		4.3		REG5	V
VG voltage limit						
VG voltage limit 1	VGLIM1	Normal voltage step-up limit	V_{CC}+7.0	V_{CC}+8	V_{CC}+8.5	V
VG voltage limit 2	VGLIM2	VG step-up maximum voltage limit			21	V

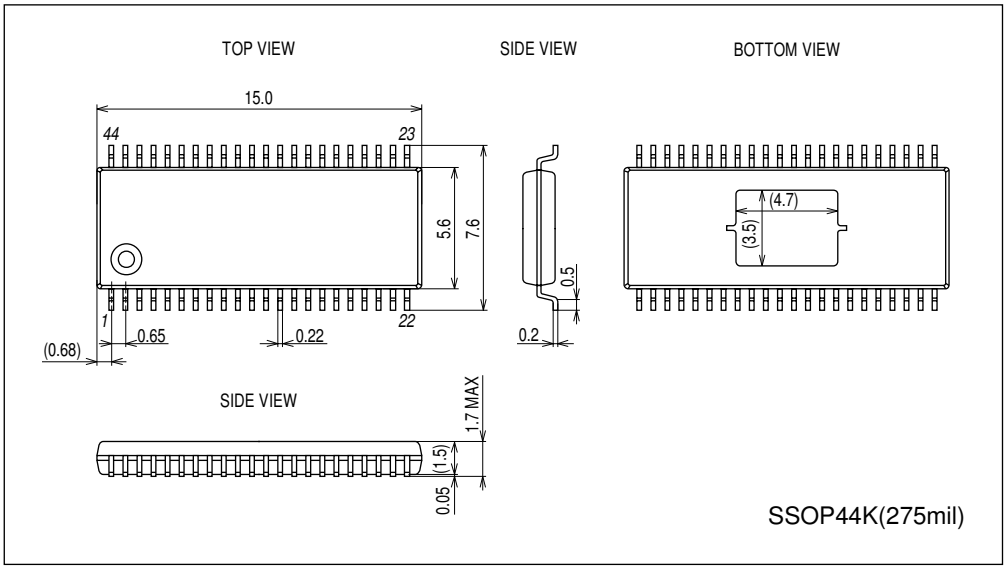
LV8282PV control truth value table

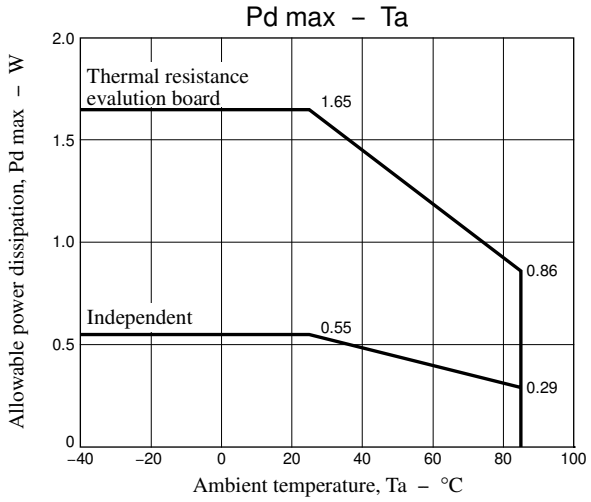
input			Drive channel				Remarks
EN1	EN2	SWREG	1,2ch	3ch	4ch	VREF (5VREG)	
H	H	*	ACTIVE	MUTE	ACTIVE	ACTIVE	4chBTL: Controlled w/IN5 (LD) External control reference (VREF) input
H	L	*	ACTIVE	ACTIVE	ACTIVE	ACTIVE	4chBTL:Controlled w/IN4 (SL) External control reference (VREF) input
L	H	*	MUTE	MUTE	ACTIVE	ACTIVE	4chBTL: Controlled w/IN5 (LD) Switches to internal control reference voltage (typ=1.65V)
L	L	H	MUTE	MUTE	MUTE	ACTIVE	
L	L	L	MUTE	MUTE	MUTE	MUTE	Standby mode

SWREG	Variable REG
H	ACTIVE
L	MUTE

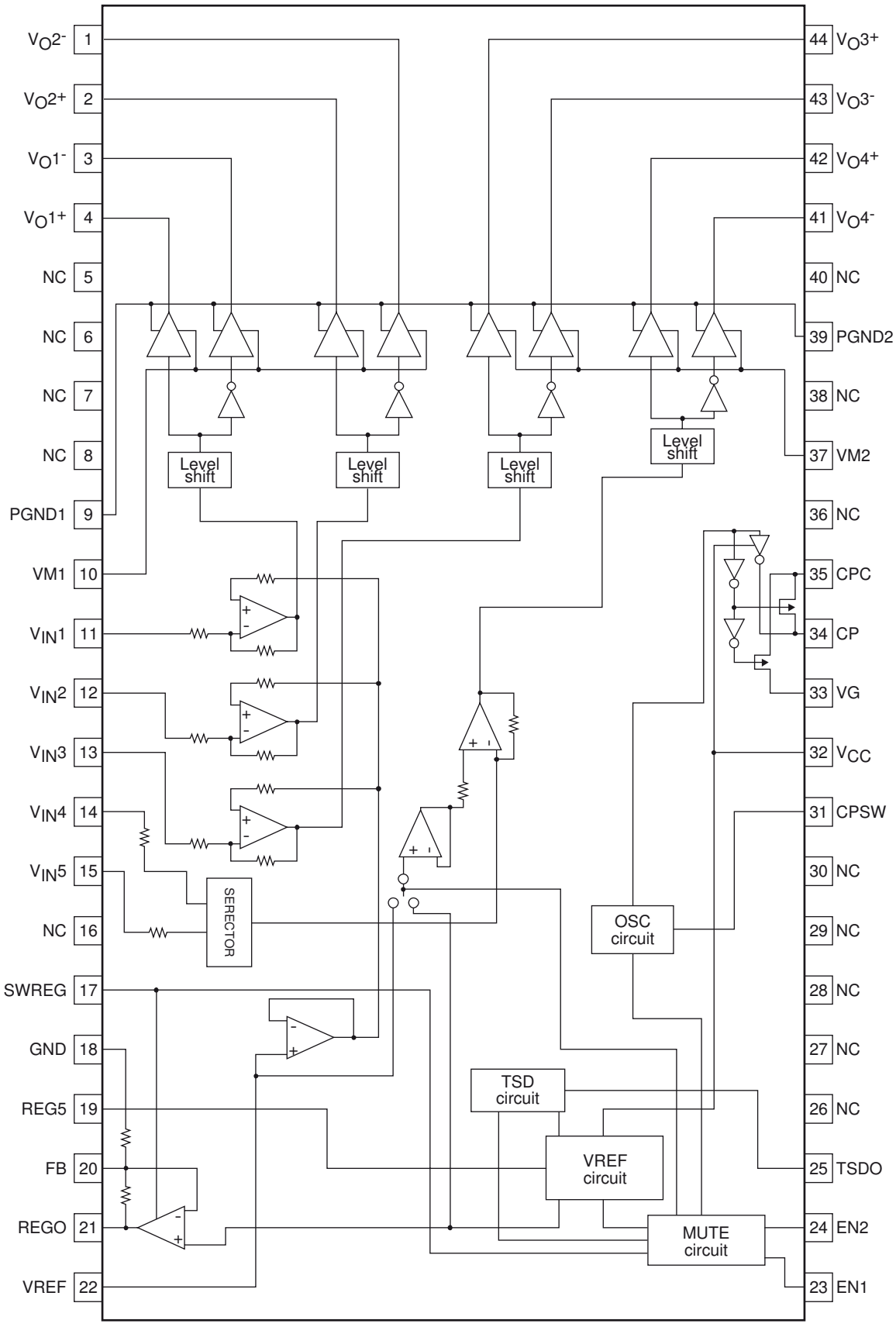
Package Dimensions

unit : mm (typ)
3333A

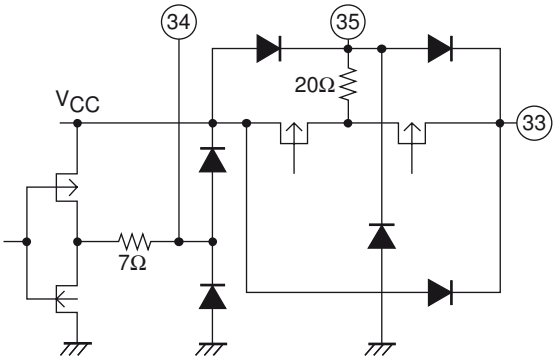
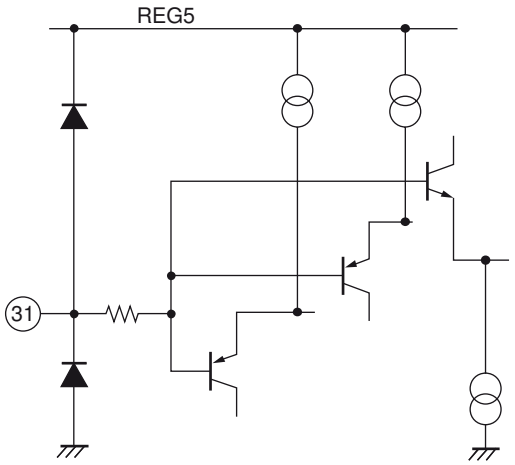
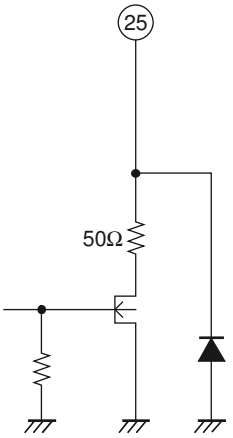
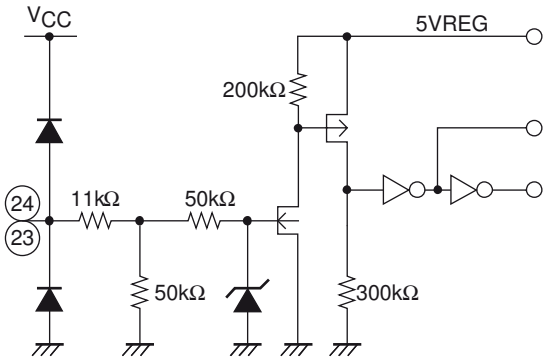




Block Diagram (Pin assignment Top view)



Pin Function

Pin No.	Pin name	Function	Equivalent circuit
35	CPC	Charge pump step-up pin. Make sure to connect a capacitor between CPC and CP (PIN11).	
34	CP	Charge pump step-up pin. Make sure to connect a capacitor between CP and CPC (PIN10).	
33	VG	Charge pump step-up output pin. Connect a capacitor between this pin and GND.	
32	V_{CC}	Small signal block power pin	
31	CPSW	Switching frequency switching pin for charge pump	
25	TSDO	Thermal Shutdown circuit operation output pin	
24 23	EN2 EN1	Control signal input pin	

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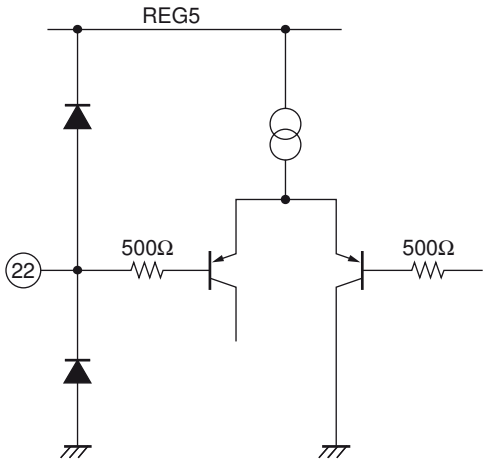
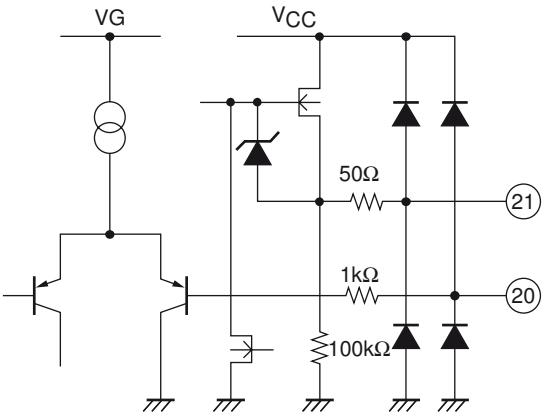
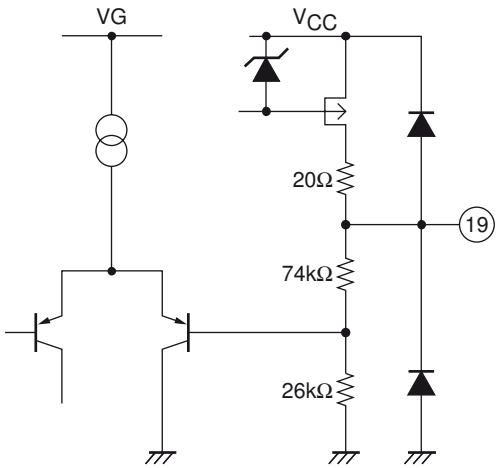
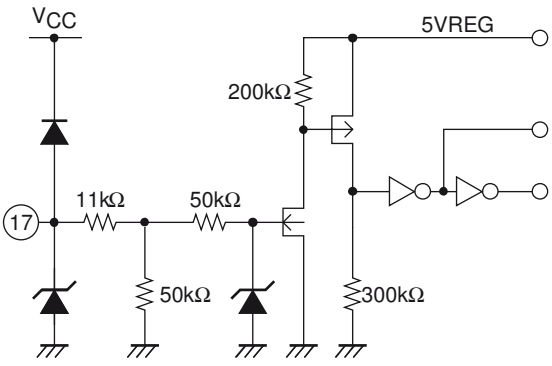
Pin No.	Pin name	Function	Equivalent circuit
22	VREF	VREF reference voltage input pin	
21 20	REGO FB	Regulator error amplifier output. Make sure to connect this pin to the base of the external NPN-transistor. Regulator error amplifier input.	
19	REG5	Internal regulator output pin	
18	GND	Small signal system circuit GND pin.	
17	SWREG	Regulator ON-OFF control pin	

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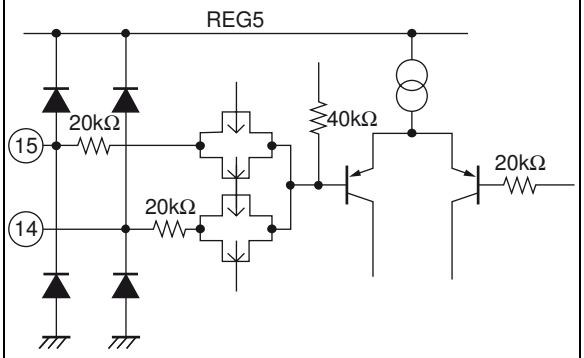
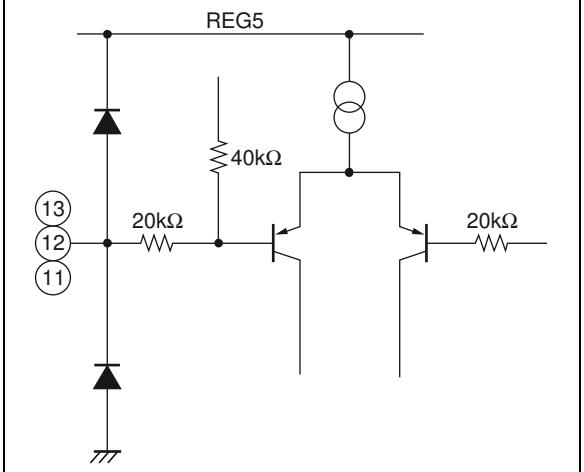
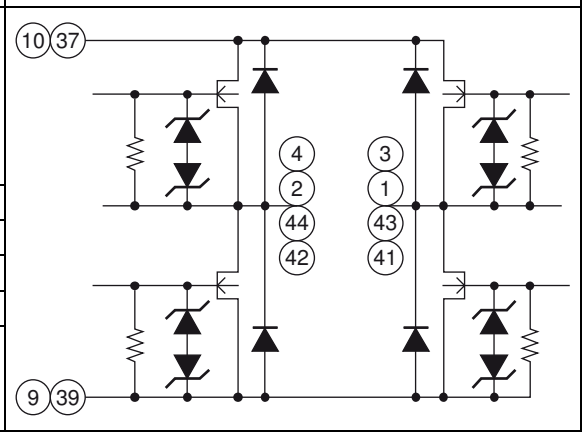
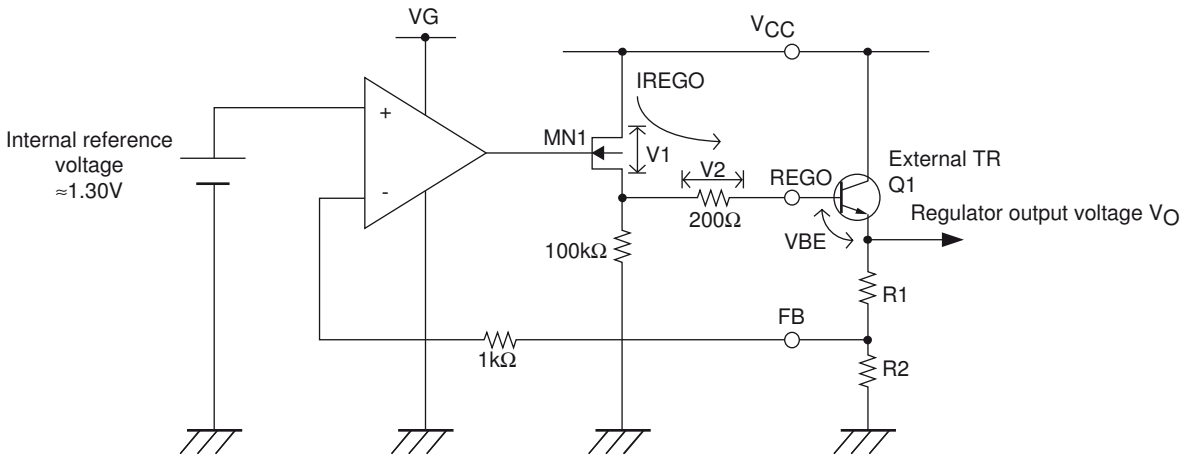
Pin No.	Pin name	Function	Equivalent circuit
15 14	$V_{IN}5$ $V_{IN}4$	• CH5 control signal input pin • CH4 control signal input pin	
13 12 11	$V_{IN}3$ $V_{IN}2$ $V_{IN}1$	• CH3 control signal input pin • CH2 control signal input pin • CH1 control signal input pin	
37 10 3, 4 1, 2 43, 44 41, 42 39 9	VM2 VM1 V_O1-/+ V_O2-/+ V_O3-/+ V_O4-/+ PGND2 PGND1	CH3, CH4 motor power supply pin CH1, CH2 motor power supply pin Make sure to connect a capacitor between GND and this pin. CH1 inverted/non-inverted output pin CH2 inverted/non-inverted output pin CH3 inverted/non-inverted output pin CH4 inverted/non-inverted output pin CH1, CH2, CH3, CH4 POWER GND pin	

LV8282 caution for use

1. Supply voltage of VM1 and VM2
   This IC is intended to be used under the following condition: VM1 = VM2 = V_{CC}. However, if you wish to use this IC with a different voltage, cautions are required.
   Make sure that power supply of VM2 (3ch, 4ch motor power supply) is the same as that of V_{CC}. If you supply different voltage to VM1 (1ch, 2ch motor power supply), the voltage should be as follows: VM2 = V_{CC} ≥ VM1
   Supply power to V_{CC} = VM2 first.
   Do not supply power to VM1 alone.

2. Variable regulator
   Variable Regulator ON-OFF control pin: SWREG is a gate input pin of Nch MOS. If this pin is open, the operation of variable regulator may be unstable. If by any possibility SWREG pin is set to open, countermeasure is required such as use of a pull-down resistor.

Variable regulator block

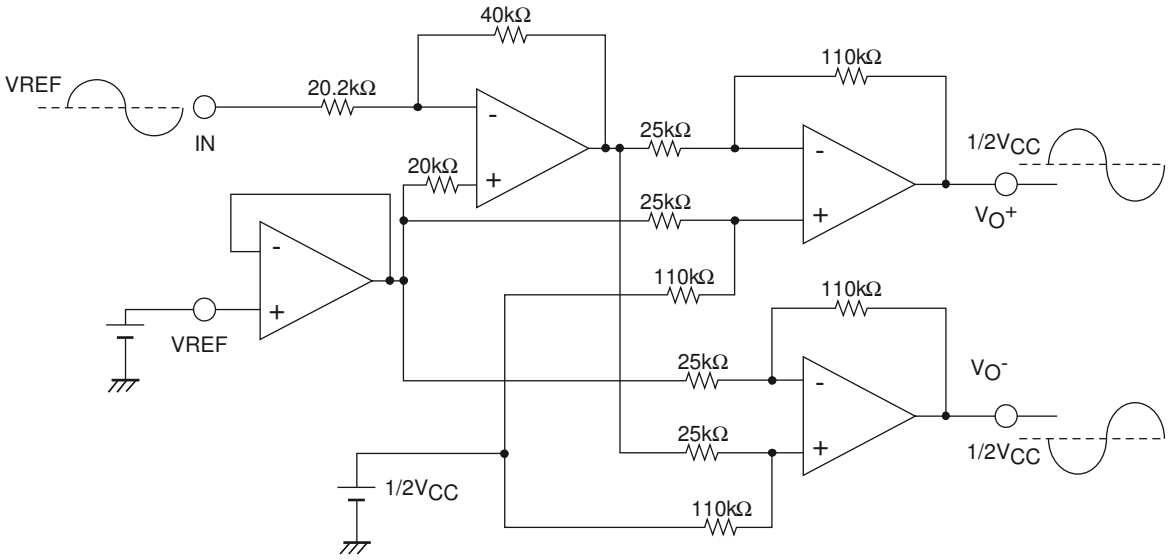


Regulator output voltage V_O = (R1/R2+1) × 1.3V

The maximum setting voltage of the regulator output voltage V_O is expressed as V_O max = V_{CC}-(VBE+V1+V2) as shown in the figure above. (Approximately, this is VBE+V1+V2 ≈ 1V. Since VBE varies depending on the output load and the external Q1 to be used, check it by means of an actual application.)

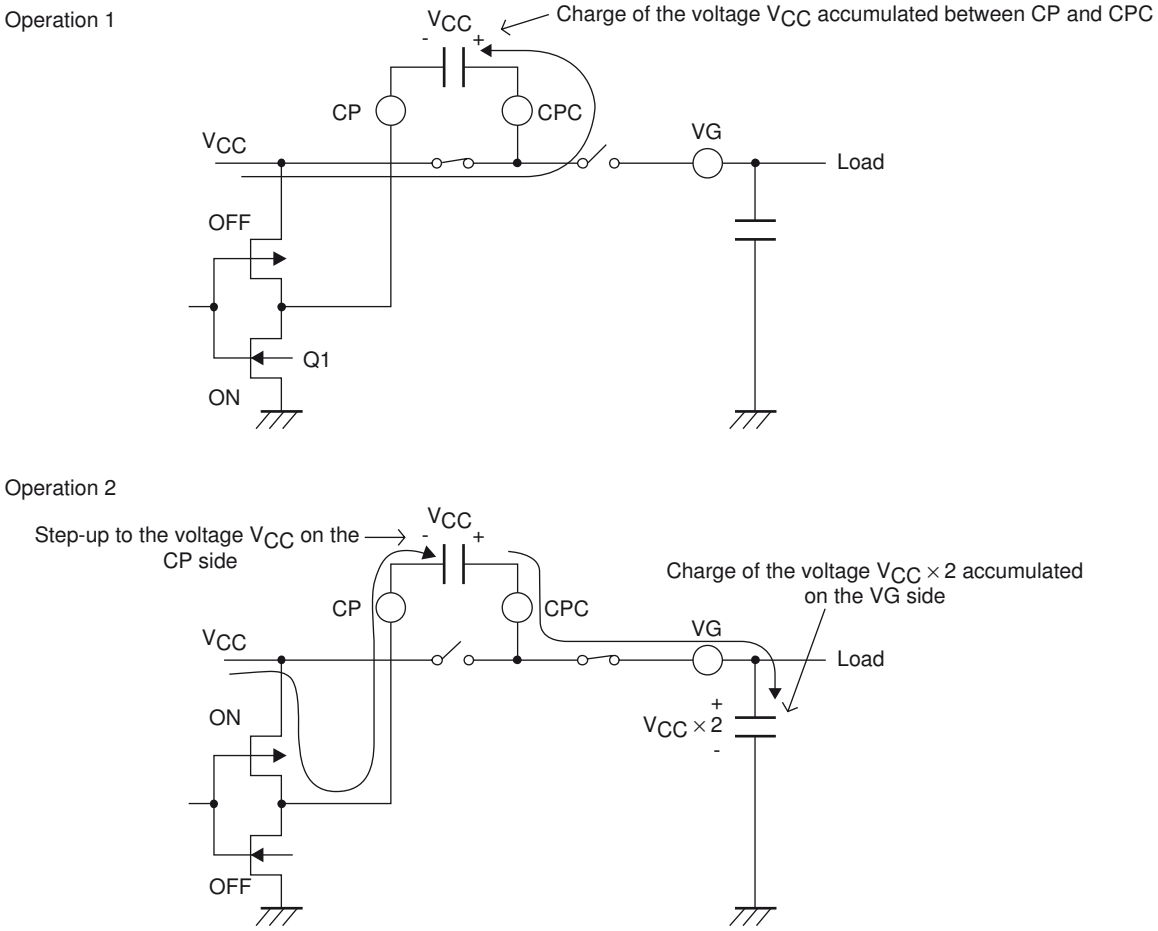
3. Timing of control signal input to EN1, EN2, and SWREG pins
   When supplying voltage (V_{CC}, VM) to LV8282, make sure to adjust the timing so that power is supplied to EN1, EN2 and SWREG after the voltage levels are set to “L” level.
   After power supply, make sure to perform control when the voltage is stabilized. (The time varies depending on V_{CC} of LV8282 and capacitor between VM and GND.)

4. Relationship of input and output and internal gain setting for LV8282 1, 2, 3 and 4ch



The signal phases of IN input and V_O+ output are the same.

5. Charge pump operation, and the VG voltage limit



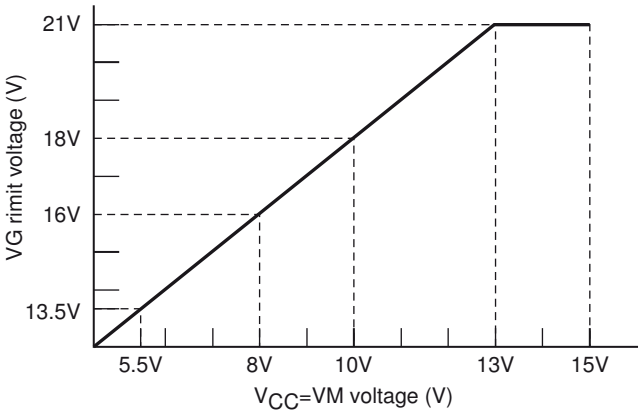
When the VG pin voltage reaches the set voltage, the operation 1 controls (reduces) ON-DUTY of transistor Q1, limiting the charge level of the capacitor. (When the VG pin voltage exceeds the set voltage, the step-up operation is stopped. This is called VG limit voltage)

In principle, V_{CC} voltage can be doubled and output to VG. However in general, the voltage becomes lower than the theoretical value depending on the load conditions. This is because of the loss due to the transistor ON resistance and the resistance of charge transfer switch.

ON/OFF of Q1 (switching frequency fcp: 120kHz: CPSW = 0V)

The relationship between the V_{CC} = VM voltage and the VG pin set voltage (VG limit voltage) is as follows.

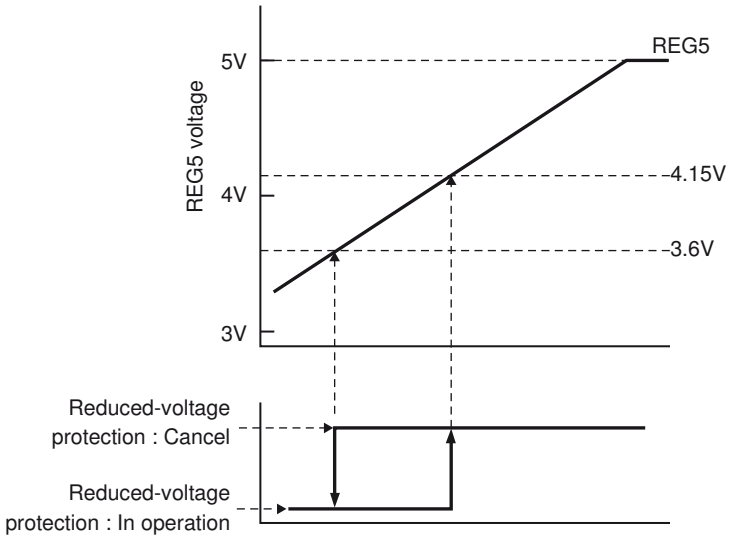
Correlation diagram brtween V_{CC}=VM and VG limit voltage



6. Reduced-voltage protection function (LVS)

When the voltage of internal regulator (REG5) is monitored and if the voltage is 3.6V (TYP) or lower, BTL output (V_O1, 2, 3, 4+-) and the external regulator (REGO) are turned off. When REG5 is 4.15V (typ) or higher, control is performed according to truth value table (p3).

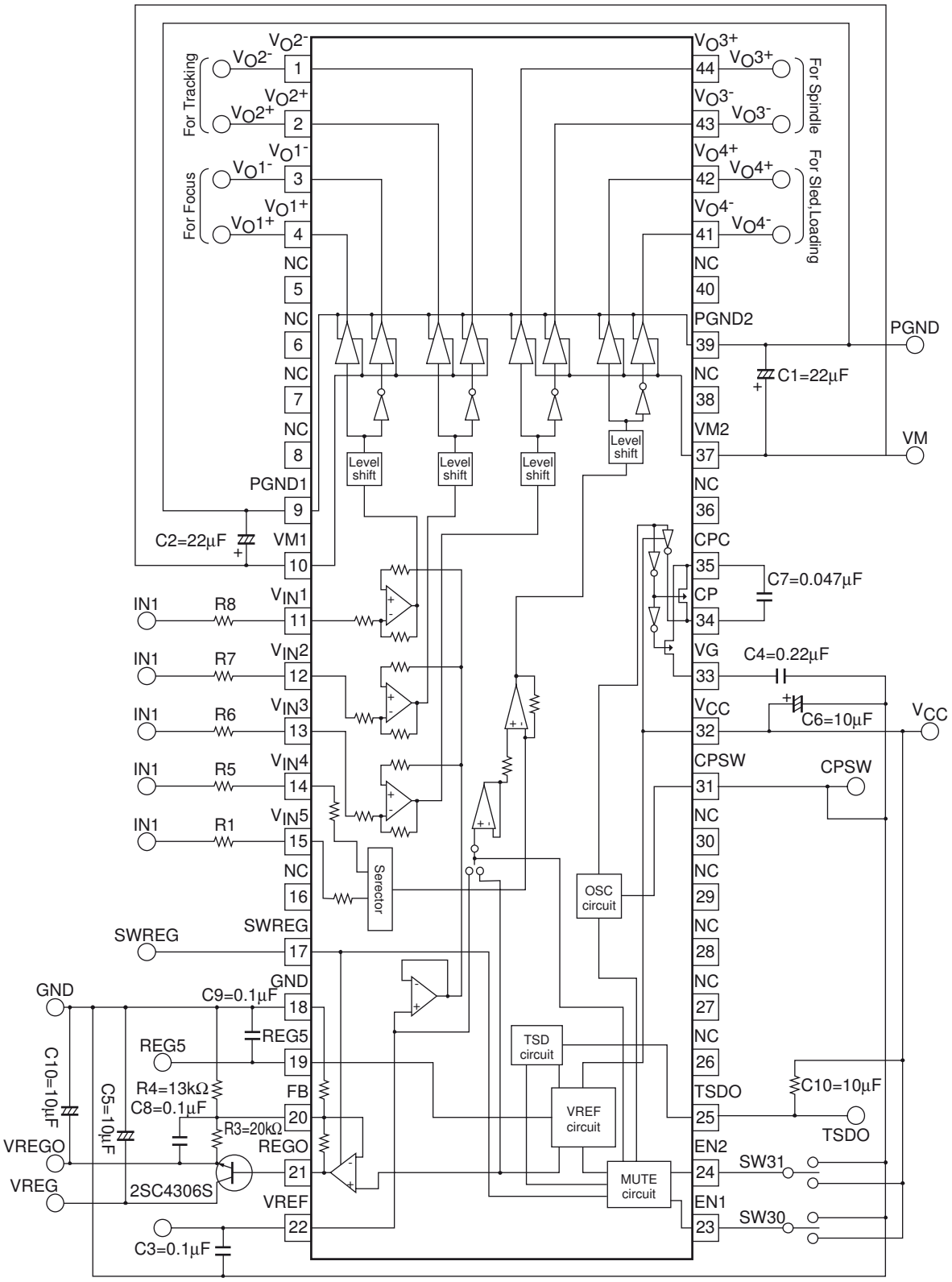
Correlation diagram brtween reduced-voltage protection operation and internal 5V regulator voltage (REG5)



7. TSD

When TSDO is used with pull-up resistor, during operation of thermal shutdown circuit, the voltage level is set to “L”. In this case, V_O1, 2, 3, 4+- output of CH1, 2, 3, 4 are turned off.
(REGO: external regulator control circuit is not turned off.)

Application Circuit Example



Regarding C4, C7 as shown in the example of application circuit, VG max voltage (21V) may be supplied due to V_{CC} (= VM1, 2). Hence, caution is required on withstanding voltage of the part for use.