Ordering number : ENN7813

SANYO Semiconductors

DATA SHEET

Bi-CMOS IC

# LV8224FN — Motor driver system in CD and MD players

## Overview

The LV8224FN is a system motor driver IC that implements all the motor driver circuits needed for CD and MD products. The LV8224FN provides a three-phase PWM spindle driver, a sled driver (either three-phase or PWM H bridge operation can be selected), and focus and tracking drivers (as two PWM H bridge driver channels). Since the LV8224FN uses BICDMOS devices, it can contribute to further miniaturization, thinner from factors, and lower power in end products.

The adoption of the direct PWM sensorless drive method for the spindle driver makes it possible to implement high-efficiency motor drive with few external parts.

## Functions

- PWM H bridge motor drivers (2 channels)
- Three-phase stepping motor driver, and direct PWM sensorless motor driver

## Specifications

### Absolute Maximum Ratings at Ta = 25°C

| Parameter | Symbol | Conditions | Ratings | Unit |
|---|---|---|---|---|
| Supply voltage | $V_{CC}$ max | | 5.0 | V |
| Output block supply voltage | $V_S$ max | | 4.5 | V |
| Predriver voltage (gate voltage) | $V_G$ max | | 6.5 | V |
| Output current | $I_O$ max | | 0.8 | A |
| Allowable power dissipation | Pd max1 | Independent IC | 0.35 | W |
| | Pd max2 | Mounted on a 50.0 × 50.0 × 0.8 mm glass epoxy PCB (reference value) | 1.10 | W |
| Operating temperature | Topr | | –30 to +85 | °C |
| Storage temperature | Tstg | | –55 to +150 | °C |

### Recommended Operating Conditions at Ta = 25°C

| Parameter | Symbol | Conditions | Ratings | Unit |
|---|---|---|---|---|
| Supply voltage | $V_{CC}$ | | 1.9 to 4.0 | V |
| Output block supply voltage | $V_S$ | | 0 to $V_G$ – 3.0 | V |
| Predriver voltage (gate voltage) | $V_G$ | | $V_S$ + 3 to 6.3 | V |




SANYO Electric Co.,Ltd. Semiconductor Company

TOKYO OFFICE Tokyo Bldg., 1-10, 1 Chome, Ueno, Taito-ku, TOKYO, 110-8534 JAPAN

## Electrical Characteristics at Ta = 25°C, $V_{CC}$ = 2.3 V

| Parameter | Symbol | Conditions | Ratings | | | Unit |
|---|---|---|---|---|---|---|
| | | | min | typ | max | |
| Current drain 1 | $I_{CC}1$ | S/S pin: high | | 1.0 | 1.5 | mA |
| Current drain 2 | $I_{CC}2$ | S/S pin: low (standby mode) | | | 20 | μA |
| [Charge Pump Output] | | | | | | |
| Output voltage | $V_G$ | | 5.4 | 5.9 | 6.2 | V |
| Actuator Block<br>[Position Detector Comparator Block] | | | | | | |
| Input offset voltage | $V_{AOFS}$ | | –9 | | +9 | mV |
| Common-mode input voltage range | $V_{ACM}$ | | 0 | | $V_{CC}$ | V |
| High-level output voltage | $V_{ACH}$ | $I_O$ = –0.5 mA | $V_{CC}$ – 0.5 | | $V_{CC}$ | V |
| Low-level output voltage | $V_{ACL}$ | $I_O$ = 0.5 mA | | | 0.5 | V |
| [Output Block] (OUT1F/R, OUT2F/R, and SUO to SWO pins) | | | | | | |
| SOURCE1 | Ron (H1) | $I_O$ = 0.5 A, $V_S$ = 1.2 V, $V_G$ = 6 V,<br>Forward transistor | | 0.4 | 0.6 | Ω |
| SOURCE2 | Ron (H2) | $I_O$ = 0.5 A, $V_S$ = 1.2 V, $V_G$ = 6 V,<br>Reverse transistor | | 0.4 | 0.6 | Ω |
| SINK | Ron (L) | $I_O$ = 0.5 A, $V_S$ = 1.2 V, $V_G$ = 6 V | | 0.4 | 0.6 | Ω |
| SOURCE + SINK | Ron (H+L) | $I_O$ = 0.5 A, $V_S$ = 1.2 V, $V_G$ = 6 V | | 0.8 | 1.2 | Ω |
| Output transmission delay time | $T_{RISE}$ | Design target value* | | 0.1 | 1.0 | μs |
| (H bridge) | $T_{FALL}$ | Design target value* | | 0.1 | 0.7 | μs |
| Minimum input pulse width<br>(H bridge) | tmin | With the channel 1 and channel 2 pulse widths ≥ 2/3 tmin, Design target value* | 200 | | | ns |
| [Decoder and Actuator Input Pins] (IN1F/R, IN2F/R, and S1 to S3 pins) | | | | | | |
| High-level input voltage range | $V_{IH}$ | | $V_{CC}$ – 0.5 | | $V_{CC}$ | V |
| Low-level input voltage range | $V_{IL}$ | | 0 | | 0.5 | V |
| High-level actuator input pin current | $I_{INH}$ | When the input pin voltage is 2.3 V | 9.5 | | 13 | μA |
| Low-level actuator input pin current | $I_{INL}$ | When the input pin voltage is 0 V | | | 1 | μA |
| [MUTE Pin] | | | | | | |
| High-level input voltage range | $V_{MUH}$ | MUTE OFF | $V_{CC}$ – 0.5 | | $V_{CC}$ | V |
| Low-level input voltage range | $V_{MUL}$ | MUTE ON | 0 | | 0.5 | V |
| High-level input pin current | $I_{MUTEH}$ | When the input pin voltage is 2.3 V | 9.5 | | 13 | μA |
| Low-level input pin current | $I_{MUTEL}$ | When the input pin voltage is 0 V | | | 1 | μA |

*: Design target value parameters are not tested.

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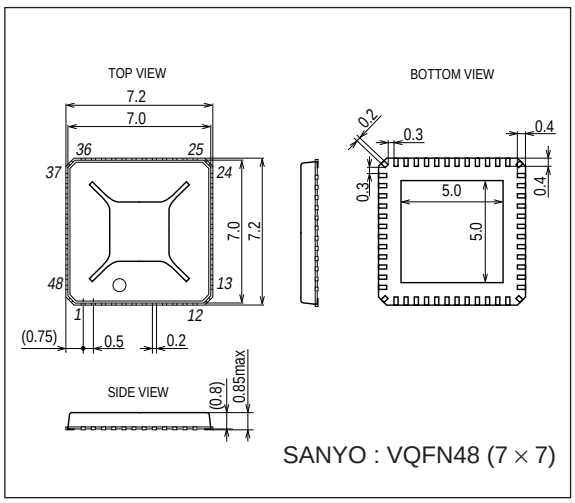
| Parameter | Symbol | Conditions | Ratings | | | Unit |
|---|---|---|---|---|---|---|
| | | | min | typ | max | |
| Spindle Motor Driver Block [Output Block] | | | | | | |
| SOURCE1 | Ron (H1) | $I_O$ = 0.5 A, $V_S$ = 1.2 V, $V_G$ = 6 V, Forward transistor | | 0.4 | 0.6 | Ω |
| SOURCE2 | Ron (H2) | $I_O$ = 0.5 A, $V_S$ = 1.2 V, $V_G$ = 6 V, Reverse transistor | | 0.4 | 0.6 | Ω |
| SINK | Ron (L) | $I_O$ = 0.5 A, $V_S$ = 1.2 V, $V_G$ = 6 V | | 0.4 | 0.6 | Ω |
| SOURCE + SINK | Ron (H+L) | $I_O$ = 0.5 A, $V_S$ = 1.2 V, $V_G$ = 6 V | | 0.8 | 1.2 | Ω |
| [Position Detector Comparator] | | | | | | |
| Input offset voltage | $V_{SOFS}$ | | –9 | | 9 | mV |
| [Startup Oscillator Pin] | | | | | | |
| OSC pin high-level voltage | $V_{OSCH}$ | | 0.85 | 1.05 | 1.25 | V |
| OSC pin low-level voltage | $V_{OSCL}$ | | 0.40 | 0.60 | 0.80 | V |
| [S/S Pin] | | | | | | |
| High-level input voltage range | $V_{SSH}$ | Start | $V_{CC}$ – 0.5 | | $V_{CC}$ | V |
| Low-level input voltage range | $V_{SSL}$ | Stop | 0 | | 0.5 | V |
| High-level input pin current | $I_{SSH}$ | When the input pin voltage is 2.3 V | 9.5 | | 13 | µA |
| Low-level input pin current | $I_{SSL}$ | When the input pin voltage is 0 V | | | 1 | µA |
| [BREAK Pin] | | | | | | |
| High-level input voltage range | $V_{BRH}$ | Brake off | $V_{CC}$ – 0.5 | | $V_{CC}$ | V |
| Low-level input voltage range | $V_{BRL}$ | Brake on | 0 | | 0.5 | V |
| High-level input pin current | $I_{BRKH}$ | When the input pin voltage is 2.3 V | 9.5 | | 13 | µA |
| Low-level input pin current | $I_{BRKL}$ | When the input pin voltage is 0 V | | | 1 | µA |
| [PWM Pin] | | | | | | |
| High-level input voltage range | $V_{PWMH}$ | | $V_{CC}$ – 0.5 | | $V_{CC}$ | V |
| Low-level input voltage range | $V_{PWML}$ | | 0 | | 0.5 | V |
| High-level input pin current | $I_{PWMH}$ | When the input pin voltage is 2.3 V | 9.5 | | 13 | µA |
| Low-level input pin current | $I_{PWML}$ | When the input pin voltage is 0 V | | | 1 | µA |
| PWM input frequency | $V_{PWMIN}$ | | | | 190 | kHz |
| [CLK Pin] | | | | | | |
| High-level input voltage range | $V_{CLKH}$ | | $V_{CC}$ – 0.5 | | $V_{CC}$ | V |
| Low-level input voltage range | $V_{CLKL}$ | | 0 | | 0.5 | V |
| High-level input pin current | $I_{CLKH}$ | When the input pin voltage is 2.3 V | 9.5 | | 13 | µA |
| Low-level input pin current | $I_{CLKL}$ | When the input pin voltage is 0 V | | | 1 | µA |
| [FG Output Pin] | | | | | | |
| High-level output voltage | $V_{FGH}$ | $I_O$ = –0.5 mA | $V_{CC}$ – 0.5 | | $V_{CC}$ | V |
| Low-level output voltage | $V_{FGL}$ | $I_O$ = 0.5 mA | | | 0.5 | V |

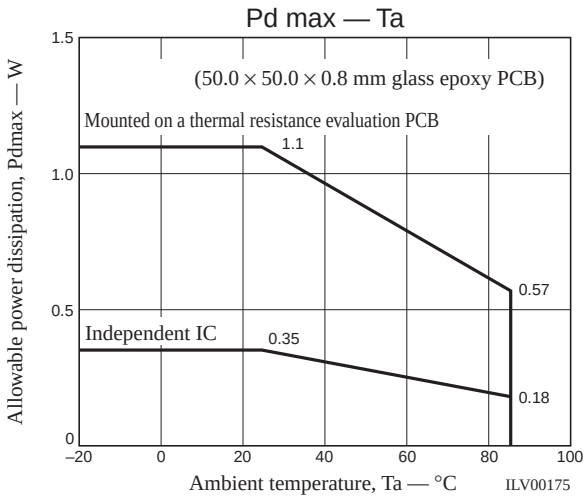
## Package Dimensions

unit : mm

3272




SANYO : VQFN48 (7 × 7)



## Actuator Truth Tables

### Focus and Tracking Blocks

| MUTE | IN1, 2F | IN1, 2R | OUT1, 2F | OUT1, 2R |
|---|---|---|---|---|
| H | L | L | L | L |
| H | H | L | H | L |
| H | L | H | L | H |
| H | H | H | L | L |
| L | × | × | Z | Z |

### Sled Drive Block Stepping Drive Mode (When the 3/H pin (pin 47) is high)

| MUTE | S1 | S2 | S3 | SUO | SVO | SWO |
|---|---|---|---|---|---|---|
| H | L | L | L | H | L | Z |
| H | H | L | L | H | Z | L |
| H | L | H | L | Z | H | L |
| H | H | H | L | L | H | Z |
| H | L | L | H | L | Z | H |
| H | H | L | H | Z | L | H |
| H | L | H | H | Z | Z | Z |
| H | H | H | H | Z | Z | Z |
| L | × | × | × | Z | Z | Z |

Z: Open

### Sled Drive Block H Bridge Drive Mode (When the 3/H pin (pin 47) is low)

| MUTE | S1 | S2 | SUO | SVO |
|---|---|---|---|---|
| H | L | L | L | L |
| H | H | L | H | L |
| H | L | H | L | H |
| H | H | H | L | L |
| L | × | × | Z | Z |

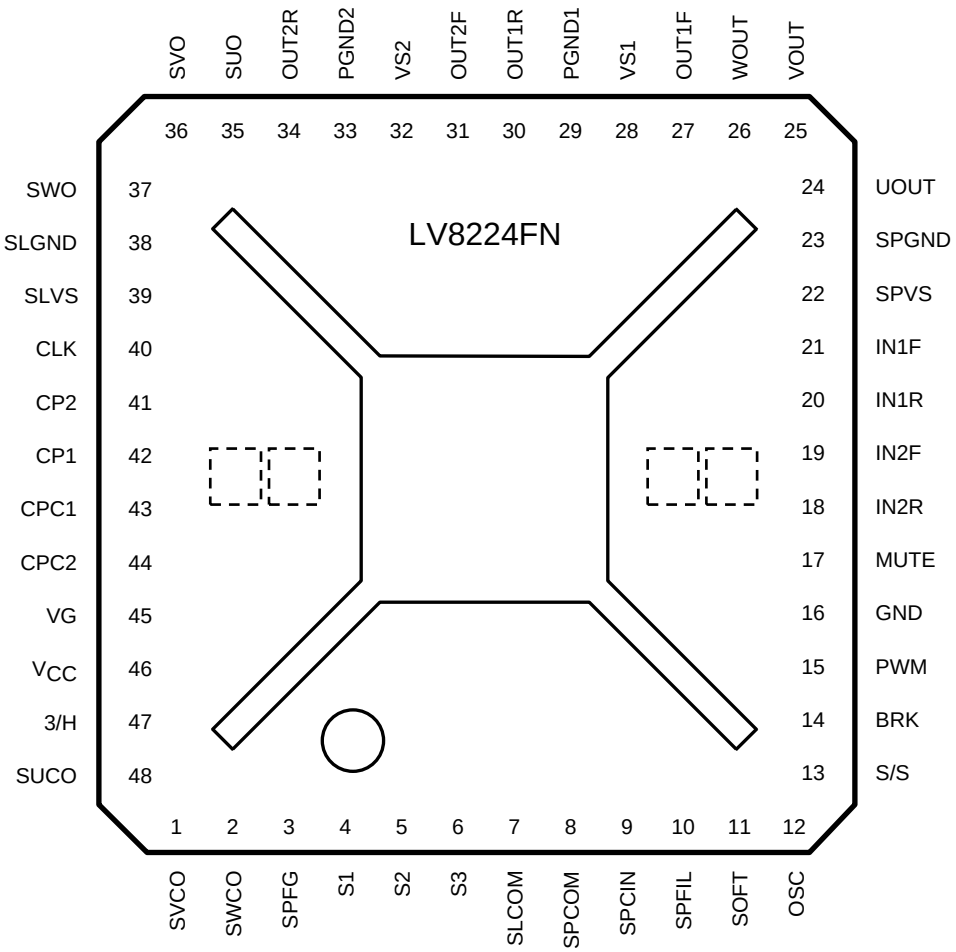
| MUTE | S3 | SWO |
|---|---|---|
| H | L | L |
| H | H | H |
| L | × | Z |

Z: Open

Notes:

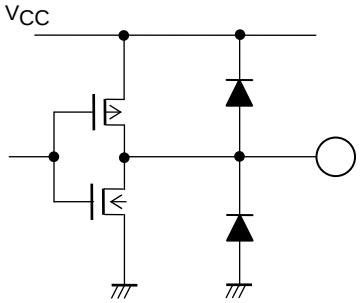
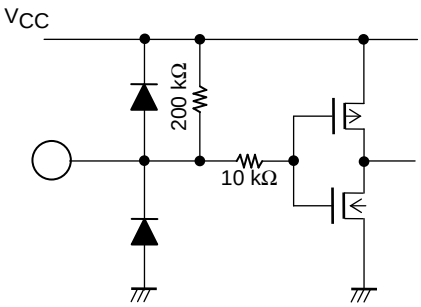
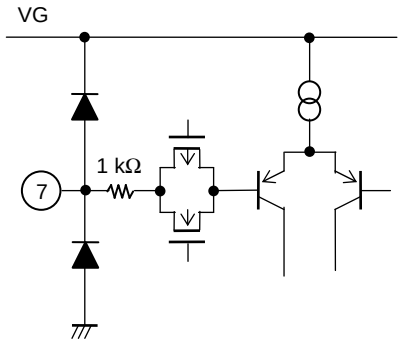
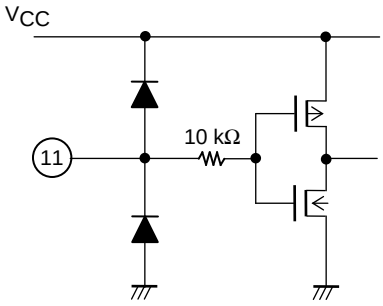
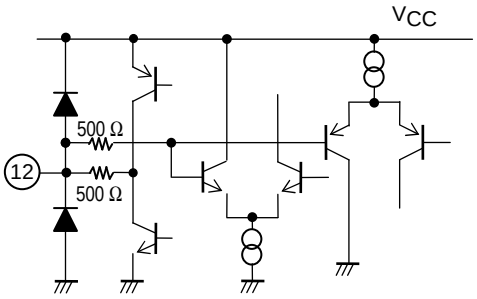
When the 3/H pin is set to select H bridge mode, SUO and SVO operate as PWM H bridge outputs according to the S1 and S2 inputs, and SWO operates as a half-bridge circuit output according to the S3 input.

**Pin Assignment** VQFN48 (7 × 7)




Top view

## Pin Functions

| Pin No. | Pin Name | Pin Description | Equivalent circuit |
|---|---|---|---|
| 48<br>1<br>2 | SUCO<br>SVCO<br>SWCO | Sled driver block position detector comparator outputs |  |
| 3 | SPFG | FG pulse output.<br>This pin outputs a three Hall sensor system equivalent pulse signal. | |
| 4<br>5<br>6 | S1<br>S2<br>S3 | Three-phase sled block logic inputs. Pins 35, 36, and 37 are the corresponding outputs. |  |
| 7 | SLCOM | Sled driver block position detector comparator common input |  |
| 11 | SOFT | Spindle driver block drive current waveform selection. Set this pin low when using a cored motor and high when using a coreless motor. |  |
| 12 | OSC | Startup oscillator connection. When this pin is connected to $V_{CC}$, the startup frequency will be equivalent to $f_{CLK}/4096$, and connected to ground, that frequency will be $f_{CLK}/3072$. If any other startup frequency is to be set, insert a capacitor between this pin and ground. The startup frequency can be set freely by changing the value of the capacitor. |  |

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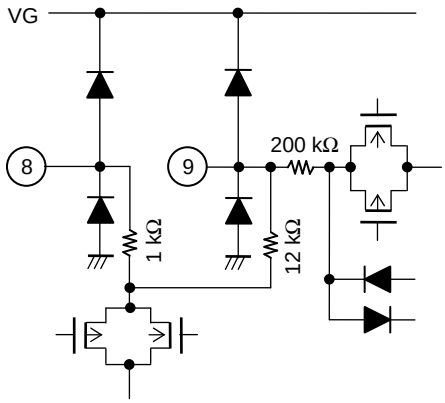
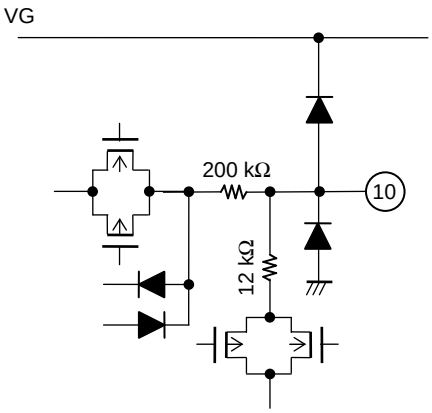
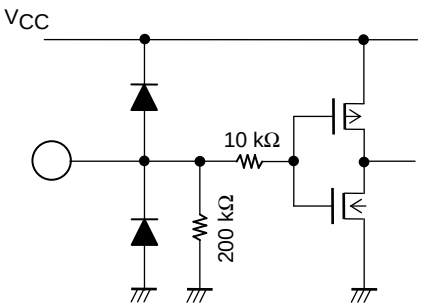
| Pin No. | Pin Name | Pin Description | Equivalent circuit |
|---|---|---|---|
| 8 | SPCOM | Spindle motor common point connection |   |
| 9 | SPCIN | Position detector comparator differential input. Insert a capacitor between this pin and the SPFIL pin (pin 10). | |
| 10 | SPFIL | Waveform synthesis signal filter connection. Insert a capacitor between this pin and the SPCIN pin (pin 9). |   |
| 13 | S/S | Spindle motor block start/stop control. A high-level input sets the block to start mode. |   |
| 14 | BRK | Spindle motor block braking control. A low-level input sets the block to reverse torque braking. | |
| 15 | PWM | PWM signal input. The output transistor is on when this input is high. | |
| 17 | MUTE | Muting control for the H bridge 1 and 2 blocks and the sled driver block. When a low level is input, these channel outputs all go to the high-impedance state. | |
| 21, 20 19, 18 | IN1F/R IN2F/R | Actuator H bridge block logic inputs | |
| 40 | CLK | Logic circuit operation reference clock input. Supply a frequency 32 times that of the spindle PWM frequency. | |
| 16 | GND | Small-signal system circuit ground | |

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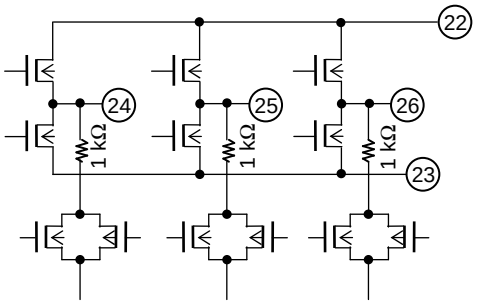
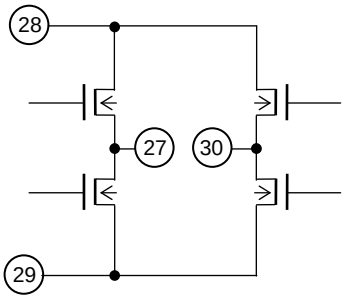
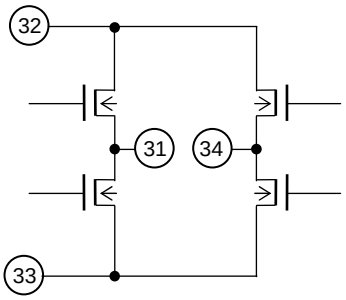
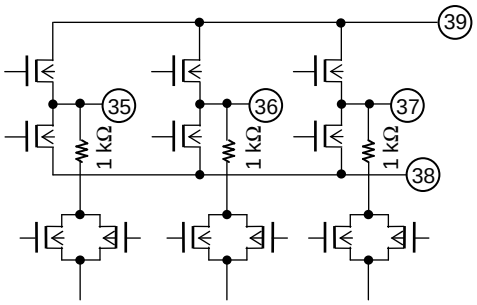
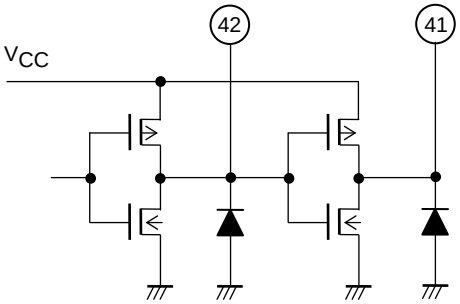
| Pin No. | Pin Name | Pin Description | Equivalent circuit |
|---|---|---|---|
| 22 | SPVS | Spindle motor drive power supply. Insert a capacitor between this pin and ground. |  |
| 24<br>25<br>26 | UOUT<br>VOUT<br>WOUT | Spindle driver outputs. Connect these pins to the spindle motor. | |
| 23 | SPGND | Spindle output block ground | |
| 28<br>27, 30<br>29 | VS1<br>OUT1F/R<br>PGND1 | H bridge 1 output block.<br>Insert a capacitor between the VS1 pin (pin 28) and ground. |  |
| 32<br>31, 34<br>33 | VS2<br>OUT2F/R<br>PGND2 | H bridge 2 output block.<br>Insert a capacitor between the VS2 pin (pin 32) and ground. |  |
| 39 | SLVS | Sled motor drive power supply.<br>Insert a capacitor between this pin and ground. |  |
| 35<br>36<br>37 | SUO<br>SVO<br>SWO | Sled driver outputs. Connect these pins to the sled motor. | |
| 38 | SLGND | Sled output block ground | |
| 42 | CP1 | Charge pump step-up pulse output. Insert a capacitor between this pin and the CPC1 pin (pin 43). Leave this pin open when using this circuit as a 2× step-up circuit. |  |
| 41 | CP2 | Charge pump step-up pulse output. Insert a capacitor between this pin and the CPC2 pin (pin 44). | |

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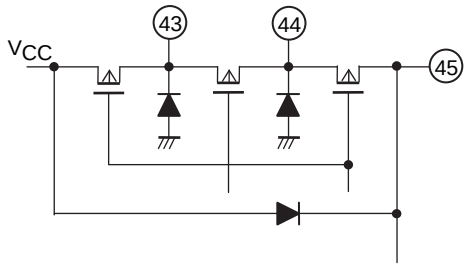
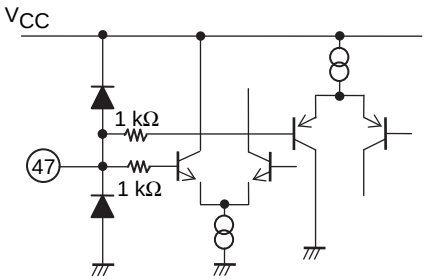
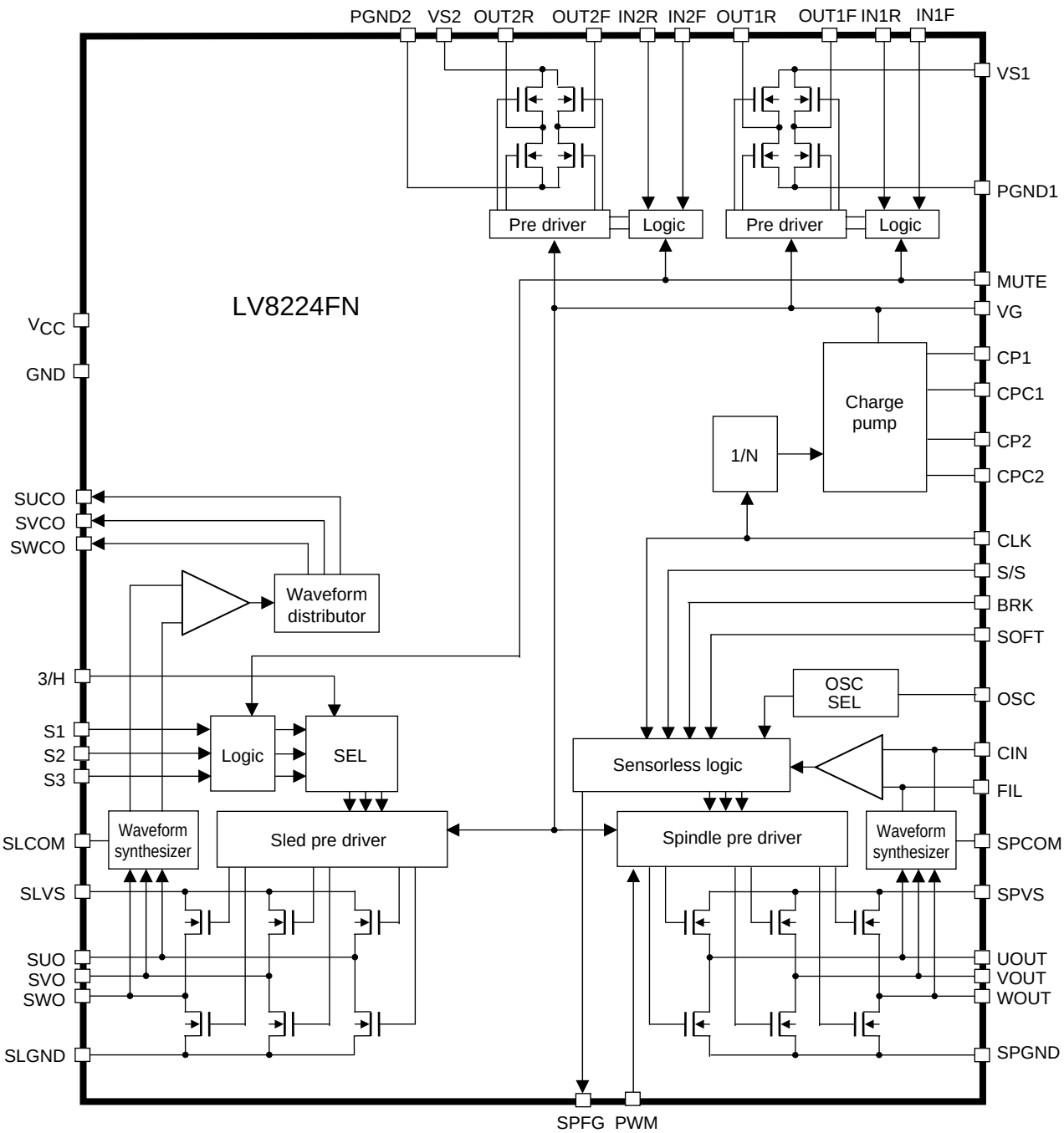
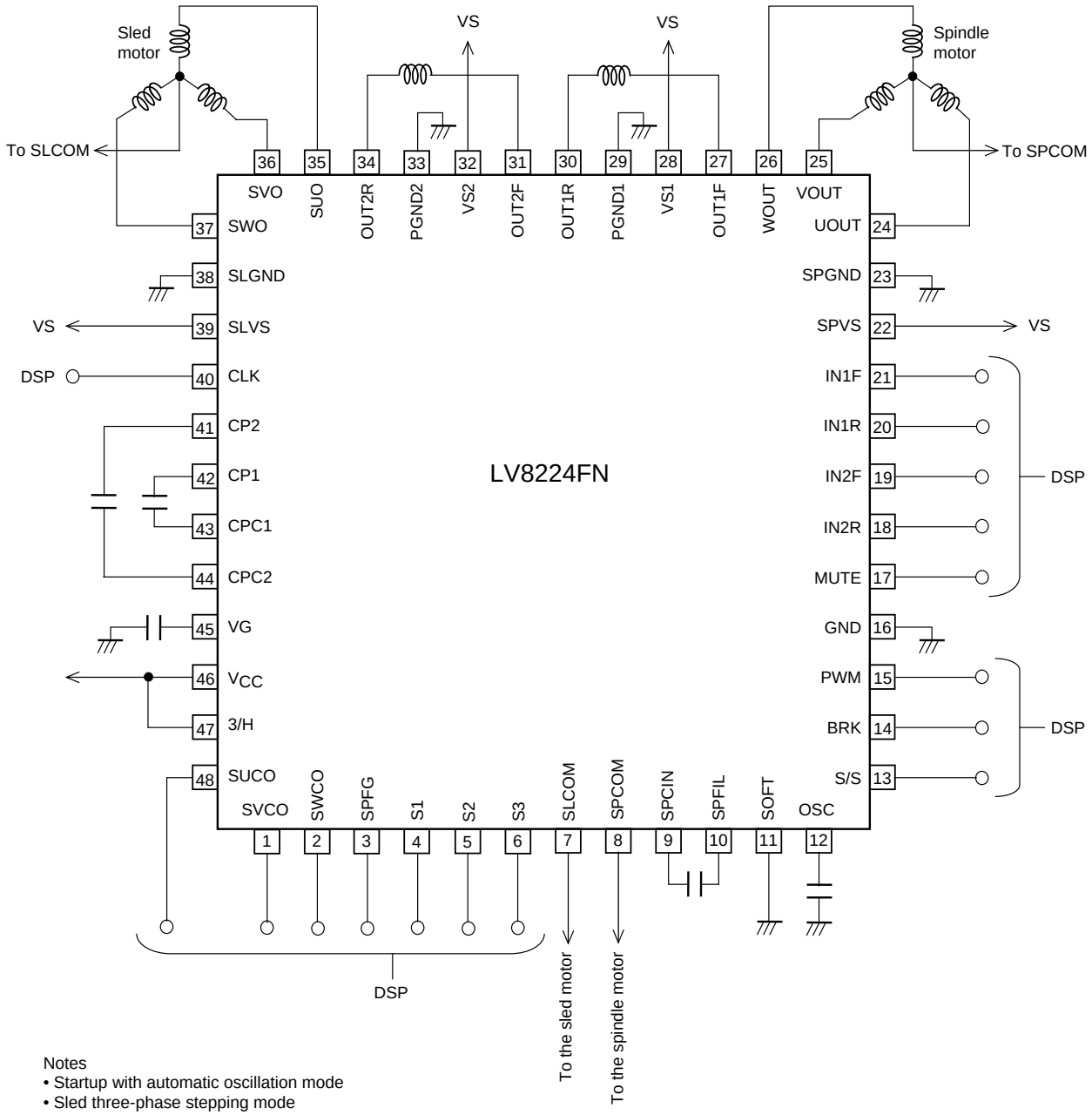
| Pin No. | Pin Name | Pin Description | Equivalent circuit |
|---|---|---|---|
| 43 | CPC1 | Charge pump step-up connection. Insert a capacitor between this pin and the CP1 pin (pin 42). |  |
| 44 | CPC2 | Charge pump step-up connection. Insert a capacitor between this pin and the CP2 pin (pin 41). | |
| 45 | VG | Charge pump stepped up voltage output.<br>Insert a capacitor between this pin and ground. | |
| 46 | $V_{CC}$ | Small-signal system power supply.<br>Insert a capacitor between this pin and ground. | |
| 47 | 3/H | Sled drive mode selection. A high-level input selects three-phase stepping mode, and a low-level input selects H bridge + half bridge mode. This pin must not be left open. |  |

## Block Diagram



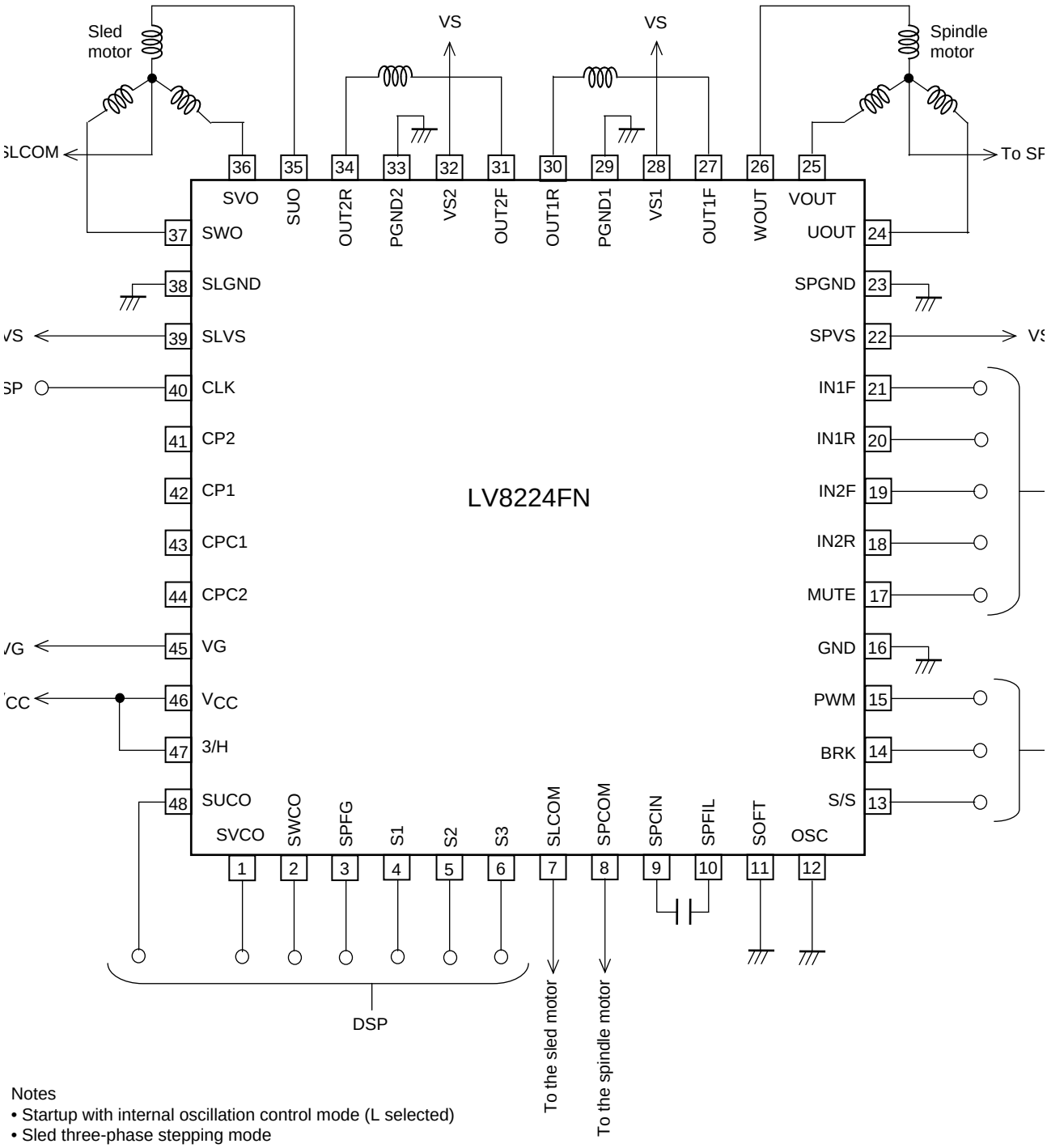
## Sample Application Circuit 1




Notes
- Startup with automatic oscillation mode
- Sled three-phase stepping mode
- Cored motor spindle motor mode

Capacitors must be inserted between each VS and PGND pair, and between each $V_{CC}$ and GND pair.

## Application Circuit Example 2




Notes
- Startup with internal oscillation control mode (L selected)
- Sled three-phase stepping mode
- Cored motor spindle motor mode
- Using an external stepped-up power supply

Capacitors must be inserted between each VS and ground, between each $V_{CC}$ and ground, and between each VG and ground.

## LV8224FN Functional Description and Notes on External Components

The LV8224FN is a system driver IC that implements, in a single chip, all the motor driver circuits required for CD and MD players. Since the LV8224FN provides a spindle motor driver (three-phase PWM sensorless drive), a sled stepping motor driver that supports either three-phase stepping or PWM H bridge drive, and two PWM H bridge drivers for the focus and tracking blocks, it can contribute to thinner form factors and further miniaturization in end products. Since the spindle motor driver uses a direct PWM sensorless drive technique, it achieves high-efficiency motor drive with a minimal number of external components.
Read the following notes before designing driver circuits using the LV8224FN to design a system with fully satisfactory characteristics.

### Output Drive Circuit and Speed Control Methods

The LV8224FN adopts the synchronous commutation direct PWM drive method to minimize power loss in the output circuits. Low on-resistance DMOS devices (total high and low side on-resistance: 0.8 Ω, typical) are used as the output transistors.
The spindle motor driver speed is controlled by BRK and PWM signals provided by an external DSP. The PWM signal controls the sink side transistor. That transistor is switched according to the input duty of the signal input to the PWM pin (pin 15) to control the motor speed. (The sink side transistor is on when the PWM input is high, and off when the PWM input is low.)
The LV8224FN also uses variable duty soft switching to achieve quieter motor drive.

### Soft Switching Mode Selection

The LV8224FN spindle drive block uses variable PWM duty soft switching to reduce motor drive noise. The SOFT pin (pin 11) selects the soft switching drive mode, that is, it selects different conditions for optimally quiet drive depending on the motor structure (coil inductance). Set the SOFT pin to the high level for coreless motors (motors with a low inductance) and to the low level for cored motors (motors with a high inductance) for optimal soft switching.
Although the SOFT pin has an MOS input circuit, it does not have a built-in pull-up or pull-down resistor, and thus must be set to the high or low level. This pin must not be left open.

### S/S and MUTE Circuits

The S/S pin (pin 13) functions as the spindle motor driver's start/stop pin; a high-level input specifies that the operation is in the start state. The MUTE pin (pin 17) operates on all driver blocks other than the spindle block; a low-level input mutes these outputs. In the muted state, the corresponding drivers (H bridge and three-phase sled drivers) all go to the high-impedance state, regardless of the states of the logic inputs. Since the S/S and MUTE pins operate independently, low-level inputs must be applied to both the S/S and MUTE pins to set the IC to the standby state (power saving mode).

### Braking Circuit

The BRK pin (pin 14) switches the direction of the torque applied by the spindle motor driver; when a low level is applied to the BRK pin, the driver switches to reverse torque braking mode. When the motor decelerates to an adequately low speed in reverse torque braking mode, the driver switches to short-circuit braking mode to stop the motor. (Note: the IC cannot be set to low-power mode at this time.)

### Notes on the CLK and PWM Signals

The LV8224FN CLK pin (pin 40) is used as the sensorless logic reference clock, for step-up circuit pulse generation, and for other purposes. Therefore, the CLK signal must be supplied at all times when the LV8224FN is in start mode. The CLK input signal must have a frequency 32 times that of the PWM input signal. We recommend that the CLK input frequency be less than 6 MHz.

### FG Output Circuit

The SPFG pin (pin 3) is the spindle block FG output. It outputs a pulse signal equivalent to a three Hall sensor FG output. This output has an MOS circuit structure.

Spindle Block Position Detector Comparator Circuit

The spindle block position detection comparator circuit is provided to detect the position of the rotor using the back EMF generated when the motor turns. The IC determines the timing with which the output block applies current to the motor based on the position information acquired by this circuit. Startup problems due to comparator input noise can be resolved by inserting a capacitor (about 1000 to 4700 pF) between the SPCIN pin (pin 9) and the SPFIL pin (pin 10). Note that if this capacitor is too large, the output commutation timing may be delayed at higher speeds and efficiency may be reduced.

OSC Circuit

The OSC pin (pin 12) is an oscillator pin provided for sensorless motor startup commutation. The LV8224FN provides two main clock dividing modes and a self-oscillation mode.
The main clock division modes are selected by setting the OSC pin to either $V_{CC}$ or ground. The startup frequency is created by dividing the signal input to the CLK pin (pin 40), and is either CLK/4096 (when the OSC pin is connected to $V_{CC}$) or CLK/3072 (when the OSC pin is connected to ground). Self-oscillation mode is set up by inserting a capacitor between the OSC pin and ground. When self-oscillation mode is selected, the OSC pin starts self-oscillating, and that frequency becomes the startup frequency. The oscillator frequency can be adjusted by changing the value of the external capacitor (reducing the value of the capacitor increases the startup frequency).
The number of external components can be reduced if there are no problems with the startup characteristics when the OSC pin is connected to either $V_{CC}$ or ground. However, if there are problems, select self-oscillation mode and select a value of the capacitor that provides optimal startup characteristics.

Charge Pump Circuit

The LV8224FN n-channel DMOS output structure allows it to provide a charge pump based voltage step-up circuit. A voltage 3 times the $V_{CC}$ voltage (or about 6.0 V) can be acquired from the VG pin (pin 45) by inserting capacitors (recommended value: 0.1 µF or larger) between the CP1 (pin 42) and CPC1 (pin 43) pins and between the CP2 (pin 41) and CPC2 (pin 44) pins. We recommend using this circuit with values such that the voltage relationship between the stepped-up voltage (VG) and the motor supply voltage (VS) is VG – VS ≥ 3.0 V. Note that this circuit is designed so that the stepped-up voltage (VG) is clamped at about 6.0 VDC. A larger capacitor must be used on the VG pin if the ripple on the stepped-up voltage (VG) results in VGmax exceeding 6.5 V.
Observe the following points if the VG voltage is supplied from external circuits.

- The VG voltage supplied from the external circuits must not exceed the absolute maximum rating VGmax.
- The capacitors between the CP and CPC pins (pins 41 to 44) are not required.
- There is an IC-internal diode between the $V_{CC}$ and VG pins. Therefore, supply voltages such that VCC > VG must never be applied to this IC.

Sled Driver

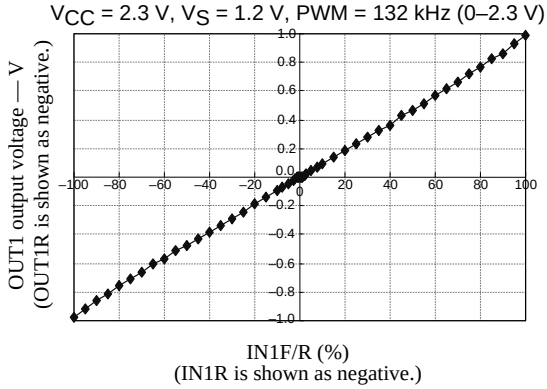
The LV8224FN sled driver block provides two output circuit structures: one appropriate for a three-phase motor and one appropriate for a DC motor. Connect the 3/H pin (pin 47) to $V_{CC}$ to set the block to use the three-phase sensorless drive structure, and connect the 3/H pin to ground to set the block to use the PWH H bridge drive structure. The S1 to S3 pins (pins 4 to 6) are the sled driver block control inputs, and the signals are supplied by the DSP. The S1 to S3 pins have built-in pull-up resistors.
The SUC0 to SWC0 pins (pins 48, 1, and 2) are the sled driver position detector comparator output pins. These signals are only output in three-phase stepping mode, and output the low-level potential in standby mode and PWM H bridge mode. These pins are used to feed back the sled motor speed and position information to the DSP or microcontroller.

Actuator Block

The LV8224FN incorporates two H bridge channels for use as actuator drivers for the focus and tracking systems. The logic input pin circuits incorporates pull-down resistors. A PWM signal is used for control, and the circuit supports synchronous commutation.
The OUT1F/R output (pins 27 and 30) is the output corresponding to the IN1F/R (pins 21 and 20) channel 1 control input, and the OUT2F/R output (pins 31 and 34) is the output corresponding to the IN2F/R (pins 19 and 18) channel 2 control input.
The figures show the dead band characteristics during motor control and the test circuit used for measuring those characteristics.

Actuator Small-Signal I/O Characteristics

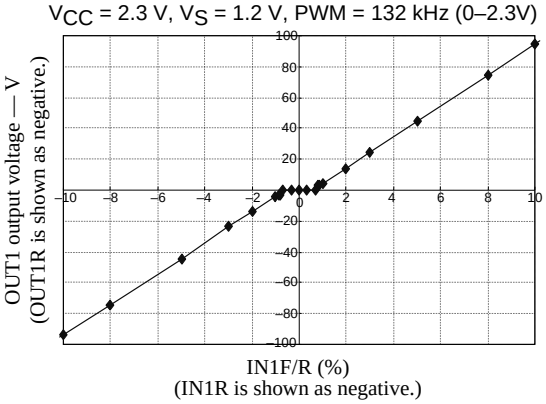
$V_{CC}$ = 2.3 V, $V_S$ = 1.2 V, PWM = 132 kHz (0–2.3 V)



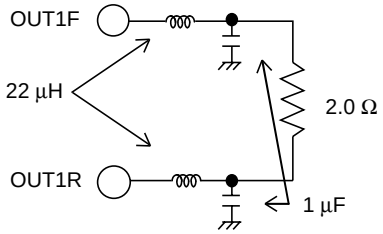

The output is passed through 22 μH inductors and smoothed with a low-pass filter consisting of a 2.0 Ω resistor and two 1 μF capacitors.

Actuator Small-Signal I/O Characteristics (magnified)

$V_{CC}$ = 2.3 V, $V_S$ = 1.2 V, PWM = 132 kHz (0–2.3V)




The output is passed through 22 μH inductors and smoothed with a low-pass filter consisting of a 2.0 Ω resistor and two 1 μF capacitors.




Notes on PCB Pattern Design

The LV8224FN is a system driver IC implemented in a Bi-DMOS process; the IC chip includes bipolar circuits, MOS logic circuits, and MOS drive circuits integrated on the same chip. As a result, extreme care is required with respect to the pattern layout when designing application circuits.

- Ground and $V_{CC}$/$V_S$ wiring layout
  The LV8224FN ground and power supply pins are classified as follows.
  Small-signal system ground pin → GND (pin 16)
  Large-signal system ground pins → PGND1 (pin 29), PGND2 (pin 33), SPGND (pin 23), SLGND (pin 38)
  Small-signal system power supply pin → $V_{CC}$ (pin 46)
  Large-signal system power supply pins → VS1 (pin 28), VS2 (pin 32), SPVS (pin 22), SLVS (pin 39)
  A capacitor must be inserted, as close as possible to the IC, between the small-signal system power supply pin (pin 46) and ground pin (pin 16).
  The large-signal system ground pins (PGND1, PGND2, SPGND, and SLGND) must be connected with the shortest possible lines, and furthermore in a manner such that there is no shared impedance with the small-signal system ground lines. Capacitors must also be inserted, as close as possible to the IC, between the large-signal system power supply pins (VS1, VS2, SPVS, and SLVS) and the corresponding large-signal system ground pins.

- Positioning the small-signal system external components
  The small-signal system external components that are also connected to ground must be connected to the small-signal system ground with lines that are as short as possible.

- Notes on components connected between IC pins
  External components connected between IC pins must be connected using the shortest lines possible.
  The capacitor between CP1 (pin 42) and CPC1 (pin 43)
  The capacitor between CP2 (pin 41) and CPC2 (pin 44)
  The capacitor between SPFIL (pin 10) and SPCIN (pin 9)