

# LV8139JA

## Sine wave PWM Drive, Pre drive IC, for Brushless Motor Drive

### Overview

The LV8139JA is a PWM system pre driver IC designed for three-phase brushless motors.

This IC reduces motor driving noise by using a high-efficiency, sine wave PWM drive type.

It incorporates a full complement of protection circuits and, by combining it with a hybrid IC in the STK611 or STK5C4 series, the number of components used can be reduced and a high level of reliability can be achieved. Furthermore, its power-saving mode enables the power consumption in the standby mode to be reduced to zero. This IC is optimally suited for driving various large-size motors such as those used in air conditioners and hot-water heaters.

### Features

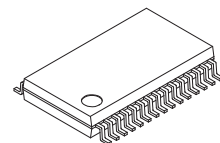
- Three-phase bipolar drive
- Sine wave PWM drive
- Drive phase setting function (Set 0-58 degrees 32 steps: There is an adjustment function corresponding to the CTL pin input)
- Supports power saving mode (power saving mode at CTL pin voltage of 0.95V (typ) or less;  $I_{CC} = 0\text{mA}$ , HB pin turned off)
- Supports bootstrap
- Automatic recovery type constraint protection circuit
- Forward/reverse switching circuit, Hall bias pin
- Current limiter circuit, low-voltage protection circuit, and thermal shutdown protection circuit
- FG1 and FG3 output (360-degree electrical angle/1 pulse and 3 pulses)

### Typical Applications

- Air Purifier
- Clothes Dryer
- Air conditioners
- Consumer

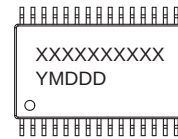


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SSOP30 (275mil)

### GENERIC MARKING DIAGRAM\*



XXXXX = Specific Device Code

Y = Year

M = Month

DDD = Additional Traceability Data

\*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "▪", may or may not be present.

### ORDERING INFORMATION

Ordering Code:  
LV8139JA-AH

Package  
SSOP30 (275mil)  
(Pb-Free / Halogen Free)

Shipping (Qty / packing)  
1000 / Tape & Reel

† For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.  
[http://www.onsemi.com/pub\\_link/Collateral/BRD8011-D.PDF](http://www.onsemi.com/pub_link/Collateral/BRD8011-D.PDF)

# LV8139JA

## Specifications

### Absolute Maximum Ratings at Ta = 25°C (Note 1)

| Parameter                   | Symbol                                       | Conditions                                     | Ratings     | Unit |
|-----------------------------|----------------------------------------------|------------------------------------------------|-------------|------|
| Supply voltage              | V <sub>CC</sub> max                          | V <sub>CC</sub> pin                            | 18          | V    |
| Output current              | I <sub>O</sub> max                           |                                                | 15          | mA   |
| Allowable power dissipation | Pd max1                                      | Independent IC                                 | 0.45        | W    |
|                             | Pd max2                                      | Mounted on a specified circuit board. (Note 2) | 1.05        | W    |
| CTL pin applied voltage     | V <sub>CTL</sub> max                         |                                                | 18          | V    |
| FG1,FG3 pin applied voltage | V <sub>FG1</sub> max<br>V <sub>FG3</sub> max |                                                | 18          | V    |
| Junction temperature        | T <sub>j</sub> max                           |                                                | 150         | °C   |
| Operating temperature       | T <sub>opr</sub>                             |                                                | -40 to +105 | °C   |
| Storage temperature         | T <sub>stg</sub>                             |                                                | -55 to +150 | °C   |

1. Stresses exceeding those listed in the Absolute Maximum Rating table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.  
2. Specified circuit board : 114.3mm × 76.1mm × 1.6mm, glass epoxy

### Recommendation Operating Range at Ta = 25°C (Note 3)

| Parameter                  | Symbol                              | Conditions | Ratings     | Unit |
|----------------------------|-------------------------------------|------------|-------------|------|
| Supply voltage range       | V <sub>CC</sub>                     |            | 9.5 to 16.5 | V    |
| VREG5 pin output current   | I <sub>REG</sub>                    |            | -10         | mA   |
| HB pin output current      | I <sub>HB</sub>                     |            | -30         | mA   |
| FG1,FG3 pin output current | I <sub>FG1</sub> , I <sub>FG3</sub> |            | 10          | mA   |

3. Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

### Electrical Characteristics at Ta = 25°C, V<sub>CC</sub> = 15V (Note 4)

| Parameter                                                                                                                                      | Symbol                | Conditions                                            | Ratings   |           |          | Unit  |
|------------------------------------------------------------------------------------------------------------------------------------------------|-----------------------|-------------------------------------------------------|-----------|-----------|----------|-------|
|                                                                                                                                                |                       |                                                       | min       | typ       | max      |       |
| Supply current 1                                                                                                                               | I <sub>CC1</sub>      |                                                       |           | 4         | 6        | mA    |
| Supply current 2                                                                                                                               | I <sub>CC2</sub>      | At stop (CTL < VIL1)                                  |           | 0         | 10       | μA    |
| <b>Output Block</b> (Pin HIN1, HIN2, HIN3, LIN1, LIN2 and LIN3)                                                                                |                       |                                                       |           |           |          |       |
| High level output voltage                                                                                                                      | V <sub>HO</sub>       | I <sub>O</sub> = -10mA                                | VREG-0.40 | VREG-0.25 |          | V     |
| Upper output ON resistance                                                                                                                     | R <sub>ONH</sub>      | I <sub>O</sub> = -10mA                                |           | 25        | 40       | Ω     |
| Low level output voltage                                                                                                                       | V <sub>LO</sub>       | I <sub>O</sub> = 10mA                                 |           | 0.15      | 0.25     | V     |
| Lower output ON resistance                                                                                                                     | R <sub>ONL</sub>      | I <sub>O</sub> = 10mA                                 |           | 15        | 25       | Ω     |
| Output leakage current                                                                                                                         | I <sub>Oleak</sub>    |                                                       |           |           | 10       | μA    |
| Bootstrap charge pulse width                                                                                                                   | T <sub>boot</sub>     |                                                       | 1.6       | 2.5       | 3.4      | μs    |
| Output minimum dead time                                                                                                                       | T <sub>dt</sub>       |                                                       | 1.6       | 2.5       | 3.4      | μs    |
| <b>5V Constant Voltage Output</b> (VREG5 pin)                                                                                                  |                       |                                                       |           |           |          |       |
| Output voltage                                                                                                                                 | VREG                  | I <sub>O</sub> = -5mA                                 | 4.7       | 4.9       | 5.1      | V     |
| Voltage fluctuation                                                                                                                            | ΔV (REG1)             | V <sub>CC</sub> = 9.5 to 16.5V, I <sub>O</sub> = -5mA |           |           | 100      | mV    |
| Load fluctuation                                                                                                                               | ΔV (REG2)             | I <sub>O</sub> = -5 to -10mA                          |           |           | 100      | mV    |
| <b>Hall Amplifier</b> (Pin IN1 <sup>+</sup> , IN1 <sup>-</sup> , IN2 <sup>+</sup> , IN2 <sup>-</sup> , IN3 <sup>+</sup> and IN3 <sup>-</sup> ) |                       |                                                       |           |           |          |       |
| Input bias current                                                                                                                             | I <sub>B</sub> (HA)   |                                                       | -1        |           | 0        | μA    |
| Common-mode input voltage range 1                                                                                                              | V <sub>ICM1</sub>     | When a Hall element is used                           | 0.3       |           | VREG-1.8 | V     |
| Common-mode input voltage range 2                                                                                                              | V <sub>ICM2</sub>     | Single-sided input bias mode (when a Hall IC is used) | 0         |           | VREG     | V     |
| Hall input sensitivity                                                                                                                         | V <sub>HIN</sub>      | Sine wave, Hall element offset = 0V                   | 80        |           |          | mVp-p |
| Hysteresis width                                                                                                                               | ΔV <sub>IN</sub> (HA) |                                                       | 15        | 30        | 45       | mV    |
| Input voltage Low → High                                                                                                                       | V <sub>SLH</sub>      |                                                       | 5         | 15        | 25       | mV    |
| Input voltage High → Low                                                                                                                       | V <sub>SHL</sub>      |                                                       | -25       | -15       | -5       | mV    |

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# LV8139JA

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| Parameter                                                              | Symbol                  | Conditions                                             | Ratings |      |                 | Unit |
|------------------------------------------------------------------------|-------------------------|--------------------------------------------------------|---------|------|-----------------|------|
|                                                                        |                         |                                                        | min     | typ  | max             |      |
| CSD Oscillator Circuit (CSD pin)                                       |                         |                                                        |         |      |                 |      |
| High level output voltage                                              | V <sub>OH</sub> (CSD)   |                                                        | 2.75    | 2.95 | 3.15            | V    |
| Low level output voltage                                               | V <sub>OL</sub> (CSD)   |                                                        | 0.85    | 1.05 | 1.25            | V    |
| Amplitude                                                              | V (CSD)                 |                                                        | 1.7     | 1.9  | 2.1             | Vp-p |
| External capacitor charging current                                    | ICHG1 (CSD)             | VCHG1 = 2.0V                                           | -14     | -10  | -6              | μA   |
| External capacitor discharging current                                 | ICHG2 (CSD)             | VCHG2 = 2.0V                                           | 6       | 10   | 14              | μA   |
| Lock detection ON/OFF time ratio                                       | LRT0                    | Drive OFF/drive ON                                     |         | 11   |                 |      |
| PWM Oscillator (PWM pin)                                               |                         |                                                        |         |      |                 |      |
| High level output voltage                                              | V <sub>OH</sub> (PWM)   |                                                        | 3.3     | 3.5  | 3.7             | V    |
| Low level output voltage                                               | V <sub>OL</sub> (PWM)   |                                                        | 1.3     | 1.5  | 1.7             | V    |
| Amplitude                                                              | V (PWM)                 |                                                        | 1.8     | 2.0  | 2.2             | Vp-p |
| Oscillation frequency                                                  | f (PWM)                 | C = 2200pF, R = 15kΩ<br>(design target value)          |         | 17.3 |                 | kHz  |
| Current Limiter Operation (RF pin)                                     |                         |                                                        |         |      |                 |      |
| Limiter voltage                                                        | VRF                     |                                                        | 0.225   | 0.25 | 0.275           | V    |
| Thermal Shutdown Protection Operation                                  |                         |                                                        |         |      |                 |      |
| Thermal shutdown protection operating temperature                      | TSD                     | Design target value (Note 5)<br>(junction temperature) | 150     | 175  |                 | °C   |
| Hysteresis width                                                       | ΔTSD                    | Design target value (Note 5)<br>(junction temperature) |         | 35   |                 | °C   |
| TH pin                                                                 |                         |                                                        |         |      |                 |      |
| Protection start voltage                                               | VTH                     |                                                        | 0.50    | 0.65 | 0.80            | V    |
| Hysteresis width                                                       | ΔVTH                    |                                                        | 0.32    | 0.42 | 0.52            | V    |
| HB pin                                                                 |                         |                                                        |         |      |                 |      |
| Output ON resistance                                                   | R <sub>ON</sub> (HB)    | IHB = -10mA                                            |         | 10   | 20              | Ω    |
| Output leakage current                                                 | I <sub>L</sub> (HB)     | Power saving mode V <sub>CC</sub> = 15V                |         |      | 10              | μA   |
| Low Voltage Protection Circuit (detecting V <sub>CC</sub> voltage)     |                         |                                                        |         |      |                 |      |
| Operation voltage                                                      | VSD                     |                                                        | 7.4     | 7.9  | 8.4             | V    |
| Hysteresis width                                                       | ΔVSD                    |                                                        | 0.35    | 0.5  | 0.65            | V    |
| FG1 FG3 Pin                                                            |                         |                                                        |         |      |                 |      |
| Output ON resistance                                                   | R <sub>ON</sub> (FG)    | IFG = 5mA                                              |         | 40   | 60              | Ω    |
| Output leakage current                                                 | I <sub>L</sub> (FG)     | VFG = 18V                                              |         |      | 10              | μA   |
| CTL Amplifier (drive mode)                                             |                         |                                                        |         |      |                 |      |
| Input voltage range                                                    | V <sub>IN</sub> (CTL)   |                                                        | 0       |      | V <sub>CC</sub> | V    |
| High level input voltage                                               | V <sub>IH</sub> (CTL)   | HIN pin PWM ON duty 100%                               | 4.4     | 4.6  | 4.8             | V    |
| Middle level input voltage 1<br>(At drive start)                       | V <sub>IM1</sub> (CTLI) | HIN pin PWM ON duty 0%                                 | 2.15    | 2.35 | 2.55            | V    |
| Middle level input voltage 2<br>(During drive)                         | V <sub>IM2</sub> (CTLI) | HIN pin PWM ON duty 0%                                 | 1.9     | 2.1  | 2.3             | V    |
| Input current<br>(During drive in 120-degree<br>current-carrying mode) | I <sub>IH1</sub> (CTLI) | VCTL = 3.5V                                            | 13      | 25   | 37              | μA   |
| Input current<br>(During drive in sine wave<br>current-carrying mode)  | I <sub>IH2</sub> (CTLI) | VCTL = 3.5V                                            | 10      | 20   | 30              | μA   |
| CTL Amplifier (power saving mode)                                      |                         |                                                        |         |      |                 |      |
| Low level input voltage                                                | V <sub>IL1</sub> (CTL)  | Power saving mode                                      | 0.75    | 0.95 | 1.15            | V    |
| Hysteresis width                                                       | ΔCTL                    |                                                        | 0.15    | 0.35 | 0.55            | V    |

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# LV8139JA

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| Parameter                                                 | Symbol                | Conditions               | Ratings |      |      | Unit |
|-----------------------------------------------------------|-----------------------|--------------------------|---------|------|------|------|
|                                                           |                       |                          | min     | typ  | max  |      |
| <b>F/R Pin</b>                                            |                       |                          |         |      |      |      |
| High level input voltage range                            | V <sub>IH</sub> (FR)  |                          | 3.0     |      | VREG | V    |
| Low level input voltage range                             | V <sub>IL</sub> (FR)  |                          | 0       |      | 0.7  | V    |
| Input open voltage                                        | V <sub>IO</sub> (FR)  |                          |         | 0    | 0.3  | V    |
| Hysteresis width                                          | V <sub>IS</sub> (FR)  |                          | 0.15    | 0.3  | 0.45 | V    |
| High level input current                                  | I <sub>IH</sub> (FR)  | VF/R = VREG              | 25      | 45   | 65   | μA   |
| Low level input current                                   | I <sub>IL</sub> (FR)  | VF/R = 0V                | -2      | 0    | +2   | μA   |
| <b>FAULT Pin</b>                                          |                       |                          |         |      |      |      |
| Drive stop voltage                                        | VFOF                  |                          | 0       |      | 0.5  | V    |
| Drive start voltage                                       | VFON                  |                          | 3.0     |      | VREG | V    |
| Input open voltage                                        | V <sub>IO</sub> (FLT) |                          | 4.6     | VREG |      | V    |
| High level input current                                  | I <sub>IH</sub> (FLT) | VFAULT=VREG              |         | 0    | 10   | μA   |
| Low level input current                                   | I <sub>IL</sub> (FLT) | VFAULT=0V                | -200    | -160 | -120 | μA   |
| <b>ADP1 Pin</b> (drive phase adjustment)                  |                       |                          |         |      |      |      |
| Minimum lead angle                                        | Vadp01                | VADP1 = 0V               |         | 0    | 2    | Deg  |
| Maximum lead angle                                        | Vadp16                | VADP1 = VREG             | 56      | 58   |      | Deg  |
| Current ratio with the ADP2 pin current                   | ADP                   | VCTL = 5.5V, IADP1/IADP2 | 1.8     | 2    | 2.2  | A/A  |
| <b>ADP2 Pin</b> (drive phase adjustment)                  |                       |                          |         |      |      |      |
| High level output voltage                                 | VADP2H                | VCTL = 5.5V              | 2.25    | 2.45 | 2.65 | V    |
| Low level output voltage                                  | VADP2L                | VCTL = 1.5V              | 0       |      | 0.3  | V    |
| <b>DPL Pin</b> (drive-phase-adjustment limit setting pin) |                       |                          |         |      |      |      |
| Lead angle limit high level voltage                       | VDPLH                 |                          | 3.3     | 3.5  | 3.7  | V    |
| Lead angle limit low level voltage                        | VDPLL                 |                          | 1.3     | 1.5  | 1.7  | V    |

4. Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

5. These are design target values and no measurements are made.

# LV8139JA

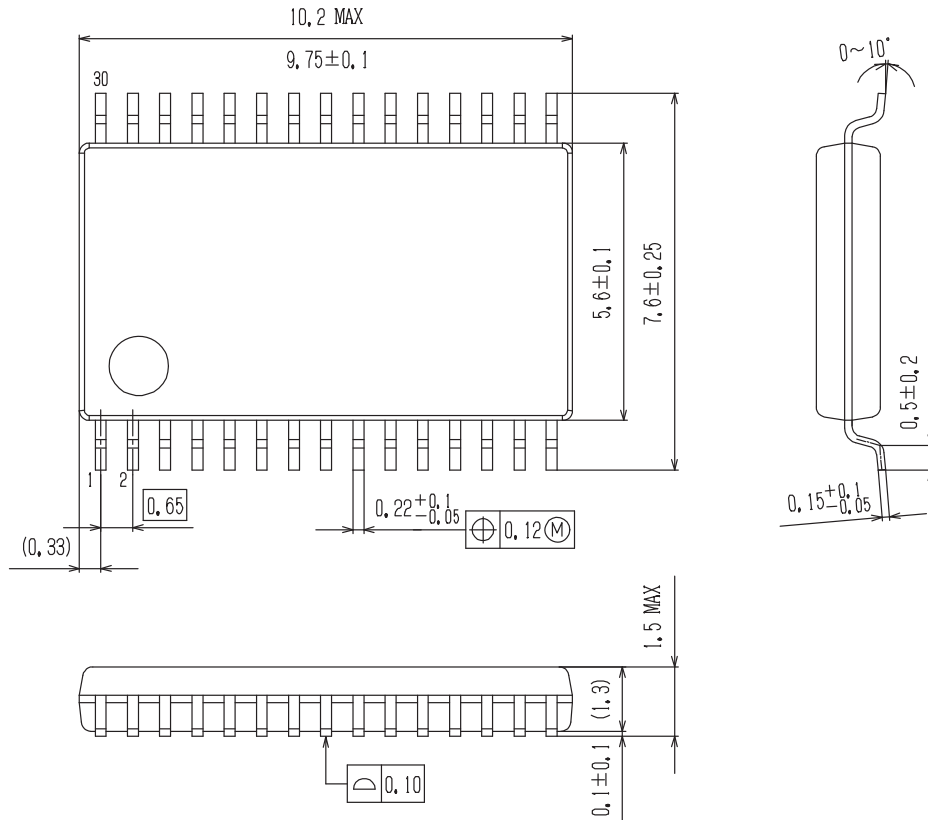
## Package Dimensions

unit : mm (typ)

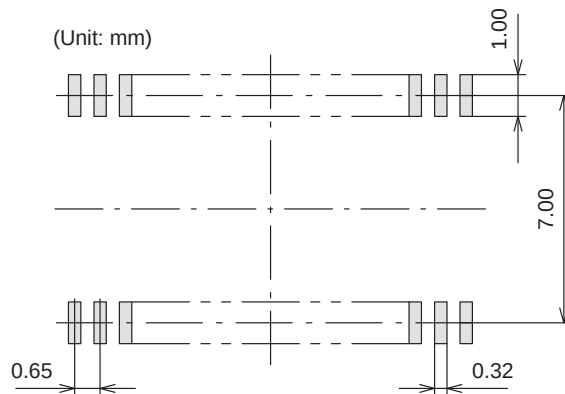
### SSOP30 (275mil)

CASE 565AT

ISSUE A



### SOLDERING FOOTPRINT\*

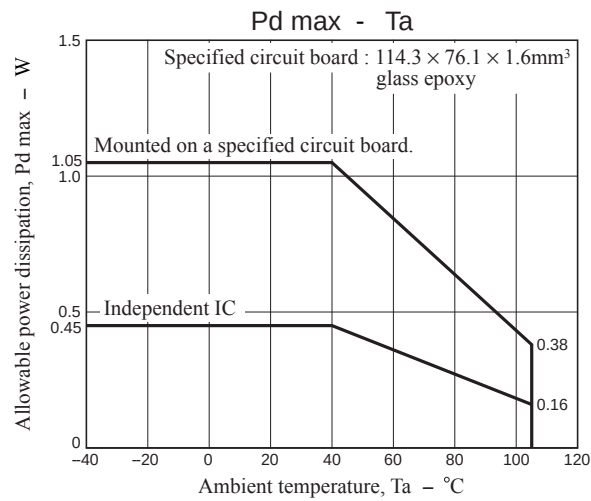


NOTE: The measurements are not to guarantee but for reference only.

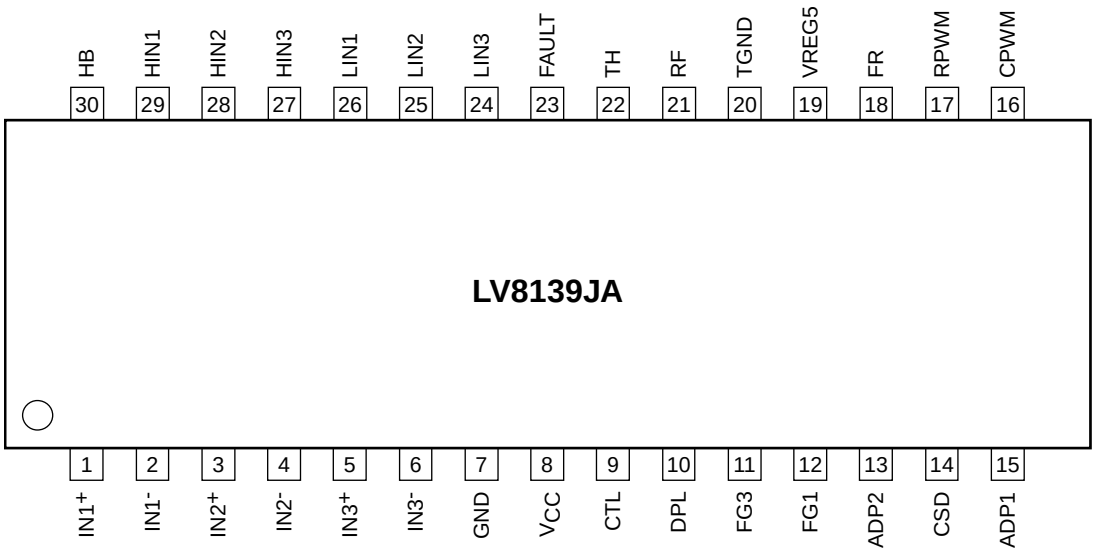
\*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

# LV8139JA

Pdmax-Ta diagram



Pin Assignment



Top view

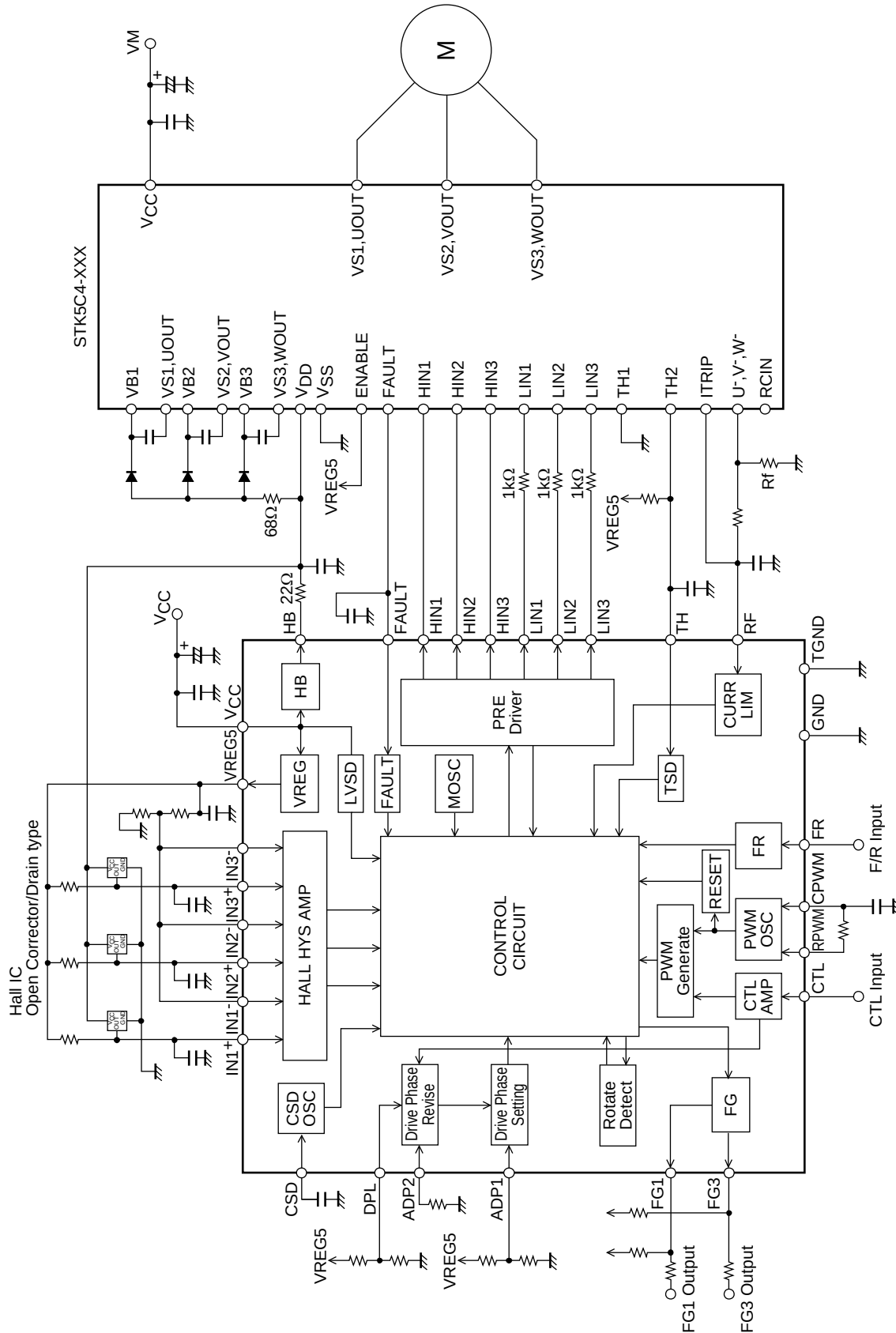
# LV8139JA

## Sample Application Circuit 1 (Hall IC, HIC)

The Hall IC to be used must be of open-collector or open-drain output type, and it must be pulled up by VREG5.

The type of Hall IC incorporating a pull-up resistor cannot be used.

Furthermore, when using an element that cannot turn off the control power while VM is being applied, the control power must be supplied from the VCC pin rather than from the HB pin.



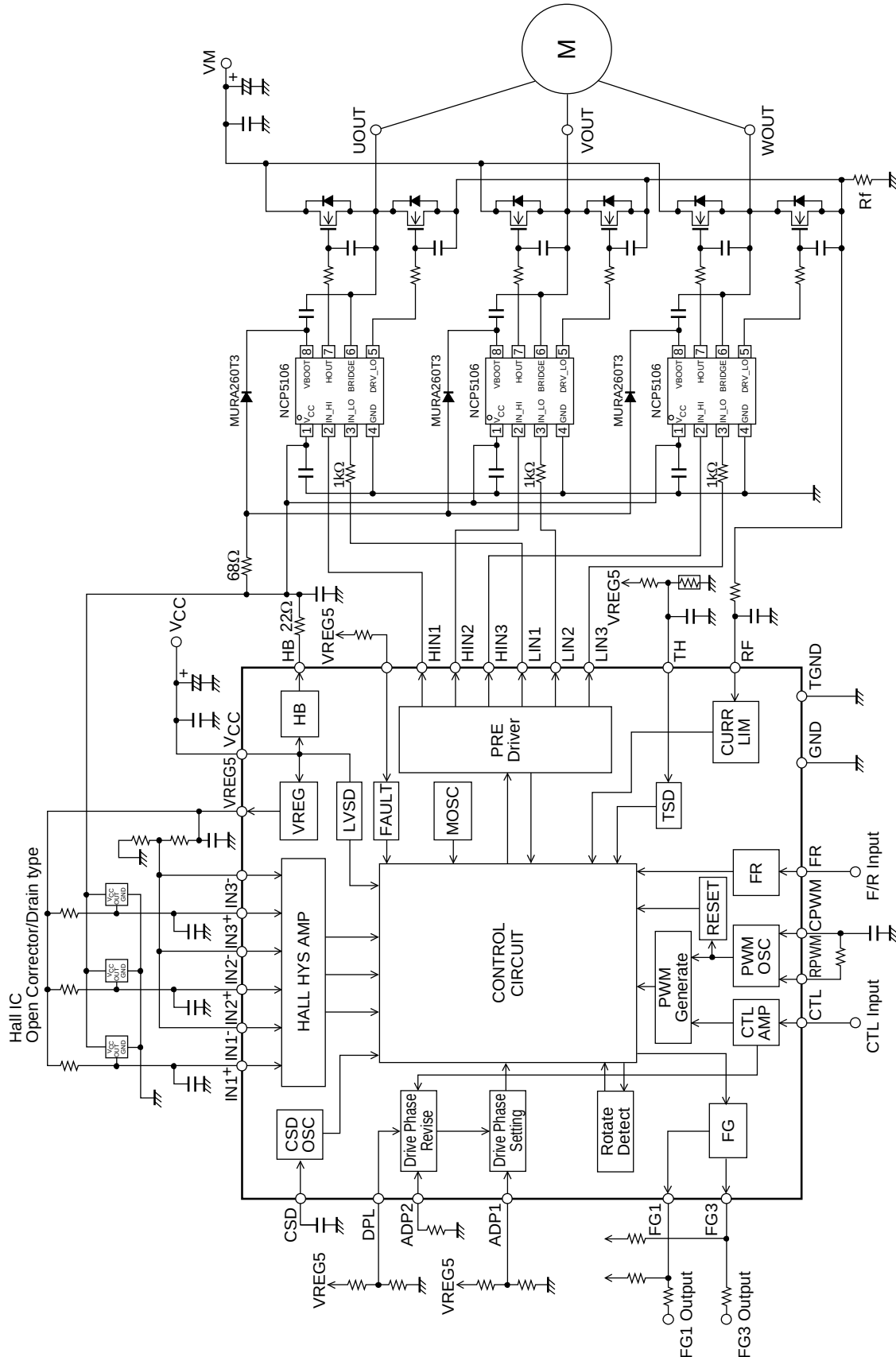
# LV8139JA

## Sample Application Circuit 2 (Hall IC, FET)

The Hall IC to be used must be of open-collector or open-drain output type, and it must be pulled up by VREG5.

The type of Hall IC incorporating a pull-up resistor cannot be used.

Furthermore, when using a gate driver that cannot turn off the control power while VM is being applied, the control power must be supplied from the VCC pin rather than from the HB pin. An element with a short reverse recovery time must be selected as the output FET.





# LV8139JA

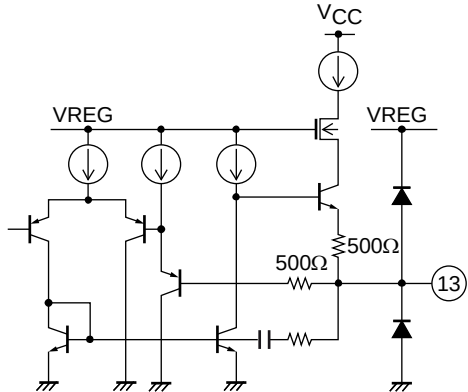
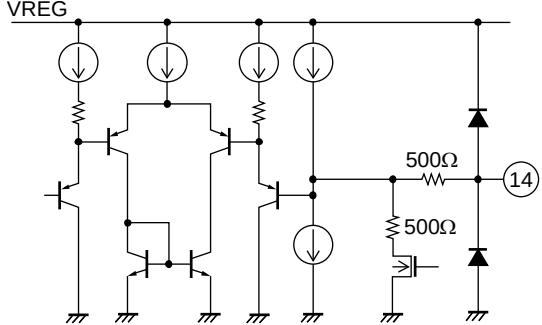
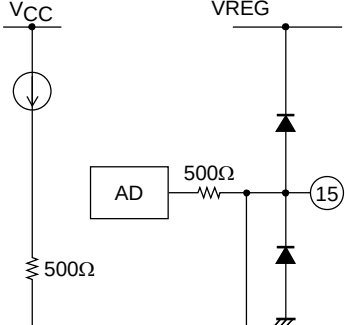
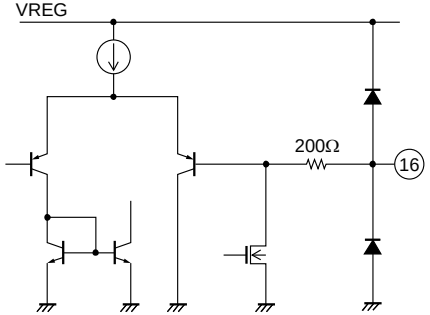
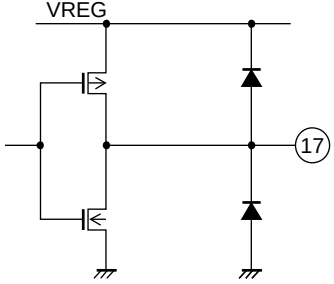
## Pin Functions

| Pin No.                    | Pin Name                                                                                                             | Pin function                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                               | Equivalent Circuit |
|----------------------------|----------------------------------------------------------------------------------------------------------------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|--------------------|
| 1<br>2<br>3<br>4<br>5<br>6 | IN1 <sup>+</sup><br>IN1 <sup>-</sup><br>IN2 <sup>+</sup><br>IN2 <sup>-</sup><br>IN3 <sup>+</sup><br>IN3 <sup>-</sup> | Hall signal input pins.<br>The high state is when IN <sup>+</sup> is greater than IN <sup>-</sup> , and the low state is the reverse.<br>An amplitude of at least 100mVp-p (differential) is desirable for the Hall signal inputs. If noise on the Hall signals is a problem, insert capacitors between IN <sup>+</sup> and IN <sup>-</sup> pins.<br>If input is provided from a Hall IC, fix one side of the inputs (either the "+" or "-" side) at a voltage within the common-mode input range (0.3V to VREG-1.8V), and use the other input side as an input over the 0V to VREG range. |                    |
| 7                          | GND                                                                                                                  | Ground pin of the control circuit block.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                   |                    |
| 8                          | V <sub>CC</sub>                                                                                                      | Power supply pin for control.<br>Insert a capacitor between this pin and ground to prevent the influence of noise, etc.                                                                                                                                                                                                                                                                                                                                                                                                                                                                    |                    |
| 9                          | CTL                                                                                                                  | Control input pin. When CTL pin voltage rises, the IC changes the output signal PWM duty to increase the torque output.<br>In sine wave mode, Nch FET (in equivalent circuit diagram) OFF<br>In 120-degree current-carrying mode, Nch FET ON                                                                                                                                                                                                                                                                                                                                               |                    |
| 10                         | DPL                                                                                                                  | Setting pin for drive phase adjustment limit.<br>This pin is used to limit the lead angle of the drive phase. The lead angle is limited to zero degrees when the voltage is 1.5V or lower and the limit is released when the voltage is 3.5V or higher.                                                                                                                                                                                                                                                                                                                                    |                    |
| 11<br>12                   | FG3<br>FG1                                                                                                           | FG3 : 3-Hall FG signal output pin.<br>8-pole motor outputs 12 FG pulses per one rotation. In power saving mode, high-level is output.<br>FG1 :1-Hall FG signal output pin.<br>8-pole motor outputs 4 pulses per one rotation. In power saving mode, high-level is output.                                                                                                                                                                                                                                                                                                                  |                    |

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# LV8139JA

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| Pin No. | Pin Name | Pin function                                                                                                                                                                                                               | Equivalent Circuit                                                                   |
|---------|----------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|--------------------------------------------------------------------------------------|
| 13      | ADP2     | Setting pin for phase drive correction.<br>This pin sets the amount of correction made to the lead angle according to the CTL input. Insert a resistor between this pin and ground to adjust the amount of correction.     |    |
| 14      | CSD      | Pin to set the operating time of the motor constraint protection circuit.<br>Insert a capacitor between this pin and ground.<br>Connect this pin to ground when the constraint protection circuit is not going to be used. |    |
| 15      | ADP1     | Drive phase adjustment pin.<br>The drive phase can be advanced from 0 to 58 degrees during 180-degree current carrying drive. The lead angle becomes 0 degrees when 0V is input and 58 degrees when VREG is input.         |  |
| 16      | CPWM     | Triangle wave oscillation pin for PWM generation.<br>Insert a capacitor between this pin and ground and a resistor between this pin and RPWM for triangle wave oscillation.                                                |  |
| 17      | RPWM     | Oscillation pin for PWM generation.<br>Insert a resistor between this pin and CPWM.                                                                                                                                        |  |

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# LV8139JA

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| Pin No. | Pin Name | Pin function                                                                                                                                                                                                                                                                                     | Equivalent Circuit |
|---------|----------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|--------------------|
| 18      | FR       | FR<br>Forward/reverse rotation setting pin.<br>A low-level specifies forward rotation and a high-level specifies reverse rotation. This pin is held low when open.                                                                                                                               |                    |
| 20      | TGND     | TGND<br>Test pin. Connect this pin to ground.                                                                                                                                                                                                                                                    |                    |
| 19      | VREG5    | 5V regulator output pin<br>(control circuit power supply).<br>Insert a capacitor between this pin and ground for power stabilization.<br>0.1μF or so is desirable.                                                                                                                               |                    |
| 21      | RF       | Output current detection pin.<br>This pin is used to detect the voltage across the current detection resistor (Rf).<br>The maximum output current is determined by the equation $I_{OUT} = 0.25V/R_f$ .                                                                                          |                    |
| 22      | TH       | Thermistor connection pin.<br>The thermistor detects heat generated from HIC and turns off the drive output when an overheat condition occurs.<br>All the HIN/LIN output pins are set to low at a pin voltage of 0.6V or less.<br><br>* For further details, refer to "Description of LV8139JA." |                    |

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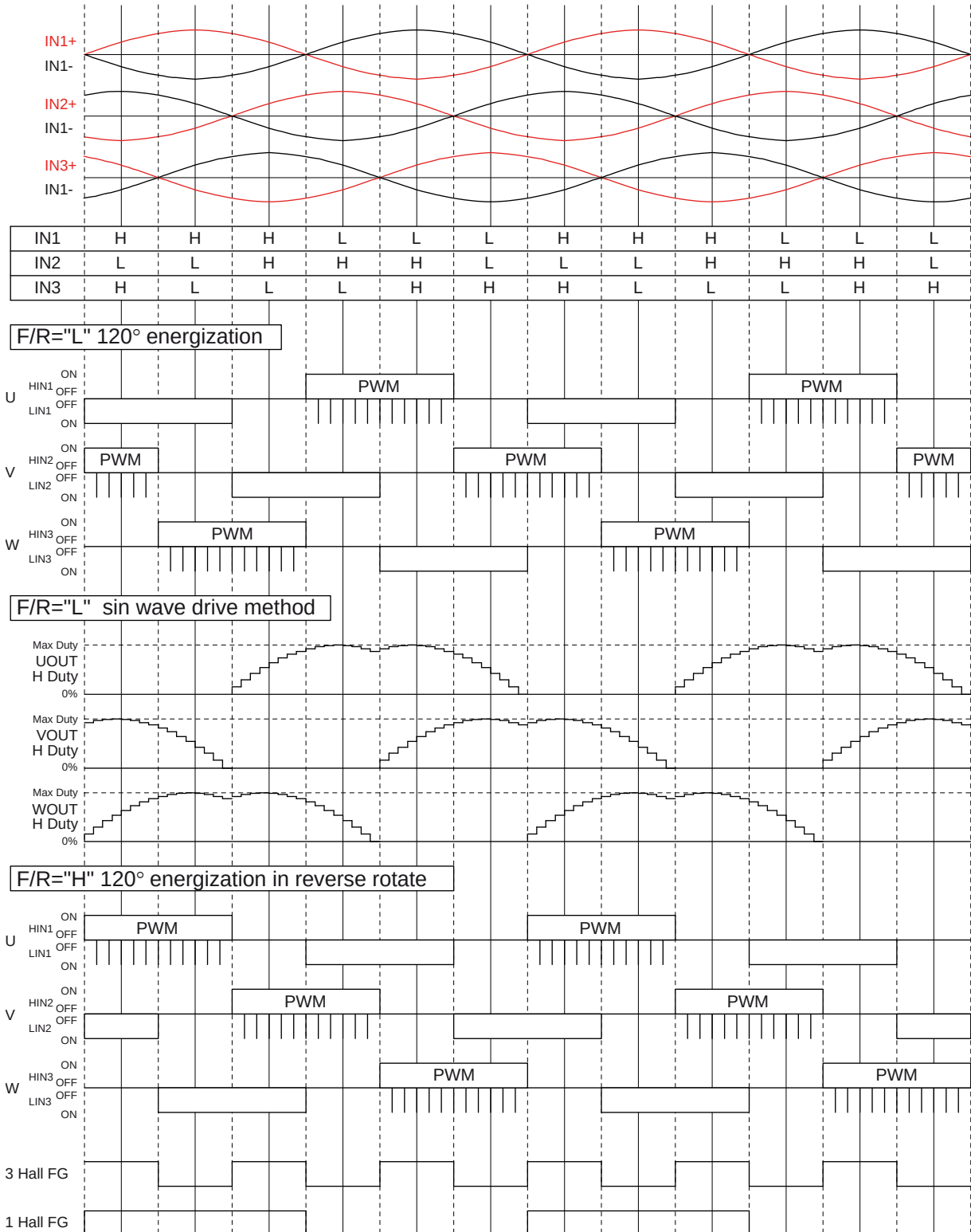
| Pin No.        | Pin Name             | Pin function                                                                                                                                                                                                                                                                                                   | Equivalent Circuit |
|----------------|----------------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|--------------------|
| 23             | FAULT                | HIC protection signal input pin.<br>This pin accepts an error mode detection signal generated by the HIC side.<br>With a low-level input, the error mode detection condition is established, and all the HIN/LIN output pins are set to low.<br><br>* For further details, refer to "Description of LV8139JA." |                    |
| 24<br>25<br>26 | LIN3<br>LIN2<br>LIN1 | LIN1, LIN2, and LIN3 :<br>L side drive signal output pin.<br>Generate 0 to VREG push-pull outputs.                                                                                                                                                                                                             |                    |
| 27<br>28<br>29 | HIN3<br>HIN2<br>HIN1 | HIN1, HIN2, and HIN3 :<br>H side drive signal output pin.<br>Generate 0 to VREG push-pull outputs.                                                                                                                                                                                                             |                    |
| 30             | HB                   | Hall bias HIC power supply pin.<br>Insert a capacitor between this pin and ground.<br>This pin is set to high-impedance state in power saving mode. By supplying Hall bias and HIC power using this pin, the power consumption by Hall bias and HIC in power saving mode can be reduced to zero.               |                    |

# LV8139JA

**Timing Chart** (IN = "H" indicates the state in which IN<sup>+</sup> is greater than IN<sup>-</sup>.)

(1) F/R pin = L

Normal Hall input Lead Angle=0°



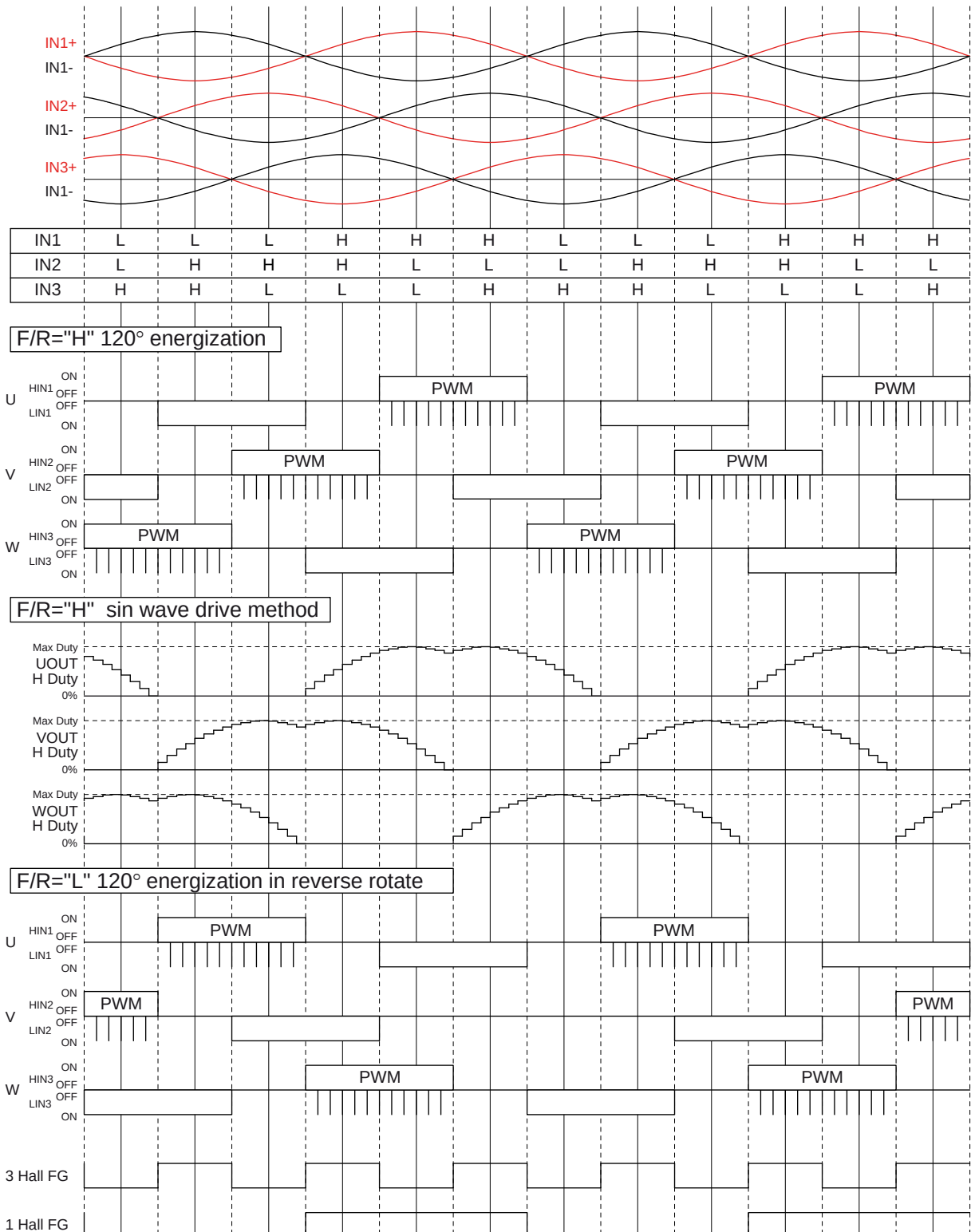
The energization is switched to 120° when 3 Hall FG frequency is 5.15Hz (typ) or lower  
A direction of rotation is detected from Hall signal according to F/R pin input

If the motor rotates in reverse against F/R pin input 120° energization is maintained forcibly

# LV8139JA

(2) F/R pin = H

Reverse Hall input Lead Angle=0°



The energization is switched to 120° when 3 Hall FG frequency is 5.15Hz (typ) or lower  
A direction of rotation is detected from Hall signal according to F/R pin input

If the motor rotates in reverse against F/R pin input 120° energization is maintained forcibly

## Functional Description

- Basic operation of 120-degree  $\Leftrightarrow$  Sine wave current-carrying switching

At startup, this IC starts at 120-degree current-carrying. The current-carrying is switched to sine wave when the 3-Hall FG frequency is 5.15Hz (typ) or above and the rising edge of the IN2 signal has been detected twice in succession.

- Concerning the Hall signal input sequence

This IC controls the motor rotation direction commands and Hall signal input sequence in order to set the lead angle. If the motor rotation direction commands and Hall signal input sequence do not conform to what is shown on the timing chart, the motor is driven by 120-degree current-carrying. Shown below are two Hall signal input sequences.

Sequence 1 : When the Hall signal has been input with the following logic

|     |   |   |   |   |   |   |   |   |   |   |   |
|-----|---|---|---|---|---|---|---|---|---|---|---|
| IN1 | H | → | H | → | H | → | L | → | L | → | L |
| IN2 | L | → | L | → | H | → | H | → | H | → | L |
| IN3 | H | → | L | → | L | → | L | → | H | → | H |

When F/R pin input is high  $\rightarrow$  120-degree current-carrying

When F/R pin input is low  $\rightarrow$  180-degree current-carrying

Sequence 2 : When the Hall signal has been input with the following logic

|     |   |   |   |   |   |   |   |   |   |   |   |
|-----|---|---|---|---|---|---|---|---|---|---|---|
| IN1 | H | → | L | → | L | → | L | → | H | → | H |
| IN2 | L | → | L | → | H | → | H | → | H | → | L |
| IN3 | H | → | H | → | H | → | L | → | L | → | L |

When F/R pin input is high  $\rightarrow$  180-degree current-carrying

When F/R pin input is low  $\rightarrow$  120-degree current-carrying

- CTL pin input

- a) Power-saving mode  $V_{CTL} < V_{IL}$  (0.95V : typ)
  - $L_{IN1}$  to  $L_{IN3}$  and  $H_{IN1}$  to  $H_{IN3}$  outputs all set to low
  - $I_{CC} = 0$ , HB pin = OFF

The power consumption of the IC can now be set to 0, and the power consumption of the Hall element connected to the HB pin and the output block can also be set to 0.

\* When the PWM oscillation frequency setting is 17kHz, the maximum duty ratio in the 120-degree current carrying mode is 88% (typ).

- The CTL pin is pulled down by 170k $\Omega$  (120-degree mode) : Typ, 131.6k $\Omega$  (sine wave mode) : typ inside the IC. Caution is required when the control input voltage input is subjected to resistance division, for example.

- b) Standby mode While stopped:  $V_{IL} < V_{CTL} < V_{IM1}$  (2.33V: typ); while running:  $V_{IL} < V_{CTL} < V_{IM2}$  (2.1V: typ)
 

The  $U_{IN1}$  to 3 outputs are set to low, and the bootstrap charge pulse (pulse width: 2.5 $\mu$ s: design target) is output to the  $L_{IN1}$  to 3 outputs in preparation for drive start.

- Bootstrap capacitor initial charging mode
 

When the mode is switched from the power-saving mode to the standby mode and then to the drive mode, the IC enters the bootstrap capacitor charging mode ( $H_{IN1}$ ,  $H_{IN2}$ ,  $H_{IN3}$  pins = L  $L_{IN1}$ ,  $L_{IN2}$ ,  $L_{IN3}$  pins = H 4.55ms typ) in order to charge the bootstrap capacitor.

- c) Drive mode At drive start:  $V_{IM1} < V_{CTL} < 7V$ ; during drive:  $V_{IM2} < V_{CTL} < 7V$  ( $V_{IH}$  4.7V: typ)
 

The motor is driven at the PWM duty ratio that corresponds to  $V_{CTL}$ . When  $V_{CTL}$  is increased, the PWM duty ratio increases, and the maximum duty ratio is established at “ $V_{IH}$ .”

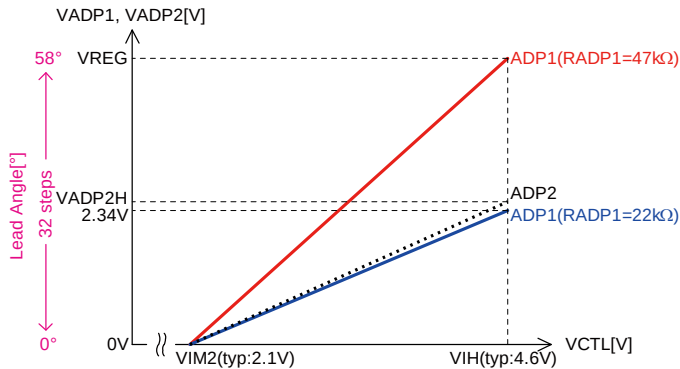
- d) Test mode  $8.5V < V_{CTL} < V_{CC}$ 

When the CTL pin voltage is 8V or higher, the IC enters the test mode, and the motor is driven at the 120-degree current-carrying and maximum duty\* ratio.

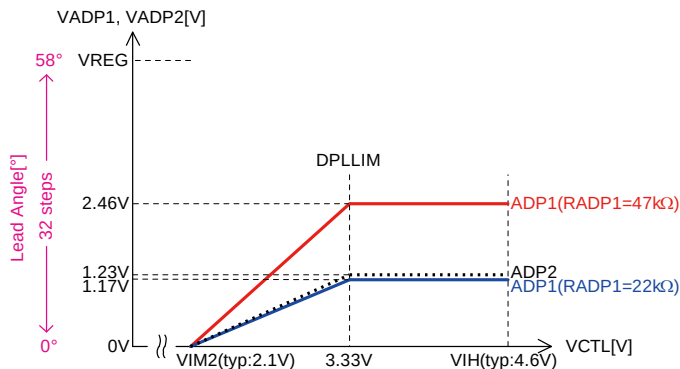
• Drive phase adjustment

During 180-degree current-carrying drive, any lead angle from 0 to 58 degrees can be set using the ADP1 pin voltage (lead angle control). This setting can be adjusted in 32 steps (in 1.875-degree increments) from 0 to 58 degrees using the ADP1 pin voltage, and it is updated every Hall signal cycle (it is sampled at the rising edge of the IN3 input and updated at its falling edge).

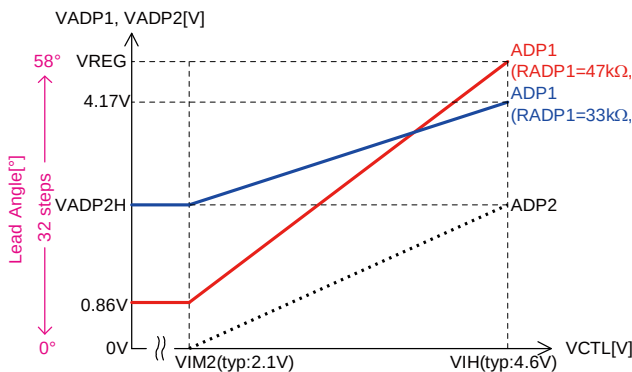
A number of lead angle adjustments proportionate to the CTL pin voltage can be undertaken by adjusting



2. The ADP2 pin rise can be halted (a limit on the lead angle adjustment can be set by means of the CTL voltage) by setting DPL (pin 10).



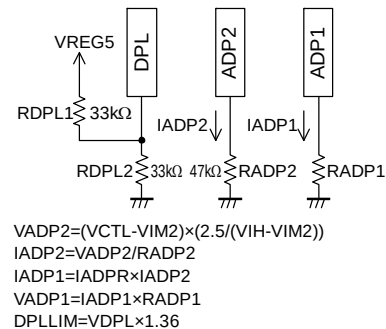
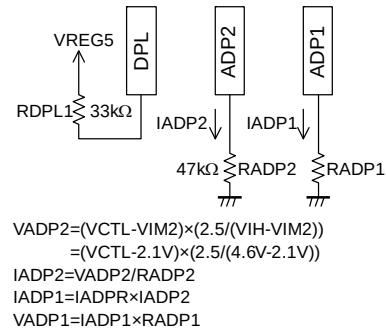
3. The offset and slope can be adjusted as desired by setting RADP1 and RADP12 of ADP1 (pin 15). (It is also possible to set a limit on the lead angle



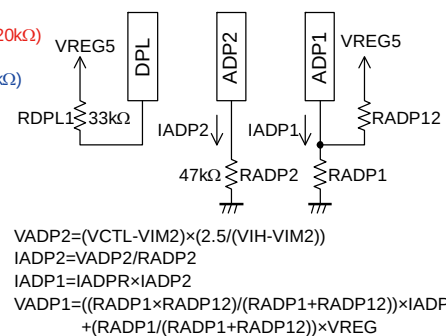
4. When the lead angle is not adjusted  
ADP1 pin: shorted to ground; ADP2 pin and DPL pin: pulled down to ground using the resistors

the resistance levels of resistors connected to the ADP1 pin, ADP2 pin and DPL pin. When these pins are not going to be used, reference must be made to section 4.5, and the pins must not be used in the open status. Furthermore, a resistance of 47kΩ or more must be used for the resistor (RADP2) that is connected to the ADP2 pin.

1. The slopes of VCTL and VADP1 can be adjusted by setting the resistance level of the resistor (RADP1) connected to ADP1 (pin 15).



adjustment by means of the CTL voltage by setting DPL.)



5. When the lead angle is not adjusted by means of the CTL pin voltage (for use with a fixed lead angle)  
ADP1 pin: lead angle setting by resistance division from VREG5; ADP2 pin and DPL pin: pulled down to ground by the resistors



## Description of LV8139

### 1. Current Limiter Circuit

The current limiter circuit limits the output current peak value to a level determined by the equation  $I = V_{RF}/R_f$  (where  $V_{RF} = 0.25V$  typ,  $R_f$  is the value of the current detection resistor). The current limiter operates by reducing the  $H_{IN}$  output on duty to suppress the current.

The current limiter circuit detects the reverse recovery current of the diode due to PWM operation. To assure that the current limiting function does not malfunction, its operation has a delay of approx.  $1\mu s$ . If the motor coils resistance or a low inductance, current fluctuation at startup (when there is no back electromotive force in the motor) will be rapid. The delay in this circuit means that at such times the current limiter circuit may operate at a point well above the set current. Application must take this increase in the current due to the delay into account when the current limiter value is set.

### 2. Power Saving Circuit (CTL pin)

This IC goes into the power saving mode that stops operation of all the circuits to reduce the power consumption. If the HB pin is used for the Hall element bias and the output block, the current consumption in the power-saving mode is zero.

### 3. Hall Input Signal

Signals with an amplitude in excess of the hysteresis is required for the Hall inputs. However, considering the influence of noise and phase displacement, an amplitude of over 100mV is desirable.

If noise disrupts the output waveform, this must be prevented by inserting capacitors or other devices across the Hall inputs. The Hall inputs are used by the circuit inside the IC as decision signals so if noise enters, a malfunction occurs in the operation.

Although the circuit is designed to tolerate a certain amount of noise, care is required.

Furthermore, when the Hall signal amplitude has changed as a result of a change in temperature, the drive phase may possibly shift due to the Hall amplifier hysteresis. It is the user who is responsible for giving due consideration to this aspect. Use of a Hall IC is recommended unless there is a reason not to use one.

If all three phases of the Hall input signal go to the same input state (HHH or LLL), all the  $H_{IN}/L_{IN}$  outputs are set to low.

If the outputs from a Hall IC are used, fix one side of the inputs (either the “+” or “-” side) at a voltage within the common-mode input voltage range (0.3V to  $V_{REG}-1.8V$ ), and use the other input side as an input over the 0V to  $V_{REG}$  range.

### 4. Constraint Protection Circuit

A constraint protection circuit is incorporated in order to protect the output elements and motor when the motor is constrained. The circuit is activated when the Hall signal is not switched for a specific period of time when the motor is in operation. The counter is reset each time the motor rotates 360 degrees in terms of the electrical angle.

All the  $H_{IN}$  and  $L_{IN}$  outputs are set to the low level when the constraint protection circuit is in operation. This time is determined by the capacitance of the capacitor connected to the CSD pin.

Oscillation time of CSD pin (1 pulse)  $T = |$

$(V_{OH}-V_{OL})/ICHG1 | \times C (\mu F) + |$

$(V_{OH}-V_{OL})/ICHG2 | \times C (\mu F)$

Constraint protection detection time  $T1 (s) = T \times 256$  (count)

Constraint protection time  $T2 (s) = T \times 2816$  (count)

When a  $0.022\mu F$  capacitor is attached,  $T = 8.36ms$ ,  $T1 = 2.14s$  and  $T2 = 23.54s$  are established as the typical ratings. After the motor has been constrained, the constraint protection state is established at 2.14 (s), and then after 23.54 (s) has elapsed, the constraint protection circuit is reset automatically. A time that provides some leeway in the motor start time that factors in any fluctuations must be selected as the setting.

Conditions for releasing the constraint protection state other than by automatic resetting:

When CTL pin voltage <  $V_{IM2}$  input → protection release and CSD count reset

When the low level is detected on the TH pin → protection release and CSD count reset

When FR has been switched → protection release and CSD count reset

When TSD protection is detected → CSD count stop

### 5. Power Supply Stabilization

Since this IC adopts a switching drive technique, the power-supply line level can be disrupted easily. Thus capacitors large enough to stabilize the power supply voltage must be inserted between the  $V_{CC}$  pins and ground. If the electrolytic capacitors cannot be connected close to their corresponding pins, ceramic capacitors of about  $0.1\mu F$  must be connected near these pins.

If diodes are inserted in the power-supply line to prevent destruction of the device when the power supply is connected with reverse polarity, the power supply line levels will be even more easily disrupted, and even larger capacitors must be used.

## 6. VREG Stabilization

Connect a capacitor with a capacitance of 0.1μF or more between VREG5 and ground in order to stabilize the VREG voltage that is the power supply of the control circuit.

The ground lead of that capacitor must be located as close as possible to the control system ground (SGND) of the IC.

## 7. Forward/Reverse Switching (F/R pin)

Switching between forward rotation and reverse rotation must not be undertaken while the motor is running.

## 8. TH Pin

The TH pin must normally be pulled up to VREG5 for use. When this pin has been set to low, all the H<sub>IN</sub>/L<sub>IN</sub> outputs are set to low. When reset is initiated, the bootstrap initial charging mode is established.

## 9. FAULT Pin

The FAULT pin must normally be pulled up to VREG5 for use. When this pin has been set to low, all the H<sub>IN</sub>/L<sub>IN</sub> outputs are set to low. When reset is initiated, the bootstrap initial charging mode is established.

All the outputs are set to low. In addition, the FG1/FG3 output goes off, too. When reset is initiated, the bootstrap initial charging mode is established.

## 10. PWM Frequency Setting

$$f_{CPWM} \approx 1 / (1.7CR)$$

Components with good temperature characteristics must be used.

An oscillation frequency of about 17kHz is obtained when a 2200pF capacitor and 15kΩ resistor are used.

If the PWM frequency is too low, switching noise will be heard from the motor; conversely, if it is too high, the output power loss will increase. For this reason, a frequency between 15kHz and 30kHz or so is desirable. The capacitor ground must be connected as close as possible to the control system ground (SGND pin) of the IC to minimize the effects of the outputs.

If there are no fluctuations in the capacitance or resistance of the external capacitors or resistors and only the IC fluctuations are to be considered, an actual capability of ±3% can be expected.

## 11. Concerning the power-raising operation

This IC provides sine wave PWM drive so it performs operations similar to synchronous rectification. These operations are such that current is sometimes returned to the motor power supply side depending on the conditions of use. For instance, this may happen when:

- The drive phase is shifted.
- The motor has been suddenly accelerated.
- The output duty ratio has been decreased sharply while the motor is running.

If the output duty ratio has been decreased sharply, it is highly likely that current will return to the motor power supply.

The extent to which the motor supply voltage increases differs depending on the size of the capacitors used in the product that incorporates the motor, the size of the capacitor inserted between the motor power supply and ground on the motor circuit board and the motor used; as such, it is the user who is responsible for giving due consideration to this aspect.

It is necessary to take remedial action such as increasing the capacitance of the capacitors or reducing the speed at which the duty ratio will be reduced when the motor supply voltage rises to ensure that the maximum withstand voltage of the element used for output is not exceeded.

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