SAMSUNG ELECTRONICS

Approval

LEAD-FREE

TO : DELL

DATE : Feb. 26. 2010

SAMSUNG TFT-LCD

MODEL NO : LTN133AT17

NOTE : Extension code [-1]
→ LTN133AT17-**1**
Surface type [Anti-Glare]

The information described in this SPEC is preliminary and can be changed without prior notice.

APPROVED BY :

PREPARED BY : **LCD Application Engineering Part I**

SAMSUNG ELECTRONICS CO., LTD.

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REVISION HISTORY

Approval

Date	Revision No.	Page	Summary
Feb. 26. 2010	A00	All	LTN133AT17-1 model spec was issued first.
May. 20. 2010	A01	All	NEC D-IC ECR

Samsung Secret

GENERAL DESCRIPTION

DESCRIPTION

LTN133AT17-1 is a color active matrix TFT (Thin Film Transistor) liquid crystal display (LCD) that uses amorphous silicon TFT as switching devices. This model is composed of a TFT LCD panel, a driver circuit and a backlight system. The resolution of a 13.3" contains 1366 x 768 pixels and can display up to 262,144 colors. 6 O'clock direction is the optimum viewing angle.

FEATURES

- High contrast ratio
- 1366 x 768 pixels resolution (16:9, HD)
- Fast Response Time
- Low power consumption
- LED BLU Structure with embeded LED driver
- DE (Data enable) only mode
- eDP (Display Port) interface (1lane @ 2.7GHz)
- On board EDID chip
- RoHS compliance
- PVC free compliance
- BFR free compliance
- AS free compliance

APPLICATIONS

- Notebook PC
- If the usage of this product is not for PC application, but for others, please contact SEC

GENERAL INFORMATION

Item	Specification	Unit	Note
Display area	293.42(H) x 164.97(V) (13.3” diagonal)	mm	
Driver element	a-Si TFT active matrix		
Display colors	262,144		
Number of pixel	1366 x 768	pixel	16 : 9
Pixel arrangement	RGB vertical stripe		
Pixel pitch	0.2148 (H) x 0.2148 (V) (typ)	mm	
Display Mode	Normally white		
Surface treatment	Haze 17%, Hardness 3H		Anti-Glare

Mechanical Information

Item		Min.	Typ.	Max.	Unit	Note
Module size	Horizontal (H)	307.1	307.6	308.1	mm	
	Vertical (V)	182.6	183.1	183.6	mm	
	Depth (D)	4.7	5.0	5.3	mm	(1)
Weight		-	-	350	g	

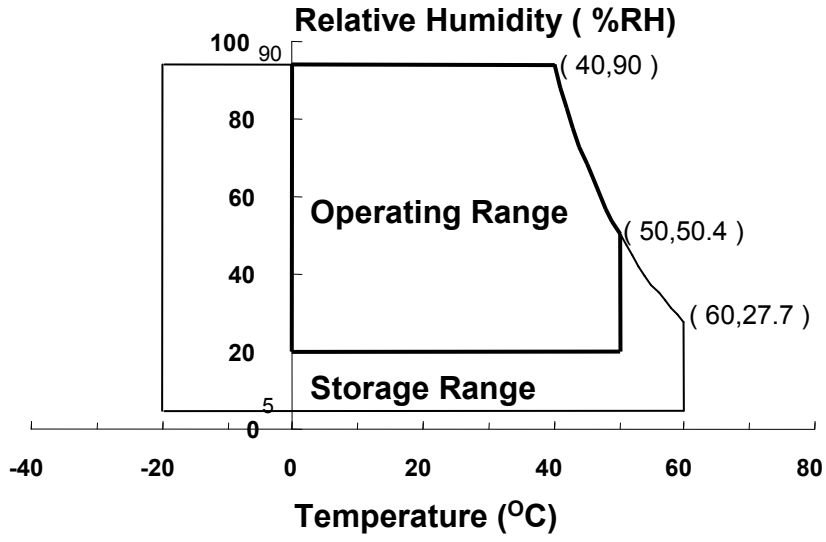
Note (1) Measurement condition of outline dimension
. Equipment : Vernier Calipers
. Push Force : 500g ·f (minimum)

1. ABSOLUTE MAXIMUM RATINGS

1.1 ENVIRONMENTAL ABSOLUTE RATINGS

Item	Symbol	Min.	Max.	Unit	Note
Storage temperate	TSTG	-20	60	°C	(1)
Operating temperate (Temperature of glass surface)	TOPR	0	50	°C	(1)
Shock (non-operating)	Snop	-	240	G	(2),(4)
Vibration (non-operating)	Vnop	-	2.41	G	(3),(4)

Note (1) Temperature and relative humidity range are shown in the figure below.
95 % RH Max. (40 °C ≥ Ta)
Maximum wet - bulb temperature at 39 °C or less. (Ta > 40 °C) No condensation



(2) 2ms, half sine wave, one time for ±X, ±Y, ± Z.
(3) 5 - 500 Hz, random vibration, 30min for X, Y, Z.
(4) At testing Vibration and Shock, the fixture in holding the Module to be tested have to be hard and rigid enough so that the Module would not be twisted or bent by the fixture.

1.2 ELECTRICAL ABSOLUTE RATINGS

(1) TFT LCD MODULE

V_{DD} =3.3V, V_{SS} = GND = 0V

Item	Symbol	Min.	Max.	Unit	Note
Power Supply Voltage	V_{DD}	V_{DD} – 0.3	V_{DD} + 0.3	V	(1)
Logic Input Voltage	V_{DD}	V_{DD} – 0.3	V_{DD} + 0.3	V	(1)

Note (1) Within Ta (25 ± 2 °C)

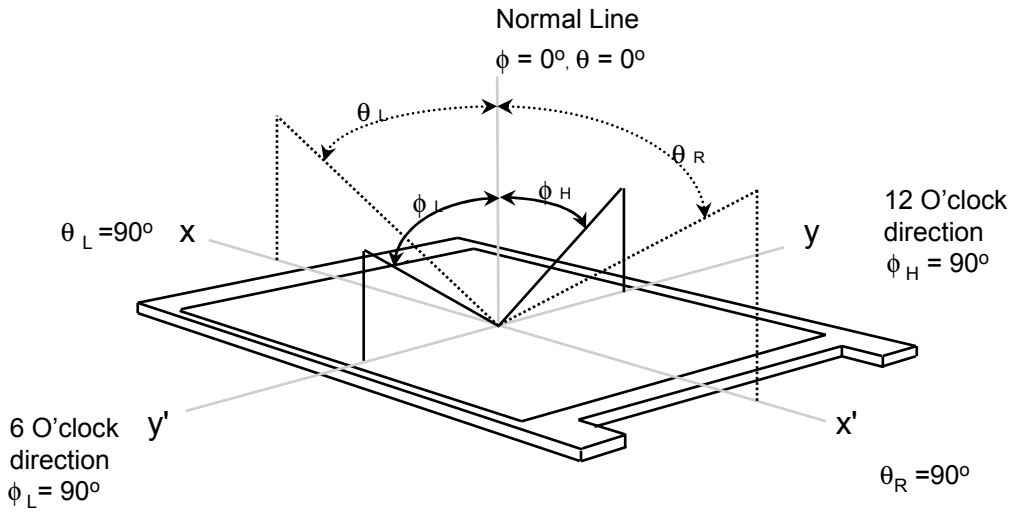
2. OPTICAL CHARACTERISTICS

The following items are measured under stable conditions. The optical characteristics should be measured in a dark room or equivalent state with the methods shown in Note (5). Measuring equipment : TOPCON SR-3

* Ta = 25 ± 2 °C, V_{DD}=3.3V, fv= 60Hz, f_{DCLK} = 72.14 MHz, I_F = 20 mA

Item		Symbol	Condition	Min.	Typ.	Max	Unit	Note
Contrast Ratio (5 Points)		CR		300	-	-	-	(1), (2), (5)
Response Time at Ta (Rising + Falling)		$T_{RT\_B/W}$		-	16	25	msec	(1), (3)
Average Luminance of White (5 Points)		$Y_{L,AVE}$	Normal Viewing Angle $\phi = 0$ $\theta = 0$	200	220	-	cd/m^2	I_L=19mA (1), (4)
Color Chromaticity (CIE)	Red	R_X		0.560	0.590	0.620	-	(1), (5) PR-650
		R_Y		0.320	0.350	0.380		
	Green	G_X		0.290	0.320	0.350		
		G_Y		0.505	0.535	0.565		
	Blue	B_X		0.125	0.155	0.185		
		B_Y		0.085	0.115	0.145		
	White	W_X		0.283	0.313	0.343		
		W_Y		0.299	0.329	0.359		
Color Gamut				-	45	-	%	
Viewing Angle	Hor.	θ_L	CR ≥ 10	40	-	-	Degrees	(1), (5) BM-5A
		θ_R		40	-	-		
	Ver.	ϕ_H		15	-	-		
		ϕ_L		30	-	-		
	Hor.	θ_L	CR ≥ 100	20	-	-	Degrees	
		θ_R		20	-	-		
	Ver.	ϕ_H		5	-	-		
		ϕ_L		10	-	-		
13 Points White Variation		δ_L		-	-	1.54	-	(6)

Note 1) Definition of Viewing Angle : Viewing angle range(10 ≤ C/R)

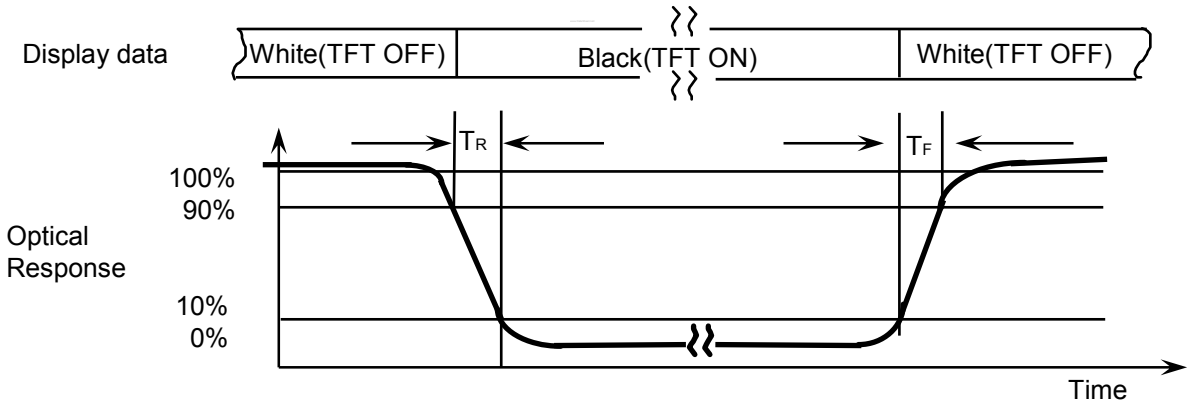


Note 2) Definition of Contrast Ratio (CR) : Ratio of gray max (Gmax) ,gray min (Gmin) at 5 points (33, 55, 77, 37, 73)

$$CR = \frac{CR(33) + CR(55) + CR(77) + CR(37) + CR(73)}{5}$$

Points : 33, 55, 77, 37, 73 at the figure of Note (6).

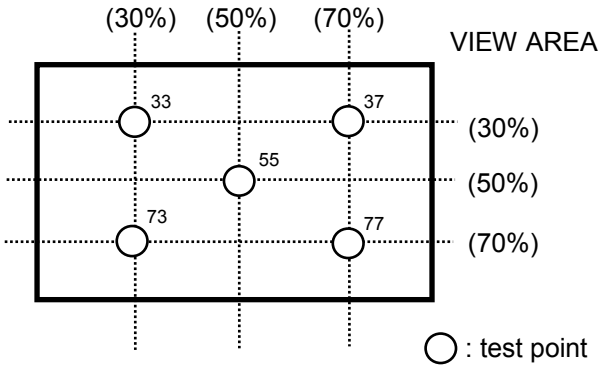
Note 3) Definition of Response time :



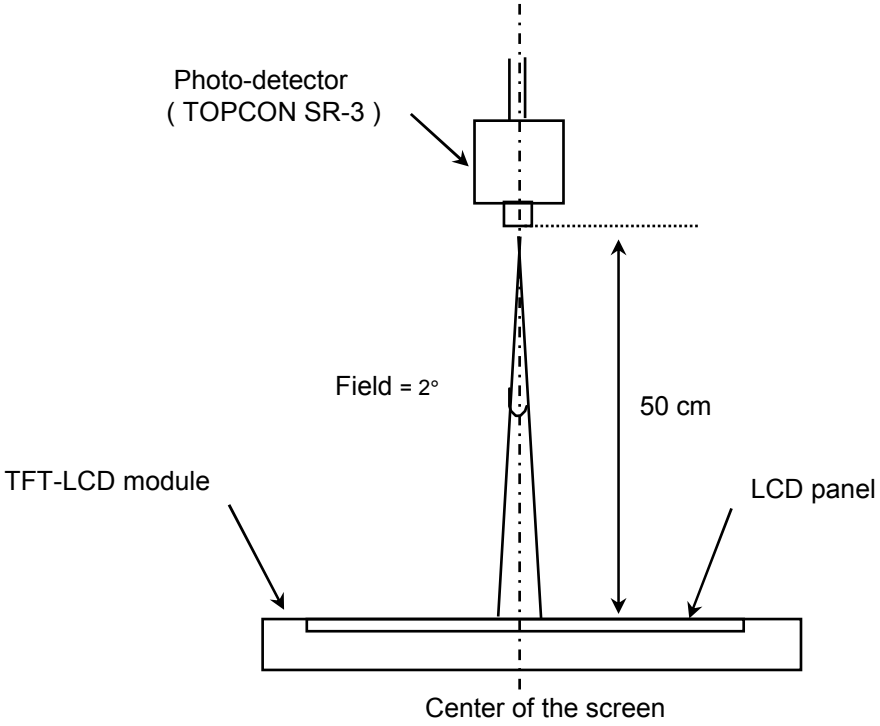
Note 4) Definition of Average Luminance of White : measure the luminance of white at 5 points.

Average Luminance of White ($Y_{L,AVE}$)

$$Y_{L,AVE} = \frac{Y_{L33} + Y_{L55} + Y_{L77} + Y_{L37} + Y_{L73}}{5}$$



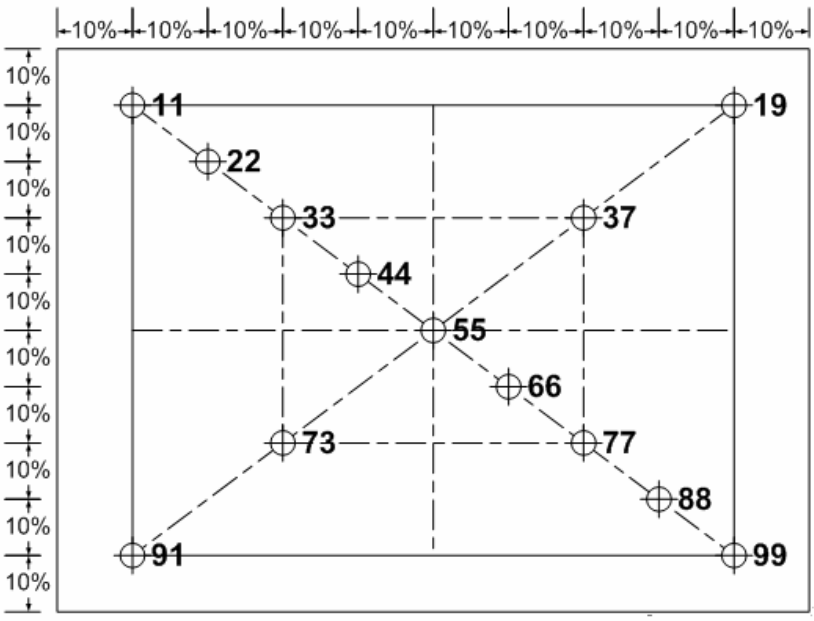
Note 5) After stabilizing and leaving the panel alone at a given temperature for 30 min , the measurement should be executed. Measurement should be executed in a stable, windless,and dark room.
30 min after lighting the backlight. This should be measured in the center of screen.
LED current : 20 mA
Environment condition : Ta = 25 ± 2 °C



[Optical characteristics measurement setup]

Note 6) Definition of 13 points white variation (δ_L), [11 ~ 99]

$$\delta_L = \frac{\text{Maximum luminance of 13 points}}{\text{Minimum luminance of 13 points}}$$



○ : test point

3. ELECTRICAL CHARACTERISTICS

3.1 TFT LCD MODULE

Ta= 25 ± 2°C

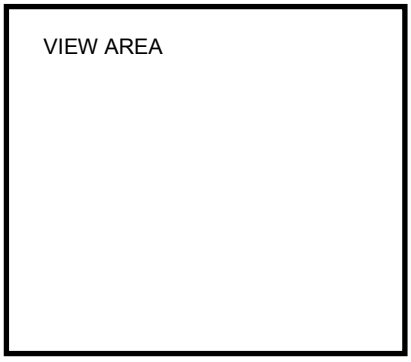
Item		Symbol	Min.	Typ.	Max.	Unit	Note
Voltage of Power Supply		V_{DD}	3.0	3.3	3.6	V	
Interface Type		eDP	eDP V1(D11) Va(Rx/Tx)				(1)
Vsync Frequency		fv	-	60	-	Hz	
Hsync Frequency		f_H	-	47.40	-	KHz	
Main Frequency		f_{DCLK}	-	72.14	-	MHz	
Rush Current		I_{RUSH}	-	-	2	A	(4)
Current of Power Supply	White	I_{DD}	-	350	-	mA	(2),(3)*a
	Mosaic		-	360	-	mA	(2),(3)*b
	Black		-	380	400	mA	(2),(3)*c

Note (1) Display Port interface characteristics should be based on VESA standard (eDP V1 draft11)

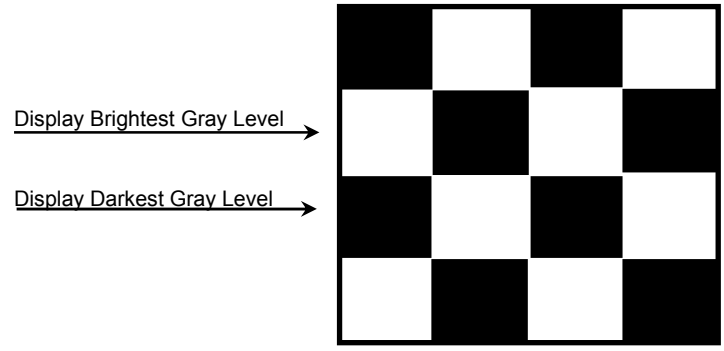
(2) f_V = 60Hz, f_{DCLK} = 72.14 MHZ, V_{DD} = 3.3V , DC Current.

(3) Power dissipation pattern

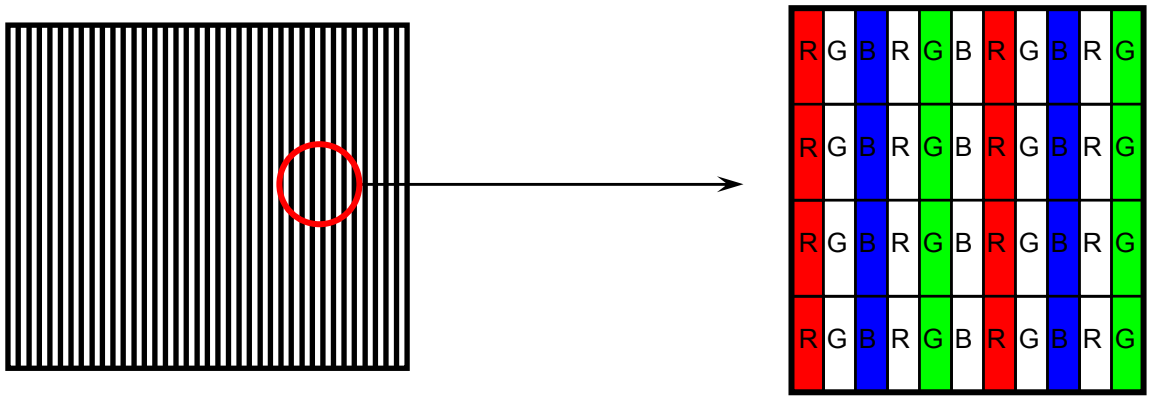
*a) White Pattern



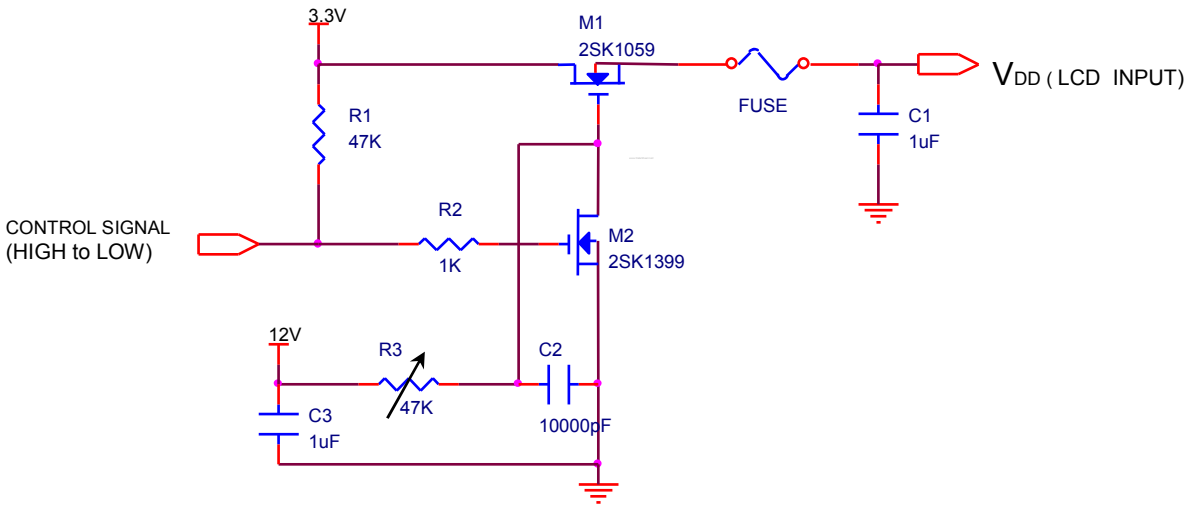
*b) Mosaic Pattern



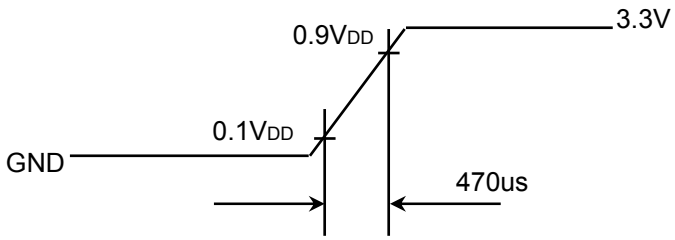
*c) 1dot Vertical stripe pattern



4) Rush current measurement condition



VDD rising time is 470us



3.2 BACK-LIGHT UNIT

Ta= 25 ± 2 °C

Item	Symbol	Min.	Typ.	Max.	Unit	Note
LED Forward Current	IF	-	20	-	mA	
LED Forward Voltage	VF	3.0	3.2	3.4	V	
LED Array Voltage	VP	27.0	28.8	30.6	V	VF X 9 LEDs
Power Consumption	P	-	-	3.5	W	IF X VF X 36 LEDs (w/ Converter Efficiency)

3.3 LED Driver

- LED Driver Manufacturer : Max17061 (Maxim)

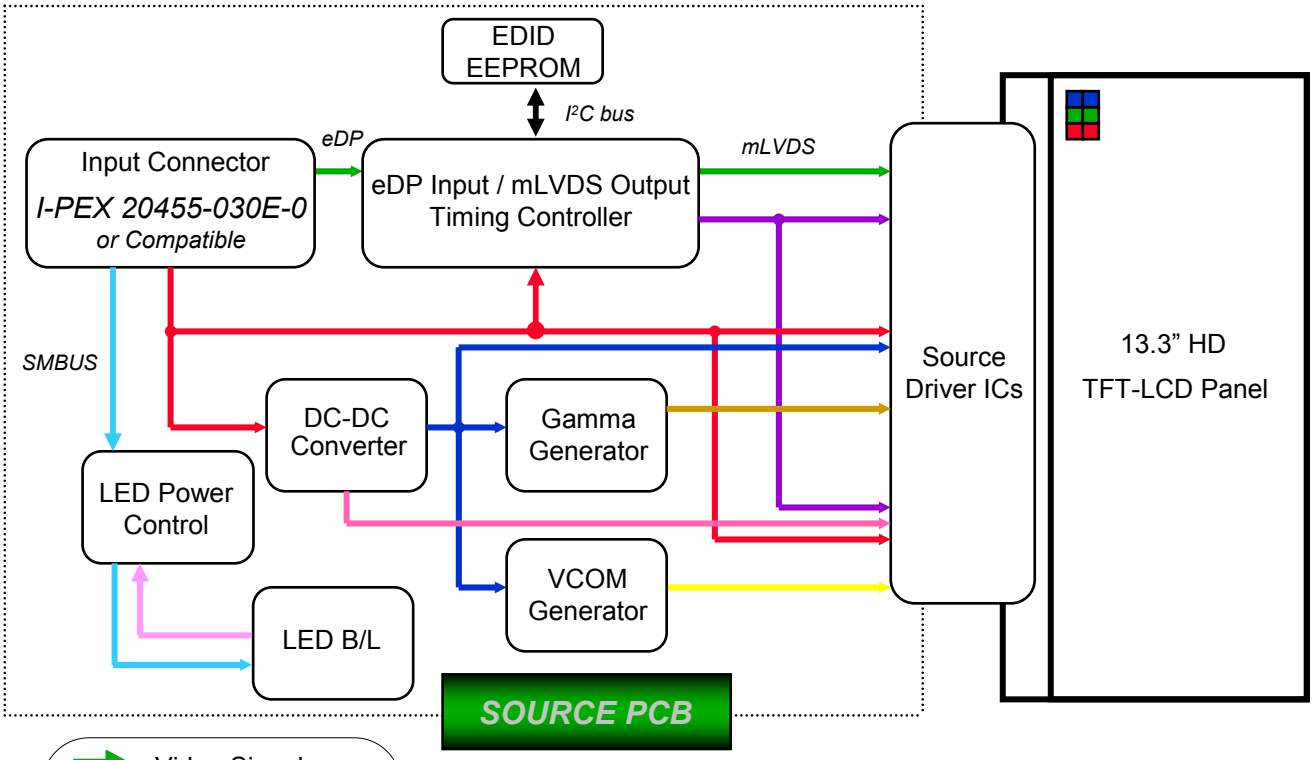
Ta= 25 ± 2 °C

Item	Symbol	Min.	Typ.	Max.	Unit	Note
Input Voltage	V_{in}	7.5	12	21	V	
Input Current	I	400	240	130	mA	
Input Power	P	3.00	2.88	2.73	W	P= V_{in} X I
Operating Frequency	F_o	0.9	-	1.1	MHz	
PWM Input Frequency	F_{PWM}	5	-	100	kHz	
PWMI Duty Cycle	D	0	-	100	%	
Output Current (each LED string)	I_{out}	28.6	30	31.4	mA	Vin=7.5~21V, RISET = 133kohm
		19.1	20	20.9	mA	Vin=7.5~21V, RISET = 200kohm
		18.1	19	19.9	mA	Vin=7.5~21V, RISET = 211kohm
		14.3	15	15.7	mA	Vin=7.5~21V, RISET = 266kohm

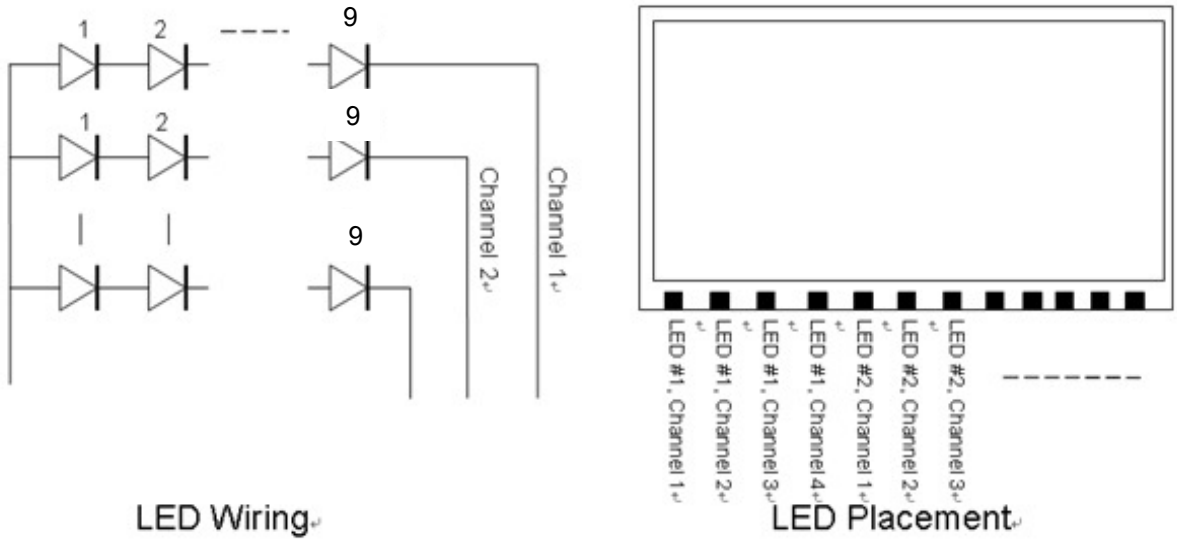
Note - Test Equipment : Fluke 45

4. BLOCK DIAGRAM

4.1 TFT LCD Module



4.2 LED connection and placement



LED Wiring

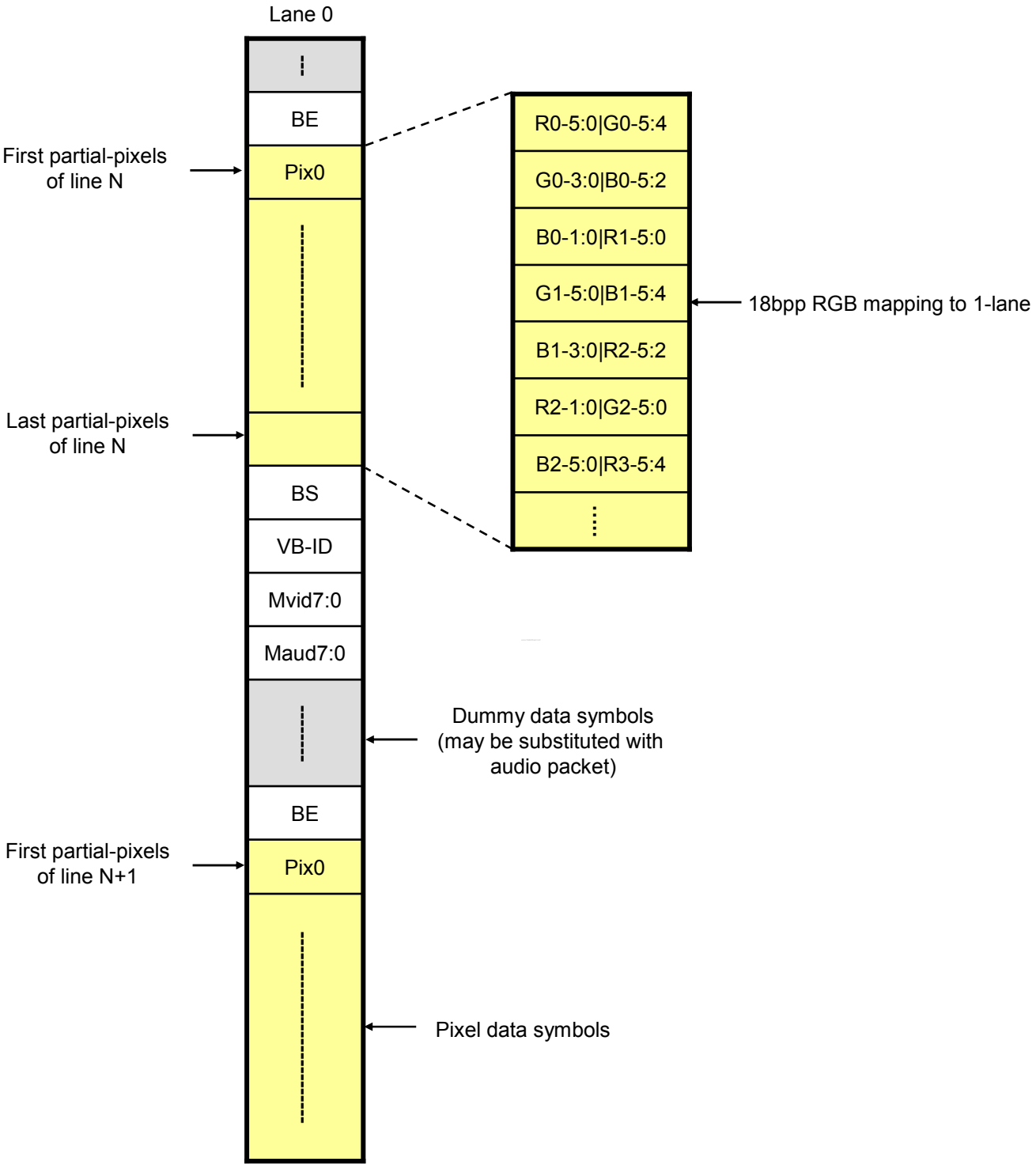
LED Placement

5. INPUT TERMINAL PIN ASSIGNMENT

5.1. Input Signal & Power (eDP, Connector : 20455-030E-02 by I-PEX or equivalent)

PIN #	Symbol	Description
1	DIAG_LOOP	Diag pin for Dell testing. Pin 1 & 30 must be connected
2	H_GND	High Speed Ground
3	NC	No Connection (Reserved for 2lane)
4	NC	No Connection (Reserved for 2lane)
5	H_GND	High Speed Ground
6	Lane0_N	Complement Signal Link - Lane 0
7	Lane0_P	True Signal Link - Lane 0
8	H-GND	High Speed Ground
9	AUX+	True Signal - Auxiliary Channel
10	AUX-	Complement Signal - Auxiliary Channel
11	H-GND	High Speed Ground
12	VCC	VCC for LCD Module (3.3V)
13	VCC	VCC for LCD Module (3.3V)
14	BIST	Build-In Self Test Enable
15	GND	Ground
16	GND	Ground
17	HPD	HPD(Hot Plug Detect) signal pin
18	BL_GND	BL Ground
19	BL_GND	BL Ground
20	BL_GND	BL Ground
21	BL_GND	BL Ground
22	NC	No Connection (Reserved)
23	BL_PWM	System PWM Signal Input
24	SMBUS_CLK	Backlight Control CLK
25	SMBUS_DATA	Backlight Control Data
26	VBL	Backlight Power
27	VBL	Backlight Power
28	VBL	Backlight Power
29	VBL	Backlight Power
30	DIAG_LOOP	Diag pin for Dell testing. Pin 1 & 30 must be connected

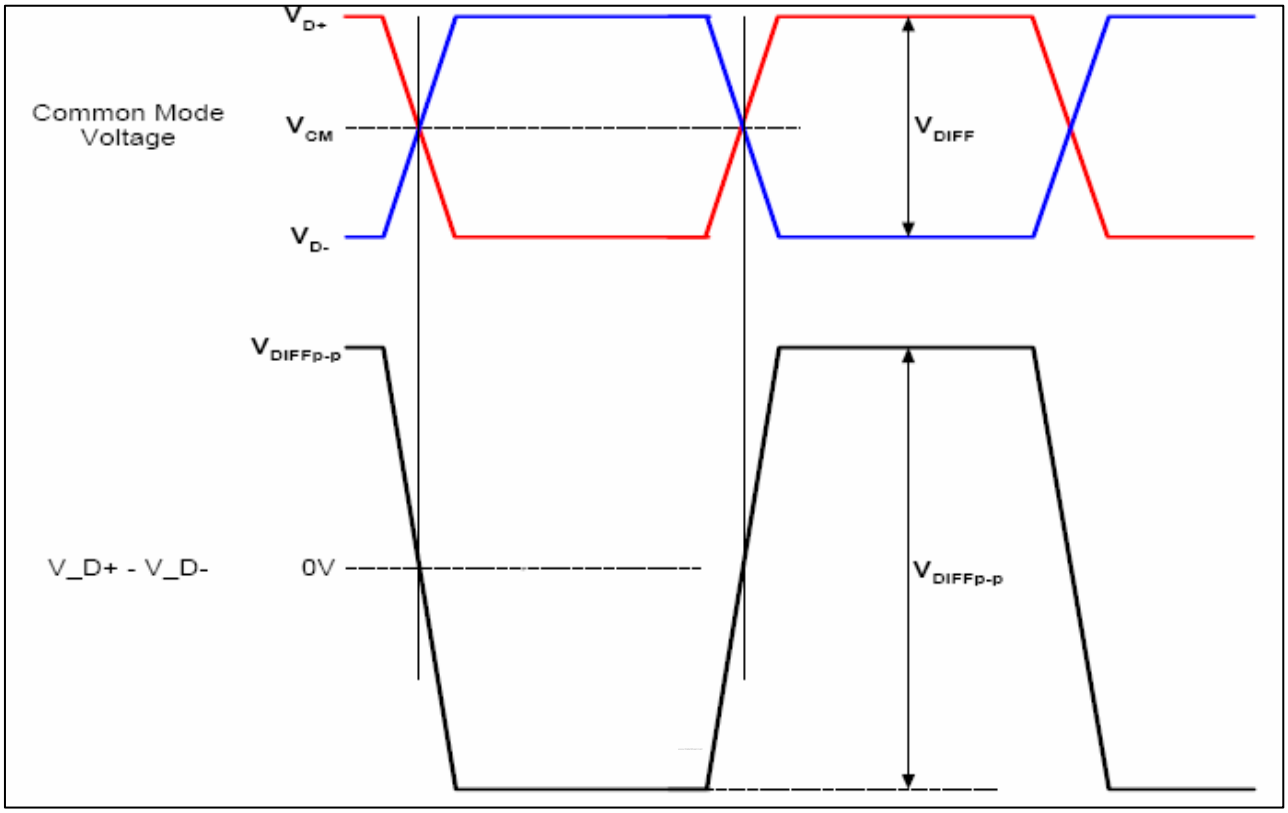
5.2 eDP Interface : (compliant to DP spec v1.1a & eDP spec v1.1)



5.3 Timing Diagrams of eDP For Transmission

eDP Receiver : Integrated T-CON

The following requirements are compliant to VESA DisplayPort Standard v1.1a



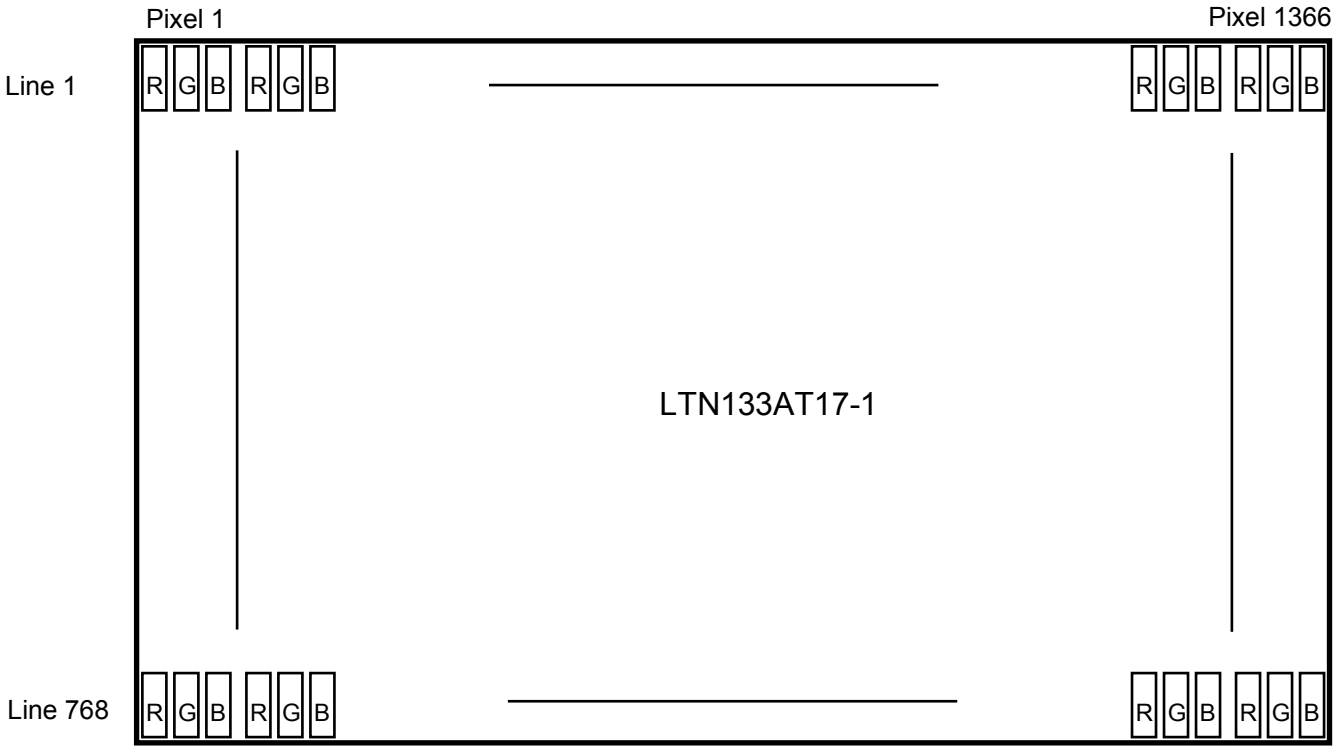
Parameter	Symbol	Min.	Typ.	Max.	Unit	Note
Receiver Jitter Tolerance (HBR)	-	1227	-	-	mUI	at 2MHz
	-	548	-	-	mUI	at 10MHz
	-	505	-	-	mUI	at 20MHz
	-	491	-	-	mUI	at 100MHz
Receiver Jitter Tolerance (HBR)	-	1648	-	-	mUI	at 2MHz
	-	778	-	-	mUI	at 10MHz
	-	747	-	-	mUI	at 20MHz
Differential peak-to-peak input voltage	$V_{RX-DIFFp-p}$	100	-	1320	mV	HBR & RBR
RX DC Common Mode Voltage	VRX-DC-CM	-	GND	-	V	-
Lane Intra-pair Skew	$L_{RX-SKEW-INTRA\_PAIR}$	-	-	150	ps	High Bit Rate
	$L_{RX-SKEW-INTRA\_PAIR}$	-	-	300	ps	Reduced Bit Rate

5.2 Input Signals, Basic Display Colors and Gray Scale of Each Color

Color	Display	Data Signal																		Gray Scale Level
		Red						Green						Blue						
		R0	R1	R2	R3	R4	R5	G0	G1	G2	G3	G4	G5	B0	B1	B2	B3	45	B5	
Basic Colors	Black	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	-
	Blue	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	-
	Green	0	0	0	0	0	0	1	1	1	1	1	1	0	0	0	0	0	0	-
	Cyan	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1	-
	Red	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	-
	Magenta	1	1	1	1	1	1	0	0	0	0	0	0	1	1	1	1	1	1	-
	Yellow	1	1	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	-
	White	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	-
Gray Scale Of Red	Black	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	R0
	Dark	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	R1
	↑	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	R2
	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	R3~R60
	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	
	↓	1	0	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	R61
	Light	0	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	R62
	Red	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	R63
Gray Scale Of Green	Black	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	G0
	Dark	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	G1
	↑	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	G2
	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	G3~G60
	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	
	↓	0	0	0	0	0	0	1	0	1	1	1	1	0	0	0	0	0	0	G61
	Light	0	0	0	0	0	0	0	1	1	1	1	1	0	0	0	0	0	0	G62
	Green	0	0	0	0	0	0	1	1	1	1	1	1	0	0	0	0	0	0	G63
Gray Scale Of Blue	Black	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	B0
	Dark	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	B1
	↑	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	B2
	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	B3~B60
	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	
	↓	0	0	0	0	0	0	0	0	0	0	0	0	1	0	1	1	1	1	B61
	Light	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	B62
	Blue	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	B63

Note 1) Definition of gray :
Rn: Red gray, Gn: Green gray, Bn: Blue gray (n=gray level)
Note 2)Input signal: 0 =Low level voltage, 1=High level voltage

5.3 Pixel Format in the display

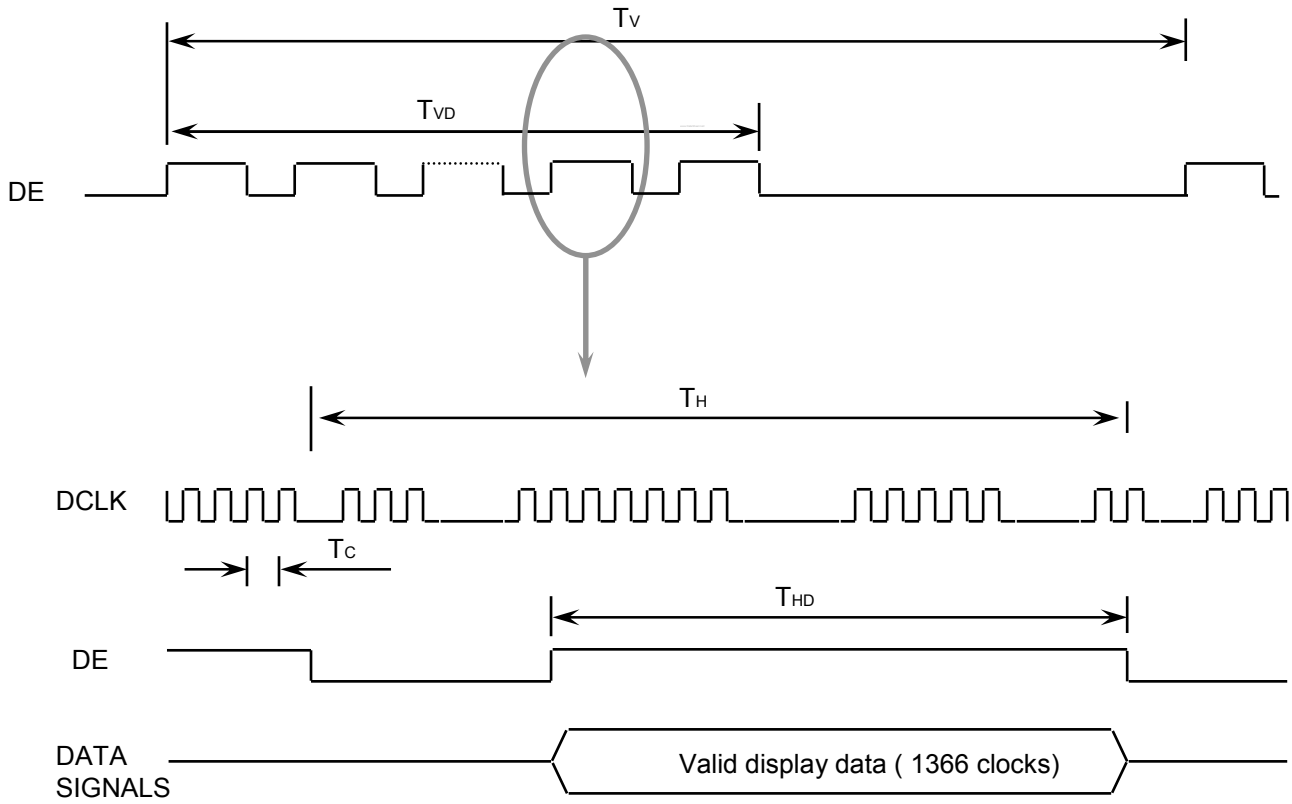


6. INTERFACE TIMING

6.1 Timing Parameters

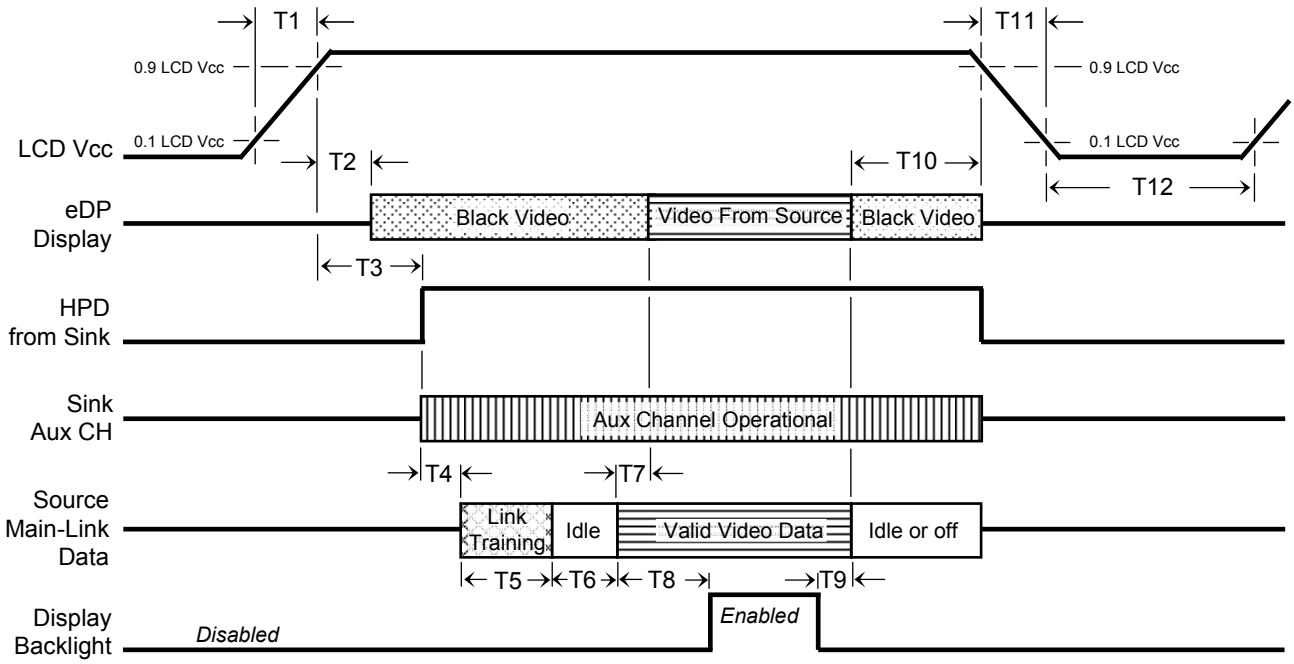
Signal	Item	Symbol	Min.	Typ.	Max.	Unit	Note
Frame Frequency	Cycle	TV	780	790	800	Lines	-
Vertical Active Display Term	Display Period	TVD	-	768	-	Lines	-
One Line Scanning Time	Cycle	TH	1450	1522	1572	Clocks	-
Horizontal Active Display Term	Display Period	THD	-	1366	-	Clocks	-

6.2 Timing diagrams of interface signal

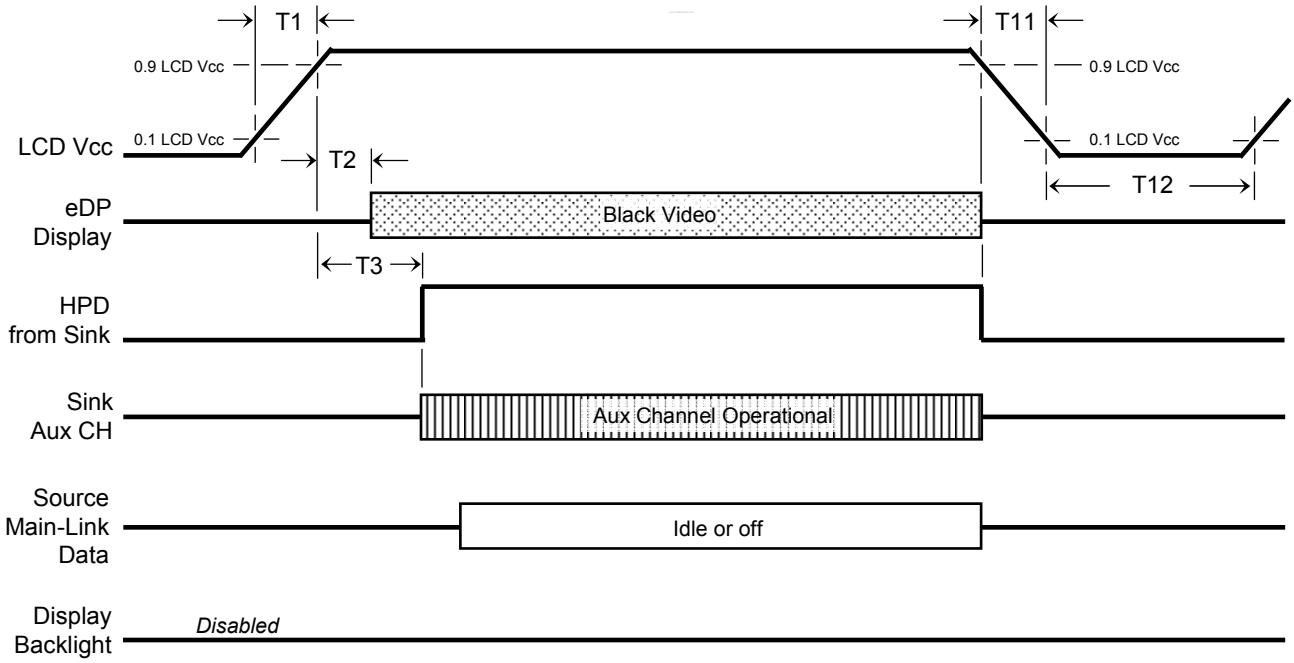


6.3 Power ON/OFF Sequence

: The Power ON/OFF sequence is described as follows :



Power ON/OFF Sequence, Normal System Operation



Power ON/OFF Sequence, Aux Channel Transaction Only

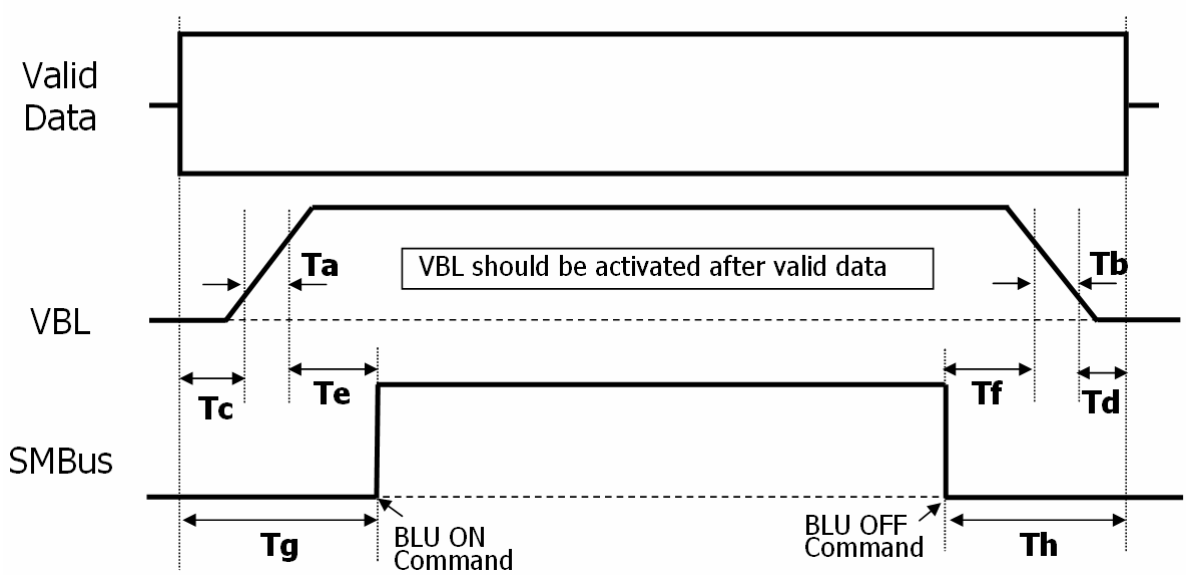
Timing Parameter	Description	Reqd. By	Limits (ms)		Notes
			Min	Max	
T1	Power rail rise time, 10% to 90%	Source	0.5	10	
T2	Delay from LCD Vcc to black video generation	Sink	0	200	Prevents display noise until valid video data is received from Source (see note1 below)
T3	Delay from LCD Vcc to HPD high	Sink	0	200	Sink Aux Channel must be operational upon HPD high
T4	Delay from HPD high to link training initialization	Source	-	-	Allows for Source to read Link capability and initialize
T5	Link training duration	Source	-	-	Dependant on Source link training protocol
T6	Link idle	Source	-	-	Min accounts for required BS-Idle pattern. Max allows for Source frame synchronization
T7	Delay from valid video data from Source to video on display	Sink	0	50	Max allows Sink validate video data and timing
T8	Delay from valid video data from Source to backlight	Source	-	-	Source must assure display video is stable
T9	Delay from backlight disable to end of valid video data	Source	-	-	Source mush assure backlight is no longer illuminated (see note 1 below)
T10	Delay from end of valid video data from Source to power off	Source	0	500	
T11	Power rail fall time, 90% to 10%	Source		10	
T12	Power off time	Source	500	-	

Power Sequence Timing Parameters

Note 1) The Sink must include the ability to generate black video autonomously. The Sink must automatically enable black video under the following conditions:
- Upon LCD Vcc power-on (within T2 max)
- When the “NoVideoStream_Flag” (VB-ID Bit 3) is received from the Source (at the end of T9)
- When no Main Link data, or invalid video data, is received from the Source. Black video must be displayed within 50ms (max) from the start of either condition. Video data can be deemed invalid based on MSA and timing information, for example.

Note 2) The Sink may implement the ability to disable the black video function, as described in Notes 1, above, for system development and debugging purposes.

Note 3) The Sink must support Aux Channel polling by the Source immediately following LCD Vcc power-on without causing damage to the Sink device (the Source can re-try if the Sink is not ready). The Sink must be able to respond to an Aux Channel transaction with the time specified within T3 max.



#	Description	Limits (ms)		#	Description	Limits (ms)	
		Min	Max			Min	Max
Ta	VBL rising time	0.5	10	Te	VBL rising to BLU on (SMBus)	20	-
Tb	VBL falling time	0.5	10	Tf	BLU off to VBL falling (SMBus)	20	-
Tc	Valid data to VBL rising	10	-	Tg	Valid data to BLU on	200	-
Td	VBL falling to Valid data	10	-	Th	BLU off to Valid data	200	-

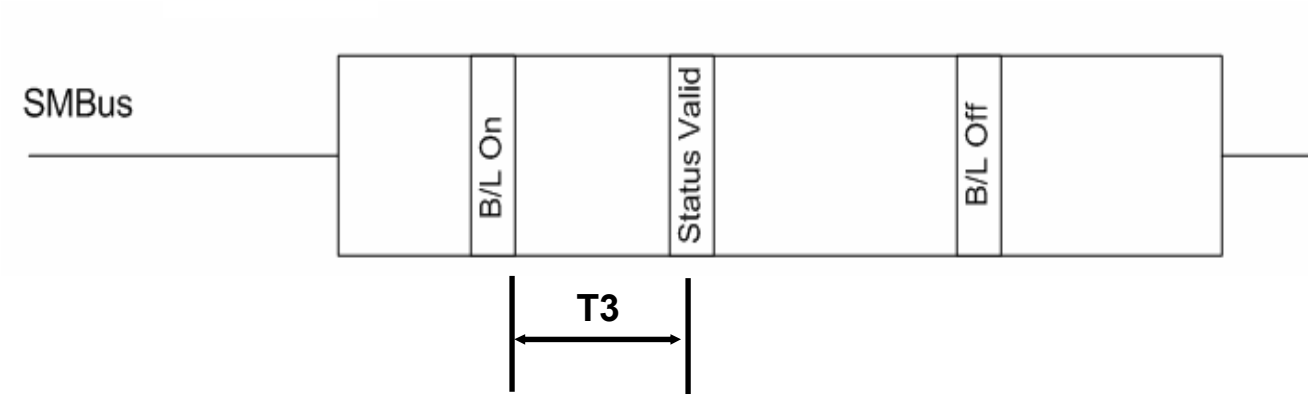
Backlight Power Sequence Timing Parameters

Note 1) VBL should follow the Valid data to prevent BLU malfunction for preventing Fuse open, IC burnt, No BLU LED by surge current

6.4 Input video tolerance of Vsync and Hsync

Resolution	Refresh Rate	Blank Mode	Pixel Clock Rate (MHz)	Color Depth Support (bpp)	Horizontal Blank(clock)			Vertical Blank(line)			Default Rom Data	
					Min	Typ	Max	Min	Typ	Max	H_ blank	V_ blank
1280x800	60Hz	Reduced	71	18/24	80	160	500	4	23	2000	160	23
1366x768	60Hz	Reduced	85.5	18/24	80	160	500	4	22	2000	160	22
1440x900	60Hz	Reduced	88.75	18/24	80	160	500	4	26	2000	160	26
1440x900	60Hz	Normal	106.5	18	80	464	500	4	34	2000	464	34
1600x900	60Hz	Reduced	97.75	18	80	160	500	4	26	2000	160	26
1280x1024	60Hz	Normal	108	18	80	432	500	4	39	2000	432	39
1400x1050	60Hz	Reduced	101	18	80	160	500	4	30	2000	160	30
1680x1050	60Hz	Reduced	119	18	80	160	500	4	30	2000	160	30

6.5 Fault / Status BIT timing



Signal	Item	Min.	Typ.	Max.	Unit	Note
Fault / status BIT timing	T3	10	-	15	mS	-

Note 1) T3 timing is SMBus “on command” to valid status / Fault register.
(Min time delay from B/L on to status register “read”.)

7. MECHANICAL OUTLINE DIMENSION

Approval

It will be attached with PDF file

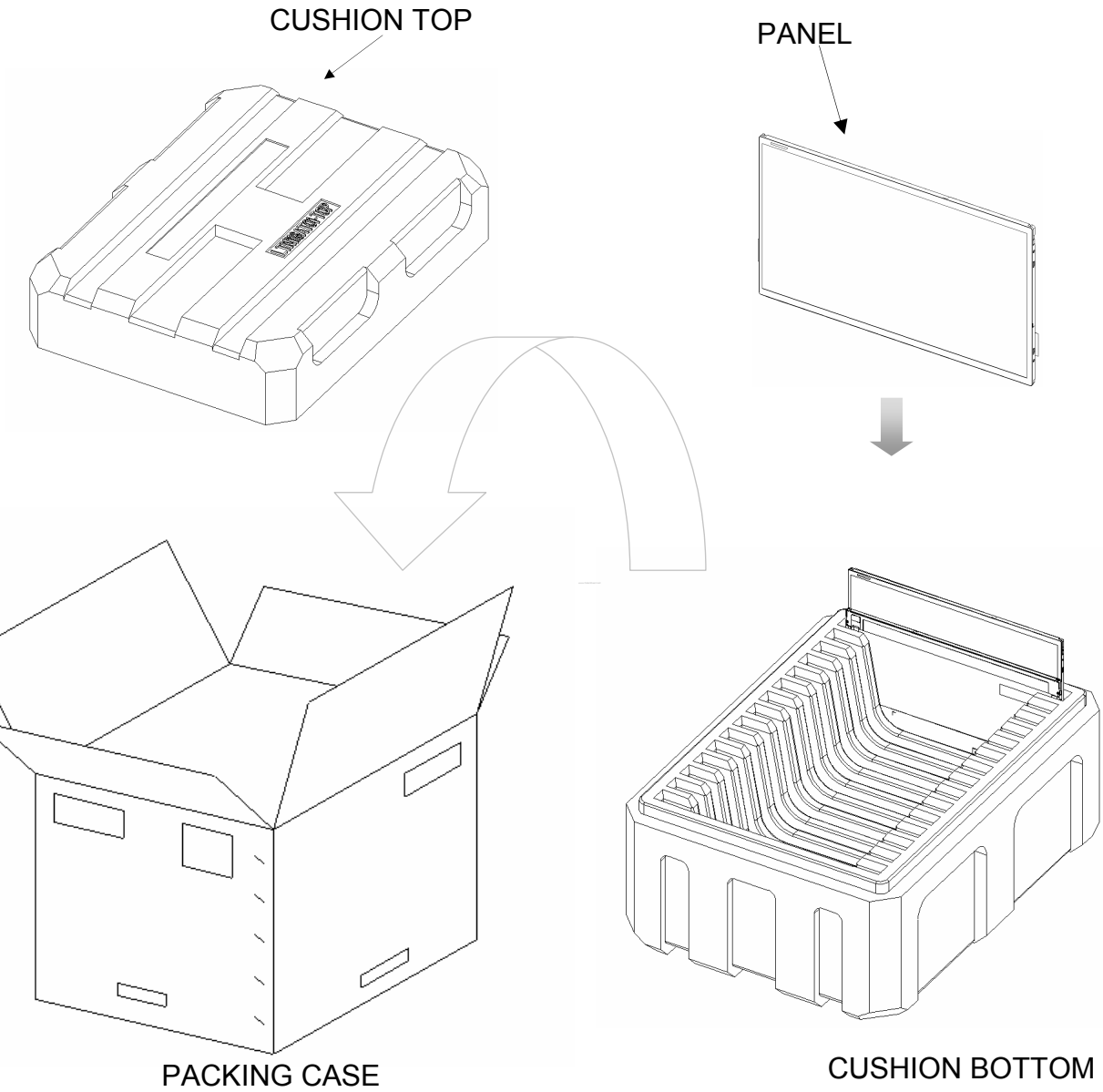
Samsung Secret

8. PACKING

1. CARTON(Internal Package)

(1) Packing Form
Corrugated Cardboard box and Corrupad form as shock absorber

(2) Packing Method



Note 1) Total Weight : Approximately 12 kg
2) Acceptance number of piling : 30 sets
3) Carton size : 418(W) x 490(D) x 301(H)

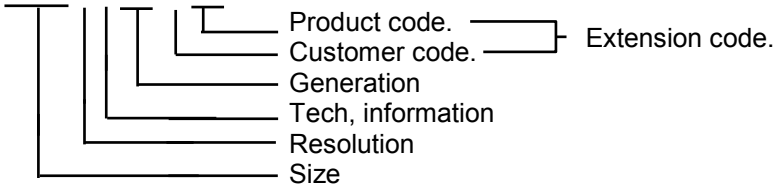
(3) Packing Material

No	Part name	Quantity
1	Static electric protective sack	30 pcs
2	Packing case (Inner box) included shock absorber	1 set
3	Pictorial marking	2 pcs
4	Carton	1 set

9. MARKINGS & OTHERS

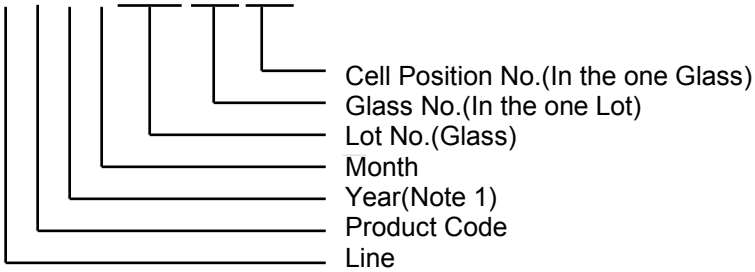
A nameplate bearing followed by is affixed to a shipped product at the specified location on each product.

(1) Parts number : LTNXXXXXXX-XXX



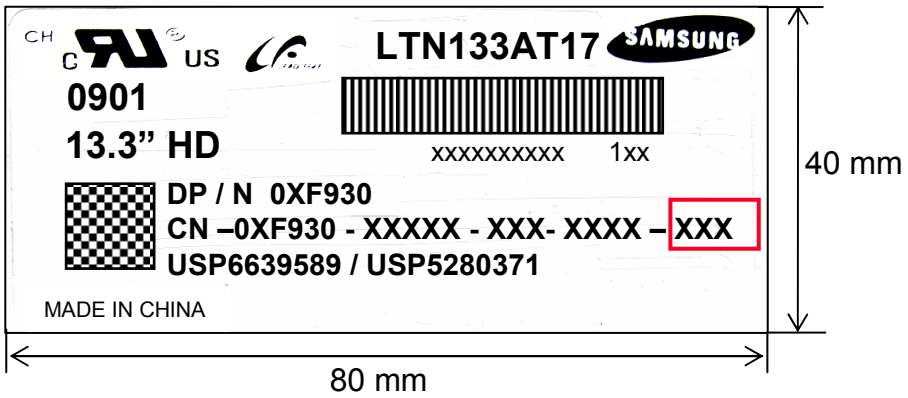
(2) Revision : Three letters

(3) Lot number : X X X X XXX XX X



NOTE 1). This code indicating year is omitted in the products of KIHEUNG site.

(4) Nameplate Indication(Following example is only for reference)



Parts name : LTN133AT17-1
Lot number : xxxxxxxxxx
Inspected work week : 0901 Number (2009 year 1st week)
DP/N : Dell Part No ("**0XF930**" is for LTN133AT17-1)
XXX : Product Revision Code

※ Panel revision code scheme (Refer to the Red box on the label)

Build Name(s)	Revision Code(s)
SST (WS)	X00, X01, X02, … X09
PT (ES)	X10, X11, X12, … X19
ST (CS)	X20, X21, X23, … X29
XB (MP)	A00, A01, A02, … A99

(6) Packing small box attach (Following example is only for reference)

0XXXXX : DELL P/N

10. GENERAL PRECAUTIONS

Approval

1. Handling

(a) When the module is assembled, It should be attached to the system firmly using every mounting holes. Be careful not to twist and bend the modules.

(b) Refrain from strong mechanical shock and / or any force to the module. In addition to damage, this may cause improper operation or damage to the module.

(c) Note that polarizers are very fragile and could be easily damaged. Do not press or scratch the surface harder than a HB pencil lead.

(d) Wipe off water droplets or oil immediately. If you leave the droplets for a long time, Staining and discoloration may occur.

(e) If the surface of the polarizer is dirty, clean it using some absorbent cotton or soft cloth.

(f) The desirable cleaners are water, IPA (Isoprophyl Alcohol) or Hexane.
Do not use Ketone type materials(ex. Acetone), Ethyl alcohol, Toluene, Ethyl acid or Methyl chloride. It might permanent damage to the polarizer due to chemical reaction.

(g) If the liquid crystal material leaks from the panel, it should be kept away from the eyes or mouth . In case of contact with hands, legs or clothes, it must be washed away thoroughly with soap.

(h) Protect the module from static , it may cause damage to the C-MOS Gate Array IC.

(i) Use fingerstalls with soft gloves in order to keep display clean during the incoming inspection and assembly process.

(j) Do not disassemble the module.

(k) Do not pull or fold the lamp wire.

(l) Do not adjust the variable resistor which is located on the back side.

(m) Protection film for polarizer on the module shall be slowly peeled off just before use so that the electrostatic charge can be minimized.

(n) Pins of I/F connector shall not be touched directly with bare hands.

2. STORAGE

(a) Do not leave the module in high temperature, and high humidity for a long time. It is highly recommended to store the module with temperature from 0 to 35 °C and relative humidity of less than 70%.

(b) Do not store the TFT-LCD module in direct sunlight.

(c) The module shall be stored in a dark place. It is prohibited to apply sunlight or fluorescent light during the store.

3. OPERATION

(a) Do not connect,disconnect the module in the " Power On" condition.

(b) Power supply should always be turned on/off by following item 6.3 " Power on/off sequence ".

(c) Module has high frequency circuits. Sufficient suppression to the electromagnetic interference shall be done by system manufacturers. Grounding and shielding methods may be important to minimize the interference.

(d) The standard limited warranty is only applicable when the module is used for general notebook applications. If used for purposes other than as specified, SEC is not to be held reliable for the defective operations. It is strongly recommended to contact SEC to find out fitness for a particular purpose.

(e) The standard limited warranty is only applicable when the module is used for general notebook applications. If used for purposes other than as specified, SEC is not to be held reliable for the defective operations. It is strongly recommended to contact SEC to find out fitness for a particular purpose.

4. OTHERS

(a) Ultra-violet ray filter is necessary for outdoor operation.

(b) Avoid condensation of water. It may result in improper operation or disconnection of electrode.

(c) Do not exceed the absolute maximum rating value. (the supply voltage variation, input voltage variation, variation in part contents and environmental temperature, so on) Otherwise the module may be damaged.

(d) If the module displays the same pattern continuously for a long period of time,it can be the situation when the image "sticks" to the screen.

(e) This module has its circuitry PCB's on the rear side and should be handled carefully in order not to be stressed.

11. EDID

Approval

	Byte (hex)	Field Name and Comments	Value (hex)	Value (binary)
Header	0	Header	00	00000000
	1	Header	FF	11111111
	2	Header	FF	11111111
	3	Header	FF	11111111
	4	Header	FF	11111111
	5	Header	FF	11111111
	6	Header	FF	11111111
	7	Header	00	00000000
Vendor / Product EDID Version	8	EISA manufacture code = 3 Character ID	4C	01001100
	9	EISA manufacture code (Compressed ASCII)	A3	10100011
	0A	Panel Supplier Reserved – Product Code	41	01000001
	0B	Panel Supplier Reserved – Product Code	54	01010100
	0C	LCD module Serial No - Preferred but Optional ("0" if not used)	00	00000000
	0D	LCD module Serial No - Preferred but Optional ("0" if not used)	00	00000000
	0E	LCD module Serial No - Preferred but Optional ("0" if not used)	00	00000000
	0F	LCD module Serial No - Preferred but Optional ("0" if not used)	00	00000000
	10	Week of manufacture	FF	11111111
	11	Year of manufacture	14	00010100
	12	EDID structure version # = 1	01	00000001
	13	EDID revision # = 4	04	00000100
Display Parameters	14	Video I/P definition = Digital I/P	95	10010101
	15	Max H image size = (Rounded to cm)	1D	00011101
	16	Max V image size = (Rounded to cm)	10	00010000
	17	Display gamma = (gamma ×100)-100 = Example: (2.2× 100) – 100 = 120	78	01111000
	18	Feature support (DPM (Standby, Suspend, Active), Color Type, Other Feature)	0A	00001010
Panel Color Coordinates	19	Red/Green Low bit (RxRy/GxGy)	20	00100000
	1A	Blue/White Low bit (BxBy/WxWy)	E5	11100101
	1B	Red X Rx = 0.xxx	97	10010111
	1C	Red Y Ry = 0.xxx	59	01011001
	1D	Green X Gx = 0.xxx	52	01010010
	1E	Green Y Gy = 0.xxx	89	10001001
	1F	Blue X Bx = 0.xxx	27	00100111
	20	Blue Y By = 0.xxx	1D	00011101
	21	White X Wx = 0.xxx	50	01010000
	22	White Y Wy = 0.xxx	54	01010100
Established Timings	23	Established timings 1 (00h if not used)	00	00000000
	24	Established timings 2 (00h if not used)	00	00000000
	25	Manufacturer's timings (00h if not used)	00	00000000
Standard Timing ID	26	Standard timing ID1 (01h if not used)	01	00000001
	27	Standard timing ID1 (01h if not used)	01	00000001
	28	Standard timing ID2 (01h if not used)	01	00000001
	29	Standard timing ID2 (01h if not used)	01	00000001
	2A	Standard timing ID3 (01h if not used)	01	00000001
	2B	Standard timing ID3 (01h if not used)	01	00000001
	2C	Standard timing ID4 (01h if not used)	01	00000001
	2D	Standard timing ID4 (01h if not used)	01	00000001
	2E	Standard timing ID5 (01h if not used)	01	00000001
	2F	Standard timing ID5 (01h if not used)	01	00000001
	30	Standard timing ID6 (01h if not used)	01	00000001
	31	Standard timing ID6 (01h if not used)	01	00000001
	32	Standard timing ID7 (01h if not used)	01	00000001
	33	Standard timing ID7 (01h if not used)	01	00000001
	34	Standard timing ID8 (01h if not used)	01	00000001
	35	Standard timing ID8 (01h if not used)	01	00000001

Timing Descripter #1	36	Pixel Clock/10,000 (LSB)	2E	00101110
	37	Pixel Clock/10,000 (MSB)	1C	00011100
	38	Horizontal Active = xxxx pixels (lower 8 bits)	56	01010110
	39	Horizontal Blanking (Thbp) = xxxx pixels (lower 8 bits)	9C	10011100
	3A	Horizontal Active/Horizontal blanking (Thbp) (upper4:4 bits)	50	01010000
	3B	Vertical Active = xxxx lines	00	00000000
	3C	Vertical Blanking (Tvbp) = xxxx lines (DE Blanking typ. for DE only panels)	16	00010110
	3D	Vertical Active : Vertical Blanking (Tvbp) (upper4:4 bits)	30	00110000
	3E	Horizontal Sync, Offset (Thfp) = xxxx pixels	30	00110000
	3F	Horizontal Sync, Pulse Width = xxxx pixels	20	00100000
	40	Vertical Sync, Offset (Tvfp) = xx lines Sync Width = xx lines	25	00100101
	41	Horizontal Vertical Sync Offset/Width upper 2 bits	00	00000000
	42	Horizontal Image Size =xxx mm	25	00100101
	43	Vertical image Size = xxx mm	A5	10100101
	44	Horizontal Image Size / Vertical image size	10	00010000
	45	Horizontal Border = 0 (Zero for Notebook LCD)	00	00000000
	46	Vertical Border = 0 (Zero for Notebook LCD)	00	00000000
	47	Bit[7] 0: Non-interlace, 1: Interlace Bit[6:5] 00: Normal display, no strero, XX: See table xx for definition Bit[4:3] 00: Analog composite, 01: Bipolar analog composite, 10: Digital composite, 11: Digital separate Bit[2:1] :The interpretation of bits 2 and 1 is dependent on the decode of bits 4 and 3 - see Table 3.18. Bit[0] :See Table VESA EDID spec for definition Referenced Default = 1Ah	1A	00011010
Timing Descripter #2	48	Pixel Clock/10,000 (LSB)	C9	11001001
	49	Pixel Clock/10,000 (MSB)	12	00010010
	4A	Horizontal Active = xxxx pixels (lower 8 bits)	56	01010110
	4B	Horizontal Blanking (Thbp) = xxxx pixels (lower 8 bits)	9C	10011100
	4C	Horizontal Active/Horizontal blanking (Thbp) (upper4:4 bits)	50	01010000
	4D	Vertical Active = xxxx lines	00	00000000
	4E	Vertical Blanking (Tvbp) = xxxx lines (DE Blanking typ. for DE only panels)	16	00010110
	4F	Vertical Active : Vertical Blanking (Tvbp) (upper4:4 bits)	30	00110000
	50	Horizontal Sync, Offset (Thfp) = xxxx pixels	30	00110000
	51	Horizontal Sync, Pulse Width = xxxx pixels	20	00100000
	52	Vertical Sync, Offset (Tvfp) = xx lines Sync Width = xx lines	25	00100101
	53	Horizontal Vertical Sync Offset/Width upper 2 bits	00	00000000
	54	Horizontal Image Size =xxx mm	25	00100101
	55	Vertical image Size = xxx mm	A5	10100101
	56	Horizontal Image Size / Vertical image size	10	00010000
	57	Horizontal Border = 0 (Zero for Notebook LCD)	00	00000000
	58	Vertical Border = 0 (Zero for Notebook LCD)	00	00000000
	59	Bit[7] 0: Non-interlace, 1: Interlace Bit[6:5] 00: Normal display, no strero, XX: See table xx for definition Bit[4:3] 00: Analog composite, 01: Bipolar analog composite, 10: Digital composite, 11: Digital separate Bit[2:1] :The interpretation of bits 2 and 1 is dependent on the decode of bits 4 and 3 - see Table 3.18. Bit[0] :See Table VESA EDID spec for definition Referenced Default = 1Ah	1A	00011010

Timing Descripter #3 Dell specific information	5A	Flag	00	00000000
	5B	Flag	00	00000000
	5C	Flag	00	00000000
	5D	Data Type Tag: Alphanumeric Data String (ASCII)	FE	11111110
	5E	Flag	00	00000000
	5F	Dell P/N 1st Character	58	01011000
	60	Dell P/N 2nd Character	46	01000110
	61	Dell P/N 3rd Character	39	00111001
	62	Dell P/N 4th Character	33	00110011
	63	Dell P/N 5th Character	30	00110000
	64	LCD Supplier EEDID Revision # Bit[7] : 0=X, 1=A Bit[6:0] : 00, 01, 02…for SST 10, 11, 12…for PT 20, 21, 22…for ST 00, 01, 02…for X-Build (if Bit[7]=1)	80	10000000
	65	Manufacturer P/N	31	00110001
	66	Manufacturer P/N	33	00110011
	67	Manufacturer P/N	33	00110011
	68	Manufacturer P/N	41	01000001
	69	Manufacturer P/N	54	01010100
	6A	Manufacturer P/N	0A	00001010
	6B	Manufacturer P/N (If <13 char, then terminate with ASCII code 0Ah, set remaining char = 20h)	20	00100000
Timing Descripter #4	6C	Flag	00	00000000
	6D	Flag	00	00000000
	6E	Flag	00	00000000
	6F	Data Type Tag: Manufacturer Specified Data 00	00	00000000
	70	Flag	00	00000000
	71	Color Management (True Color Depth, 2-bit FRC)	00	00000000
	72	Panel Type & Configurations (Bulb/LED string #, Structure Revision, Panel Structure)	41	01000001
	73	Frame Rate Details (SDRRS, DRRS, Max Frame Rate, Min Frame Rate)	01	00000001
	74	Light Controller Interface and Maximum Typical Luminance	16	00010110
	75	Front Surface / Polarizer and Pixel Structure (Transflective, AG/Glossy)	00	00000000
	76	Multi-Media Features (Dynamic Backlight Control, Color Management)	00	00000000
	77	Multi-Media Features (Active Gamma Control, Motion Blur)	00	00000000
	78	Special Features #1 (In-Cell Scanner, Wireless)	00	00000000
	79	Special Features #2 (In-Cell Touch, Interface, Over Drive, LVDS Channel or eDP Lane)	09	00001001
	7A	Special Features #3 (3D, E-Privacy, BIST Support)	01	00000001
	7B	(If <13 char, then terminate with ASCII code 0Ah, set remaining char = 20h)	0A	00001010
	7C	(If <13 char, then terminate with ASCII code 0Ah, set remaining char = 20h)	20	00100000
	7D	(If <13 char, then terminate with ASCII code 0Ah, set remaining char = 20h)	20	00100000
Checksum	7E	Extension flag (# of optional 128 EDID extension blocks to follow, Typ = 0)	00	00000000
	7F	Checksum (The 1-byte sum of all 128 bytes in this EDID block shall = 0)	9D	10011101