16V_{IN}, 12A Ultralow Noise Silent Switcher 3 µModule Regulator

FEATURES

- **Complete Solution in <1cm² (Single-Sided PCB) or 0.5cm² (Dual-Sided PCB)**
- **Low Noise Silent Switcher®3 Architecture**
  - **Ultralow EMI Emissions**
  - **Ultralow RMS Noise (10Hz to 100kHz): 8µV_{RMS}**
- **±1.5% Maximum Total DC Output Voltage Error Over Line, Load, and Temperature**
- Input Voltage Range: 3V to 16V
- Output Voltage Range: 0.3V to 6V
- 12A Maximum Continuous Output Current
- Adjustable and Synchronizable: 300kHz to 3MHz
- Current Mode Control, Fast Transient Response
- Forced Continuous Mode (FCM) Capability
- Multiphase Parallel with Current Sharing
- Programmable Power Good
- 6.25mm × 6.25mm × 5.07mm BGA Package

APPLICATIONS

- Telecom, Networking, and Industrial Equipment
- RF Power Supplies: PLLs, VCOs, Mixers, LNAs, PAs
- Low Noise Instrumentation
- High Speed/High Precision Data Converters
- Medical Equipment

DESCRIPTION

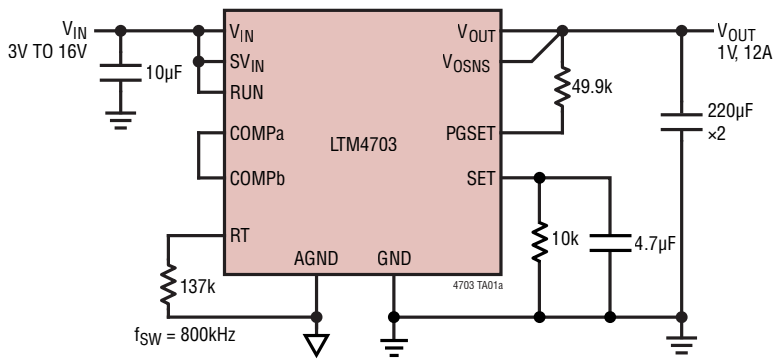
The LTM®4703 is a complete 12A step-down Silent Switcher 3 µModule® (micromodule) regulator in a tiny 6.25mm × 6.25mm × 5.07mm ball grid array (BGA) package.The package includes the switching controller, the power MOSFETs, an inductor, and support components. Operating over an input voltage range of 3V to 16V, the LTM4703 supports an output range of 0.3V to 6V. A single resistor sets the output voltage, providing unity gain operation over the output range and resulting in virtually constant output noise independent of the output voltage. Only bulk input and output capacitors are needed to finish the design.

The LTM4703 employs Silent Switcher 3 architecture with internal hot loop bypass capacitors to achieve both low electromagnetic interference (EMI) and high efficiency. Also, the LTM4703 has an ultralow noise architecture to obtain exceptional low-frequency (<100kHz) output noise. These low EMI and low noise features make the LTM4703 ideal for high current and noise-sensitive applications, which benefit from the high efficiency of a synchronous switching regulator.

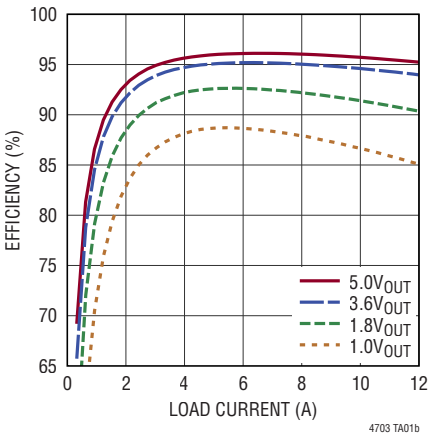
The LTM4703 is available with a RoHS-compliant terminal finish.

TYPICAL APPLICATION

3V to 16V Input to 1V, 12A Output



Efficiency, 12V_{IN}, f_{SW} = 800kHz

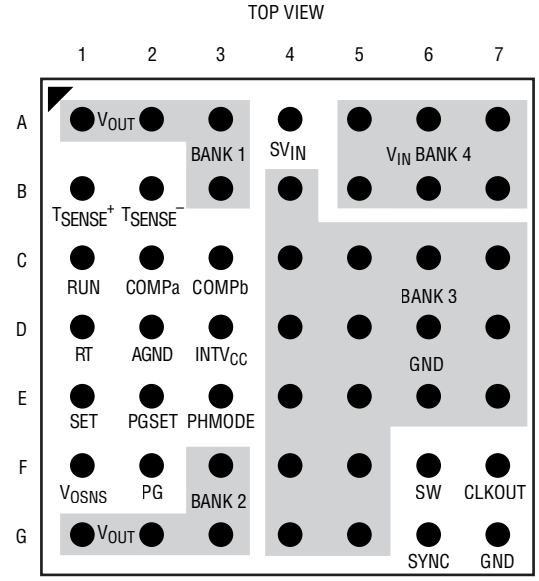


ABSOLUTE MAXIMUM RATINGS

(Notes 1, 2)

V_{IN}, SV_{IN}, RUN, PG 18V
SYNC, PGSET 6V
V_{OUT}, V_{OSNS}, SET 6.3V
PHMODE, COMPa, RT 4V
T_{SENSE}^+ to T_{SENSE}^- (Current) 5mA
Internal Operating Junction Temperature Range
E-Grade, I-Grade ..... –40°C to 125°C
Storage Temperature Range ..... –55°C to 125°C
Peak Solder Reflow Body Temperature ..... 250°C

PIN CONFIGURATION



BGA PACKAGE
49-PIN (6.25mm × 6.25mm × 5.07mm)
T_{JMAX} = 125°C, θ_{JA} = 19.6°C/W, θ_{JCtop} = 15.2°C/W,
$\theta_{JCbottom}$ = 4.0°C/W, WEIGHT = 0.7g

θ VALUES ARE DETERMINED BY SIMULATION PER JESD-51 CONDITIONS.
θ_{JA} VALUE IS OBTAINED WITH EVALUATION BOARD.
SEE THE TYPICAL PERFORMANCE CHARACTERISTICS SECTION FOR LAB MEASUREMENT AND DERATING CURVES.

ORDER INFORMATION

PART NUMBER	PAD OR BALL FINISH*	PART MARKING		PACKAGE TYPE	MSL RATING	TEMPERATURE RANGE (SEE NOTE 2)
		DEVICE	FINISH CODE			
LTM4703EY#PBF	SAC305 (RoHS)	4703	e1	BGA	4	–40°C to 125°C
LTM4703IY#PBF	SAC305 (RoHS)	4703	e1	BGA	4	–40°C to 125°C

- Contact the factory for parts specified with wider operating temperature ranges. *Pad or ball finish code is per IPC/JEDEC J-STD-609.
- Recommended LGA and BGA PCB Assembly and Manufacturing Procedures
- LGA and BGA Package and Tray Drawings

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications that apply over the specified internal operating junction temperature range (Note 2), otherwise specifications are at T_A = 25°C, V_{IN} = 12V, per the typical application (Note 5).

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{IN}	Power Input DC Voltage		●	3		16	V
SV_{IN}	Signal Input DC Voltage (Note 8)		●	3		16	V
$V_{OUT(RANGE)}$	Output Voltage Range	V_{PGSET} = 0.5V	●	0.3		6	V
$V_{OUT(DC)}$	Output Voltage, Total Variation with Line and Load	V_{SET} = 1V, V_{IN} = 3V to 16V, SV_{IN} = 6V, I_{OUT} = 100mA to 12A (Note 7)	●	0.985	1	1.015	V
I_{SET}	SET Pin Current	V_{IN} = SV_{IN} = 6V, V_{SET} = 1V		99.2	100	100.8	µA
I_{SET_START}	Fast Start-Up Set Pin Current	V_{IN} = SV_{IN} = 12V, V_{SET} = 1V, V_{PGSET} = 0V		2.2	2.7	3.2	mA
t_{START}	Start-Up Time (Notes 3, 9)	V_{OUT} = 1V, C_{SET} = 1µF, V_{PGSET} = 0.5V V_{OUT} = 1V, C_{SET} = 4.7µF, V_{PGSET} = 0.5V V_{OUT} = 1V, C_{SET} = 1µF, R_{PGSET} = 49.9k V_{OUT} = 1V, C_{SET} = 4.7µF, R_{PGSET} = 49.9k			25 120 1 2.5		ms ms ms ms
V_{RUN}	RUN Pin ON Threshold	V_{IN} = SV_{IN} = 6V, V_{RUN} Rising	●	1.27	1.32	1.37	V
	RUN Pin Hysteresis				50		mV
I_{RUN}	RUN Pin Input Current	V_{IN} = SV_{IN} = 6V, V_{RUN} = 2V		–40		40	nA
I_{Q_SVIN}	SV_{IN} Quiescent Current	SV_{IN} = 12V, V_{RUN} = 0V, Shutdown SV_{IN} = 12V, R_T = 47k, FCM			50 40		µA mA
$V_{OUT\_SPOTNOISE}$	Output Noise Spectral Density (2kHz) (Notes 3, 4, 6, 7)	SV_{IN} = 12V, V_{OUT} = 1V, C_{OUT} = 200µF, R_{SET} = 10k, C_{SET} = 4.7µF, f_{SW} = 2MHz			4		$nV/\sqrt{Hz}$
$V_{OUT\_RMSNOISE}$	Output RMS Noise (10Hz to 100kHz) (Notes 3, 4, 6, 7)	SV_{IN} = 12V, V_{OUT} = 1V, BW = 10Hz to 100kHz, I_{OUT} = 0.5A, C_{OUT} = 200µF, R_{SET} = 10k, C_{SET} = 4.7µF, 2MHz			8		$µV_{RMS}$
$I_{OUT(DC)}$	Output Continuous Current	V_{IN} = 12V, V_{OUT} = 1V (Note 4)				12	A
ΔV_{OUT} (LINE)/ V_{OUT}	Output Voltage Line Regulation	V_{OUT} = 1V, V_{IN} = 3V to 16V, SV_{IN} = 6V, I_{OUT} = 100mA, V_{SET} = 1V	●		0.025	0.1	%/V
ΔV_{OUT} (LOAD)/ V_{OUT}	Output Voltage Load Regulation	V_{OUT} = 1V, V_{IN} = 6V, SV_{IN} = 6V, I_{OUT} = 100mA to 12A, V_{SET} = 1V	●			1.35	%
I_{VOSNS}	V_{OSNS} Output Current			80	160	240	nA
$V_{OUT(AC)}$	Output Ripple Voltage (Note 3)	I_{OUT} = 100mA, C_{OUT} = 400µF, V_{IN} = 12V, V_{OUT} = 1V, R_T = 137k			8		mV
$I_{SHORT\_CIRCUIT}$	Output Short-Circuit	V_{IN} = 16V, SV_{IN} = 6V, V_{OUT} = 1V			24		A
I_{OUT_PK}	Output Current Limit	V_{IN} = 16V, SV_{IN} = 6V, V_{OUT} = 1V			19		A
t_{ON_MIN}	Minimum On-Time	V_{IN} = 16V, SV_{IN} = 6V			17		ns
V_{PGSET}	PGSET Upper Threshold PGSET Upper Threshold Hysteresis PGSET Lower Threshold PGSET Lower Threshold Hysteresis	V_{IN} = 6V, SV_{IN} = 6V, PGSET Rising PGSET Falling		525 455	540 7 465 7	550 475	mV mV mV mV
I_{PGSET}	PGSET Pin Current	V_{IN} = 6V, SV_{IN} = 6V, V_{PGSET} = 0.5V			10		µA
I_{PG}	PG Leakage	V_{IN} = 12V, SV_{IN} = 0V, V_{PG} = 3.3V		–40		40	nA
R_{PG}	PG Pull-Down Resistance	V_{PG} = 0.5V			380	650	Ω
f_{OSC}	Oscillator Frequency	R_T = 392k R_T = 47k R_T = 28.7k			300 2 3		kHz MHz MHz
SYNC_LEVEL	SYNC Threshold	V_{IN} = SV_{IN} = 6V SYNC DC and Clock Low-Level Voltage SYNC DC and Clock High-Level Voltage		 0.7		 1.5	 V V
V_{PHMODE}	PHMODE Thresholds	V_{IN} = SV_{IN} = 6V 180° Phase Shift 90° Phase Shift		 2.7		 0.7 	 V V

ELECTRICAL CHARACTERISTICS

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect the device's reliability and lifetime.

Note 2: The LTM4703 is tested under pulsed load conditions such that $T_J \approx T_A$. The LTM4703E is guaranteed to meet performance specifications over the 0°C to 125°C internal operating temperature range. Specifications over the full –40°C to 125°C internal operating temperature range are assured by design, characterization, and correlation with statistical process controls. The LTM4703I is guaranteed to meet specifications over the full –40°C to 125°C internal operating temperature range. Note that the maximum ambient temperature consistent with these specifications is determined by specific operating conditions in conjunction with board layout, the rated package thermal resistance, and other environmental factors.

Note 3: Not subject to the production test.

Note 4: V_{OSNS} connects directly to V_{OUT}.

Note 5: The EC table test circuits and the test conditions could be different than typical applications.

Note 6: Adding a capacitor across the SET pin resistor decreases the output voltage noise. Adding this capacitor bypasses the SET pin resistor's thermal noise and the reference current's noise. The use of a SET pin bypass capacitor also increases start-up time.

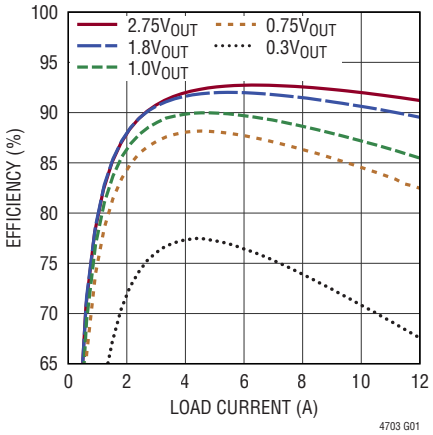
Note 7: See the output current derating curves for different V_{IN}, V_{OUT}, and T_A values in the Typical Performance Characteristics section.

Note 8: SV_{IN} supplies current to the internal circuitry and regulator. SV_{IN} should be above 4V to achieve regulation of ±1.5% maximum total DC output voltage error over line, load, and temperature. Also, to provide sufficient headroom for the SET pin current reference, SV_{IN} must be 0.4V higher than the desired V_{OUT}.

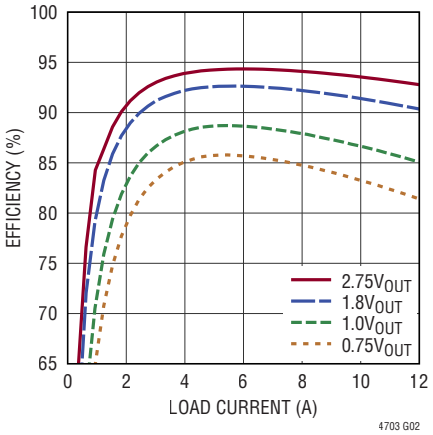
Note 9: The start-up time is defined as the time it takes from the RUN pin rising above the RUN threshold to when the V_{OUT} has reached 90% of final values.

TYPICAL PERFORMANCE CHARACTERISTICS T_A = 25°C, unless otherwise noted.

Efficiency vs Load, $12V_{IN}$, f_{SW} = 400kHz



Efficiency vs Load, $12V_{IN}$, f_{SW} = 600kHz



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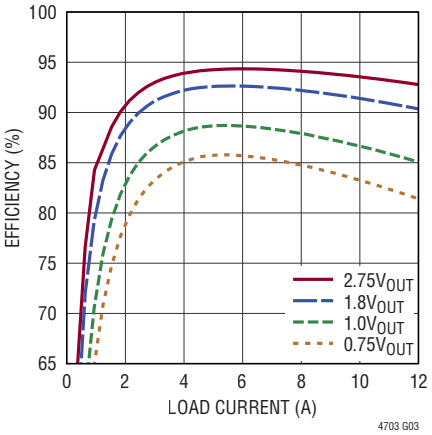

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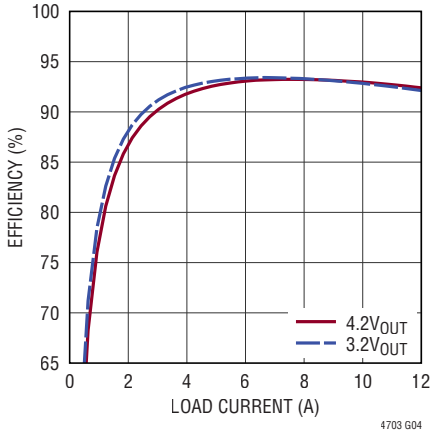

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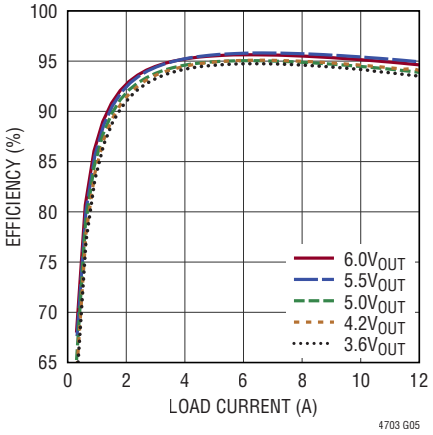

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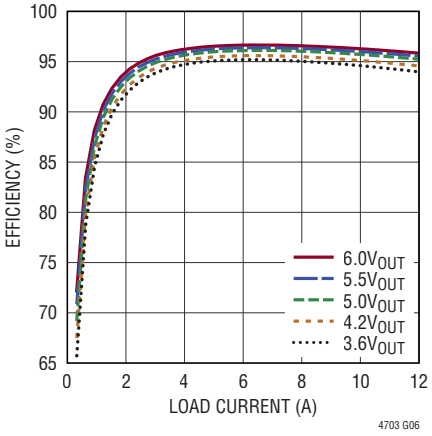
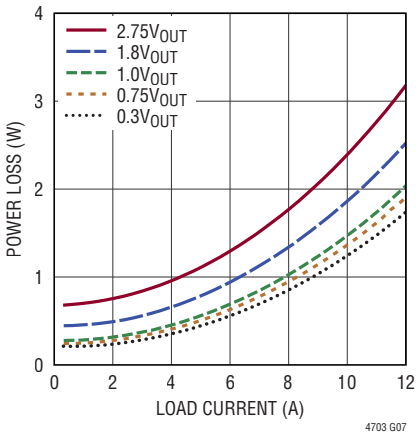


Power Loss vs Load, 12V_{IN}, f_{SW} = 400kHz



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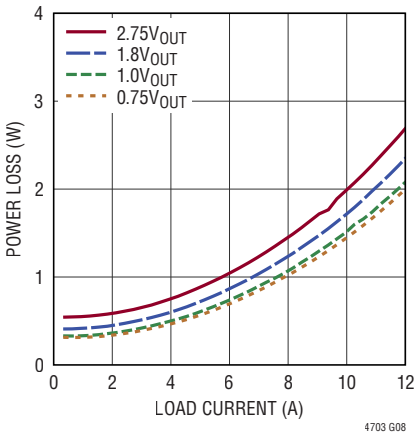

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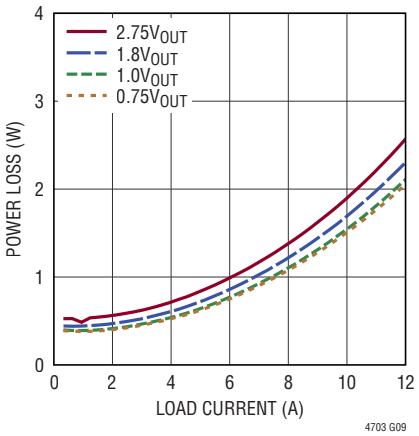

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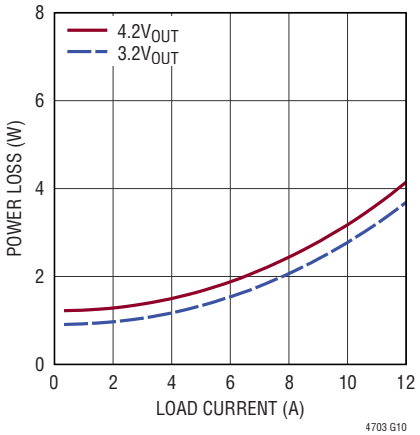

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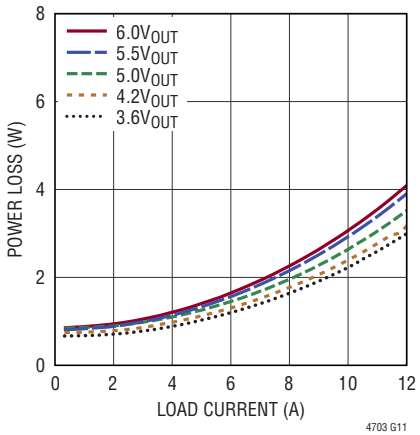

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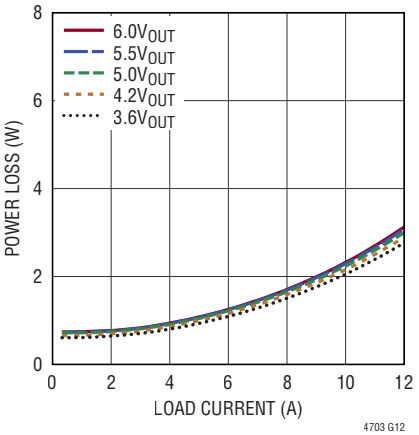
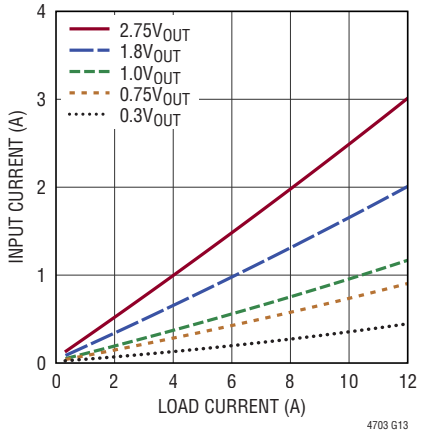


TYPICAL PERFORMANCE CHARACTERISTICS T_A = 25°C, unless otherwise noted.

Input vs Load, $12V_{IN}$, f_{SW} = 400kHz



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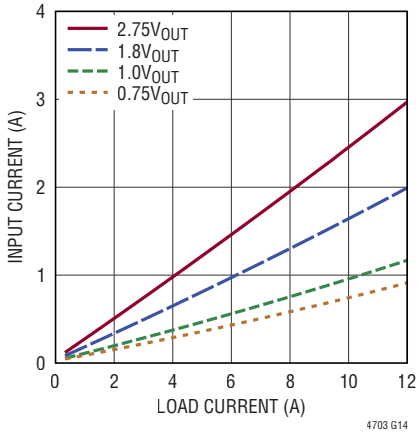

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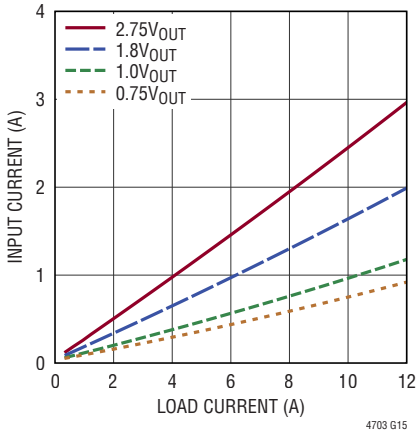

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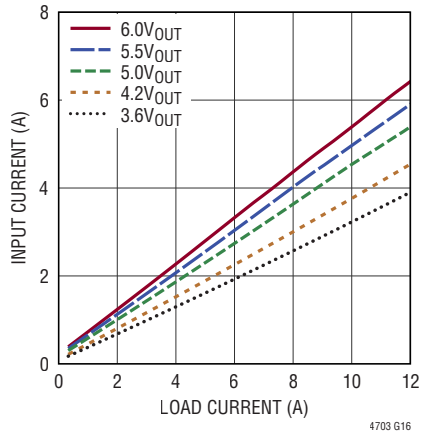

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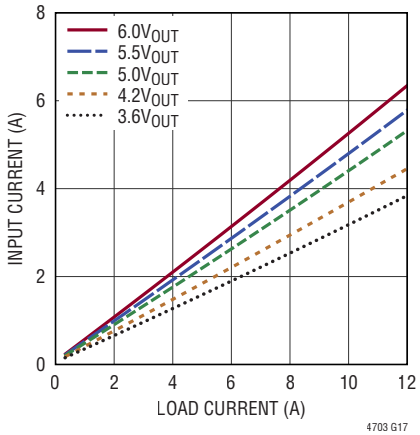
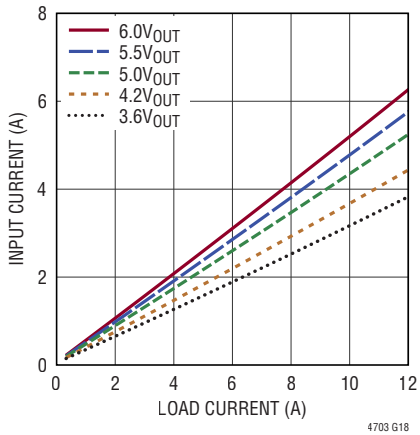
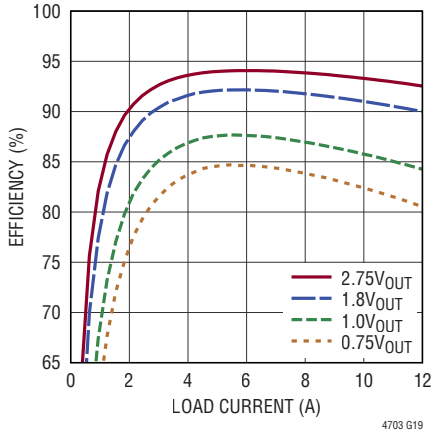


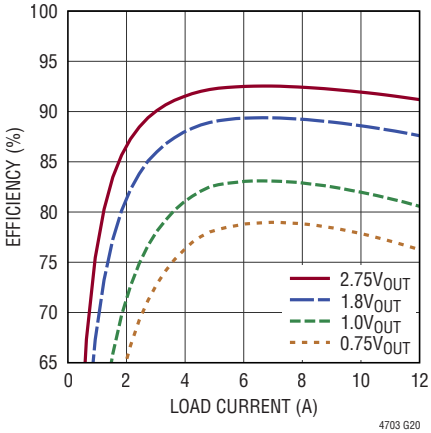
Input vs Load, $12V_{IN}$, f_{SW} = 800kHz



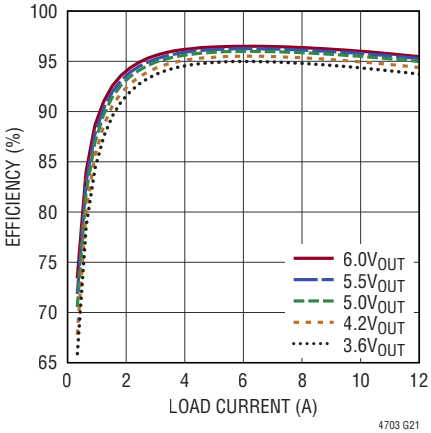
Efficiency vs Load, $12V_{IN}$, f_{SW} = 1MHz



Efficiency vs Load, $12V_{IN}$, f_{SW} = 2MHz

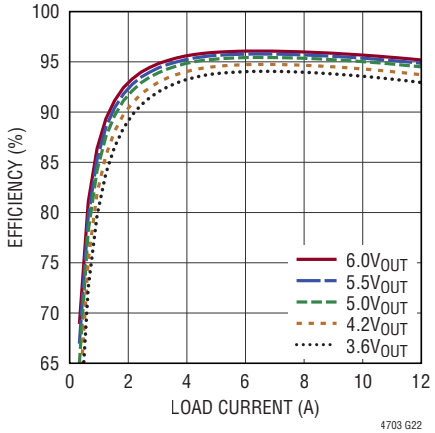


Efficiency vs Load, $12V_{IN}$, f_{SW} = 1MHz

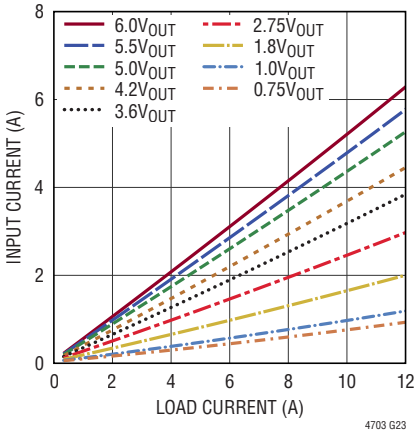


TYPICAL PERFORMANCE CHARACTERISTICS T_A = 25°C, unless otherwise noted.

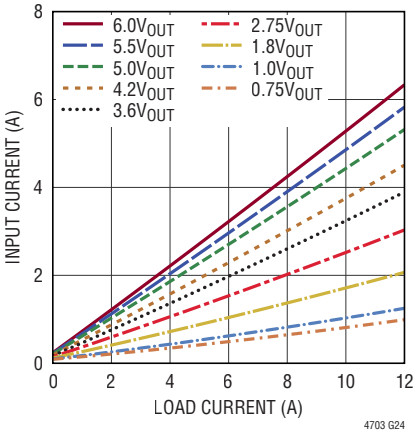
Efficiency vs Load, 12V_{IN}, f_{SW} = 2MHz



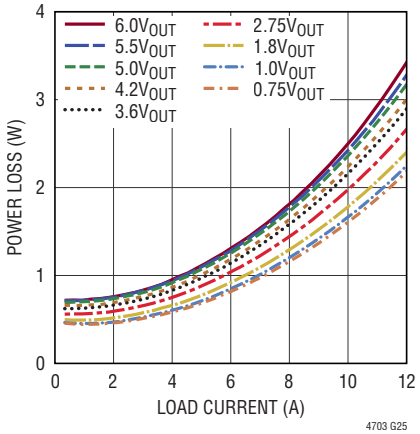
Input vs Load, 12V_{IN}, f_{SW} = 1MHz



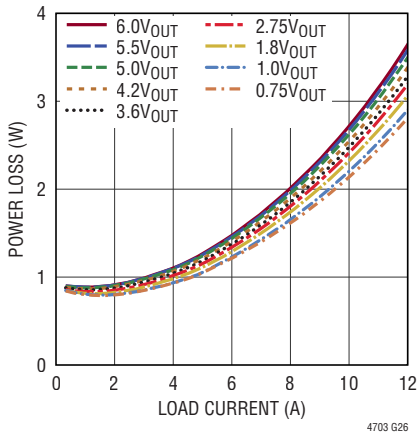
Input vs Load, 12V_{IN}, f_{SW} = 2MHz



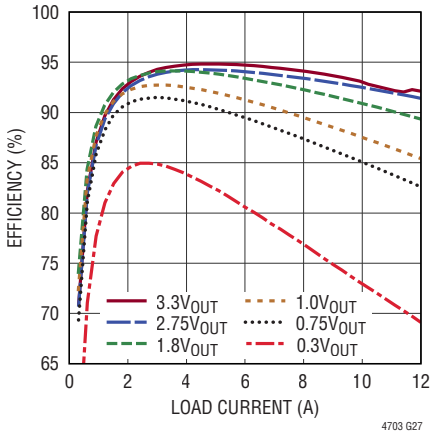
Power Loss vs Load, 12V_{IN}, f_{SW} = 1MHz



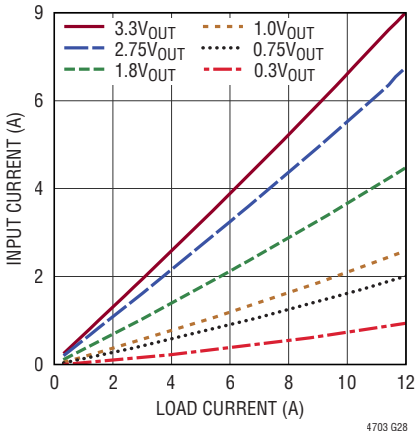
Power Loss vs Load, 12V_{IN}, f_{SW} = 2MHz



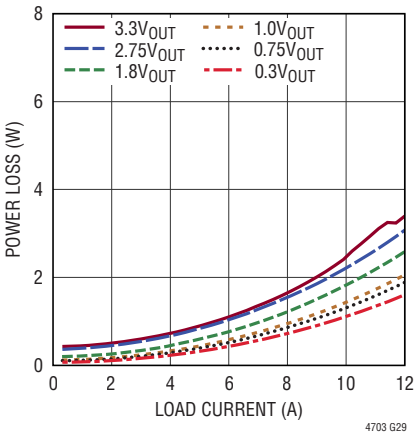
Efficiency vs Load, 5V_{IN}, f_{SW} = 400kHz



Input vs Load, 5V_{IN}, f_{SW} = 400kHz

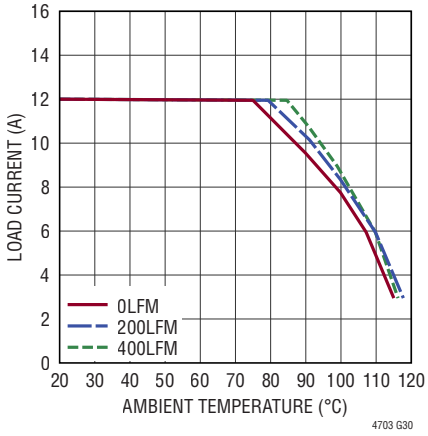


Power Loss vs Load, 5V_{IN}, f_{SW} = 400kHz

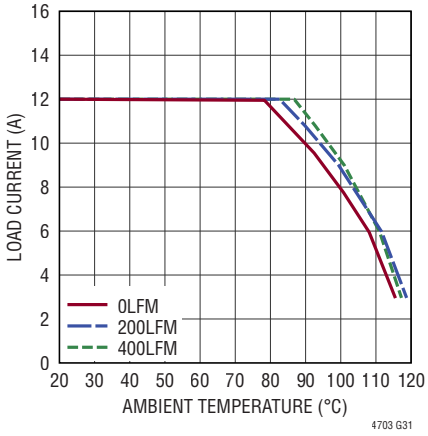


TYPICAL PERFORMANCE CHARACTERISTICS T_A = 25°C, unless otherwise noted.

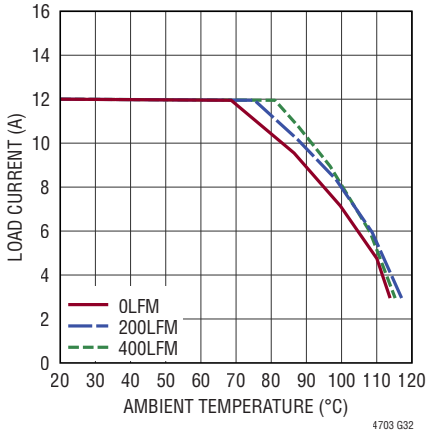
Derating Curve, V_{IN} = 5V, V_{OUT} = 1V, f_{SW} = 400kHz



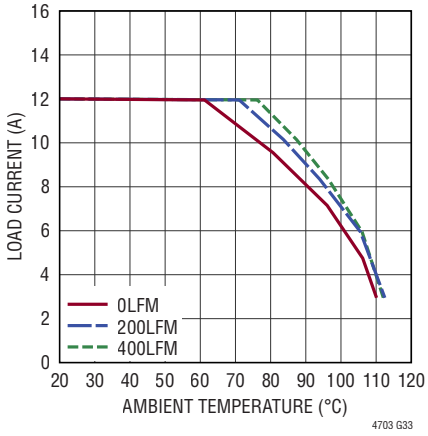
Derating Curve, V_{IN} = 5V, V_{OUT} = 1.5V, f_{SW} = 400kHz



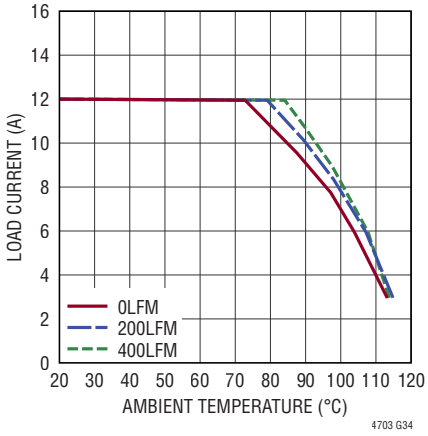
Derating Curve, V_{IN} = 5V, V_{OUT} = 2.5V, f_{SW} = 400kHz



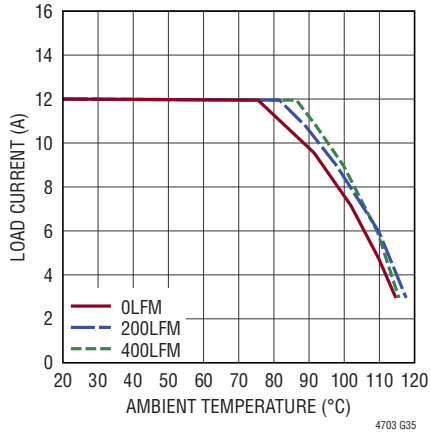
Derating Curve, V_{IN} = 5V, V_{OUT} = 3.3V, f_{SW} = 400kHz



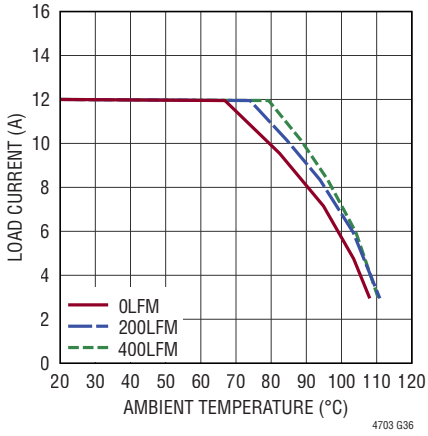
Derating Curve, V_{IN} = 12V, V_{OUT} = 1V, f_{SW} = 400kHz



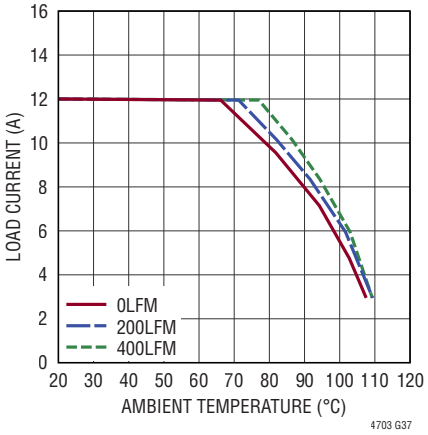
Derating Curve, V_{IN} = 12V, V_{OUT} = 1.5V, f_{SW} = 600kHz



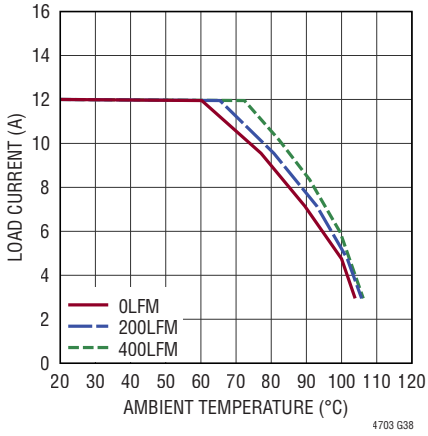
Derating Curve, V_{IN} = 12V, V_{OUT} = 2.5V, f_{SW} = 600kHz



Derating Curve, V_{IN} = 12V, V_{OUT} = 3.3V, f_{SW} = 800kHz

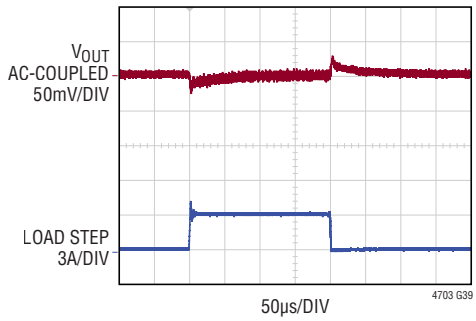


Derating Curve, V_{IN} = 12V, V_{OUT} = 5V, f_{SW} = 800kHz



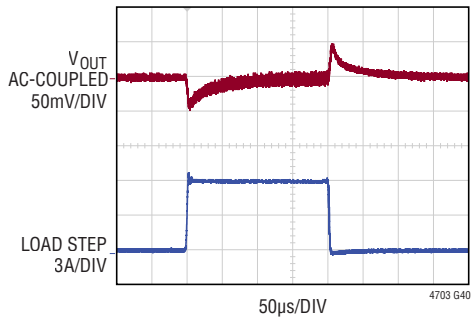
TYPICAL PERFORMANCE CHARACTERISTICS T_A = 25°C, unless otherwise noted.

1V Output Transient Response f_{SW} = 800kHz



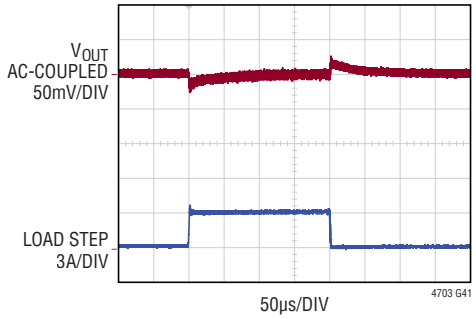
V_{IN} = 12V, V_{OUT} = 1V, I_{OUT} = 6A TO 9A
C_{OUT} = 100µF ×4 CERAMIC CAPACITOR
INTERNAL COMPENSATION,
CONNECT COMPa TO COMPb

1V Output Transient Response f_{SW} = 800kHz



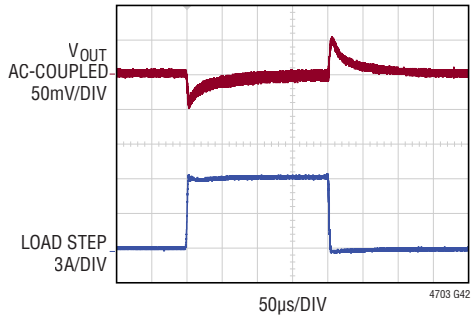
V_{IN} = 12V, V_{OUT} = 1V, I_{OUT} = 6A TO 12A
C_{OUT} = 100µF ×4 CERAMIC CAPACITOR
INTERNAL COMPENSATION,
CONNECT COMPa TO COMPb

5V Output Transient Response f_{SW} = 2MHz



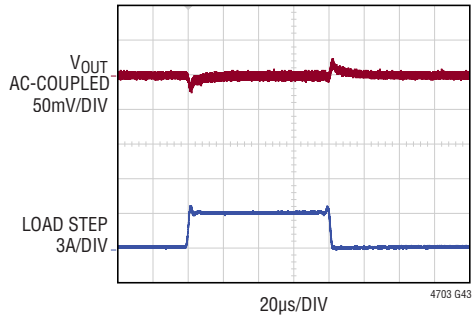
V_{IN} = 12V, V_{OUT} = 5V, I_{OUT} = 6A TO 9A
C_{OUT} = 100µF ×4 CERAMIC CAPACITOR
INTERNAL COMPENSATION,
CONNECT COMPa TO COMPb

5V Output Transient Response f_{SW} = 2MHz



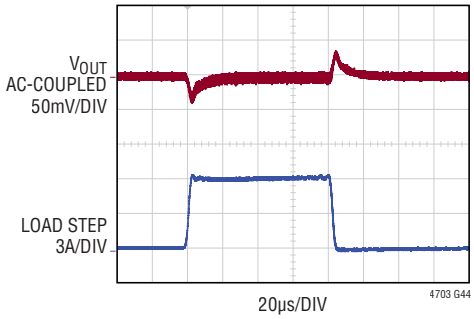
V_{IN} = 12V, V_{OUT} = 5V, I_{OUT} = 6A TO 12A
C_{OUT} = 100µF ×4 CERAMIC CAPACITOR
INTERNAL COMPENSATION,
CONNECT COMPa TO COMPb

5V Output Transient Response f_{SW} = 2MHz



V_{IN} = 12V, V_{OUT} = 5V, I_{OUT} = 6A TO 9A
C_{OUT} = 100µF ×4 CERAMIC CAPACITOR
EXTERNAL COMPENSATION,
R_{COMP} = 1.33k, C_{COMP} = 4.7nF

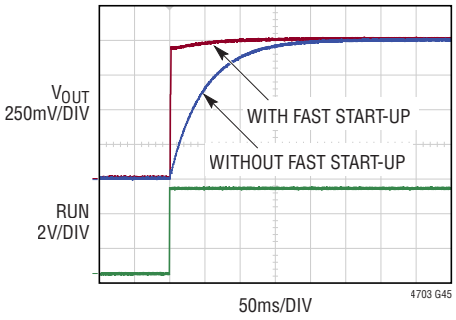
5V Output Transient Response f_{SW} = 2MHz



V_{IN} = 12V, V_{OUT} = 5V, I_{OUT} = 6A TO 12A
C_{OUT} = 100µF ×4 CERAMIC CAPACITOR
EXTERNAL COMPENSATION,
R_{COMP} = 1.33k, C_{COMP} = 4.7nF

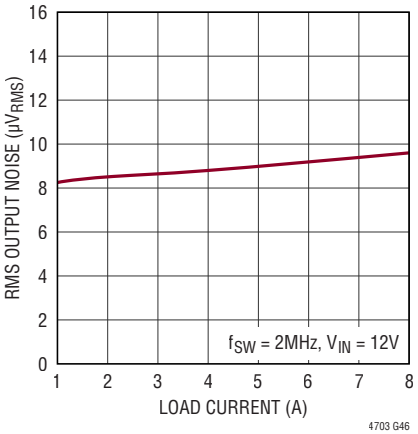
TYPICAL PERFORMANCE CHARACTERISTICS T_A = 25°C, unless otherwise noted.

Start-Up Time with and without Fast Start-Up Circuitry (Large C_{SET})

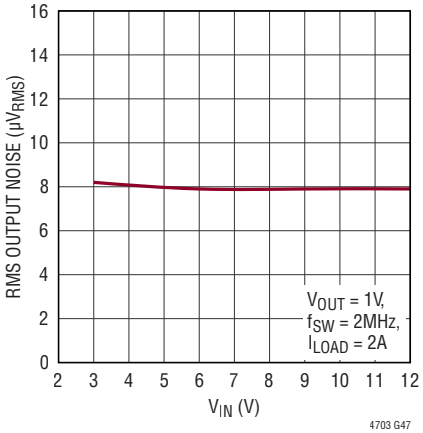


V_{IN} = SV_{IN} = 5V, R_{SET} = 10k, C_{SET} = 4.7µF
f_{SW} = 2MHz
R_L = 1Ω

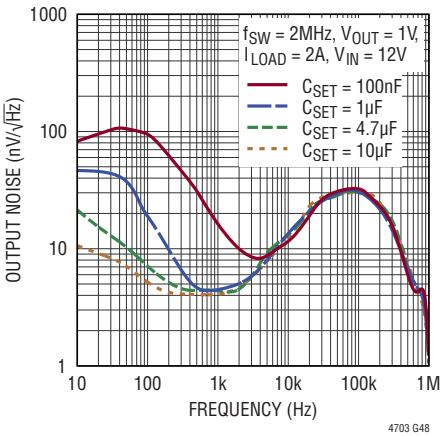
Integrated RMS Output Noise (10Hz to 100kHz) vs Load



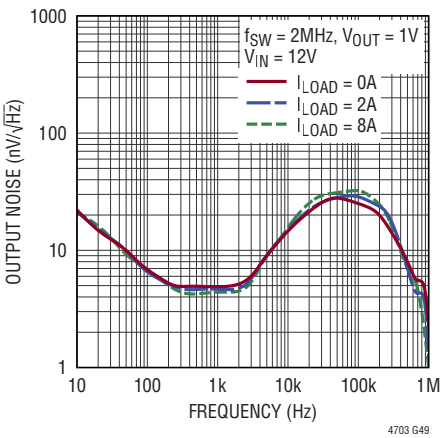
Integrated RMS Output Noise (10Hz to 100kHz) vs V_{IN}



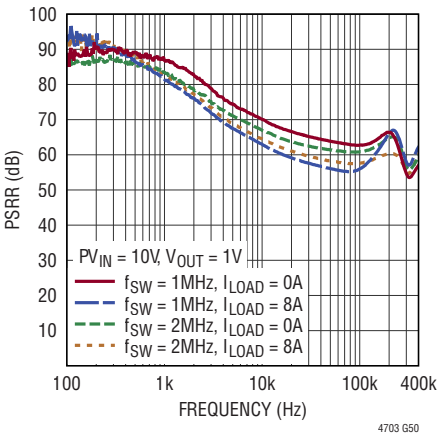
Noise Spectral Density vs C_{SET}



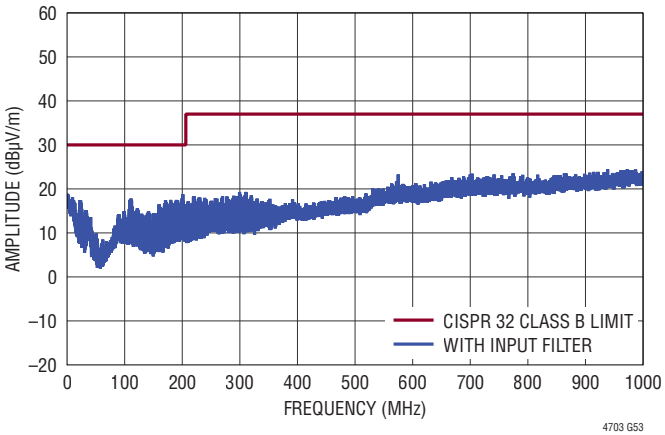
Noise Spectral Density vs Load



Power Supply Ripple Rejection



CISPR32 Radiated Emission Test with Class B 10m



EVAL-LTM4703-AZ EVALUATION BOARD
V_{IN} = 12V, V_{OUT} = 1V, I_{OUT} = 12A, f_{SW} = 400kHz

Rev. 0

PIN FUNCTIONS

PACKAGE ROW AND COLUMN LABELING MAY VARY AMONG µModule PRODUCTS. REVIEW EACH PACKAGE LAYOUT CAREFULLY.

SV_{IN} (Pin A4): Signal V_{IN}. This pin supplies current to the LTM4703 internal circuitry and regulator. If connected to a different supply other than V_{IN}, place a 1µF local bypass capacitor on this pin.

V_{OUT} (Banks 1 and 2): Power Output Pins. Apply an output load between these pins and the GND pins. Recommend placing an output decoupling capacitor directly between these pins and the GND pins.

GND (Bank 3 and Pin G7): Power Ground Pins for Both Input and Output Returns.

V_{IN} (Bank 4): Power Input Pins. Apply input voltage between these pins and the GND pins. Recommend placing an input decoupling capacitor directly between the V_{IN} pins and the GND pins.

T_{SENSE}^+ (Pin B1): High-Side of the Internal Temperature Monitor Pin. An internal diode-connected NPN transistor is placed between the T_{SENSE}^+ and T_{SENSE}^- pins. See the Applications Information section.

T_{SENSE}^- (Pin B2): Low-Side of the Internal Temperature Monitor Pin.

RUN (Pin C1): Run Control Input. Enables chip operation by connecting RUN above 1.32V (typical). Connecting it below 0.4V shuts down the part.

COMPa (Pin C2): Output of the Internal Error Amplifier. The voltage on this pin controls the peak switch current. Connect the COMPa pins from different channels together for parallel operation. Connect to COMPb to use the internal compensation. Or connect to an external RC network to use customized compensation.

COMPb (Pin C3): Internal Compensation Network. Connect to COMPa to use the internal compensation in the majority of applications.

RT (Pin D1): This pin sets the oscillator frequency with an external resistor to AGND.

AGND (Pin D2): Analog Ground. Ground return for SYNC, RT, and COMP pins. The AGND and GND pins are internally connected.

$INTV_{CC}$ (Pin D3): Internal 3.4V Regulator Bypass Pin. The internal power drivers and control circuits are powered by this voltage. Do not load the $INTV_{CC}$ pin with external circuitry. This pin should be floated.

SET (Pin E1): Output Voltage Set. This pin is the non-inverting input of the error amplifier and the regulation set-point for the LTM4703. The SET pin sources a precision 100µA current that flows through an external resistor connected between SET and GND. The LTM4703's output voltage is determined by $V_{SET} = I_{SET} \bullet R_{SET}$. The output voltage range is from 0.3V to 6V. Adding a capacitor from SET to GND improves noise at the expense of increased start-up time. For optimum load regulation, Kelvin connects the ground side of the SET pin resistor directly to the load.

PGSET (Pin E2): Power Good Set. The PG pin pulls low if PGSET increases above 540mV or decreases below 465mV. Connecting a pull-up resistor between V_{OUT} and PGSET sets the programmable power good threshold with Equation 1.

$$R_{PGSET} = (2 \bullet V_{OUT} - 1) \bullet 49.9k \quad (1)$$

As discussed in the Applications Information section, PGSET also activates the fast start-up circuitry. If the power is good and the fast start-up functionalities are not needed, the PGSET pin must be connected to an external 0.5V. Do not float the PGSET pin.

PHMODE (Pin E3): The PHMODE pin sets the phase shift of the clock signal of the CLKOUT pin. Connect PHMODE to ground for a 180° phase shift, float for a 120° phase shift, and connect high to $INTV_{CC}$ (~3.4V) or an external supply >3V for a 90° phase shift.

V_{OSNS} (Pin F1): Output Voltage Sense. This pin is the inverting input to the error amplifier. For optimal transient performance and load regulation, Kelvin connects V_{OSNS} directly to the output capacitor and the load. Also, connect the GND connections of the output capacitor and the SET pin capacitor directly together.

PIN FUNCTIONS

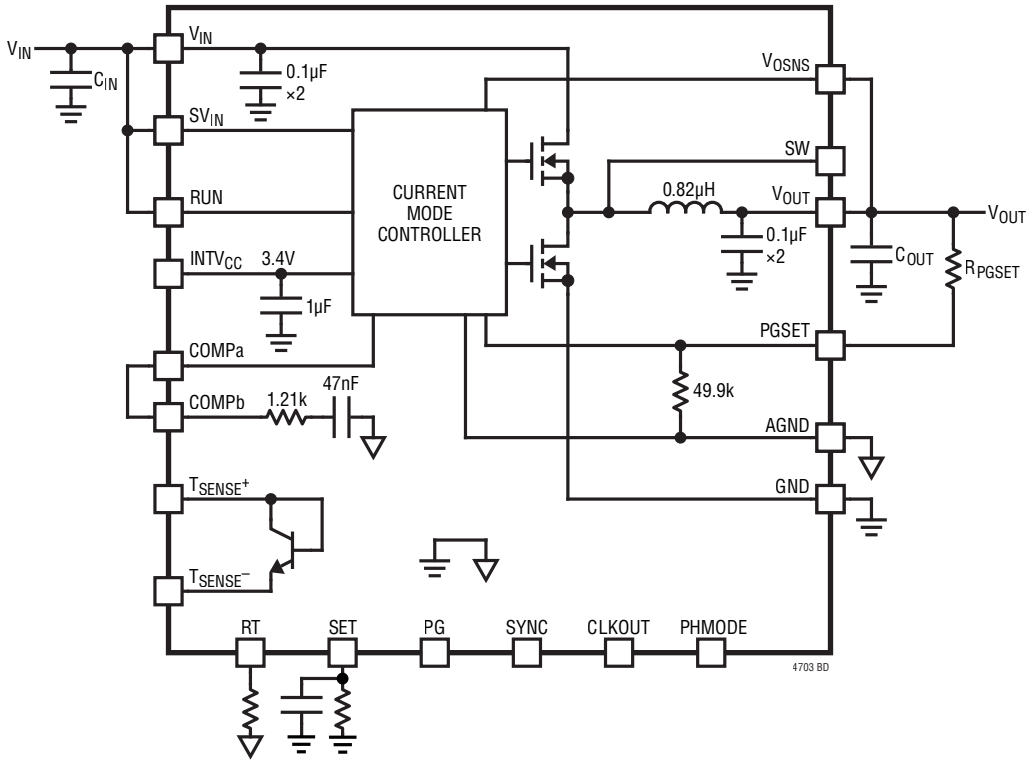
PG (Pin F2): Output Power Good Indicator. The PG pin is the open-drain output of an internal comparator. The PG pin remains low until the V_{OSNS} pin is within ±7.5% of the final regulation voltage, and there are no fault conditions. The PG is also pulled low when RUN is below 1V, $INTV_{CC}$ has fallen too low, SV_{IN} is too low, or during the thermal shutdown. The PG pin is valid when SV_{IN} is above 3V.

SW (Pin F6): Switching node of the LTM4703. This pin is for test purposes only. Do not load the SW pin with external circuitry.

CLKOUT (Pin F7): Output Clock Signal for PolyPhase® Operation. The CLKOUT pin provides a 50% duty-cycle square wave of the switching frequency. The phase of CLKOUT with respect to the LTM4703 internal clock is determined by the state of the PHMODE pin. The CLKOUT's peak-to-peak amplitude is $INTV_{CC}$ to GND. Float this pin if the CLKOUT function is not used.

SYNC (Pin G6): This pin programs three different operating modes: 1) Pulse-skipping mode (PSM). Connect this pin to GND for PSM to improve efficiency at light loads. 2) Forced continuous mode (FCM). This mode offers fast transient response and full-frequency operation over a wide load range. Connect this pin high to $INTV_{CC}$ (~3.4V) or an external supply >3V for FCM. The LTM4703 operates in this mode by default if this pin is left floating. 3) Synchronization mode. Drive this pin with a clock source synchronized to an external clock and put the LTM4703 in FCM.

BLOCK DIAGRAM



OPERATION

The LTM4703 is a standalone, nonisolated step-down switching DC/DC power supply that can deliver up to 12A. The continuous current is determined by the internal operating temperature. It provides a precisely regulated output voltage programmable through one external resistor from 0.3V to 6V. The input voltage range is 3V to 16V. Given that the LTM4703 is a step-down converter, ensure that the input voltage is high enough to support the desired output voltage and the load current. See the simplified Block Diagram.

The LTM4703 contains a current mode controller, power switching elements, a power inductor, and a modest amount of input and output capacitance. The LTM4703 is a fixed-frequency PWM regulator. The switching frequency is set by simply connecting the appropriate resistor value from the RT pin to the GND.

An internal regulator provides power to the control circuitry. To improve efficiency across all loads, supply current to the control circuitry can be sourced from the SV_{IN} pin when it is biased at 3V or above, instead of connecting SV_{IN} to V_{IN}. If the RUN pin is below 0.4V, the LTM4703 is shutdown, and draws 55µA from the input. When the RUN pin rises above 1.32V (typical), the LTM4703 becomes active.

To enhance efficiency at light load, the LTM4703 automatically operates in pulse-skipping mode (PSM) in light load situations. The SYNC pin is connected low for PSM operation and connected to $INTV_{CC}$, or to a voltage higher than 3V for forced continuous mode (FCM). If a clock is applied to the SYNC pin, the part synchronizes to an external clock frequency and it operates in FCM.

The LTM4703 can operate in FCM for fast transient response and full-frequency operation over a wide load range. When in FCM, the oscillator operates continuously, and positive SW transitions are aligned to the clock. A negative inductor current is allowed. The LTM4703 can sink current from the output and return this charge to the input in this mode, improving the load step transient response.

The LTM4703 incorporates fast start-up circuitry, which allows the part to start-up at a short time while using a larger value SET pin capacitor for ultralow-noise applications. See the Applications Information section for more details.

The LTM4703 contains a power good comparator that trips when the PGSET pin is between 462.5mV and 537.5mV, typical. The PG output is an open-drain transistor that is off when the output is in regulation, allowing an external resistor to pull the PG pin high. The PG signal is valid when SV_{IN} is above 3V. If SV_{IN} is above 3V and RUN is low, PG remains low.

The LTM4703 is equipped with a thermal shutdown that inhibits power switching at high junction temperatures. The activation threshold of this function is above 125°C to avoid interfering with normal operation. Therefore, prolonged or repetitive operation under a condition in which the thermal shutdown activates may damage or impair the reliability of the device.

Two or more LTM4703 devices may be operated in parallel to produce higher currents.

APPLICATIONS INFORMATION

For most applications, the design process is straightforward and summarized below.

1. See Table 1 for the row with the desired input range and output voltage.
2. Apply the recommended C_{IN}, C_{OUT}, R_{SET}, and R_T values.
3. Apply the C_{SET} (from SET to AGND), or C_{SHARE} (from COMPa to AGND) capacitors as required.

While these component combinations have been tested for proper operation. Ensure that the system operates correctly within the defined line, load, and environmental conditions. The maximum output current is limited by the junction temperature, the relationship between the input and the output voltage magnitude, the polarity, and other factors. See the graphs in the Typical Performance Characteristics section for guidance.

The maximum frequency (and attendant R_T value) at which the LTM4703 should be allowed to switch is shown in Table 1 in the Maximum f_{SW} column, while the recommended frequency (and R_T value) for optimal efficiency over the given input condition is given in the f_{SW} column. Additional conditions must be satisfied if the synchronization function is used. See the Synchronization section for details.

Capacitor Selection Considerations

The C_{IN}, and C_{OUT} capacitor values in Table 1 are the minimum recommended values for the associated operating conditions. Applying capacitor values below those indicated in Table 1 is not recommended and may result in undesirable operation. Using larger values is generally acceptable, and can yield improved dynamic response, if necessary. Ensure that the system operates correctly within the defined line, load, and environmental conditions.

Ceramic capacitors are small, robust, and have very low ESR. However, not all ceramic capacitors are suitable. The X5R and X7R types are stable over temperature and applied voltage and give dependable service. Other types, including Y5V and Z5U have large temperature and voltage coefficients of capacitance. In an application circuit, they may have only a small fraction of their nominal capacitance resulting in much higher output voltage ripple than expected.

Ceramic capacitors are also piezoelectric. Since the LTM4703 operates at a lower current limit during pulse-skipping mode (PSM) operation, the noise is typically very quiet to a casual ear. If this audible noise is unacceptable, use a high performance electrolytic capacitor at the output. It may also be a parallel combination of a ceramic capacitor and a low cost electrolytic capacitor.

A final precaution regarding ceramic capacitors concerns the maximum input voltage rating of the LTM4703. A ceramic input capacitor combined with a trace, or a cable inductance, forms a high-Q (underdamped) tank circuit. If the LTM4703 circuit is plugged into a live supply, the input voltage can ring to twice its nominal value, possibly exceeding the device's rating. This situation is easily avoided (see the Hot-Plugging Safely section) for details.

Table 1. Recommended Component Values and Configuration (T_A = 25°C)

V_{IN}[1] (V)	V_{OUT} (V)	R_{SET} (kΩ)	C_{IN}[2]	C_{OUT}	f_{SW} (MHz)	R_T (kΩ)	MAX f_{SW} (MHz)	MIN R_T (kΩ)	COMPENSATION[3]
3 to 16	1	10	10µF X7R 25V 1210	100µF ×4 X7R 6.3V 1210	0.4	287	2.5	35.7	Internal Compensation
3.1 to 16	1.8	18.2	10µF X7R 25V 1210	100µF ×4 X7R 6.3V 1210	0.8	137	2.5	35.7	Internal Compensation
4.2 to 16	2.75	27.4	10µF X7R 25V 1210	100µF ×4 X7R 10V 1210	1.0	105	2.5	35.7	Internal Compensation
5.7 to 16	3.6	36.5	10µF X7R 25V 1210	100µF ×4 X7R 10V 1210	1.2	86.6	2.5	35.7	Internal Compensation
8.3 to 16	5	49.9	10µF X7R 25V 1210	100µF ×4 X7R 10V 1210	1.5	66.5	3	28.7	Internal Compensation
8.6 to 16	6	60.4	10µF X7R 25V 1210	100µF ×4 X7R 10V 1210	2.0	47	3	28.7	Internal Compensation

[1] The LTM4703 may be capable of the operating at lower input voltage but may skip switching cycles.

[2] A bulk capacitor is required.

[3] Short COMPa and COMPb pins for internal compensation.

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Frequency Selection

The LTM4703 uses a constant-frequency PWM architecture, which can be programmed to switch from 300kHz to 3MHz by using a resistor connected from the RT pin to the ground. Table 2 shows a list of R_T resistor values and their resultant frequencies.

Table 2. Switching Frequency vs R_T Value

f_{SW} (MHz)	R_T (kΩ)
0.3	392
0.4	287
0.5	226
0.6	187
0.7	154
0.8	137
0.9	118
1.0	105
1.2	86.6
1.4	71.5
1.6	61.9
1.8	53.6
2	47
2.5	35.7
3	28.7

Operating Frequency Trade-Offs

It is recommended that you apply the optimal R_T value given in Table 2 for the input and output operating conditions. System-level or other considerations, however, may necessitate another operating frequency. While the LTM4703 is flexible enough to accommodate a wide range of operating frequencies, a haphazardly chosen one may result in undesirable operation under certain operating or fault conditions. A frequency that is too high can reduce efficiency, generate excessive heat, or even damage the LTM4703 device if the output is overloaded or short-circuited. A frequency that is too low can result in a final design that has too much output ripple or too large of an output capacitor.

Maximum Load

The maximum practical continuous load that the LTM4703 can drive, while rated at 12A, actually depends upon both the internal current limit and the internal temperature. The internal current limit is designed to prevent damage to the LTM4703 in the case of overload or short-circuit. The internal temperature of the LTM4703 depends on the operating conditions, such as the ambient temperature, the power delivered, and the heat sinking capability of the system. See the derating curve for V_{OUT} = 1V in the Typical Performance Characteristics section.

Load Sharing

Two or more LTM4703 devices may be paralleled to produce higher currents. To do this, connect the V_{IN}, V_{OUT}, V_{OSNS}, COMPa, and COMPb pins of all the paralleled LTM4703 devices together. Figure 12 is an example of two LTM4703 devices configured for load sharing.

The CLKOUT signal can be connected to the SYNC pin of the following LTM4703 device to line up both the frequency and the phase of the entire system. Connecting the PHMODE pin to GND, $INTV_{CC}$, or floating the pin generates a phase difference between LTM4703's internal clock and CLKOUT of 180°, 90°, or 120°, respectively, which corresponds to a 2-phase, a 4-phase, or a 3-phase operation. A total of 12 phases can be paralleled to run simultaneously out-of-phase with respect to each other by programming the PHMODE pin of each LTM4703 to different voltage levels. During FCM and synchronization modes, all devices operate at the same frequency. When load sharing among a number (n) of units and using a single R_{SET} resistor, the value of the resistor is given by Equation 2.

$$R_{SET} = \frac{V_{OUT}}{n \bullet 100\mu A} \quad (2)$$

Minimum Input Voltage

The LTM4703 is a step-down converter; therefore, a minimum amount of headroom is required to keep the output in regulation. Keep PV_{IN} above 3V to ensure proper

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operation. If the SV_{IN} and PV_{IN} are powered from different sources, keep SV_{IN} above 3V to ensure proper operation. The voltage transients or ripple valleys that cause the SV_{IN} to fall below 3V may turn off the LTM4703.

SET Pin (Bypass) Capacitance: Noise, Transient Response, and Soft-Start

In addition to reducing output noise, using a SET pin bypass capacitor reduces sensitivity to any parasitic coupling of voltage spikes onto the SET pin. Note that any bypass capacitor leakage deteriorates the LTM4703 DC regulation. Capacitor leakage of even 100nA is a 0.1% DC error. Therefore, it is recommended to use a good-quality, low-leakage ceramic capacitor.

Also, using a SET pin bypass capacitor soft-starts the output and limits inrush current. Soft-starting the output prevents a current surge in the input supply. The SET pin capacitor and resistor values set the ramp-up time of the reference voltage, and the output voltage tracks this voltage. The SET pin resistor size is determined by the application's desired output voltage; however, the capacitor size may be selected to achieve the desired ramp-up time. It is important to remember that the size of the SET pin capacitor also plays a role in noise performance, which is typically the more important factor in determining the size of this capacitor.

Without fast start-up enabled, the RC time constant, formed by the SET pin resistor and capacitor, controls soft-start time. Connect the PGSET pin to 0.5V to disable fast start-up. The ramp-up rate from 0% to 90% of nominal V_{OUT} is given by Equation 3.

$$t_{START\_NO\_FAST\_START\text{-}UP} = 2.3 \bullet R_{SET} \bullet C_{SET} \quad (3)$$

With fast start-up enabled, the start-up time can be significantly reduced with the ramp-up time from 0% to 90% of nominal V_{OUT} as shown by Equation 4.

$$t_{START\_FAST\_START\text{-}UP} = \frac{100\mu A \bullet R_{SET} \bullet C_{SET}}{2.7mA} \quad (4)$$

In most applications, fast start-up is enabled. In this case, a minimum SET capacitor size of 1µF is strongly recommended to prevent reference voltage overcharge and ensure good noise performance.

Soft-Start and Power Sequencing

As discussed in the SET Pin (Bypass) Capacitance: Noise, Transient Response, and Soft-Start section, soft-start is achieved through the controlled ramp-up time of the SET pin voltage. The soft-start is guaranteed when all PV_{IN} and SV_{IN} pins are connected.

When PV_{IN} and SV_{IN} are powered by independent supplies, power sequencing must be considered to guarantee a soft-start. The SET pin voltage should start at 0V when PV_{IN} is applied. To guarantee a soft-start, do not power PV_{IN} last when sequencing PV_{IN}, SV_{IN}, and RUN. An example of a specific case to avoid is having SV_{IN} and RUN powered up before PV_{IN}. In this instance, the SET pin voltage rises to a voltage greater than 0V when PV_{IN} is applied, and the LTM4703 does not soft-start correctly.

Fast Start-Up

For ultralow noise applications that require low 1/f noise (i.e., at frequencies below 100Hz), a larger value SET pin capacitor is required, up to 22µF. A larger value capacitor can be used, but care should be taken regarding leakage. While normally larger capacitors would significantly increase the regulator's start-up time, the LTM4703 incorporates fast start-up circuitry, which increases the SET pin current to about 2.7mA during start-up.

Upon start-up, the 2.7mA current source remains engaged while PGSET is below the power good threshold of 462.5mV, unless the regulator is in thermal shutdown, SV_{IN} is too low, or $INTV_{CC}$ has fallen too low.

The fast start-up circuit is disabled permanently once PGSET rises above the power good threshold, until either the part is powered down, or the part is placed into shut down by pulling the RUN pin to GND.

There is one more condition under which the 2.7mA current source is disabled during start-up. The purpose of this is to prevent overcharging V_{SET}. Since the part assumes that the PGSET pin is an accurately indicates the voltage on the SET pin, it assumes that V_{OSNS} follows V_{SET} closely. However, this may not always be the case. For example, if the output capacitance is very large, or if, for some reason, the output is shorted to GND. Therefore, fast charge is also disabled whenever the COMPa pin has

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railed at its maximum value (when V_{SET} has risen significantly about V_{OSNS}). This prevents incorrect behavior where the 2.7mA current sources stays on even if V_{SET} has risen above its intended value.

Also, there is a minimum SET capacitor requirement for using a fast start-up without overcharging the reference voltage. This depends on the compensation network, as the part is depending on the COMPa pin voltage rising to its maximum value to inform the part to pause fast charge.

Due to the high g_m of the error amplifier, the capacitor in the compensation network typically dominates the COMPa voltage rise time. In this case, the minimum required SET capacitance value to prevent overcharging the reference voltage is given by Equation 5.

$$\text{Minimum } C_{SET} = 27 \bullet \frac{C_{COMP}}{V_{SET}} \quad (5)$$

If programmable power good and fast start-up capabilities are not required, the PGSET pin must be connected to 0.5V.

Prebiased Output

The LTM4703 regulates the output to the V_{SET} voltage. If the LTM4703 output is higher than the target output voltage, the LTM4703 attempts to regulate the output to the target voltage by returning a small amount of energy back to the input supply. If nothing is loading the input supply, its voltage may rise. Ensure that it does not rise too high and that the input voltage exceeds the absolute maximum rating of the LTM4703.

Forced Continuous Mode (FCM)

The LTM4703 can operate in FCM for fast transient response and full-frequency operation over a wide load range. When in FCM, the oscillator operates continuously, and positive SW transitions are aligned to the clock. A negative inductor current is allowed at light loads or under large transient conditions. The LTM4703 can sink current from the output and return this charge to the input in this mode, improving load step transient response (see Figure 1). At light loads, FCM operation is less efficient than PSM operation, but it may be desirable in applications where it is necessary to keep switching harmonics out of the signal band. The FCM must be used if the output is required to sink current. To enable FCM, connect the SYNC/MODE pin to $INTV_{CC}$ or > 1.5V, or float the pin.

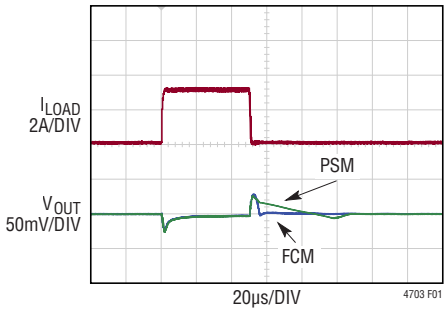

Figure 1. Load Step Transient Response with and without FCM

The FCM is disabled:

1) Under PV_{IN} overvoltage conditions (PV_{IN} pin is held above 16V),

2) If V_{OUT} is too high (the PGSET pin is held greater than 537.5mV), and

3) During start-up until the voltage on V_{OUT} has charged up to 92.5% of its final value (as indicated when the PGSET pin rises to above 462.5mV).

For the latter two conditions, it is assumed the PGSET pin is connected to the output voltage through an appropriate resistor. When FCM is disabled in these ways, the negative inductor current is not allowed, and the LTM4703 operates in PSM.

Pulse-Skipping Mode (PSM)

When not operating in FCM, the LTM4703 operates in PSM. In this mode, the oscillator operates continuously, and all switching cycles are aligned to the clock. A negative inductor current is not allowed in this mode; therefore, at light loads, the LTM4703 may be operating in discontinuous mode. Additionally, in PSM, the LTM4703 may also skip switching cycles at very light loads for improved efficiency, or at very high duty cycles to achieve better dropout. To enable PSM, connect the SYNC pin to GND.

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Synchronization

To synchronize the LTM4703 oscillator to an external frequency, connect a square wave (with about 20% to 80% duty cycle) to the SYNC pin. The square wave amplitude should have valleys, which are below 0.4V and peaks above 1.5V, with a minimum on-time and off-time of 50ns.

The LTM4703 runs in FCM to maintain regulation while synchronized to an external clock. The LTM4703 may be synchronized over a 300kHz to 3MHz range. The R_T resistor should be chosen to set the LTM4703 switching frequency to below the lowest synchronization input by approximately 20%. For example, if the synchronization signal is 500kHz or higher, the R_T should be selected for 400kHz.

Minimum Frequency for High-Duty Cycle

For duty cycles greater than 50% ($V_{OUT}/V_{IN} > 0.5$), a minimum frequency is required to avoid sub-harmonic oscillation. Refer to the Analog Devices Application Note 19. Equation 6 calculates the minimum frequency.

$$f_{SW} = \frac{2 \bullet V_{OUT} - V_{IN}}{4} \quad (6)$$

where V_{OUT} is the output voltage, V_{IN} is the input voltage, and f_{SW} is the switching frequency in MHz.

Example:

$$V_{IN} = 8V,\ V_{OUT} = 6V,\ f_{SW} = 1MHz$$

Programmable Power Good

LTM4703 features a programmable power good by using a single resistor across the V_{OUT} pin and PGSET pin as shown in Equation 7.

$$V_{OUT(PG\_THRESHOLD)} = 0.5V \bullet \left(1 + \frac{R_{PGSET}}{49.9k}\right) + I_{PGSET} \bullet R_{PGSET} \quad (7)$$

If the PGSET pin increases above 537.5mV or decreases below 462.5mV, the open-drain PG pin de-asserts and becomes high impedance. The power good comparator has 2mV hysteresis. The PGSET pin current (I_{PGSET}) from the Electrical Characteristics table must be considered when determining the resistor value. Note that the programmable power good and fast start-up capabilities are disabled when PGSET is connected to 0.5V or when the device is shutdown. Table 3 suggests some 1% R_{PGSET} resistor values for common V_{OUT} configurations.

Table 3. Suggested R_{PGSET} Resistor Values

V_{OUT} (V)	R_{PGSET} (kΩ)
0.3	Open (Externally Inject 0.5V to the PGSET Pin)
0.5	0
0.8	30.1
0.9	40.2
1	49.9
1.2	69.8
1.5	100
1.8	130
2.5	200
3.3	280
5.0	453
6.0	549

Negative Output

The LTM4703 can generate a negative output voltage by connecting its V_{OUT} to system GND and the LTM4703 GND to the negative voltage rail. Examples of this are shown in Figure 15 and Figure 16 in the Typical Applications section. The most versatile way to generate a negative output is to use a dedicated regulator, which was designed to generate a negative voltage. Using a buck regulator like the LTM4703 to generate a negative voltage is a simple and cost-effective solution, as long as certain restrictions are taken especially, $V_{IN} + |V_{OUT}| \leq 16V$. Refer to the Analog Devices Design Note 1021 (DN1021) for more details on generating negative output.

Figure 2 shows a typical negative output voltage application. Note that LTM4703 V_{OUT} is connected to system GND, and input power is applied from V_{IN} to LTM4703's V_{OUT}. As a result, the LTM4703 does not behave as a

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true buck regulator, and the maximum output current depends upon the input voltage. Figure 15 and Figure 16 illustrate how much current the LTM4703 delivers for a given input voltage.

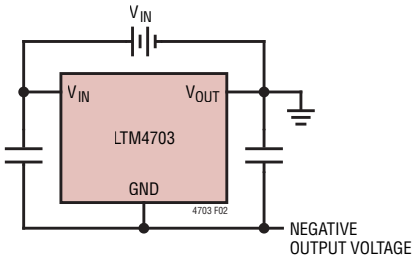

Figure 2. The LTM4703 Can Be Used to Generate a Negative Voltage

Note that the Figure 2 configuration requires that any load current transient directly affects the transient voltage onto the LTM4703 GND, as shown in Figure 3, fast load transients can disrupt the LTM4703's operation or even cause damage. Carefully evaluate whether the negative buck configuration is suitable for the application.

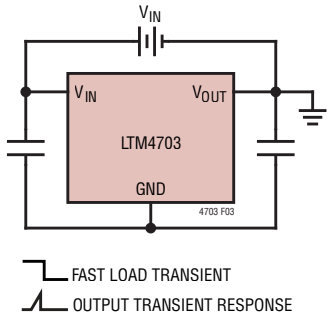

Figure 3. Any Output Voltage Transient Appears on LTM4703 GND

The C_{IN} and C_{OUT} capacitors in Figure 4 form an AC divider at the negative output voltage node. If V_{IN} is hot-plugged or rises quickly, the resultant V_{OUT} is a positive transient, which may be unhealthy for the application load. An anti-parallel Schottky diode may be able to prevent this positive transient from damaging the load. The location of this Schottky diode is important. For example, in a system where the LTM4703 is far from the load, placing the Schottky diode closest to the most sensitive load component may be the best design choice. Carefully evaluate whether the negative buck configuration is suitable for the application. When generating a negative output, connect BIAS to LTM4703 GND.

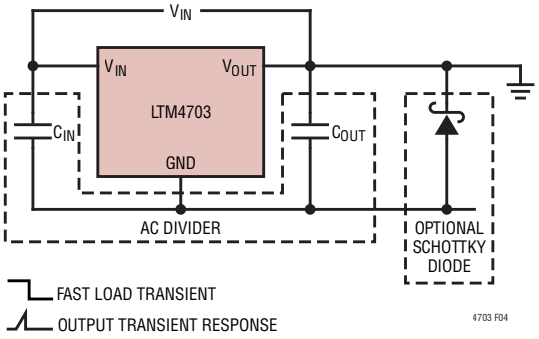

Figure 4. A Schottky Diode Can Limit the Transient Caused by a Fast Rising V_{IN} to Safe Levels

Shorted Input Protection

Care must be taken in systems where the output is held high when the power input to the LTM4703 is absent. This may occur in battery charging applications or in battery backup systems where a battery or some other supply is diode OR-ed with the LTM4703's output. If the PV_{IN} pin is allowed to float and the RUN pin is held high (either by a logic signal or because it is connected to V_{IN}), then the LTM4703's internal circuitry pulls its quiescent current through its internal power switch. This is fine if your system can tolerate a few milliamps in this state. If you ground the RUN pin, the internal current drops to essentially zero. However, if the PV_{IN} pin is grounded while the output is held high, parasitic diodes inside the LTM4703 can pull large currents from the output through the PV_{IN} pin. Figure 5 shows a circuit that runs only when the input voltage is present and protects against a shorted or reversed input.

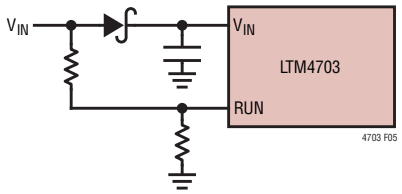

Figure 5. The Input Diode Prevents a Shorted Input from Discharging a Backup Battery Connect to the Output. It Also Protects the Circuit from a Reversed Input. The LTM4703 Only Runs When the Input is Present

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Temperature Monitoring

Measuring the absolute temperature of a diode is possible due to the relationship between current, voltage, and temperature described by the classic diode Equation 8.

$$I_D = I_S \bullet e\left(\frac{V_D}{\eta \bullet V_T}\right)$$

or (8)

$$V_D = \eta \bullet V_T \bullet \ln\frac{I_D}{I_S}$$

where I_D is the diode current, V_D is the diode voltage, η is the ideal factor (typically close to 1.0), and I_S (saturation current) is a process-dependent parameter. V_T can be broken out by Equation 9.

$$V_T = \frac{k \bullet T}{q} \quad (9)$$

where T is the diode junction temperature in Kelvin, q is the electron charge, and k is Boltzmann's constant. V_T is approximately 26mV at room temperature (298K) and scales linearly with Kelvin temperature. It is this linear temperature relationship that makes diodes suitable temperature sensors. The I_S term in Equation 9 is the extrapolated current through a diode junction when the diode has zero volts across the terminals. The I_S term varies from process to process, varies with temperature, and by definition must always be less than I_D. Combining all of the constants into one term (Equation 10).

$$K_D = \frac{\eta \bullet k}{q} \quad (10)$$

where $K_D = 8.26^{-5}$, and knowing ln (I_D/I_S) is always positive because I_D is always greater than I_S, leaves us with Equation 11.

$$V_D = T_{(KELVIN)} \bullet K_D \bullet \ln\frac{I_D}{I_S} \quad (11)$$

where V_D appears to increase with temperature. It is common knowledge that a silicon diode biased with a current source has an approximate –2mV/°C temperature relationship (Figure 6), which is at odds with the equation. The I_S term increases with temperature, reducing the absolute value and yielding an approximate –2mV/°C composite diode voltage slope.

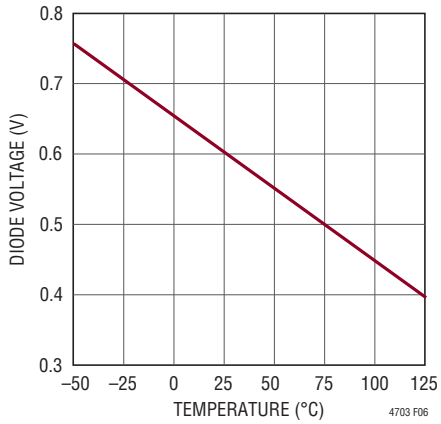

Figure 6. Diode Voltage V_D vs Temperature

To obtain a linear voltage proportional to temperature we cancel the I_S variable in the natural logarithm term to remove the I_S dependency from Equation 10. This is accomplished by measuring the diode voltage at two currents I_1, and I_2, where $I_1 = 10 \bullet I_2$) and subtracting, we get Equation 12.

$$\Delta V_D = T_{(KELVIN)} \bullet K_D \bullet \ln\frac{I_1}{I_S} - T_{(KELVIN)} \bullet K_D \bullet \ln\frac{I_2}{I_S} \quad (12)$$

Combining like terms, then simplifying the natural log terms yields Equation 13.

$$\Delta V_D = T_{(KELVIN)} \bullet K_D \bullet IN(10) \quad (13)$$

and redefining the constant given by Equation 14.

$$K'_D = K_D \bullet \ln(10) = \frac{198\mu V}{K} \quad (14)$$

yields Equation 15.

$$\Delta V_D = K'_D \bullet T_{(KELVIN)} \quad (15)$$

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Use Equation 16 for solving for temperature.

$$T_{(KELVIN)} = \frac{\Delta V_D}{K_D'} (°CELSIUS) = T_{(KELVIN)} - 273.15 \quad (16)$$

Where,

300°K = 27°C

means that you take the difference in voltage across the diode measured at two currents with a ratio of 10. The resulting voltage is 198µV per Kelvin of the junction with a zero intercept at 0 Kelvin.

The diode-connected NPN transistor across the T_{SENSE}^+ and the T_{SENSE}^- pins can be used to monitor the internal temperature of the LTM4703.

Hot-Plugging Safely

The small size, robustness, and low impedance of ceramic capacitors make them an attractive option for the input bypass capacitor of LTM4703. However, these capacitors can cause problems if the LTM4703 is plugged into a live supply (Refer to the Analog Devices Application Note 88 for a complete discussion). The low-loss ceramic capacitor combined with stray inductance in series with the power source forms an underdamped tank circuit, and the voltage at the V_{IN} pins of the LTM4703 can ring to more than twice the nominal input voltage, possibly exceeding the LTM4703's rating and damaging the part. If the input supply is poorly controlled or the LTM4703 is hot-plugged into an energized supply, the input network should be designed to prevent this overshoot. This can be accomplished by installing a small resistor in series to V_{IN}, but the most popular method of controlling input voltage overshoot is adding an electrolytic bulk cap to the V_{IN} net. This capacitor's relatively high equivalent series resistance damps the circuit and eliminates the voltage overshoot. The extra capacitor improves low-frequency ripple filtering and can slightly improve the efficiency of the circuit, though it is likely to be the largest component in the circuit.

Figure 7 shows a temperature plot of the LTM4703 with 12V input, 1V output at 12A without a heat sink and no airflow condition.

Figure 7. Thermal Image at $12V_{IN}$, 1V, 12A Output, No Airflow

Thermal Considerations

The LTM4703 output current may need to be derated if it is required to operate at a high ambient temperature. The amount of current derating is dependent upon the input voltage, output power, and ambient temperature. The derating curves shown in the Typical Performance Characteristics section can be used as a guide. These curves were generated by the LTM4703 mounted to a $75cm^2$ 4-layer FR4 printed circuit board. Boards of other sizes and layer-count can exhibit different thermal behaviors, it is your responsibility to verify proper operation over the intended system's line, load, and environmental operating conditions.

For increased accuracy and fidelity to the actual application, many designers use FEA (finite element analysis) to predict thermal performance. Therefore, below are the thermal coefficients.

1. θ_{JA} – Thermal resistance from junction to ambient.
2. θ_{JCbot} – Thermal resistance from the junction to the bottom of the product case.
3. θ_{JCtop} – Thermal resistance from junction to top of the product case.

While the meaning of each of these coefficients may seem to be intuitive, JEDEC has defined each to avoid

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confusion and inconsistency. These definitions are given in JESD51S-12, and are quoted or paraphrased below.

1. θ_{JA} is the natural convection junction-to-ambient air thermal resistance measured in a one cubic foot sealed enclosure. This environment is sometimes referred to as "still air," although natural convection causes the air to move. This value is determined with the part mounted to a JESD51-9 defined test board, which does not reflect an actual application or viable operating condition.
2. θ_{JCbot} is the junction-to-board thermal resistance with all of the component power dissipation flowing through the bottom of the package. In the typical µModule regulator, the bulk of the heat flows out the bottom of the package, but there is always heat flow out into the ambient environment. As a result, this thermal resistance value may be useful for comparing packages, but the test conditions don't generally match your application.
3. θ_{JCtop} is determined with nearly all of the component power dissipation flowing through the top of the package. As the electrical connections of the typical µModule regulator are on the bottom of the package, it is rare for an application to operate such that most of the heat flows from the junction to the top of the part. As in the case of θ_{JCbot}, this value may be useful for comparing packages, but the test conditions don't generally match your application.

Given these definitions, it is clear that none of these thermal coefficients reflect an actual physical operating condition of the µModule regulator. Thus, none of them can be individually used to accurately predict the thermal performance of the product. Likewise, it would be inappropriate to attempt to use any one coefficient to correlate to the junction temperature vs load graphs given in the product's data sheet. The only appropriate way to use the coefficients is when running a detailed thermal analysis, such as FEA, which considers all the thermal resistances simultaneously.

A graphical representation of these thermal resistances is shown in Figure 8. Some thermal resistance elements, such as heat flow out the side of the package, are not defined by the JEDEC standard, and are not shown. The blue resistances are contained within the µModule regulator, and the green are outside.

The die temperature of the LTM4703 must be lower than the maximum rating, so care must be taken in the layout of the circuit to ensure good heat sinking of the LTM4703. The bulk of the heat flow out of the LTM4703 is through the bottom of the package and the pads into the printed circuit board. Consequently, a poor printed circuit board design can cause excessive heating, resulting in impaired performance or reliability. See the PCB Layout section for a printed circuit board design suggestion.

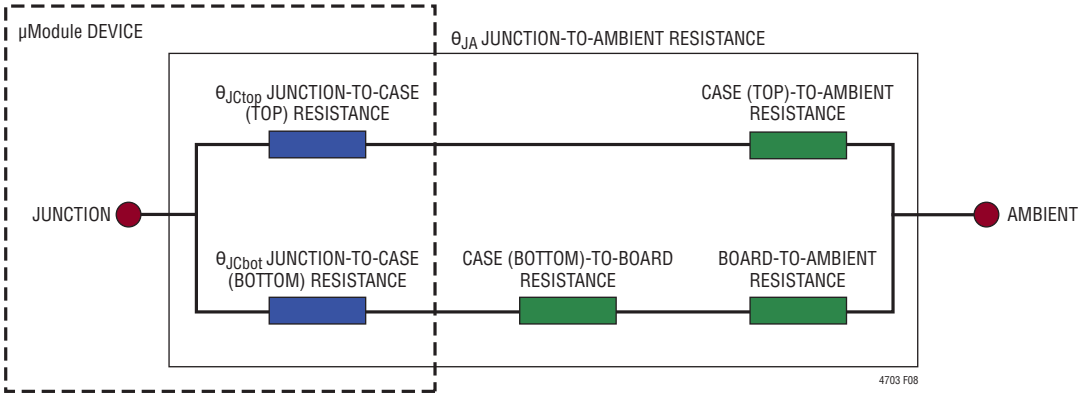

Figure 8. Graphical Representation of Thermal Coefficients, Including JESD51-12 Terms

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PCB Layout

Most of the headaches associated with the PCB layout have been alleviated, or even eliminated by the high level of integration of the LTM4703. The LTM4703 is nevertheless a switching power supply, and care must be taken to minimize EMI and ensure proper operation. Even with the high level of integration, you may fail to achieve specified operation with a haphazard or poor layout. See Figure 9 for a suggested layout. Ensure that the grounding and heat sinking are acceptable.

A few rules to keep in mind are:

1. Place C_{SET}, R_{SET}, and R_T as close as possible to their respective pins.
2. Place the C_{IN} capacitor as close as possible to the PV_{IN}/SV_{IN} and GND connection of the LTM4703.
3. Place the C_{OUT} capacitor as close as possible to the V_{OUT} and GND connection of the LTM4703.
4. Place the C_{IN}, and C_{OUT} capacitors such that their ground current flows directly adjacent to or underneath the LTM4703.
5. Connect all the GND connections to a copper pour or plane area as large as possible on the top layer. Avoid breaking the ground connection between the external components and the LTM4703.
6. Use vias to connect the GND copper area to the board's internal ground planes. Liberally distribute these GND vias to provide both a good ground connection and thermal path to the internal planes of the printed circuit board. Pay attention to the location and density of the thermal vias in Figure 9. The LTM4703 can benefit from the heat sinking supplied by vias that connect to internal GND planes at these locations, caused by their proximity to the internal power handling components. The optimum number of thermal vias depends upon the printed circuit board design. For example, a board might use very small holes. It should employ more thermal vias than a board, which uses larger holes.

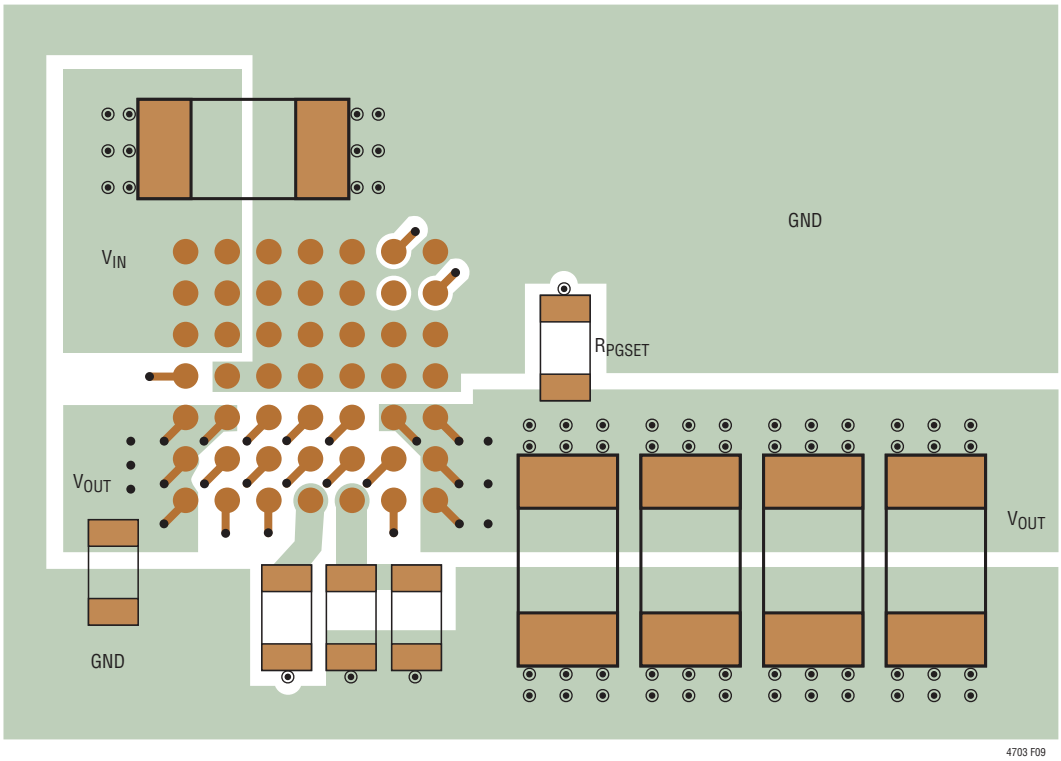
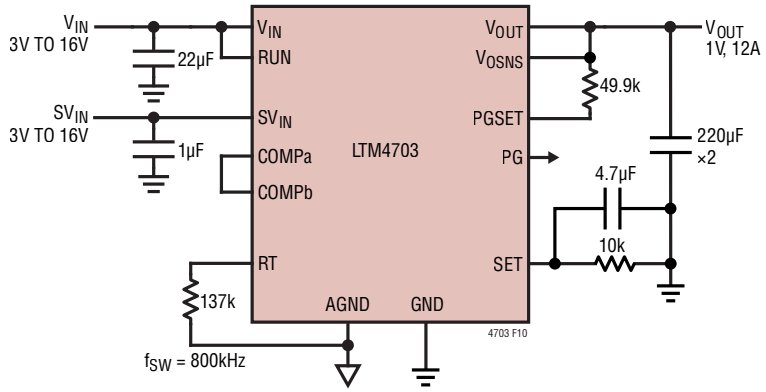


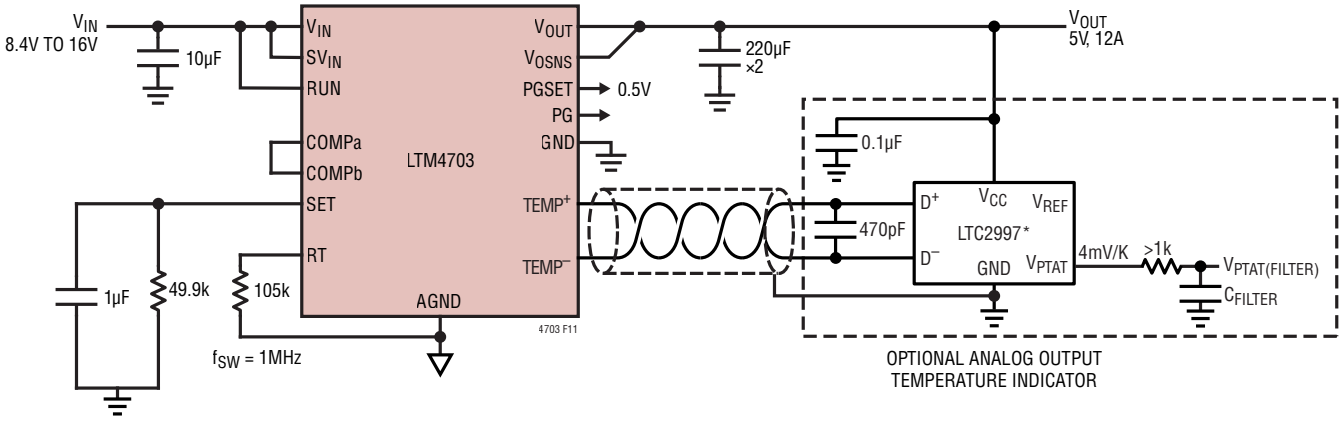
Figure 9. Layout Showing Suggested External Components, GND Plane and Thermal Vias

TYPICAL APPLICATIONS



PINS NOT USED: SW, SYNC, PHMODE, CLKOUT, $INTV_{CC}$, T_{SENSE}^+, T_{SENSE}^-.
TO GUARANTEE SOFT-START, DO NOT POWER V_{IN} LAST WHEN SEQUENCING V_{IN}, SV_{IN} AND RUN.

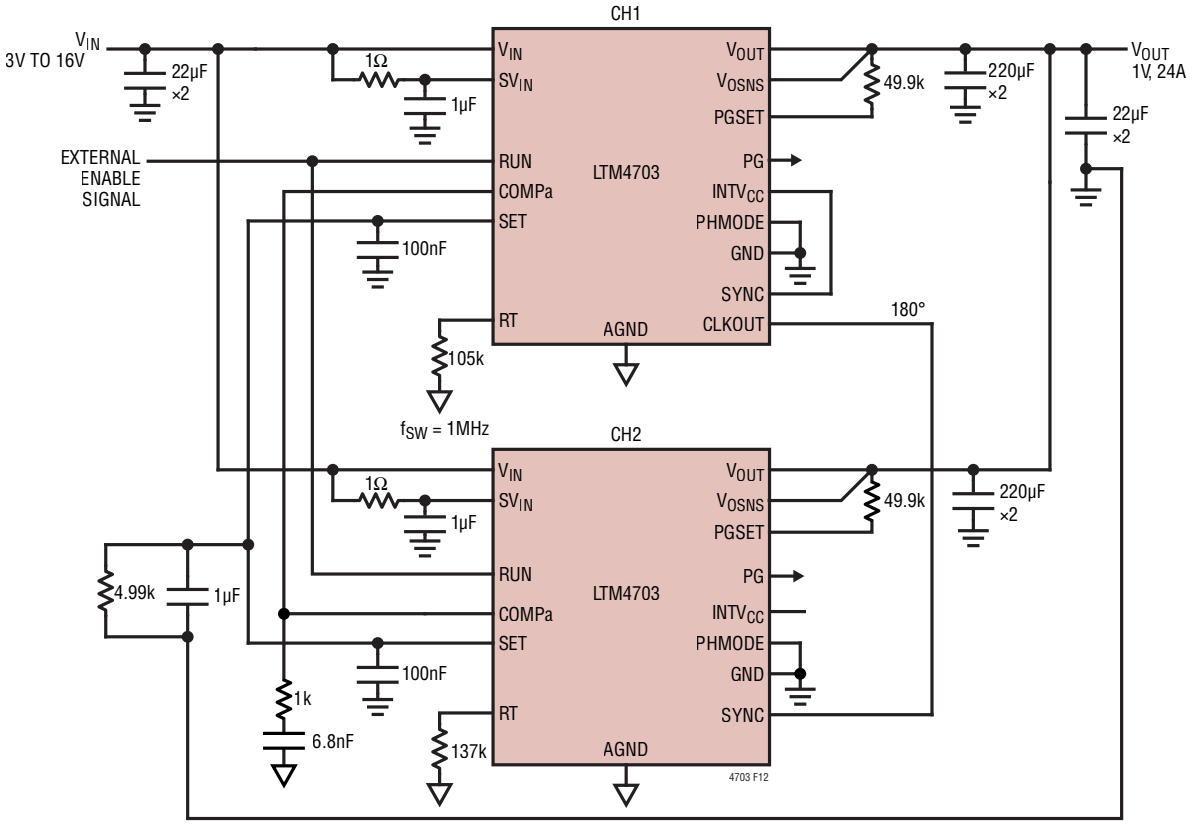
Figure 10. 1V/12A from 3V to 16V_{IN}, 800kHz with Soft-Start, Fast Start-Up and Power Good



PINS NOT USED: SW, SYNC, PHMODE, CLKOUT, $INTV_{CC}$.

Figure 11. 5V, 12A from 8.4V to 16V_{IN}, 1MHz with Soft-Start, Temperature Indicator and Power Good

TYPICAL APPLICATION

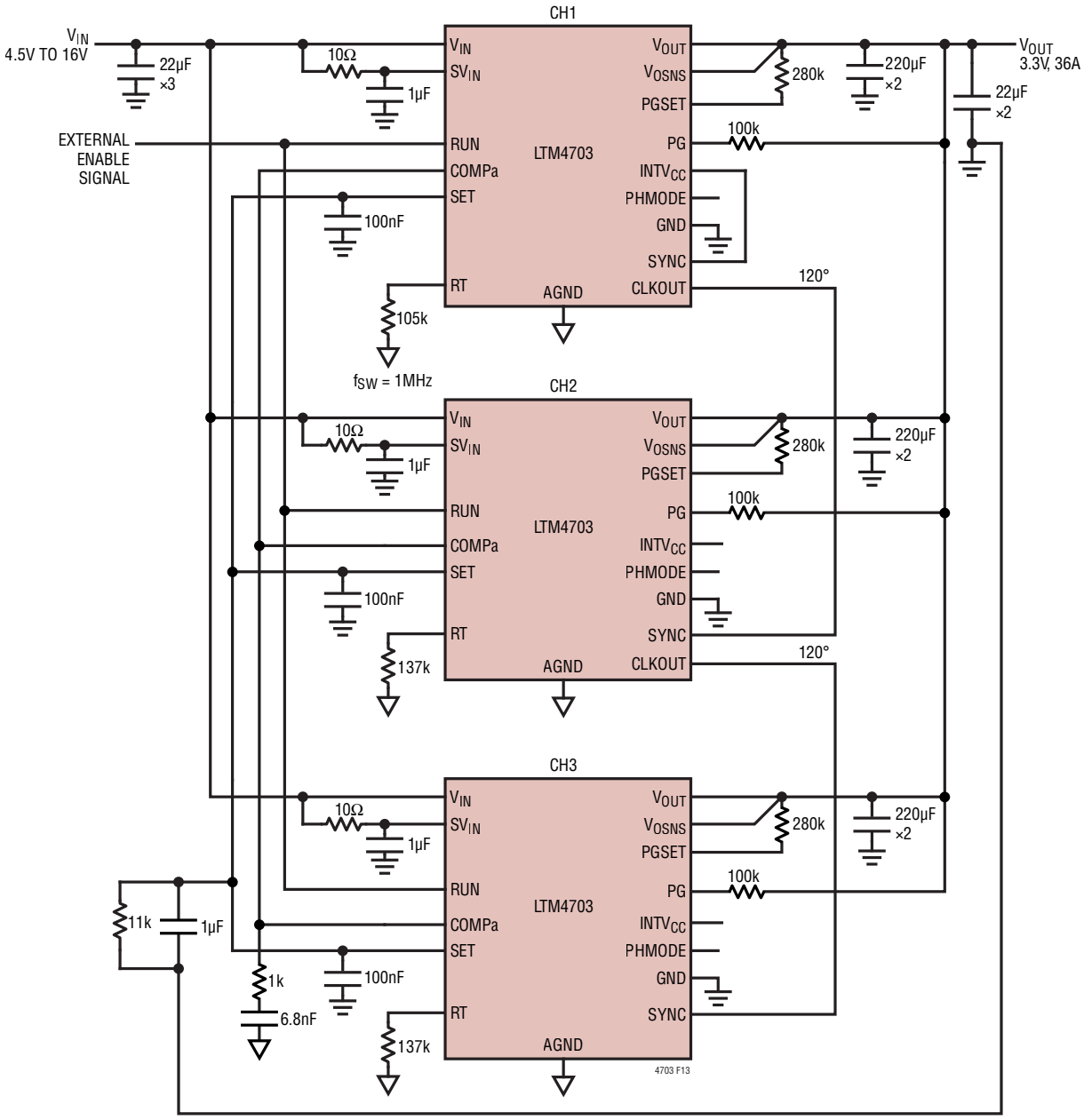


PINS NOT USED: COMPb, SW, T_{SENSE}^+, T_{SENSE}^-.

CH2 IS SYNCHRONIZED TO 1MHz VIA THE SYNC PIN. THE R_T RESISTOR VALUE MUST SET INTERNAL OSCILLATOR TO <0.8MHz (80% OF 1MHz).
COMPa PINS ARE CONNECTED TOGETHER.
PHMODE CONNECTED TO GND FOR 180°. PHASE SHIFT AT CLKOUT.
SET PINS CAN BE CONNECTED TOGETHER FOR 200µA CURRENT REFERENCE; THIS PROVIDES LOWER 1/f NOISE AND BETTER CURRENT SHARING.

Figure 12. 2-Phase 1V, 24A from 3V to 16V_{IN}, 1MHz with Soft-Start, Fast Start-Up and Power Good

TYPICAL APPLICATION

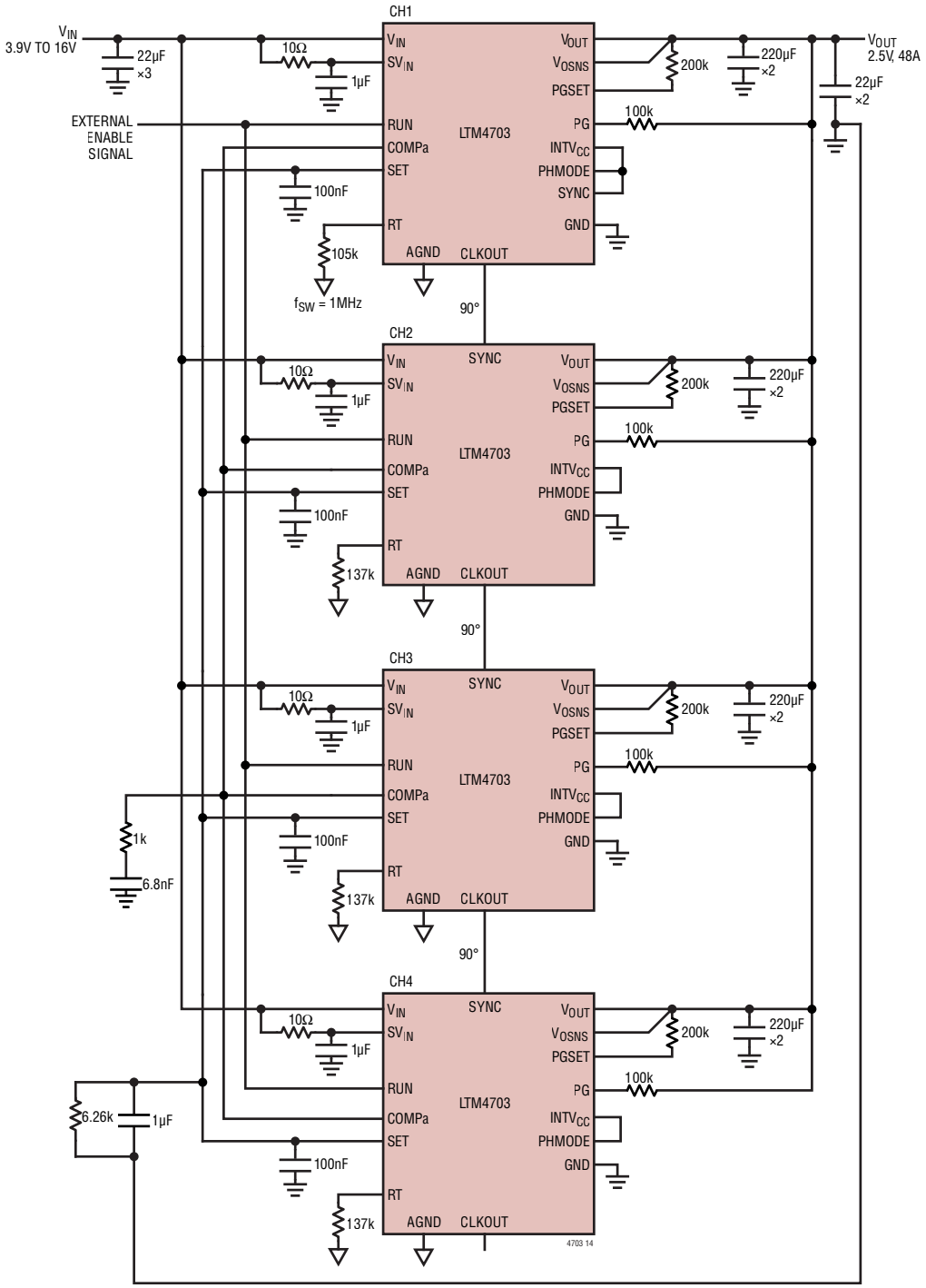


PINS NOT USED: COMPb, SW, T_{SENSE}^+, T_{SENSE}^-.

CH2 AND CH3 ARE SYNCHRONIZED TO 1MHz VIA THE SYNC PIN. THE R_T RESISTOR VALUE MUST SET INTERNAL OSCILLATOR TO <0.8MHz (80% OF 1MHz).
COMPa PINS ARE CONNECTED TOGETHER.
PHMODE PIN FLOATS FOR 120°. PHASE SHIFT AT CLKOUT.
SET PINS CAN BE CONNECTED TOGETHER FOR 300µA CURRENT REFERENCE; THIS PROVIDES LOWER 1/f NOISE AND BETTER CURRENT SHARING.

Figure 13. 3-Phase 3.3V, 36A from 4.5V to 16V_{IN}, 1MHz with Soft-Start, Fast Start-Up and Power Good

TYPICAL APPLICATION

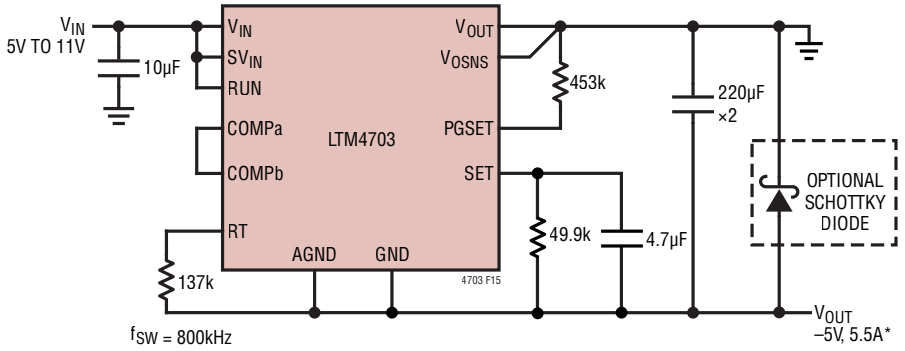


PINS NOT USED: COMPb, SW, T_{SENSE}^+, T_{SENSE}^-.

CH2 AND CH3 ARE SYNCHRONIZED TO 1MHz VIA THE SYNC PIN. THE R_T RESISTOR VALUE MUST SET INTERNAL OSCILLATOR TO <0.8MHz (80% OF 1MHz).
COMPa PINS ARE CONNECTED TOGETHER.
PHMODE IS CONNECTED TO $INTV_{CC}$ FOR 90°. PHASE SHIFT AT CLKOUT.
SET PINS CAN BE CONNECTED TOGETHER FOR 400µA CURRENT REFERENCE; THIS PROVIDES LOWER 1/f NOISE AND BETTER CURRENT SHARING.

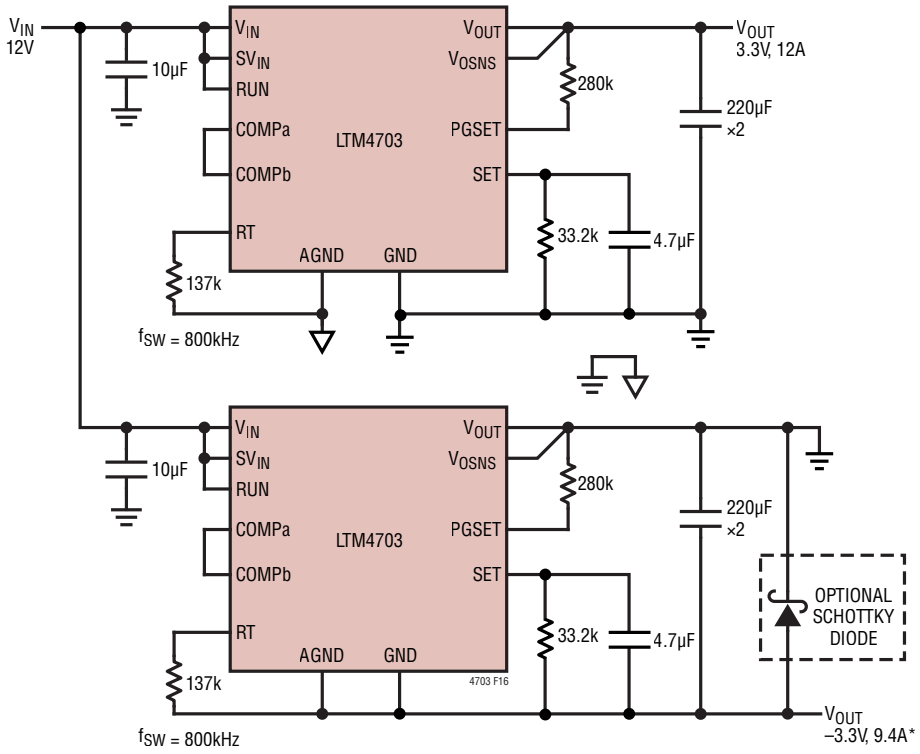
Figure 14. 4-Phase 2.5V, 48A from 3.9V to 16V_{IN}, 1MHz with Soft-Start, Fast Start-Up and Power Good

TYPICAL APPLICATION



*FOR DETAILS ON GENERATING NEGATIVE OUTPUT, REFER TO ANALOG DEVICES DESIGN NOTE 1021 (DN1021).

Figure 15. –5V, 5.5A from 5V to 11V_{IN}, 800kHz with Soft-Start



*FOR DETAILS ON GENERATING NEGATIVE OUTPUT, REFER TO ANALOG DEVICES DESIGN NOTE 1021 (DN1021).

Figure 16. 3.3V, 12A, –3.3V, 9.4A from 12V_{IN}, 800kHz with Soft-Start

PIN CONFIGURATION TABLE

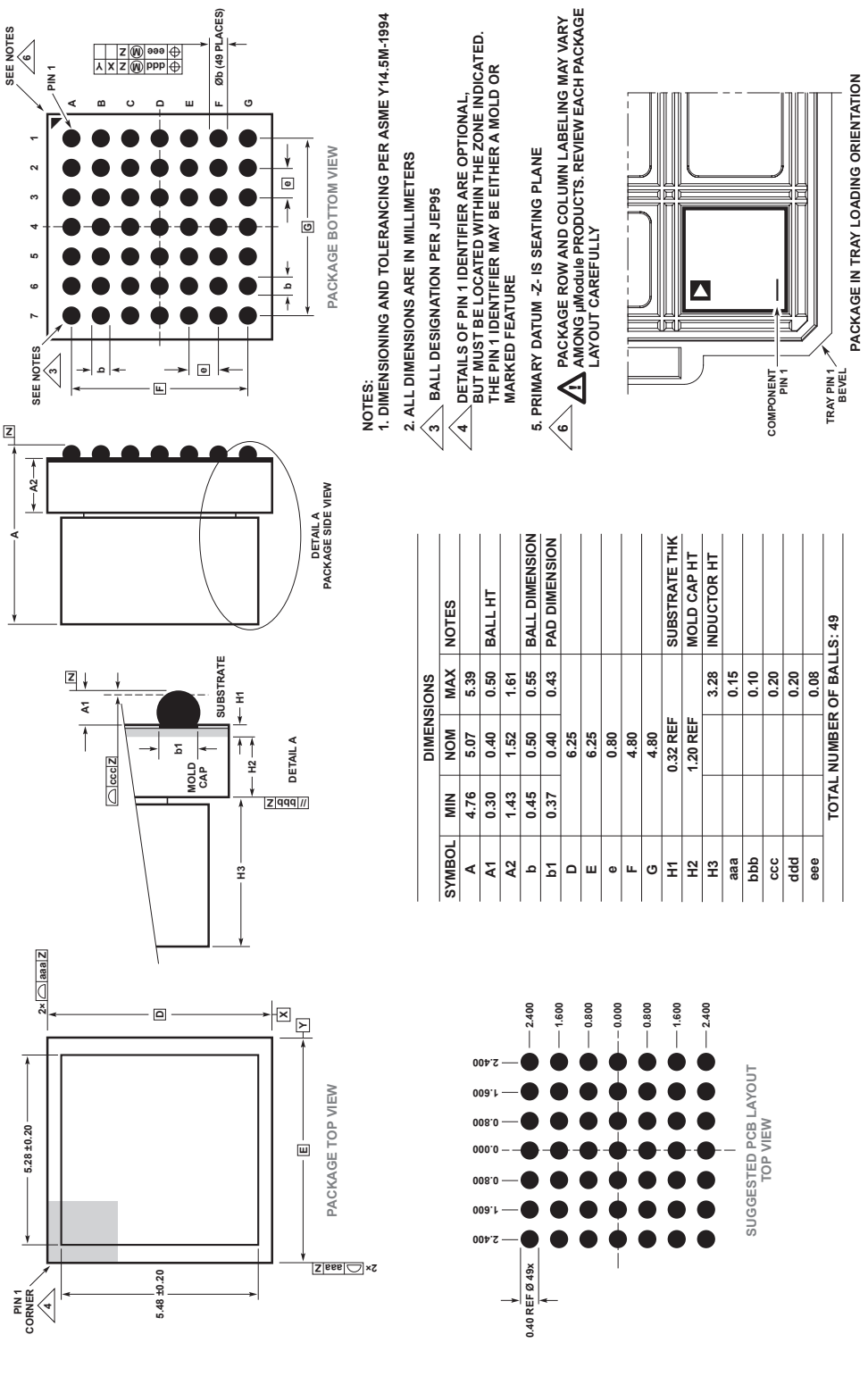
PACKAGE ROW AND COLUMN LABELING MAY VARY AMONG µModule PRODUCTS. REVIEW EACH PACKAGE LAYOUT CAREFULLY.

Table 4. LTM4703 Component BGA Pinout

PIN ID	FUNCTION	PIN ID	FUNCTION	PIN ID	FUNCTION	PIN ID	FUNCTION	PIN ID	FUNCTION	PIN ID	FUNCTION	PIN ID	FUNCTION
A1	V_{OUT}	A2	V_{OUT}	A3	V_{OUT}	A4	SV_{IN}	A5	V_{IN}	A6	V_{IN}	A7	V_{IN}
B1	T_{SENSE}^+	B2	T_{SENSE}^-	B3	V_{OUT}	B4	GND	B5	V_{IN}	B6	V_{IN}	B7	V_{IN}
C1	RUN	C2	COMPa	C3	COMPb	C4	GND	C5	GND	C6	GND	C7	GND
D1	RT	D2	AGND	D3	$INTV_{CC}$	D4	GND	D5	GND	D6	GND	D7	GND
E1	SET	E2	PGSET	E3	PHMODE	E4	GND	E5	GND	E6	GND	E7	GND
F1	V_{OSNS}	F2	PG	F3	V_{OUT}	F4	GND	F5	GND	F6	SW	F7	CLKOUT
G1	V_{OUT}	G2	V_{OUT}	G3	V_{OUT}	G4	GND	G5	GND	G6	SYNC	G7	GND

PACKAGE DESCRIPTION

49-Ball Chip Scale Package Ball Grid Array [CSP_BGA]
6.25mm × 6.25mm × 5.07mm
(Reference DWG # BC-49-9)



NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994
2. ALL DIMENSIONS ARE IN MILLIMETERS
3. BALL DESIGNATION PER JEP95
4. DETAILS OF PIN 1 IDENTIFIER ARE OPTIONAL, BUT MUST BE LOCATED WITHIN THE ZONE INDICATED. THE PIN 1 IDENTIFIER MAY BE EITHER A MOLD OR MARKED FEATURE
5. PRIMARY DATUM -Z- IS SEATING PLANE
6. PACKAGE ROW AND COLUMN LABELING MAY VARY AMONG µModule PRODUCTS. REVIEW EACH PACKAGE LAYOUT CAREFULLY

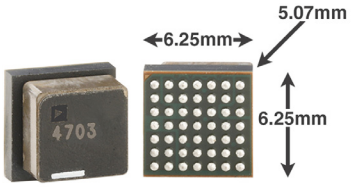
DIMENSIONS				
SYMBOL	MIN	NOM	MAX	NOTES
A	4.76	5.07	5.39	
A1	0.30	0.40	0.50	BALL HT
A2	1.43	1.52	1.61	
b	0.45	0.50	0.55	BALL DIMENSION
b1	0.37	0.40	0.43	PAD DIMENSION
D		6.25		
E		6.25		
e		0.80		
F		4.80		
G		4.80		
H1		0.32 REF		SUBSTRATE THK
H2		1.20 REF		MOLD CAP HT
H3			3.28	INDUCTOR HT
aaa			0.15	
bbb			0.10	
ccc			0.20	
ddd			0.20	
eee			0.08	
TOTAL NUMBER OF BALLS: 49				

REVISION HISTORY

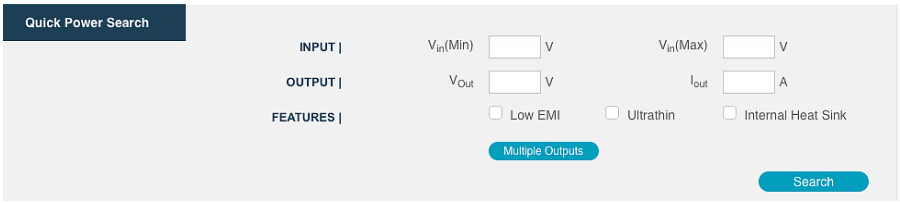
REV	DATE	DESCRIPTION	PAGE NUMBER
0	08/24	Initial Release.	—

PACKAGE PHOTOS

Part marking is either ink mark or laser mark



DESIGN RESOURCES

SUBJECT	DESCRIPTION	
µModule Design and Manufacturing Resources	Design: • Selector Guides • Demo Boards and Gerber Files • Free Simulation Tools	Manufacturing: • Quick Start Guide • PCB Design, Assembly and Manufacturing Guidelines • Package and Board Level Reliability
µModule Regulator Products Search	1. Sort table of products by parameters and download the result as a spread sheet. 2. Search using the Quick Power Search parametric table. 	
Digital Power System Management	Analog Devices' family of digital power supply management ICs are highly integrated solutions that offer essential functions, including power supply monitoring, supervision, margining and sequencing, and feature EEPROM for storing user configurations and fault logging.	

RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LTM8053	40V, 3.5A Low EMI Silent Switcher µModule Regulator	$3.4V \le V_{IN} \le 40V$, $0.97V \le V_{OUT} \le 15V$, 6.25mm × 9mm × 3.32mm BGA
LTM8065	40V, 2.5A Low EMI Silent Switcher µModule Regulator	$3.4V \le V_{IN} \le 40V$, $0.97V \le V_{OUT} \le 18V$, 6.25mm × 6.25mm × 2.32mm BGA
LTM8063	40V, 2A Low EMI Silent Switcher µModule Regulator	$3.2V \le V_{IN} \le 40V$, $0.8V \le V_{OUT} \le 15V$, 4mm × 6.25mm × 2.22mm BGA
LTM8074	40V, 1.2A Low EMI Silent Switcher µModule Regulator	$3.2V \le V_{IN} \le 40V$, $0.8V \le V_{OUT} \le 12V$, 4mm × 4mm × 1.82mm BGA
LTM8024	40V, Dual 3.5A Low EMI Silent Switcher µModule Regulator	$3V \le V_{IN} \le 40V$, $0.8V \le V_{OUT} \le 8V$, 9mm × 11.25mm × 3.32mm BGA
LTM8078	40V, Dual 1.4A Low EMI Silent Switcher µModule Regulator	$3V \le V_{IN} \le 40V$, $0.8V \le V_{OUT} \le 10V$, 6.25mm × 6.25mm × 2.32mm BGA
LTM8060	40V, Quad 3A Low EMI Silent Switcher µModule Regulator	$3V \le V_{IN} \le 40V$, $0.8V \le V_{OUT} \le 8V$, 11.9mm × 16mm × 3.32mm BGA
LTM8051	40V, Quad 1.2A Low EMI Silent Switcher µModule Regulator	$3V \le V_{IN} \le 40V$, $0.8V \le V_{OUT} \le 8V$, 6.25mm × 11.25mm × 2.32mm BGA
LTM8080	$40V_{IN}$, Dual 500mA or Single 1A Ultralow Noise, Ultrahigh PSRR µModule Regulator	$3.5V \le V_{IN} \le 40V$, $0V \le V_{OUT} \le 8V$, 6.25mm × 9mm × 3.32mm BGA
LTM4657	8A µModule Regulator, Pin Compatible with LTM4638	$3.1V \le V_{IN} \le 20V$, $0.5V \le V_{OUT} \le 5.5V$, 6.25mm × 6.25mm × 3.87mm BGA
LTM4626	12A µModule Regulator, Pin Compatible with LTM4638	$3.1V \le V_{IN} \le 20V$, $0.6V \le V_{OUT} \le 5.5V$, 6.25mm × 6.25mm × 3.87mm BGA
LTM4638	15A µModule Regulator, Pin Compatible with LTM4657/LTM4626	$3.1V \le V_{IN} \le 20V$. $0.6V \le V_{OUT} \le 5.5V$. 6.25mm × 6.25mm × 5.02mm BGA
LTM4702	$16V_{IN}$ 8A Ultralow Noise Silent Switcher µModule Regulator, Pin Compatible with LTM4703	$3V \le V_{IN} \le 16V$, $0.3V \le V_{OUT} \le 5.7V$, 6.25mm × 6.25mm × 5.07mm BGA
LTM4709	Triple 3A, Ultralow Noise, High PSRR, Ultrafast µModule Linear Regulator with Configurable Output Array	$0.6V \le V_{IN} \le 5.5V$, $0.5V \le V_{OUT} \le 4.2V$, 6mm × 12mm × 1.92mm BGA