High Efficiency Thermoelectric Cooler Controller

FEATURES

- **High Efficiency, Low Noise Topology**
- **Adjustable Output Slew Rate Reduces EMI**
- **Full-Bridge Controller for Bidirectional Current Control**
- **Adjustable Pulse-by-Pulse Bidirectional TEC Current Limit**
- **Open/Shorted Thermistor Indication**
- **Solution Footprint in Less Than 0.6" × 0.8" (Double-Sided PCB)**
- **Available in 5mm x 5mm QFN and 28-Pin SSOP Packages**
- TEC Voltage Clamping
- TEC Current, Voltage and Heat/Cool Status Outputs
- Adjustable/Synchronizable Oscillator Frequency Reduces Filter Component Size and System Noise
- 2.5V Reference Voltage Output
- 2.7V Minimum Operating Voltage

APPLICATIONS

- Laser-Based Fiber Optic Links
- Medical Instruments
- CPU Temperature Regulators

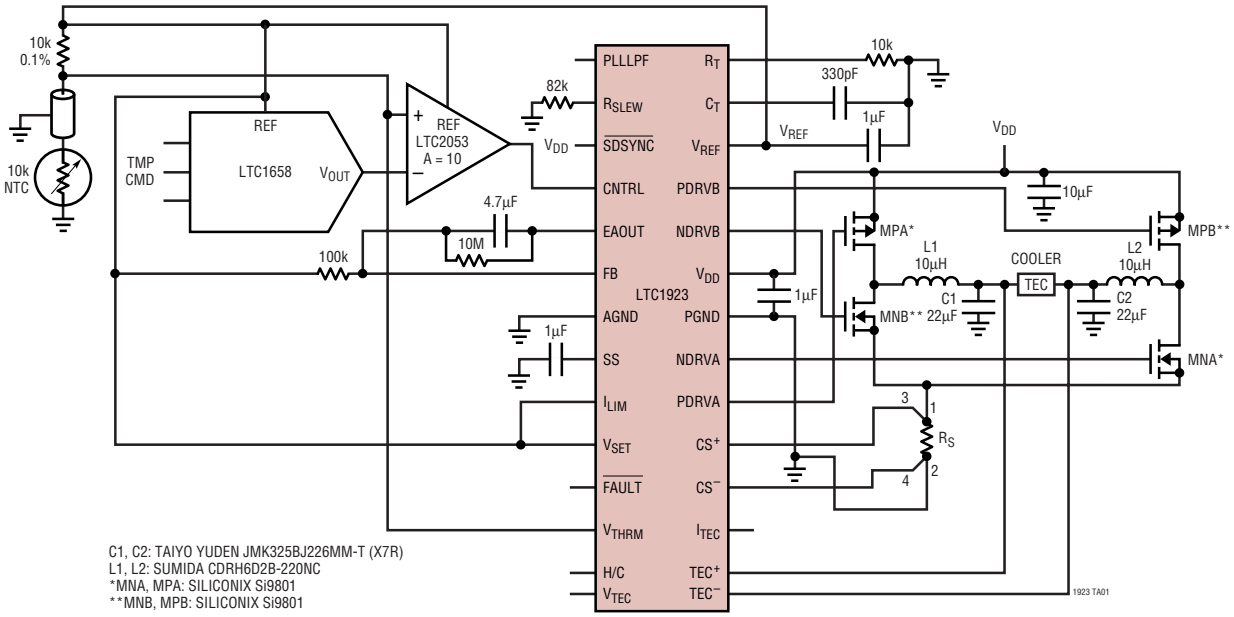
DESCRIPTION

The LTC®1923 is a pulse width modulator intended for thermoelectric cooler (TEC) or heater applications requiring either unidirectional or bidirectional drive circuits. All of the necessary control circuitry and two sets of complementary output drivers are integrated into the LTC1923 to drive a full bridge, providing an efficient means of bidirectional current flow to the TEC. An accurate temperature control loop to stabilize the temperature of a laser diode system is easily achieved with the addition of just a few external components. Typical temperature setpoint accuracy of 0.1°C is achievable with the LTC1923. Adding an instrumentation amplifier front end allows setpoint stability of 0.01°C.

The part features independent adjustable heating and cooling pulse-by-pulse current limit, current soft-start for controlled start-up, output slew rate control to reduce system noise, differential current sense and voltage amplifiers and a host of auxiliary circuits to protect the laser and provide redundant system monitoring.

TYPICAL APPLICATION

Laser Temperature Control Loop Achieving Setpoint Stability of 0.01°C

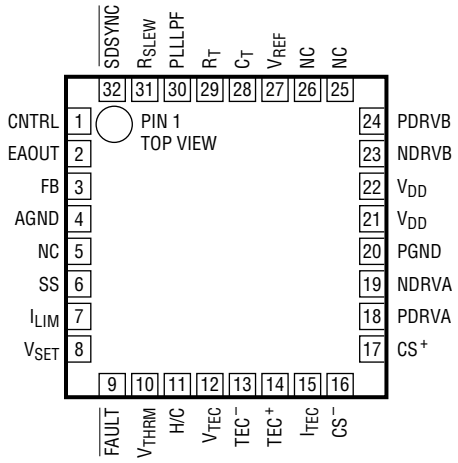


C1, C2: TAIYO YUDEN JMK325BJ226MM-T (X7R)
L1, L2: SUMIDA CDRH6D2B-220NC
*MNA, MPA: SILICONIX Si9801
**MNB, MPB: SILICONIX Si9801

ABSOLUTE MAXIMUM RATINGS (Note 1)

V_{DD} to GND ..... –0.3V to 6V
$\overline{SDSYNC}$, R_{SLEW} ..... –0.3V to 6V
FB, CNTRL, V_{THRM}, I_{LIM}, V_{SET} ..... –0.3V to 6V
CS^+, CS^-, TEC^+, TEC^- ..... –0.3V to 6V
$\overline{FAULT}$, H/C ..... –0.3V to 6V
Operating Temperature Range (Note 2) .. –40°C to 85°C
Storage Temperature Range ..... –65°C to 125°C
Lead Temperature (Soldering, 10 sec) ..... 300°C

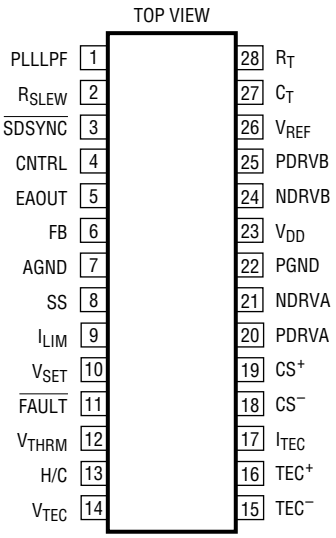
PACKAGE/ORDER INFORMATION



UH PACKAGE
32-LEAD PLASTIC QFN

T_{JMAX} = 125°C, θ_{JA} = 34°C/W

ORDER PART NUMBER
LTC1923EUH



GN PACKAGE
28-LEAD PLASTIC SSOP

T_{JMAX} = 125°C, θ_{JA} = 120°C/W

ORDER PART NUMBER
LTC1923EGN

Consult LTC Marketing for parts specified with wider operating temperature ranges.

ELECTRICAL CHARACTERISTICS

The ● denotes specifications which apply over the full operating temperature range, otherwise specifications are T_A = 25°C. V_{DD} = 5V, R_{SLEW} = V_{DD}, $\overline{SDSYNC}$ = V_{DD}, R_T = 10k, C_T = 330pF unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Input Supply							
VDD	Operating Supply Voltage		●	2.7		5.5	V
UVLO	Undervoltage Lockout	Low to High Threshold	●		2.6	2.7	V
UVHYST	Hysteresis	High to Low	●	50	130		mV
I_{DD}	Operating Supply Current	No Output Load, Outputs Not Switching			2	4	mA
I_{DDSHDN}	Shutdown I_{DD}	$\overline{SDSYNC}$ = 0V			10	25	µA
SHDNTH	Shutdown Threshold	Measured at PDRVA, PDRVB		0.3	0.8	1.4	V

ELECTRICAL CHARACTERISTICS

The ● denotes specifications which apply over the full operating temperature range, otherwise specifications are T_A = 25°C. V_{DD} = 5V, R_{SLEW} = V_{DD}, $\overline{SDSYNC}$ = V_{DD}, R_T = 10k, C_T = 330pF unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Reference							
V_{REF}	Reference Output Voltage	No Load	 ●	2.462 2.450	2.5	2.538 2.550	V V
V_{REFGD}	V_{REF} Good Threshold	V_{REF} Rising Threshold	●		2.25	2.45	V
LDREG	Load Regulation	I_{LOAD} = –1mA to –10mA			10	25	mV
LINEREG	Line Regulation	V_{DD} = 2.7V to 5.5V			5	20	mV
V_{REFISC}	Short-Circuit Current	V_{REF} = 0V		10	20		mA
Oscillator and Phase-Locked Loop							
f_{OSCI}	Initial Oscillator Frequency	R_T = 10k, C_T = 330pF		190	225	260	kHz
f_{OSC}	Frequency Variation	V_{DD} = 2.7V to 5V, C_T = 330pF, R_T = 10k	●	165	225	270	kHz
OSCPK	C_T Ramp Peak			1.4	1.5	1.6	V
OSCVLY	C_T Ramp Valley			0.4	0.5	0.6	V
C_{TICH}	C_T Charge Current	C_T = 0.3V, R_T = 10k			–150		µA
C_{TIDIS}	C_T Discharge Current	C_T = 1.8V, R_T = 10k			150		µA
PLLGAIN	Gain from PLLLPF to R_T			–1.1	–0.9	–0.7	V/V
I_{PLLLPF}	Phase Detector Output Current Sinking Sourcing	 $f_{SYNC} < f_{OSC}$ $f_{SYNC} > f_{OSC}$			 12 –12		 µA µA
MSTTH	Master Threshold On PLLLPF Pin	Measured at $\overline{SDSYNC}$ Pin		V_{DD} – 0.7	V_{DD} – 0.4		V
SDDLY	Shutdown Delay to Output			20	45		µs
Error Amplifier							
V_{OS}	Input Offset Voltage	EAOUT = 1V, V_{CM} = 2.5V		–18		18	mV
AOL	Open-Loop Gain	EAOUT = 0.45V to 1.55V, CNTRL = 2.5V			80		dB
V_{CM}	Common Mode Input Range	EAOUT = 1V		0.2		V_{DD} + 0.2	V
I_{IB}	FB and CNTRL Input Bias Currents	FB = CNTRL = 1.25		–100		100	nA
V_{OH}	Output High	I_{LOAD} = –100µA			1.65		V
V_{OL}	Output Low	I_{LOAD} = 100µA			0.3	0.45	V
I_{SOURCE}	Sourcing Current	EAOUT = 1V, FB = 2.4V, CNTRL = 2.5V			–1.5	–0.5	mA
I_{SINK}	Sinking Current	EAOUT = 1V, FB = 5V, CNTRL = 2.5V		1	2		mA
GBW	Gain-Bandwidth Product	f = 100kHz (Note 3)			2		MHz
Current Sense Amplifier							
ACS	Amplifier Gain				10		V/V
CSOFF	Amplifier Offset	Measured at I_{TEC}		–15	–2	10	mV
I_{TECH}	Output Sourcing Load Regulation	CS^+ - CS^- = 100mV, I_{LOAD} = 0 to –50µA			0.1	0.2	V
I_{TECL}	Output Sinking Load Regulation	CS^+ - CS^- = 100mV, I_{LOAD} = 0 to 50µA			0.1	0.2	V
f3dB	–3dB Frequency	(Note 3)			500		kHz
I_{LIMTH}	Current Limit Threshold	Measured at CS^+, CS^-	●	125	145	165	mV
I_{LIMDLY}	Current Limit Delay to Output				300	450	ns
SSI_{CHG}	Soft-Start Charge Current	SS = 0.75V		–2.5	–1.5	–0.5	µA
SSI_{LIM}	Soft-Start Current Limit Threshold	SS = 0.5V, Measured at CS^+, CS^-		50	70	90	mV
I_{LIM}	I_{LIM} Current Limit Threshold	I_{LIM} = 0.5V, Measured at CS^+, CS^-		50	70	90	mV

ELECTRICAL CHARACTERISTICS

The ● denotes specifications which apply over the full operating temperature range, otherwise specifications are T_A = 25°C. V_{DD} = 5V, R_{SLEW} = V_{DD}, $\overline{SDSYNC}$ = V_{DD}, R_T = 10k, C_T = 330pF unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
TEC Voltage Amplifier							
ATEC	Amplifier Gain			0.98	1	1.02	V/V
TECOFF	Amplifier Offset	Measured at V_{TEC}, V_{CM} = 2.5V			–7		mV
TECCMR	Common Mode Rejection	0.1V < V_{CM} < 4.9V			60		dB
V_{TECH}	Output High Voltage	I_{LOAD} = –50µA		4.7	4.9		V
V_{TECL}	Output Low Voltage	I_{LOAD} = 50µA			0.1	0.3	V
f3dB	–3dB Frequency	(Note 3)			1		MHz
Output Drivers							
OUTH	Output High Voltage	I_{OUT} = –100mA		4	4.5		V
OUTL	Output Low Voltage	I_{OUT} = 100mA			0.7	1.2	V
t_{RISE}	Output Rise Time	C_{LOAD} = 1nF			20		ns
t_{FALL}	Output Fall Time	C_{LOAD} = 1nF			20		ns
t_{rSLEW}	Output Rise Time	C_{LOAD} = 1nF, R_{SLEW} = 10k			20		ns
t_{fSLEW}	Output Fall Time	C_{LOAD} = 1nF, R_{SLEW} = 10k			20		ns
t_{rSLEW}	Output Rise Time	C_{LOAD} = 1nF, R_{SLEW} = 100k			90		ns
t_{fSLEW}	Output Slew Fall Time	C_{LOAD} = 1nF, R_{SLEW} = 100k			90		ns
SLEWVT	R_{SLEW} Disable Threshold				2.75		V
DLY	Output Dead Time	R_T = 10k			90		ns
Fault							
OPENTH	Open Thermistor Threshold	V_{SET} = 5V, Measured with Respect to V_{SET}			–410		mV
SHRTTH	Shorted Thermistor Threshold	V_{SET} = 5V, Measured with Respect to GND			0.975		V
FLTV	Fault Output Low Voltage	1mA Into $\overline{FAULT}$, During Fault			150	300	mV
Direction Comparator							
DIRH	Low-to-High Threshold	TEC^- = 2.5V, Measured with Respect to TEC^- Sensed When H/C Toggles Low			50		mV
DIRL	High-to-Low Threshold	TEC^- = 2.5V, Measured with Respect to TEC^- Sensed When H/C Toggles High			–50		mV
HCV	H/C Output Low Voltage	1mA Into Pin			150	300	mV

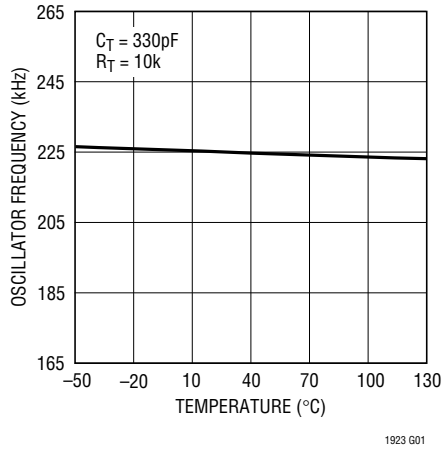
Note 1: Absolute Maximum Ratings are those values beyond which the life of a device may be impaired.

Note 2: The LTC1923E is guaranteed to meet specifications from 0°C to 70°C. Specifications over the –40°C to 85°C operating temperature range are assured by design, characterization and correlation with statistical process controls.

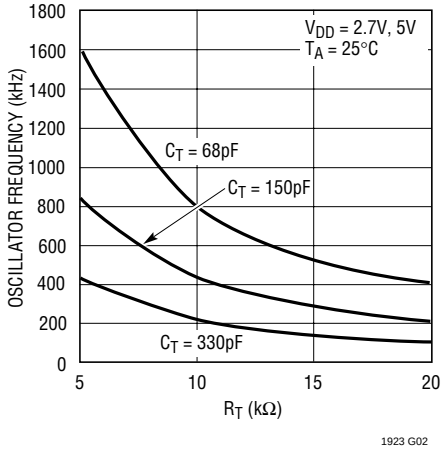
Note 3: Guaranteed by design, not tested in production.

TYPICAL PERFORMANCE CHARACTERISTICS

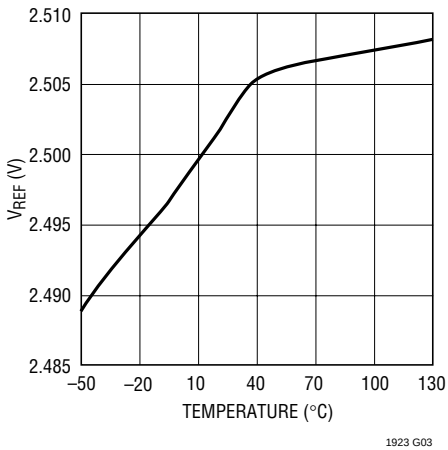
Oscillator Frequency vs Temperature



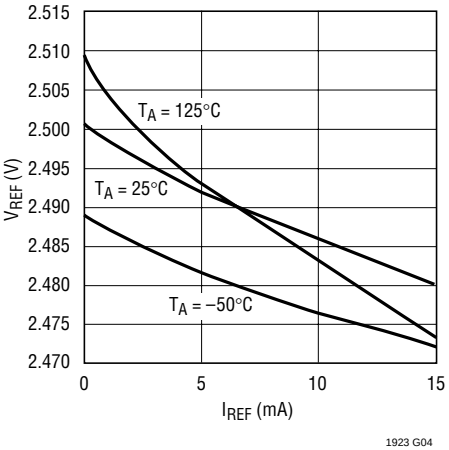
Oscillator Frequency vs R_T



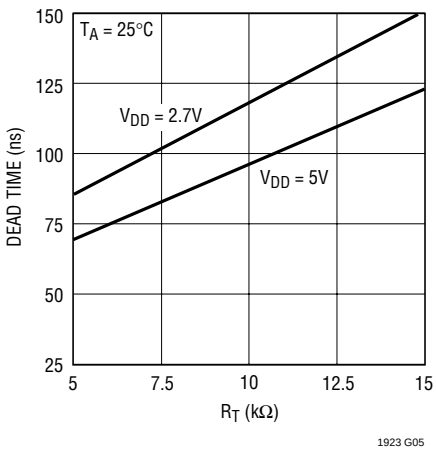
V_{REF} vs Temperature



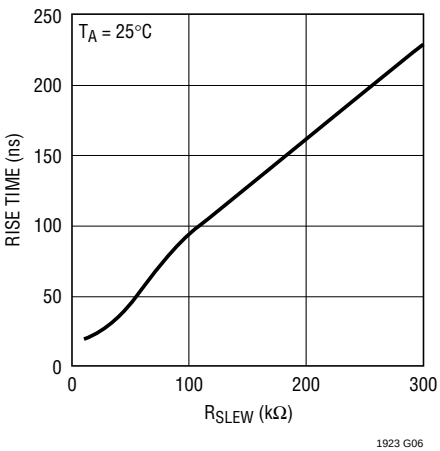
V_{REF} vs I_{REF} for Different Temperatures



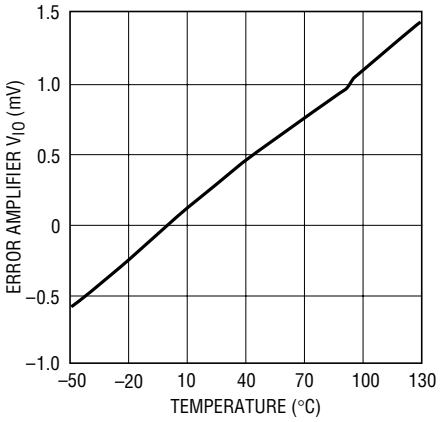
Output Dead Time vs R_T



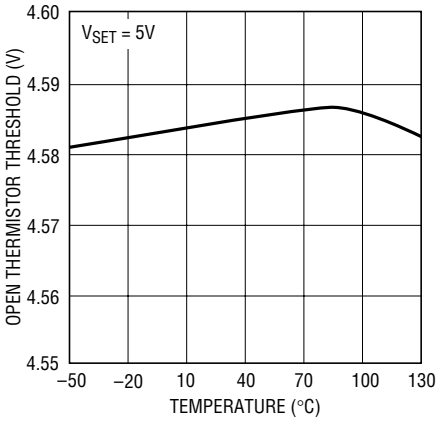
Output Rise/Fall Time vs R_{SLEW}



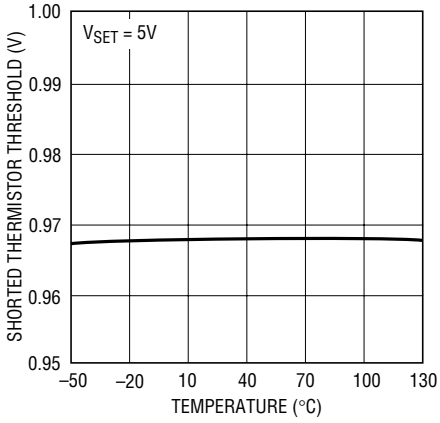
Error Amplifier Offset Voltage vs Temperature



Open Thermistor Threshold vs Temperature

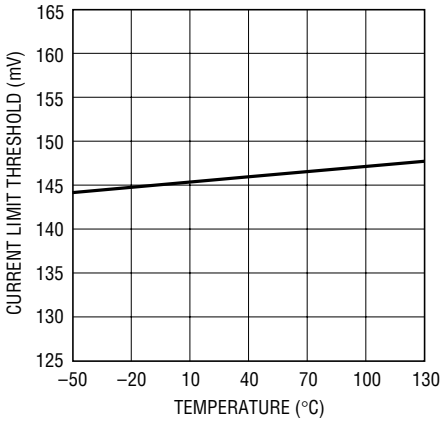


Shorted Thermistor Threshold vs Temperature

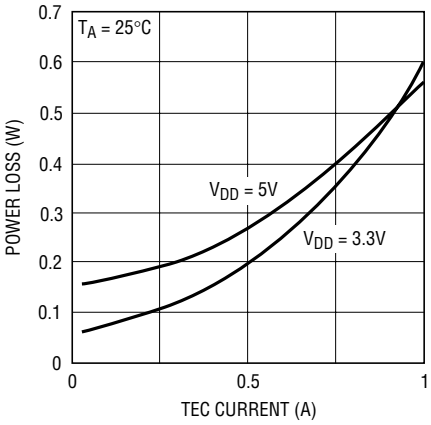


TYPICAL PERFORMANCE CHARACTERISTICS

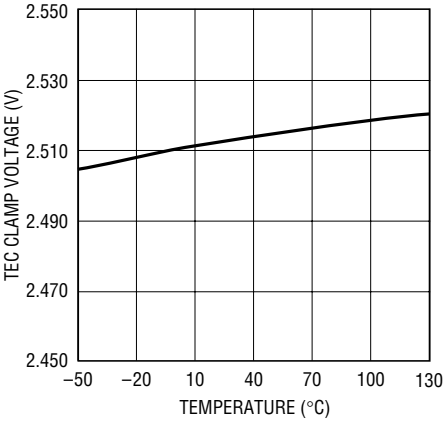
Current Limit Threshold vs Temperature



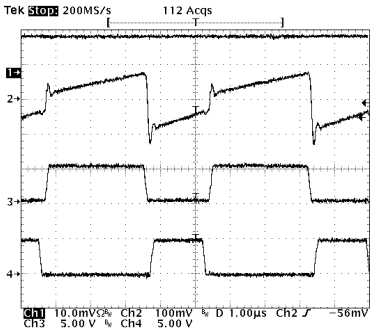
System Power Loss vs TEC Current



TEC Clamp Voltage vs Temperature



Representative Waveforms for NDRVA, NDRVB, TEC Current and CS⁺ – CS⁻



CH1: TEC CURRENT (500mA/DIV)

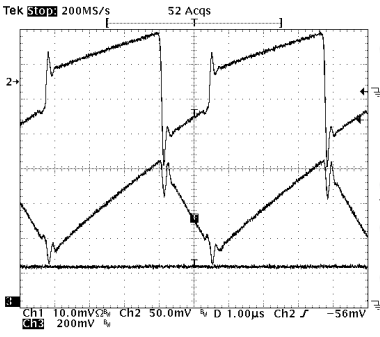
CH2: VOLTAGE ACROSS 0.1Ω SENSE RESISTOR (CS⁺ – CS⁻) 100mV/DIV

CH3: NDRVA (5V/DIV)

CH4: NDRVB (5V/DIV)

V_{DD} = 5V
R_{TEC} = 2.5Ω
R_S = 0.1Ω

Representative Waveforms for TEC Current, CS⁺ – CS⁻ and ITEC



CH2: VOLTAGE ACROSS 0.1Ω SENSE RESISTOR R_S (CS⁺ – CS⁻) 100mV/DIV

CH2

CH3: VOLTAGE ON I_{TEC} PIN EQUAL TO TEN TIMES THE ABSOLUTE VALUE OF CH2 (200mV/DIV)

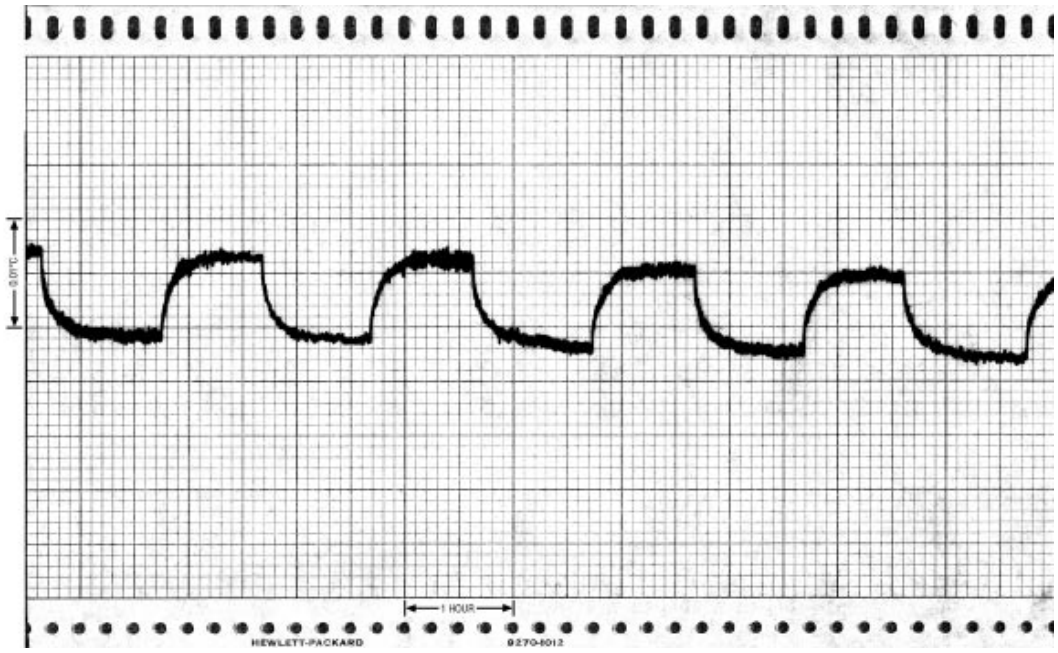
CH1: TEC CURRENT (500mA/DIV)

CH1, CH3

V_{DD} = 5V
R_{TEC} = 2.5Ω
R_S = 0.1Ω

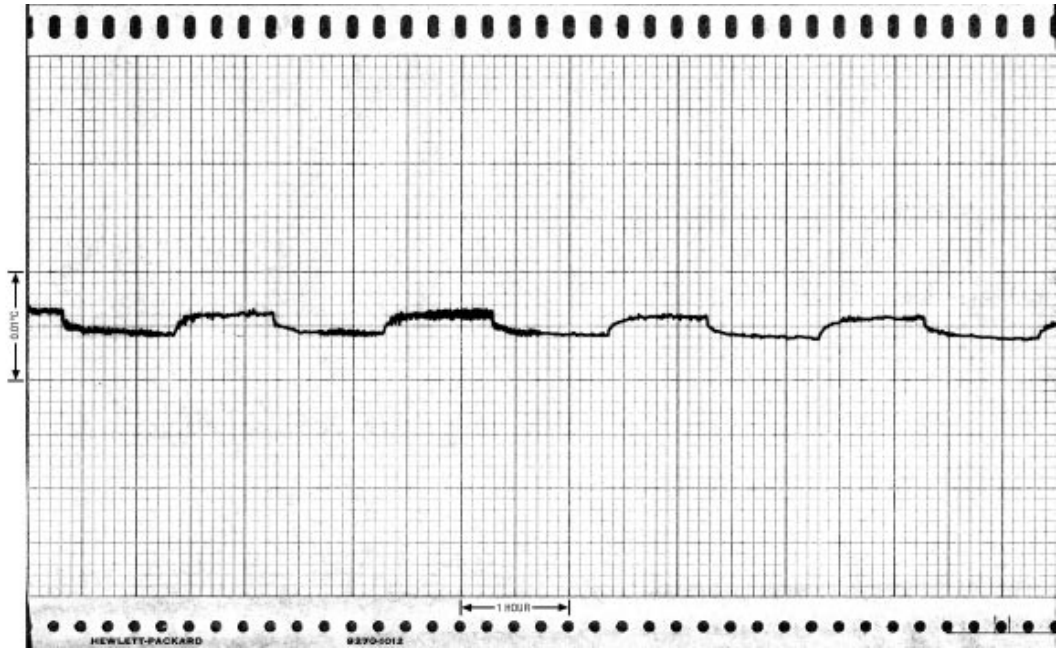
TYPICAL PERFORMANCE CHARACTERISTICS

Long-Term Cooling Mode Stability Measured in Environment that Steps 20 Degrees Above Ambient Every Hour. Data Shows Resulting 0.008°C Peak-to-Peak Variation, Indicating Thermal Gain of 2500. 0.0025°C Baseline Tilt Over Plot Length Derives From Varying Ambient Temperature



1923 G13.tif

Identical Test Conditions as Above, Except in Heating Mode. TEC's Higher Heating Mode Efficiency Results in Higher Thermal Gain. 0.002°C Peak-to-Peak Variation Is 4x Stability Improvement. Baseline Tilt, Just Detectable, Shows Similar 4x Improvement vs Above



1923 G14.tif

PIN FUNCTIONS (GN Package/UH Package)

PLLLPF (Pin 1/Pin 30): This pin serves as the lowpass filter for the phase-locked loop when the part is being synchronized. The average voltage on this pin equally alters both the oscillator charge and discharge currents, thereby changing the frequency of operation. Bringing the voltage on this pin above V_{DD} – 0.4V signifies that the part will be used as the synchronization master. This allows multiple devices on the same board to be operated at the same frequency. The $\overline{SDSYNC}$ pin will be pulled low during each C_T charging cycle to facilitate synchronization.

R_{SLEW} (Pin 2/Pin 31): Placing a resistor from this pin to AGND sets the voltage slew rate of the output driver pins. The minimum resistor value is 10k and the maximum value is 300k. Slew rate limiting can be disabled by tying this pin to V_{DD}, allowing the outputs to transition at their maximum rate.

$\overline{SDSYNC}$ (Pin 3/Pin 32): This pin can be used to disable the IC, synchronize the internal oscillator or be the master to synchronize other devices. Grounding this pin will disable all internal circuitry and cause NDRVA and NDRVB to be forced low and PDRVA and PDRVB to be forced to V_{DD}. EAOUT will be forced low. $\overline{FAULT}$ will also be asserted low indicating a fault condition. The pin can be pulled low for up to 20µs without triggering the shutdown circuitry. The part can either be slaved to an external clock or can be used as the master (see Applications Information for a more detailed explanantion).

CNTRL (Pin 4/Pin 1): Noninverting Input to the Error Amplifier.

EAOUT (Pin 5/Pin 2): Output of the Error Amplifier. The loop compensation network is connected between this pin and FB. The voltage on this pin is the input to the PWM comparator and commands anywhere between 0% and 100% duty cycle to control the temperature of the temperature sense element.

FB (Pin 6/Pin 3): The Inverting Input to the Error Amplifier. This input is connected to EAOUT through a compensating feedback network.

AGND (Pin 7/Pin 4): Signal Ground. All voltages are measured with respect to AGND. Bypass V_{DD} and V_{REF} with low ESR capacitors to the ground plane near this pin.

SS (Pin 8/Pin 6): The TEC current can be soft-started by adding a capacitor from this pin to ground. This capacitor will be charged by a 1.5µA current source. This pin connects to one of the inverting inputs of the current limit comparator and allows the TEC current to be linearly ramped up from zero. The voltage on this pin must be greater than 1.5V to allow the open/shorted thermistor window comparitor to signal a fault.

I_{LIM} (Pin 9/Pin 7): A voltage divider from V_{REF} to this pin sets the current limit threshold for the TEC. If the voltage on this pin is set higher than 1V, then I_{LIMIT} = 150mV/R_S as that is the internal current limit comparator level. If the voltage on this pin is set less than 1V, the current limit value where the comparator trips is:

$$I_{LIMIT} = [0.15 \bullet R_{ILIM1} \bullet V_{REF}]/[(R_{ILIM1} + R_{ILIM2}) \bullet R_S]$$

V_{SET} (Pin 10/Pin 8): This is the input for the setpoint reference of the temperature sense element divider network or bridge. This pin must be connected to the bias source for the thermistor divider network.

$\overline{FAULT}$ (Pin 11/Pin 9): Open-drain output that indicates by pulling low when the voltage on V_{THRM} is outside the specified window, the part is in shutdown, undervoltage lockout (UVLO), or the reference is not good. When the voltage on V_{THRM} is outside the specified window, it signifies that the thermistor impedance is out of its acceptable range. This signal can be used to flag a microcontroller to shut the system down or used to disconnect power from the bridge. See Applications Information for using this signal for redundant protection.

V_{THRM} (Pin 12/Pin 10): Voltage Across the Thermistor. If the voltage on this pin is outside the range between 410mV below V_{SET} and 0.2 • V_{SET}, the $\overline{FAULT}$ pin will be asserted (and latched) low indicating that the thermistor temperature has moved outside the acceptable range.

H/C (Pin 13/Pin 11): This open-drain output provides the direction information of the TEC current flow. If TEC^+ is greater than TEC^-, which typically corresponds to the system cooling, this output will be a logic low. If the opposite is the case, this pin will pull to a logic high.

PIN FUNCTIONS (GN Package/UH Package)

V_{TEC} (Pin 14/Pin 12): Output of the differential TEC voltage amplifier equal to the magnitude of the voltage across the TEC.

TEC⁻ (Pin 15/Pin 13): Inverting Input to the Differential TEC Voltage Amplifier. This amplifier has a fixed gain of 1 with its output being the voltage across the TEC with respect to AGND. This input, along with TEC⁺, signifies whether the TEC is heating or cooling the laser as indicated by the H/C pin.

TEC⁺ (Pin 16/Pin 14): Noninverting Input to the Differential TEC Voltage Amplifier.

I_{TEC} (Pin 17/Pin 15): Output of the Differential Current Sense Amplifier. The voltage on this pin is equal to 10 • (I_{TEC} + I_{RIPPLE}) • R_S, where I_{TEC} is the thermoelectric cooler current, I_{RIPPLE} is the inductor ripple current and R_S is the sense resistor used to sense this current. This voltage represents only the magnitude of the current and provides no direction information. Current limit occurs when the voltage on this pin exceeds the lesser of 1.5 times the voltage on SS, 1.5 times the voltage on I_{LIM} or 1.5V. When this condition is present, the pair of outputs, which are presently conducting, are immediately turned off. The current limit condition is cleared when the C_T pin reaches the next corresponding peak or valley (see Current Limit section).

CS⁻ (Pin 18/Pin 16): Inverting Input to the Differential Current Sense Amplifier.

CS⁺ (Pin 19/Pin 17): Noninverting Input of the Differential Current Sense Amplifier. The amplifier has a fixed gain of 10.

PDRVA, PDRVB (Pins 20, 25/Pins 18, 24): These push-pull outputs are configured to drive the opposite high side PMOS switches in a full-bridge arrangement.

NDRVA, NDRVB (Pins 21, 24/Pins 19, 23): These push-pull outputs are configured to drive the opposite low side switches in a full-bridge arrangement.

PGND (Pin 22/Pin 20): This is the high current ground for the IC. The external current sense resistor should be referenced to this point.

V_{DD} (Pin 23/Pins 21, 22): Positive Supply Rail for the IC. Bypass this pin to PGND and AGND with >10µF low ESL, ESR ceramic capacitors. The turn on voltage level for V_{DD} is 2.6V with 130mV of hysteresis.

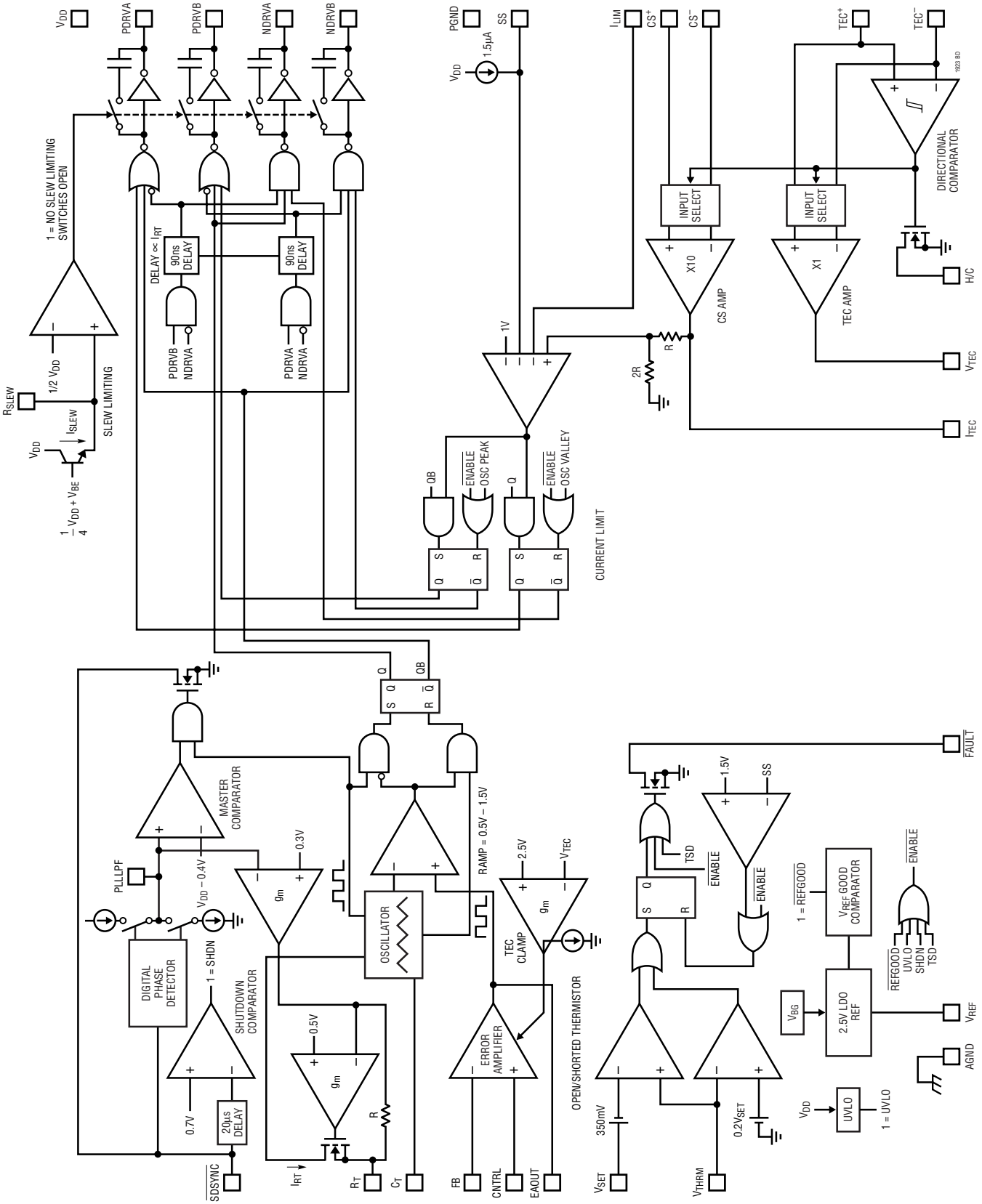
V_{REF} (Pin 26/Pin 27): This is the output of the Reference. This pin should be bypassed to GND with a 1µF ceramic capacitor. The reference is able to supply a minimum of 10mA of current and is internally short-circuit current limited.

C_T (Pin 27/Pin 28): The triangular wave oscillator timing capacitor pin is used in conjunction with R_T to set the oscillator frequency. The equation for calculating frequency is:

$$f_{OSC} = \frac{0.75}{R_T \bullet C_T} Hz$$

R_T (Pin 28/Pin 29): A single resistor from R_T to AGND sets the charging and discharging currents for the triangle oscillator. This pin also sets the dead time between turning one set of outputs off and turning the other set on to ensure the outputs do not cross conduct. The voltage on this pin is regulated to 0.5V. For best performance, the current sourced from the R_T pin should be limited to a maximum 150µA. Selecting R_T to be 10k is recommended and provides 90ns of dead time.

FUNCTIONAL DIAGRAM



OPERATION

MAIN CONTROL LOOP

The LTC1923 uses a constant frequency, voltage mode architecture to control temperature. The relative duty cycles of two pairs of N-/P-channel external MOSFETs, set up in a full-bridge (also referred to as an H-bridge) configuration are adjusted to control the system temperature. The full-bridge architecture facilitates bidirectional current flow through a thermoelectric cooler (TEC) or other heating element. The direction of the current flow determines whether the system is being heated or cooled. Typically a thermistor, platinum RTD or other appropriate element is used to sense the system temperature. The control loop is closed around this sense element and TEC.

The voltage on the output of the error amplifier, EAOUT, relative to the triangle wave on C_T, controls whether the TEC will be heating or cooling. A schematic of the external full bridge is shown in Figure 1. The "A" side of the bridge is comprised of the top left PMOS, MPA, and lower right NMOS, MNA. The gates of these devices are attached to the PDRVA and NDRVA outputs of the LTC1923, respectively. The "B" side of the bridge is comprised of PMOS, MPB and NMOS, MNB. The gates of these MOSFETs are controlled by the PDRVB and NDRVB outputs of the LTC1923.

The "A" side of the bridge is turned on (NDRVA is high and PDRVA is low) when the output of the error amplifier is less than the voltage on the C_T pin as shown in Figure 2.

For this condition, the state of each output driver is as follows: PDRVA is low, NDRVA is high, PDRVB is high and NDRVB is low. When the voltage on EAOUT is greater than the voltage on the C_T pin, the "B" side of the bridge is turned on. The average voltage across the TEC, $V_{TECOOLER}$, is approximately:

$$V_{TECOOLER} = V_{TEC}^{+} - V_{TEC}^{-} = V_{DD} \bullet (D_A - D_B)$$

where

V_{DD} = the full-bridge supply voltage

$V_{TECOOLER} = V_{TEC}^{+} - V_{TEC}^{-}$

D_A = the duty cycle of the "A" side of the bridge or the amount of time the "A" side is on divided by the oscillator period

D_B = the duty cycle of the "B" side of the bridge

Duty cycle terms D_A and D_B are related by the following equation:

$$D_A = 1 - D_B$$

In steady-state, the polarity of $V_{TECOOLER}$ indicates whether the system is being heated or cooled. Typically, when current flows into the TEC$^+$ side of the cooler, the system is being cooled and heated when current flows out of this terminal. *Note: Do not confuse the TEC$^+$ side of the TEC with the TEC$^+$ input of the LTC1923, although these two points should be connected together.*

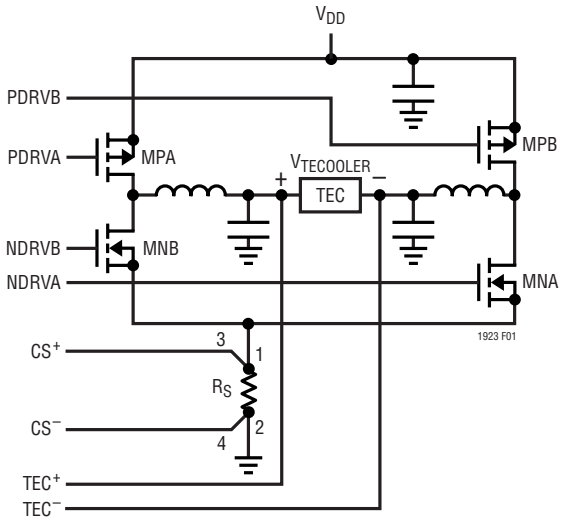


Figure 1. Full-Bridge Schematic

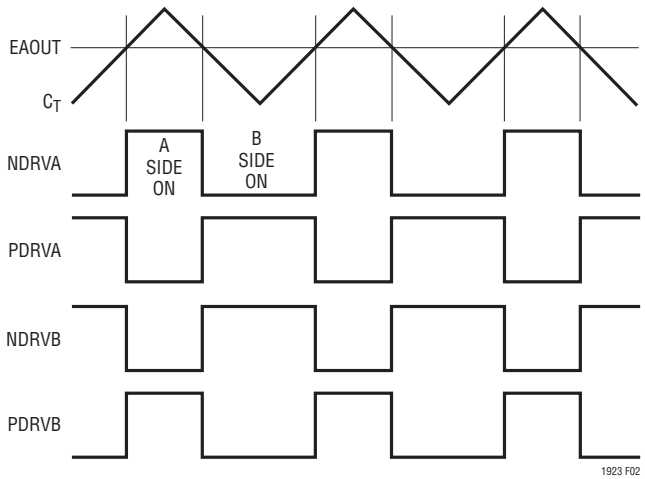


Figure 2. Error Amplifier Output, C_T and Output Driver Waveforms

OPERATION

PROTECTION FEATURES

Many protection features have been integrated into the LTC1923 to ensure that the TEC is not overstressed or the system does not thermally run away. These features include pulse-by-pulse current limiting, TEC voltage clamping and open/shorted thermistor detection.

Current Limit

The peak current in the full bridge during each switching cycle can be limited by placing a sense resistor, R_S, from the common NMOS source connections of MNA and MNB to ground. The CS^+ and CS^- connections should be made as shown in Figure 1. Current limit is comprised of a fixed gain of ten differential amplifier, an attenuator (resistor divider) and a current limit comparator. A detailed diagram of the circuitry is shown in Figure 3. The differential amplifier output, I_{TEC}, is provided to allow the user the ability to monitor the instantaneous current flowing in the bridge. If an average current is desired, an external RC filter can be used to filter the I_{TEC} output. Approximately 50ns of leading edge blanking is also internally integrated to prevent nuisance tripping of the current sense circuitry. It relieves the filtering requirements for the CS input pins.

During a switching cycle, current limit occurs when the voltage on I_{TEC} exceeds the lowest of the following three conditions: 1) 1.5 times the voltage on the SS pin, 2) 1.5 times the voltage on the I_{LIM} pin or 3) 1.5V. When a current limit condition is sensed, all four external FETs are immediately shut off. These devices are turned back on only after C_T reaches the same state (either charging or discharging) as when the current limit condition occurred. For instance, if C_T is charging when current limit occurs, the outputs are forced off for the remainder of this charging time, the entire C_T discharge time, and are only re-enabled when C_T reaches its valley voltage and begins charging again. An analogous sequence of events occurs if current limit is tripped while C_T is being discharged.

The full-bridge current can be soft-started (gradually increased) by placing a capacitor from the SS pin to ground. A 1.5µA current is sourced from the chip and will charge the capacitor. This limits the inrush current at start-up and allows the current delivered to the TEC to be linearly increased from zero.

The LTC1923 features a dedicated pin, I_{LIM}, to adjust current limit. If the voltage placed on I_{LIM} is greater than 1V, the default current limit, I_{LIMIT}, is:

$$I_{LIMIT} = 150mV/R_S$$

where R_S = the current sense resistor.

Utilizing the I_{LIM} pin allows the current limit threshold to be easily set and adjusted (the current limit threshold can also be adjusted by changing R_S). More importantly, it facilitates independent setting of the heating and cooling current limits with the addition of one transistor. Figure 4 shows how to implement this using three resistors and an external NMOS, M1. In many applications, a higher cooling capability is desired. When TEC^+ is greater than TEC^-, the H/C output is in a low state signifying that the system is being cooled (this is typical for most lasers).

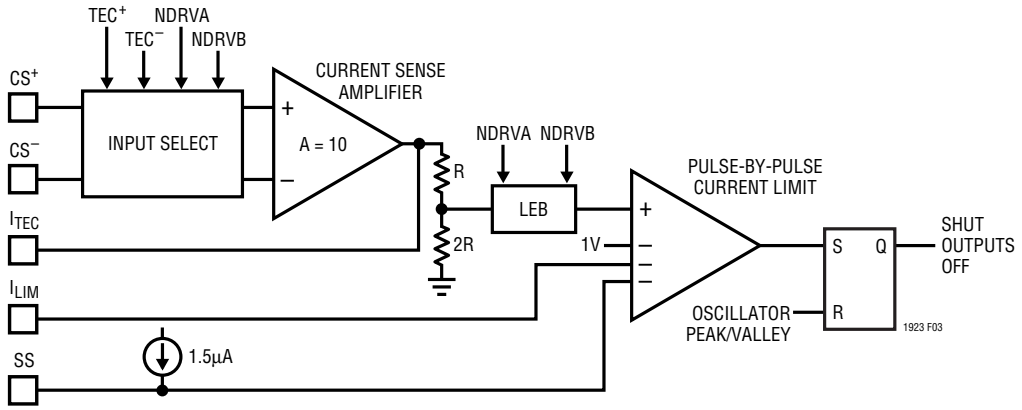


Figure 3. Current Sense Circuitry

OPERATION

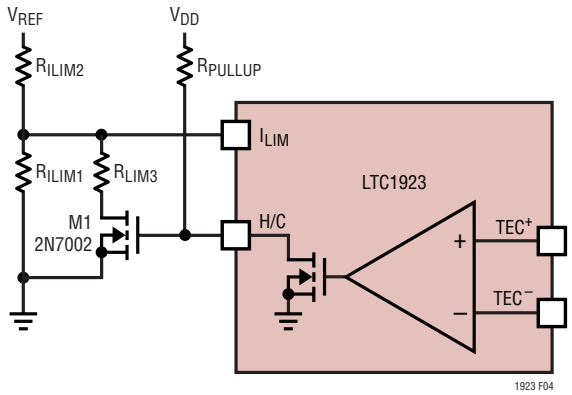


Figure 4. Independently Heating/Cooling Current Limit

Transistor M1 is off and the current limit threshold is given by:

$$I_{LIMIT} = \frac{0.15 \bullet R_{ILIM1} \bullet V_{REF}}{(R_{ILIM1} + R_{ILIM2}) \bullet R_S}$$

When TEC^- is greater than TEC^+, the open-drain output, H/C, pulls high through R_{PULLUP}, causing M1 to turn on.

The current limit value is given by:

$$I_{LIMIT} = \frac{0.15 \bullet (R_{ILIM1} \| R_{ILIM3}) \bullet V_{REF}}{(R_{ILIM2} + R_{ILIM1} \| R_{ILIM3}) \bullet R_S}$$

reducing the current limit threshold for heating. If the heating current limit needs to be greater than the cooling limit, an extra inversion can be added.

Open/Shorted Thermistor Detection

The temperature sense element (NTC thermistor, platinum RTD or other appropriate component) must be properly connected in order for the system to regulate temperature. If the sense element is incorrectly connected, the system will be unable to control the temperature and the potential exists for the system to thermally run away.

A TEC by nature produces a temperature differential between opposite sides of the device depending upon how much current is flowing through it. There is a maximum limit to the amount of temperature differential that can be produced, which depends upon a number of physical parameters including the size of the TEC and how well heatsinked the device is. The TEC itself dissipates power to produce the temperature differential, generating heat, which must also be removed. At a certain level of power dissipation in the TEC, both sides will begin to heat. This is because the TEC will not be able to pump the self-generated heat to the outside world, which can lead to thermal runaway. If the device thermally runs away, damage to the TEC and possibly the components whose temperature is being regulated will occur.

The LTC1923 contains two dedicated comparators that directly monitor the voltage on the thermistor. If this voltage is outside the valid window, a latch is set and the $\overline{FAULT}$ pin is asserted low. The output drivers are **not** shut off and the control circuitry is not disabled, meaning the part **will continue** to try to regulate temperature. It is up to the user to use the $\overline{FAULT}$ signal to disable the appropriate circuitry. There are a couple of ways to do this. The first way is to have the $\overline{FAULT}$ signal a system microprocessor to shut the system down through the $\overline{SDSYNC}$ pin. Figure 5 shows another means of protecting the system. External NMOS M1 and PMOS M2 have been added along with two pull-up resistors (RP1 and RP2). M1 and RP2 invert the $\overline{FAULT}$ signal while M2 acts as a switch in series with bridge. When no fault is present, the gate of M1 is

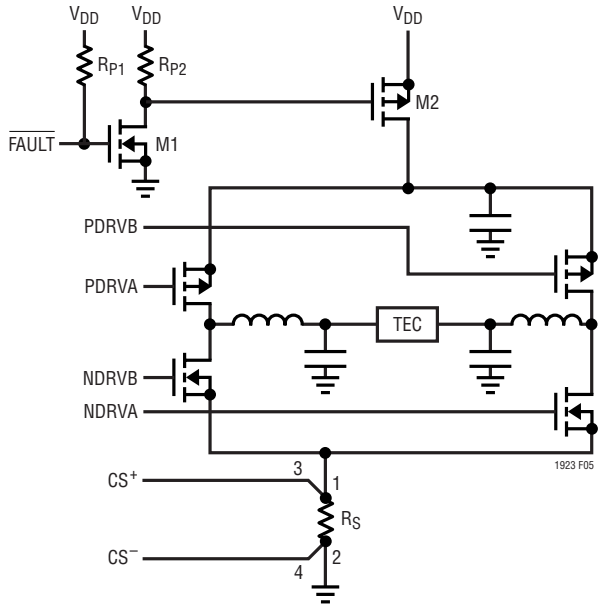


Figure 5. Redundant Fault Protection

OPERATION

pulled to V_{DD} forcing the gate of M2 low, which allows the bridge to operate as described earlier. When a fault occurs and FAULT is asserted low, M1 is shut off, forcing the gate of M2 high, shutting that device off. The power path is thus opened, ensuring no current is delivered to the TEC. M2 wants to have low $R_{DS(ON)}$ (less than the value of R_S to minimize the power losses associated with it). R_{P1} and R_{P2} can be selected on the order of 100k.

The lower comparator threshold level is 20% (twenty percent) of V_{SET} and the upper comparator threshold level is 350mV below V_{SET}, where V_{SET} is the voltage applied on the V_{SET} pin. V_{SET} is typically tied to the bias source for the thermistor divider so that any variations will track out.

The V_{SET} pin has a high input impedance so that a divided-down voltage can be supplied to this pin to modify the acceptable thermistor impedance range. This is shown in Figure 6. The voltage applied to the V_{SET} pin must be a minimum of 2V. The lower thermistor impedance threshold is:

$$R_{TH(LOWER)} = \frac{0.2 \bullet R1 \bullet R3}{R2 + 0.8 \bullet R3}$$

The upper impedance threshold is:

$$R_{TH(UPPER)} = \frac{R1\left(R3 - \alpha(R2 + R3)\right)}{R2 + \alpha(R2 + R3)}$$

where $\alpha = 0.35/V_{SET}$.

Changing R1 also changes the valid thermistor impedance range.

Example: $V_{REF} = V_{SET} = 2.5V$

R1 = 10k, R2 = 0Ω, R3 = open

R_{TH} = 10k NTC thermistor with a temperature coefficient of –4.4%/C at 25°C.

The acceptable thermistor impedance range before causing a fault is 2.5kΩ to 61kΩ. This corresponds to a valid temperature range of between about –10°C and 60°C.

To ensure the part does not power up with a latched fault at start-up, a fault will not be latched until soft-start has completed. This corresponds to the voltage on SS reaching 1.5V. For a 1µF soft-start capacitor, this delay is approximately 1 second. This provides enough time for all supplies (V_{DD}, setpoint reference and V_{REF}) to settle at their final values.

TEC Voltage Clamping

An internal clamp circuit is included to protect the TEC from an overvoltage condition. When the differential voltage across the TEC exceeds 2.5V, the error amplifier output voltage at the input of the PWM comparator is limited. This clamps the duty cycle of the output drivers, and therefore, the voltage across the TEC. The voltage where clamping occurs can be increased by placing a resistor divider in parallel with the TEC and by making the appropriate connections to TEC^+ and TEC^- as shown in Figure 7. The divider increases the voltage across the TEC, $V_{TECOOLER}$, where the clamp activates, to:

$$V_{TECOOLER} = \frac{\left(1 + \frac{R_{TE1}}{R_{TE2}} + \frac{R_{TE1}}{100k}\right) \bullet 2.5 - V_{CM}\left(\frac{R_{TE1}}{200k}\right)}{1 + \frac{R_{TE1}}{200k}}$$

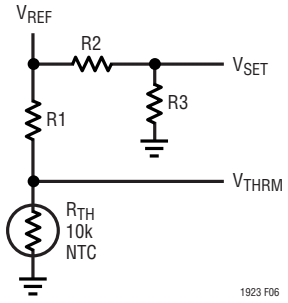


Figure 6. Modifying the Acceptable Thermistor Range

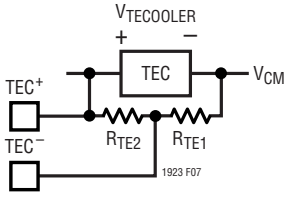


Figure 7. Increasing Voltage Clamp Threshold

OPERATION

The terms containing the fixed resistance values are the loading errors introduced by the input impedance of the differential amplifier. A common mode voltage error is also introduced since the addition of R_{TE1} and R_{TE2} change the fully differential nature of the amplifier. In order to minimize these errors select R_{TE1} and R_{TE2} to be 10k or less. The above equation reduces to:

$$V_{TECOOLER} \cong \left(1+\frac{R_{TE1}}{R_{TE2}}\right)2.5$$

The Higher Voltage Applications section shows a fully differential means to increase the clamp voltage.

This will similarly alter the heating and cooling direction thresholds by the same factor, increasing the thresholds to (R_{TE1} and R_{TE2} are assumed to be ≤10k):

$$DIRH = 50mV\left(1+\frac{R_{TE1}}{R_{TE2}}\right)$$

$$DIRL = -50mV\left(1+\frac{R_{TE1}}{R_{TE2}}\right)$$

The output voltage on the VTEC pin, V_{VTEC}, will be reduced by the same ratio:

$$V_{VTEC} = \frac{V_{TECOOLER}}{1+\frac{R_{TE1}}{R_{TE2}}}$$

Oscillator Frequency

The oscillator determines the switching frequency and the fundamental positioning of all harmonics. The switching frequency also affects the size of the inductor that needs to be selected for a given inductor ripple current (as opposed to TEC ripple current which is a function of both the filter inductor and capacitor). A higher switching frequency allows a smaller valued inductor for a given ripple current. The oscillator is a triangle wave design. A current defined by external resistor R_T is used to charge and discharge the capacitor C_T. The charge and discharge rates are equal. The selection of high quality external components (5% or better multilayer NPO or X7R ceramic capacitor) is important to ensure oscillator frequency stability.

The frequency of oscillation is determined by:

$$f_{OSC(kHz)} = 750 \bullet 10^6/[R_T(k\Omega) \bullet C_T(pF)]$$

The LTC1923 can run at frequencies up to 1MHz. The value selected for R_T will also affect the delay time between one side of the full bridge turning off and the opposite side turning on. This time is also known as the "break-before-make" time. The typical value of 10kΩ will produce a 90ns "break-before-make" time. For higher frequency applications, a smaller value of R_T may be required to reduce this delay time. For applications where significant slew rate limiting or external gate driver chips are used, a higher value for R_T may necessary, increasing the dead time. The "break-before-make" time can be approximately calculated by:

$$t_{DELAY} = R_T\,(k\Omega) \bullet 5.75 \bullet 10^{-9} + 35ns$$

Phase-Locked Loop

The LTC1923 has an internal voltage-controlled oscillator (VCO) and phase detector comprising a phase-locked loop. This allows the oscillator to be synchronized with another oscillator by slaving it to a master through the $\overline{SDSYNC}$ pin. The part can also be designated as the master by pulling the PLLLPF pin high to V_{DD}. This will result in the part toggling the $\overline{SDSYNC}$ pin at its set oscillator frequency. This signal can then be used to synchronize additional oscillators.

When being slaved to another oscillator, the frequency should be set 20% to 30% lower than the target frequency. The frequency lock range is approximately ±50%.

The phase detector is an edge sensitive digital type, which provides zero degrees phase shift between the external and internal oscillators. This detector will not lock up on input frequencies close to the harmonics of the VCO center frequency. The VCO hold-in range is equal to the capture range dfH = dfC = $\pm 0.5f_O$.

The output of the phase detector is a complementary pair of current sources charging or discharging the external filter network on the PLLLPF pin. A simplified block diagram is shown in Figure 8.

OPERATION

If the external frequency (f_{PLLIN}) is greater than the oscillator frequency, current is sourced continuously out of the PLLLPF pin. When the external frequency is less than the oscillator frequency, current is sunk by the PLLLPF pin. The loop filter components R_{LP}, C_{LP} and C_{LP2}, smooth out current pulses from the phase detector and provide a stable input to the VCO. These components also determine how fast the loop acquires lock. In most instances C_{LP2} can be omitted, R_{LP} can be set to 1k and C_{LP} can be selected to be 0.01µF to 0.1µF to stabilize the loop. Make sure that the low side of filter components is tied to AGND to keep unwanted switching noise from altering the performance of the PLL.

Figure 9 illustrates three different ways to set the oscillator frequency. In Figure 9a, the oscillator is free running with the frequency determined by R_T and C_T. In Figure 9b, the oscillator is slaved to an external clock. Figure 9c illustrates how one LTC1923 can be used as a master to synchronize other LTC1923s or additional devices requiring synchronization. To implement this, determine the values of R_T and C_T to obtain the desired free-running oscillator frequency of the master by using the equation given in the oscillator frequency section. Tie the master's PLLLPF pin to V_{DD} and the $\overline{SDSYNC}$ pin to V_{DD} through a resistor R_{PLL} as shown in Figure 9c. R_{PLL} typically can be set to 10k, but may need to be a lower value if higher frequency operation is desired (above 250kHz). Set the slave free-running frequencies to be 20% to 30% less than this. The $\overline{SDSYNC}$ pin of the master will switch at its free-running frequency (with approximately 50% duty cycle), and this can be used to synchronize the other devices.

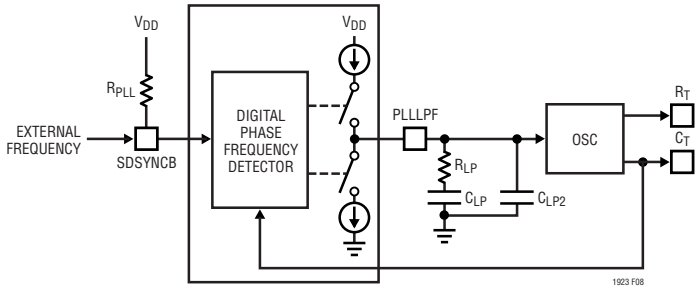
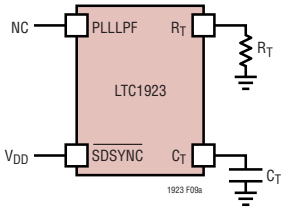
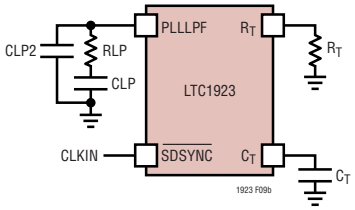


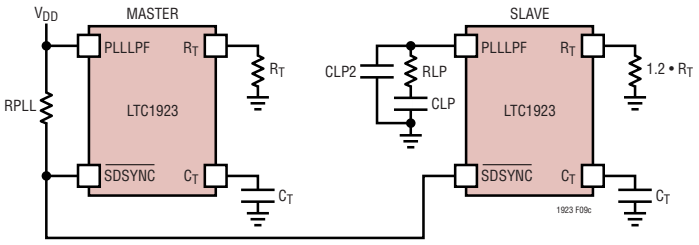
Figure 8. Phase-Locked Loop Block Diagram



(9a) Free Running



(9b) Slave Operation with External Clock—Set Oscillator Frequency at 70% to 80% of External Clock



(9c) Master/Slave Operation—Set Oscillator Frequency of Slave at 70% to 80% of Master

Figure 9. Oscillator Frequency Setup: a) Free Running b) Slaved Operation c) Master/Slave Operation

APPLICATIONS INFORMATION

The thermistor may be isolated from the control circuitry. It has a relatively high input impedance and is therefore susceptible to noise pick up. Extreme care should be taken to ensure this signal is noise free by shielding the line (coaxially). A lowpass filter can be added between the thermistor and the input to the LTC2053, but since it is in the signal path, there are limitations on how much filtering can be added.

Inductor Ripple Current

The current that flows in the bridge can be separated into two components, the DC current that flows through the TEC and the inductor ripple current that is present due to the switchmode nature of the controller. Although the TEC current has its own ripple component, proper filtering will minimize this ripple relative to the inductor ripple current, validating this assumption that the TEC current is constant (see TEC Ripple Current section). A simplified half-circuit of the bridge in steady-state is shown in Figure 10. The current, I_L, through the inductor (L) consists of the ripple current (ΔI_1) and static TEC current (I_{TEC}). The ripple current magnitude, ΔI_1, can be calculated using the following equation:

$$\Delta I_1 = (V_{BRIDGE}^2 - V_{TEC}^2)/(4 \bullet f_{OSC} \bullet L \bullet V_{BRIDGE})$$

where

V_{BRIDGE} is the full-bridge supply voltage (typically V_{DD})

f_{OSC} is the oscillator frequency

L is the filter inductor value

V_{TEC} is the DC voltage drop across the TEC

The peak inductor current is equal to $I_{TEC} + \Delta I_1/2$ and is the current level that trips the current limit comparator. Keeping the ripple current component small relative to I_{TEC} keeps the current limit trip level equal to the current flowing through the TEC.

Example: V_{BRIDGE} = 5V, R_{TEC} = 2.5Ω, V_{TEC} = 2.5V, I_{TEC} = 1A, L = 22µH, f_{OSC} = 250kHz. The peak-to-peak ripple current using the above equation is:

ΔI_1 = 170mA

The peak inductor current is therefore 1.085A in order to get 1A of DC TEC current.

TEC Ripple Current

Every TEC has a fundamental limitation (based mainly on the TEC's physical characteristics) on the maximum temperature differential that it can create between sides. The ability to create this maximum temperature differential is affected by the amount of ripple current that flows through the device, relative to the DC component. An approximation of this degradation due to TEC ripple current is given by the following equation:

$$dT/dT_{MAX} = 1/(1 + N^2)$$

where:

dT is the adjusted achievable temperature differential

dT_{MAX} is the maximum possible temperature differential when the TEC is fed strictly by DC current and is typically specified by the manufacturer

N is the ratio of TEC ripple current to DC current

TEC manufacturers typically state that N should be no greater than 10%.

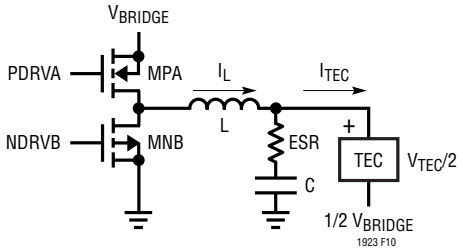


Figure 10. Full-Bridge Half Circuit

APPLICATIONS INFORMATION

In this application, the bridge supply voltage, oscillator frequency and external filter components determine the amount of ripple current that flows through the TEC. Higher valued filter components reduce the amount of ripple current through the TEC at the expense of increased board area. Filter capacitor ESR along with inductor ripple current will determine the peak-to-peak voltage ripple across the TEC and therefore the ripple current since the TEC appears resistive.

The ripple current through the TEC, $I_{TEC(RIPPLE)}$, is approximately equal to:

$$I_{TEC(RIPPLE)} \cong \frac{V_{BRIDGE}^2 - V_{TEC}^2}{16 \bullet f_{OSC}^2 \bullet L \bullet C \bullet R_{TEC} \bullet V_{BRIDGE}} + \frac{\left(V_{BRIDGE}^2 - V_{TEC}^2\right) \bullet ESR}{2 \bullet f_{OSC} \bullet L \bullet V_{BRIDGE} \bullet R_{TEC}}$$

where:

f_{OSC} = the oscillator frequency

L = the filter inductor value

C = the filter capacitor value

R_{TEC} = the resistance of the TEC

V_{TEC} = the DC voltage drop across the TEC

ESR = the equivalent series resistance of the filter capacitor

V_{BRIDGE} = the full-bridge supply voltage typically equal to V_{DD}

The equation above shows that there are two components, which comprise TEC ripple current. The first term is the increase in voltage from the charging of the filter capacitor. The second term is due to the filter capacitor ESR and is typically the dominant contributor. Therefore the filter capacitor selected wants to have a low ESR. This capacitor can be made of multilevel ceramic, OS-CON electrolytic or other suitable capacitor. Increasing the oscillator frequency will also reduce the TEC ripple current since both terms have an inverse relationship to operating frequency.

Example: V_{BRIDGE} = 5V, R_{TEC} = 2.5Ω, V_{TEC} = 2.5V, L = 22µH, C = 22µF, f_{OSC} = 250kHz, ESR = 100mΩ

$I_{TEC(RIPPLE)}$ = 3.1mA + 13.6mA = 16.7mA

For this example the DC current flowing through the TEC is 1A, making the ripple current equal to approximately 1.7% (this illustrates why I_{TEC} can be approximated to be DC).

Closing the Feedback Loop

Closing the feedback loop around the TEC and thermistor (or other temperature sensitive element) involves identifying where the thermal system's poles are located and placing electrical pole(s) (and zeroes) to stabilize the control loop. High DC loop gain is desirable to keep extremely tight control on the system temperature. Unfortunately the higher the desired loop gain, the larger the compensation values required to stabilize the system. Given the inherently slow time constants associated with thermal systems (on the order of many seconds), this can lead to unreasonably large component values. Therefore, the amount of loop gain necessary to maintain the desired temperature accuracy should be calculated, and after adding some margin, this should be the target DC loop gain for the system. A block diagram of the system is shown in Figure 11. The gain blocks are as follows:

K_{IA} = instrumentation amplifier gain (V/V)

K_{EA} = error amplifier gain (V/V)

K_{MOD} = modulator gain (d/V)

K_{PWR} = power stage gain (V/d)

K_{TEC} = TEC gain (°C/V)

K_{THRM} = Thermistor Gain (V/°C)

K_{IA} and K_{EA} are the electrical gains associated with the instrumentation and LTC1923 error amplifier. Switching regulators are sampled systems that convert voltage to duty cycle (d), which explains why the K_{MOD} and K_{PWR} gain terms are expressed as a function of duty cycle and voltage. The TEC converts voltage to temperature change, while the thermistor's impedance and therefore voltage across it changes with temperature.

The loop gain can be expressed by the following equation:

$$T \text{ (loop gain)} = K_{IA} \bullet K_{EA} \bullet K_{MOD} \bullet K_{PWR} \bullet K_{TEC} \bullet K_{THRM}$$

And the error introduced by the finite gain of the system, V_E, can be expressed by:

$$V_E = V_{IN}/(1 + T)$$

APPLICATIONS INFORMATION

This voltage error translates back into a temperature setpoint error.

Example:

R_{THRM} = 10k

NTC with 4.4%/°C at 25°C

R1 = 10k

V_{REF} = 2.5V

T = 25°C

For this thermistor with a 25°C temperature setpoint, the change in thermistor voltage with temperature is given by –25mV/°C. In order to maintain a 0.01°C temperature accuracy, this translates into a 250µV error signal, V_E. The minimum loop gain can now be calculated from the above equation:

$$V_E = V_{IN}/(1 + T)$$

A 25°C setpoint temperature requires V_{IN} = 1.25V for V_{REF} = 2.5V. The required loop gain is 5000 or 74dB.

There are two handles to adjust the loop gain, K_{IA} and K_{EA}, while the other handles are fixed and depend upon the TEC and thermistor characteristics (K_{TEC} and K_{THRM}), V_{SET} and R1 (K_{THRM}) and V_{DD} (K_{MOD} and K_{PWR}). The modulator and power gain product is given by:

$$K_{MOD} \bullet K_{PWR} = 2 \bullet V_{DD}/V_{CT} = 2 \bullet V_{DD}$$

where V_{CT} = the C_T voltage which has a fixed 1V amplitude.

The TEC gain depends upon the TEC selected and corresponds to the relationship between the voltage across the device and what temperature differential is created. This gain term changes with operating temperature, and whether the TEC is heating or cooling. TECs are inherently more efficient at heating (and therefore have a higher gain) as compared to cooling. A worst-case rough estimation of the gain can be obtained by taking the maximum TEC voltage required to force a given change in temperature from the TEC specifications:

$$K_{TEC} = dT/V_{TEC(MAX)}$$

The thermistor gain should be linearized around temperature setpoint.

Example:

Setpoint T = 25°C

V_{DD} = 5V

R_{THRM} = 10k NTC with 4.4%/°C at 25°C

R1 = 10k

V_{REF} = 2.5V

$dT/V_{TEC(MAX)}$ = 45°C/1.5V = 30°C/V

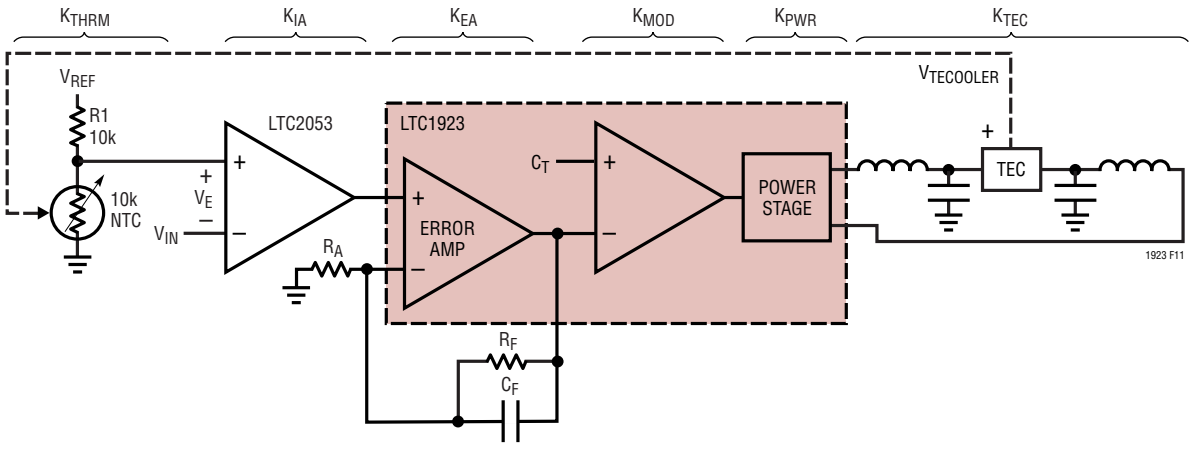


Figure 11. Simplified Loop Block Diagram

APPLICATIONS INFORMATION

The linearized thermistor gain around 25°C is –25mV/°C. For a minimum loop gain of 5000 as calculated above, the combined gain of the instrumentation and error amplifiers can be calculated:

$$K_{IA} \bullet K_{EA} = T/(K_{MOD} \bullet K_{PWR} \bullet K_{TEC} \bullet K_{THRM})$$

$$K_{IA} \bullet K_{EA} = 5000/(10 \bullet 30 \bullet 0.025) = 667$$

A combined gain of 1000 can be selected to provide adequate margin. The instrumentation amplifier gain should be set at typically 10, as this attenuates any errors by its gain factor. The error amplifier gain would then be limited to the remainder through the gain setting resistors, R_F and R_A shown in Figure 11.

$$R_F/R_A = KEA - 1$$

The multiple poles associated with the TEC/thermistor system makes it difficult to compensate. Compounding this problem is that there will be significant variations in thermal time constants for the same system, making elaborate compensation schemes difficult to reliably implement. The most robust method (i.e., least prone to oscillation) is to place a dominant pole well below the thermal system time constant (τ) (anywhere from many seconds to minutes). This time constant will set the capacitor value by the following equation:

$$C_F = \tau/R_F$$

Please refer to Application Note 89 for more detailed information on compensating the loop. Ceramic capacitors are not recommended for use as the integrating capacitor or anywhere in the signal path as they exhibit a piezoelectric effect which can introduce noise into the system. The component values shown on the front page of this data sheet provide a good starting point, but some adjustment may be required to optimize the response.

Dominant pole compensation does have its limitations. It provides good loop response over a wide range of laser module types. It does not provide the fastest transient response to step changes in temperature. If this is a necessity, a more complex compensation approach as shown in Figure 12 may be required. This approach adds an additional zero into the feedback loop to speed up the transient response. First note that the LTC2053 inputs have been swapped as the LTC1923 error amplifier is now running in an inverting configuration. Capacitor C_A is needed to provide the lead term. Resistor R_C is used to buffer the LTC2053 from capacitive loading and limit the error amplifier high frequency gain.

Since the system thermal pole locations are not known, a qualitative compensation approach must be employed. This entails looking at the transient response when the TEC is heating (due to the inherent higher gain) for a small-signal step change in temperature and modifying compensation components to improve the response. A reasonable starting point is to select components that mimic the response that will be obtained from the front page of this data sheet. Therefore R_A, R_B and C_B would be selected to be 1MΩ, 1MΩ and 0.47µF, respectively. R_C should be selected to be a factor of 100 smaller than R_A, or on the order of 10k. Make sure that the loop is stable prior to the introduction of capacitor C_A. The addition of C_A will provide some phase boost in the loop (in effect, offsetting one of the poles associated with the thermal system). Start

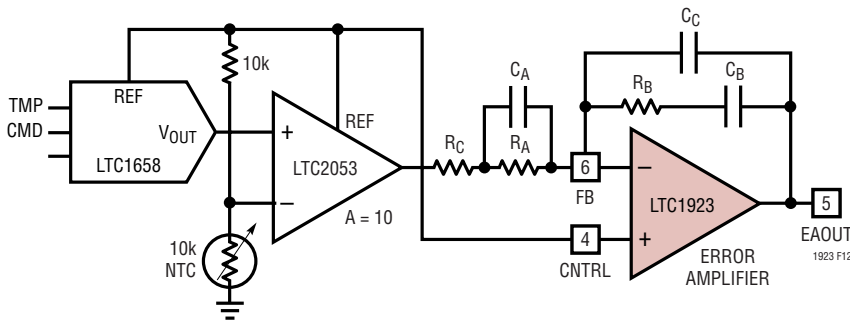


Figure 12. Alternative Compensation Method to Improve Transient Response

APPLICATIONS INFORMATION

with C_A on the order of C_B and note its affect on system response. Adjust the values based on observing whether the transient response was improved or not with the goal of reducing C_B to improve settling time. As the system thermal poles can vary between "identical" laser modules (i.e., same manufacturer and model), care must be taken to ensure that the values selected provide the desired response even with these thermal term variations. Compensation should also be tailored for each unique laser module as thermal terms can vary significantly between different brands. C_C rolls off high frequency gain , minimizing noise in the outputs. It is typically about 25 times smaller than C_B. C_A, C_B and C_C should be film capacitors.

Temperature Stability

It is important to differentiate between temperature accuracy and stability. Since each laser's output maximizes at some temperature, temperature setpoint is typically incremented until this peak is achieved. After this, only temperature stability is required. The predominant parameters which affect temperature stability are the thermistor, the thermistor biasing resistor and any offset drift of the front-end electrical circuitry. Sufficient loop gain ensures that any downstream variations do not contribute significantly to temperature stability. The relatively mild operating conditions inside the laser module promote good long-term thermistor stability. A high quality, low temperature coefficient resistor should be selected to bias the thermistor. If the 10k resistor has a 100ppm/°C temperature coefficient, this translates into a 0.18°C setpoint temperature differential over a 0°C to 70°C ambient for a desired 25°C laser setpoint. Depending upon the temperature stability requirements of the system, this is very significant. A lower temperature coefficient resistor may therefore be desired. The LTC2053 has maximum offset drift to 50nV/°C which translates into less than 0.001°C change for a 0°C to 70°C ambient.

The offset drift of the LTC1923 error amplifier divided by the gain of the LTC2053 also affects temperature stability. The offset drift of the LTC1923 (see characteristic curves) is typically 1mV over a 0°C to 70°C ambient. After attenuation by the LTC2053 gain, this translates into a temperature setpoint variation of 0.004°C. Neither of these offsets drifts significantly with aging. Depending upon the setpoint temperature stability requirements of the system, the LTC2053 instrumentation amplifier may not be necessary. Figure 13 shows a simplified schematic with the LTC2053 omitted.

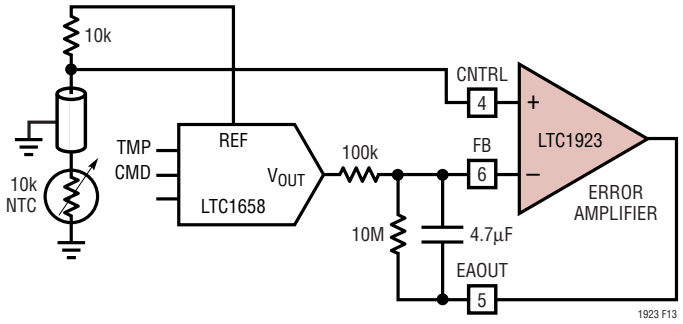


Figure 13. Simplifed Temperature Control Loop Omitting the LTC2053 Instrumentation Amplifier Front End

APPLICATIONS INFORMATION

Noise and Slew Rate Control

One disadvantage of switching regulators is that the switching creates wideband harmonic energy. The high frequency content can pose problems to associated circuitry. To combat this issue, the LTC1923 offers a pin called R_{SLEW} that controls the slew rate of the output drive waveforms. Slowing down the transition interval reduces the harmonic frequency content by spreading out the energy over a longer time period. The additional transition time causes some efficiency loss (on the order of 2% to 3%) but significantly improves the high frequency noise reflected onto the input supply.

Slew rate control is engaged by placing a resistor from R_{SLEW} to AGND. If slew rate control is not desired, the R_{SLEW} pin should be tied to V_{DD} allowing the output drivers to transition at their fastest rate. The resistor value should be set between 10k (fastest transition) and 300k (slowest transition). This provides about a 10:1 slew rate range to optimize noise performance. The "break-before-make" time may need to be increased if slew control is implemented, especially for slower transition rates. Adjustment can be done by increasing the value of R_T (C_T can be reduced to maintain the same frequency of operation), to ensure that the bridge MOSFETs receive nonoverlapping drive.

Power MOSFET Selection

Four external MOSFETs must be selected for use with the LTC1923; a pair of N-channel MOSFETs for the bottom of the bridge and a pair of P-channel MOSFETs for the top diagonals of the bridge. The MOSFETs should be selected for their $R_{DS(ON)}$, gate charge and maximum V_{DS}, V_{GS} ratings. A maximum V_{DS} rating of 20V is more than sufficient for 5V and 12V bridge applications, but as mentioned in the High Voltage Application section, a 12V maximum V_{GS} rating is insufficient and higher voltage MOSFETs must be selected. There is a trade-off between $R_{DS(ON)}$ and gate charge. The $R_{DS(ON)}$ affects the conduction losses ($I_{TEC}^2 \bullet R_{DS(ON)}$), while gate charge is a dominant contributor to switching losses. A higher $R_{DS(ON)}$ MOSFET typically has a smaller gate capacitance and thus requires less current to charge the gate for the same BV_{DSS}. For 1A TEC applications, the Si9801DY or Si9928DY complimentary N- and P-channel MOSFETs provide a good trade-off between switching and conduction losses. Above this TEC current level the MOSFETs selected should have lower $R_{DS(ON)}$ to maintain the high end efficiency.

Efficiency Considerations

Unlike typical voltage regulators, where the output voltage is fixed, independent of load current, the output voltage of this regulator changes with load current. This is because the TEC appears resistive and the current through the TEC sets the voltage. The output power of the regulator is defined as:

$$P_{OUT} = I_{TEC}^2 \bullet R_{TEC}$$

The efficiency of a switching regulator is equal to the output power divided by the input power times 100%. Often it is useful to analyze individual losses to determine what is limiting the efficiency and which change would produce the most significant improvement. Efficiency can be expressed as:

$$\text{Efficiency} = 100\% - (L1 + L2 + L3 + \ldots)$$

where L1, L2, etc. are the individual losses as a percentage of input power.

For this application, the main efficiency concern is typically at the high end of output power. A higher power loss translates into a greater system temperature rise, resulting in the need for heat sinking, increasing both the system size and cost.

There are three main sources which usually account for most of the losses in the application shown on the front page of the data sheet: Input supply current, MOSFET switching losses and I^2R losses.

1) The input supply current is comprised of the quiescent current draw from the LTC1658, LTC2053, LTC1923 and any additional circuitry added. The total maximum supply current for these devices is on the order of 5mA, which gives a total power dissipation of 25mW. This power loss is independent of TEC current.

2) The MOSFET driver current results from switching the gate capacitance of the power MOSFETs. Each time a gate is switched from low to high to low again, a packet of charge dQ moves from V_{DD} to ground. The gate charging current, $I_{GATECHG} = 2 \bullet f \bullet (Q_P + Q_N)$, where Q_P and Q_N are

APPLICATIONS INFORMATION

the total gate charges of the NMOS and PMOS on one side of the bridge, and f is the oscillator frequency. The factor of 2 arises from there being two sets of MOSFETs that make up the full bridge. Note that increasing the switching frequency will increase the dynamic current and therefore power dissipation by the same factor. This power loss is independent of TEC current.

Example: Q_N = 10nC max, Q_P = 15nC max, f = 225kHz, V_{DD} = 5V

Power loss = $2 \bullet f \bullet (Q_P + Q_N) \bullet V_{DD}$ = 56mW

3) The DC resistances of the external bridge MOSFETs, filter inductors and sense resistor are typically the dominant loss mechanism at the high end TEC current. The conduction path of the current includes one NMOS, one PMOS, two inductors and the sense resistor so the DC resistances associated with the components dissipate power.

Example:

$R_{DS(ON)NMOS}$ at 5V = 0.055Ω max

$R_{DS(ON)PMOS}$ at 5V = 0.08Ω max

R_S = 0.1Ω

R_L = 0.1Ω,

I_{TEC} = 1A

R_{TEC} = 2.5Ω

Total series resistance = 0.055 + 0.08 + 2 • 0.1 + 0.1 = 0.435Ω

Power Loss = $(1A)^2 \bullet 0.435\Omega$ = 0.435W

Output Power = $(1A)^2 \bullet 2.5\Omega$ = 2.5W

This represents a 17% efficiency loss due to conduction losses. The other two power loss mechanisms comprise a little more than a 3% efficiency loss at this output power level. This may sound alarming if electrical efficiency is the primary concern and can be easily improved by choosing lower $R_{DS(ON)}$ MOSFETs, lower series resistance inductors and a smaller valued sense resistor. If temperature rise is the primary concern, this power dissipation may be acceptable. At higher current levels, this example does illustrate that lower resistance components should be selected.

Low Voltage Requirements

All components shown on the front page of this data sheet will operate with a 2.7V input supply. Minor modifications are required to guarantee correct operation. The voltage on the REF input of the LTC2053 should be at least 1V below V_{DD}. Figure 14 shows how to implement this. By dividing down the 2.5V reference with 500Ω of impedance, feeding this to the REF input of the LTC2053 and the integrating resistor of the LTC1923 error amplifier, any common mode issues will be avoided.

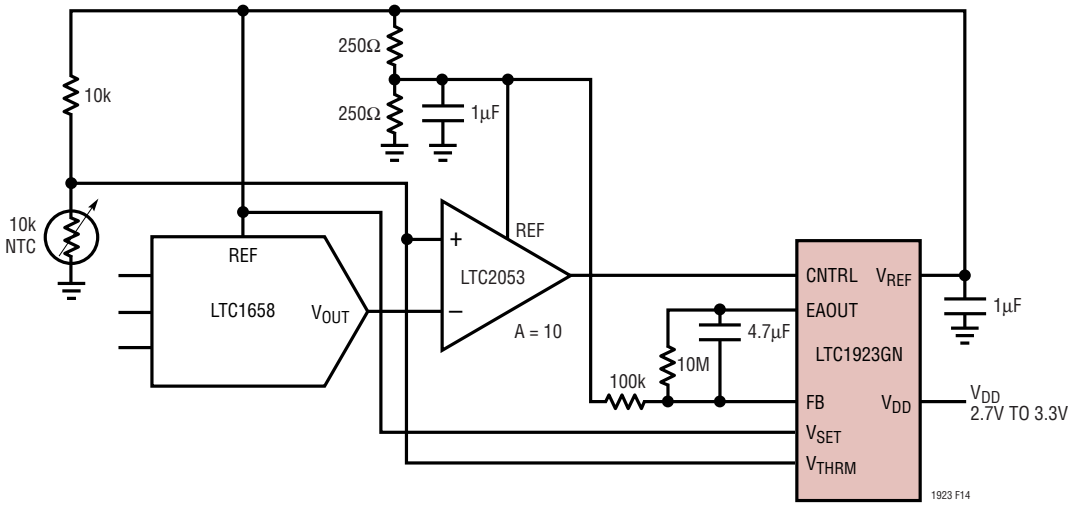


Figure 14. Low Input Supply Voltage Circuit

APPLICATIONS INFORMATION

Higher Voltage Applications

A bank of TECs can be wired in series to minimize board real estate utilized by the application. A higher voltage supply may be required depending upon how many TECs are placed in series and what their maximum voltage drop is. In other applications, only one high current supply may be available, with the output voltage of this supply being greater than the LTC1923's absolute maximum voltage rating. The absolute maximum input voltage for the LTC1923 is 6V. Since the current drawn by the LTC1923 is small, it can be powered from a low current, 5V (or less) supply. A 12V application for driving the full bridge is shown in Figure 15. Two LTC1693-1 high speed dual MOSFET drivers are used to step up the lower voltage produced by the LTC1923 drivers to the higher voltage levels required to drive the full bridge. The LTC1693 requires proper bypassing and grounding due to its high switching speed and large AC currents. Mount the low ESR bypass capacitors as close to the pins as possible, shortening the leads as much as possible to reduce inductance. Refer to the LTC1693 data sheet for more information. Since the LTC1693-1 low-to-high and high-to-low propagation delays are almost identical (typically 35ns), there is minimal skew introduced by the addition of these drivers. Sufficient dead time (typically 50ns) between one leg of the bridge shutting off and the other turning on, as set up by the LTC1923, will be maintained. If this dead time is insufficient, the resistor tied to the R_T pin can be increased to increase this time.

Care must be taken to ensure that the external MOSFETs are properly selected based on the maximum drain-source voltage, V_{DS}, gate-source voltage, V_{GS}, and $R_{DS(ON)}$. Many MOSFETs that have an absolute maximum V_{DS} of 20V have a maximum V_{GS} of only 12V, which is insufficient for 12V applications. Even the 14V maximum V_{GS} rating of the Si9801DY may not provide adequate margin for a 12V bridge supply voltage. Refer to Efficiency Considerations for more discussion about selecting a MOSFET with $R_{DS(ON)}$.

Two pairs of resistors, R_{T1} and R_{T2}, must be added to ensure that the absolute maximum input voltage is not exceeded on the TEC$^+$ and TEC$^-$ inputs. The maximum voltage on TEC$^+$ and TEC$^-$ must be less than the V_{DD} input supply to the LTC1923 which, for this example, is 5V. The following equation will guarantee this:

$$\frac{V_{BRIDGE}}{\left(1+\frac{R_{T1}}{R_{T2}}+\frac{R_{T1}}{100k}\right)} < V_{DD}$$

where V_{BRIDGE} is the supply voltage to the external bridge circuitry and V_{DD} is the input supply to the LTC1923.

These additional level shifting resistors affect some parameters in the data sheet. The direction comparator thresholds are increased to:

$(1 + R_{T1}/R_{T2} + R_{T1}/100k) \bullet 50mV$ and

$(1 + R_{T1}/R_{T2} + R_{T1}/100k) \bullet -50mV$

The output voltage on the V_{TEC} pin represents the voltage across the TEC ($V_{TECOOLER}$) reduced by a factor of $(1 + R_{T1}/R_{T2} + R_{T1}/100k)$ or:

$$V_{VTEC} = V_{TECOOLER}/(1 + R_{T1}/R_{T2} + R_{T1}/100k)$$

The term containing 100k is the loading error introduced by the input impedance of the differential amplifier. Typically this value will be 100k, but can vary due to normal process tolerances and temperature (up to ±30%). Due to this variability, it may be desirable to minimize the loading effect to try to keep a tight tolerance on the TEC clamp voltage. Although it will increase quiescent current draw, this can be accomplished by making the value of R_{T1} as small as possible.

As a result of this level shifting, the TEC voltage necessary to activate the clamp is raised. The voltage across the TEC where the voltage clamp activates will be:

$$V_{TECOOLER} = (1 + R_{T1}/R_{T2} + R_{T1}/100k) \bullet 2.5V$$

One drawback with using the LTC1693 MOSFET drivers is the inability to adjust the slew rate of the output drivers to reduce system noise.

APPLICATIONS INFORMATION

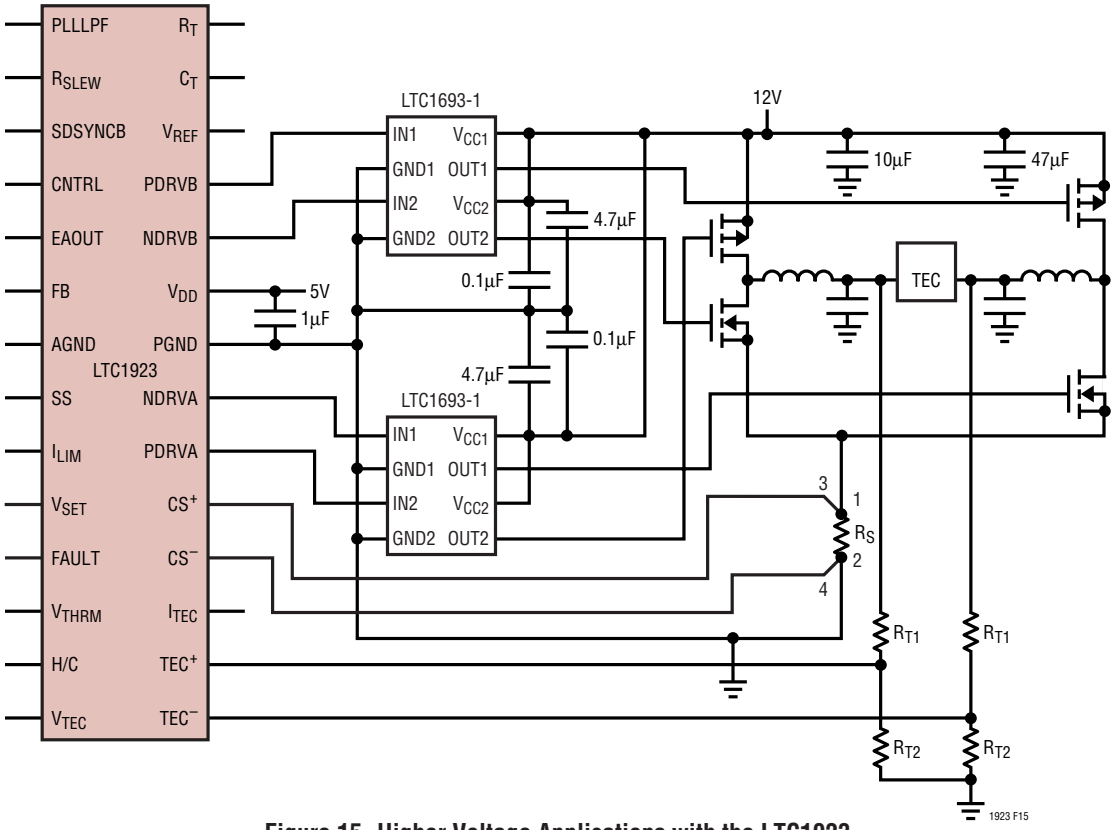
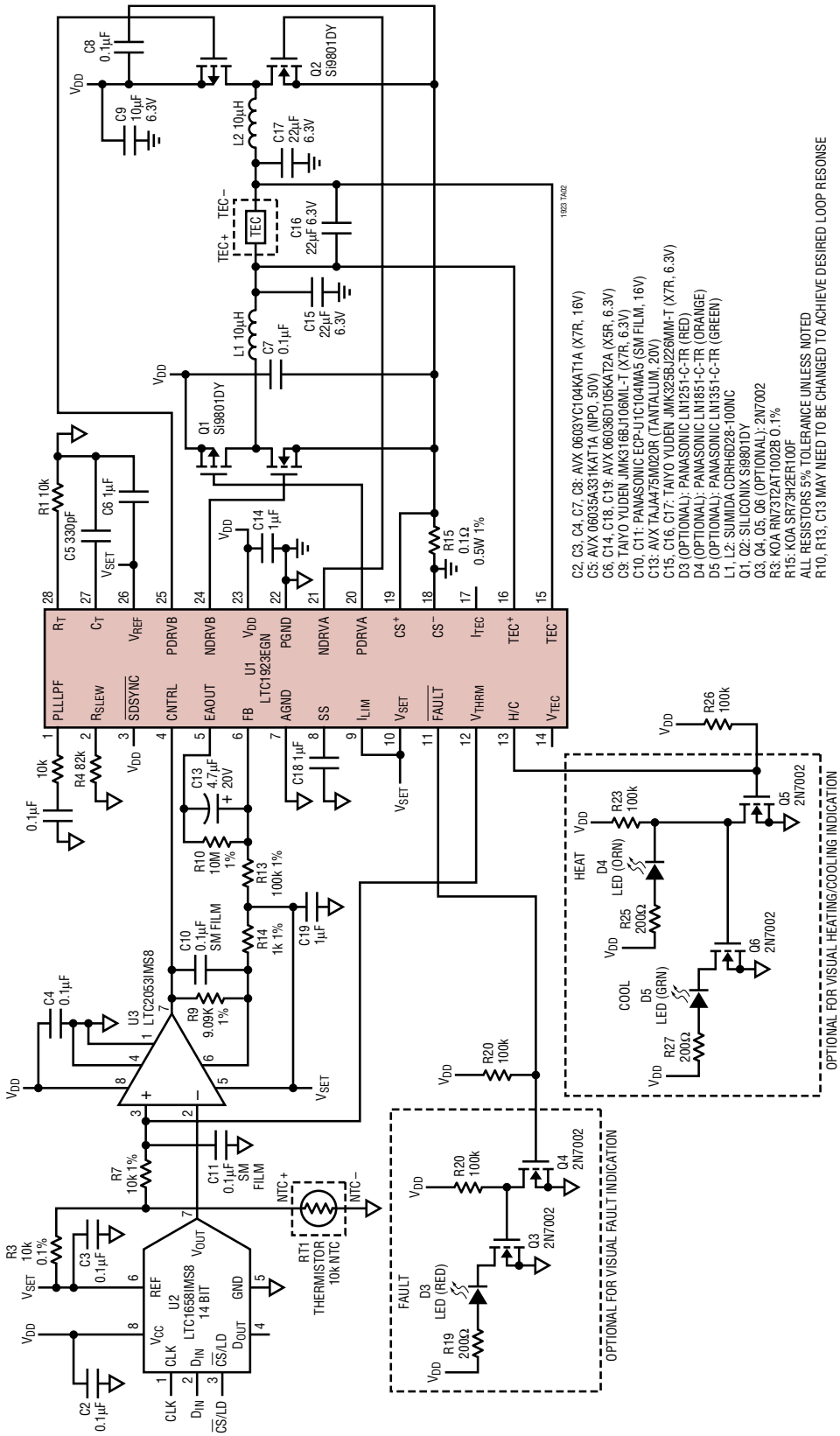


Figure 15. Higher Voltage Applications with the LTC1923

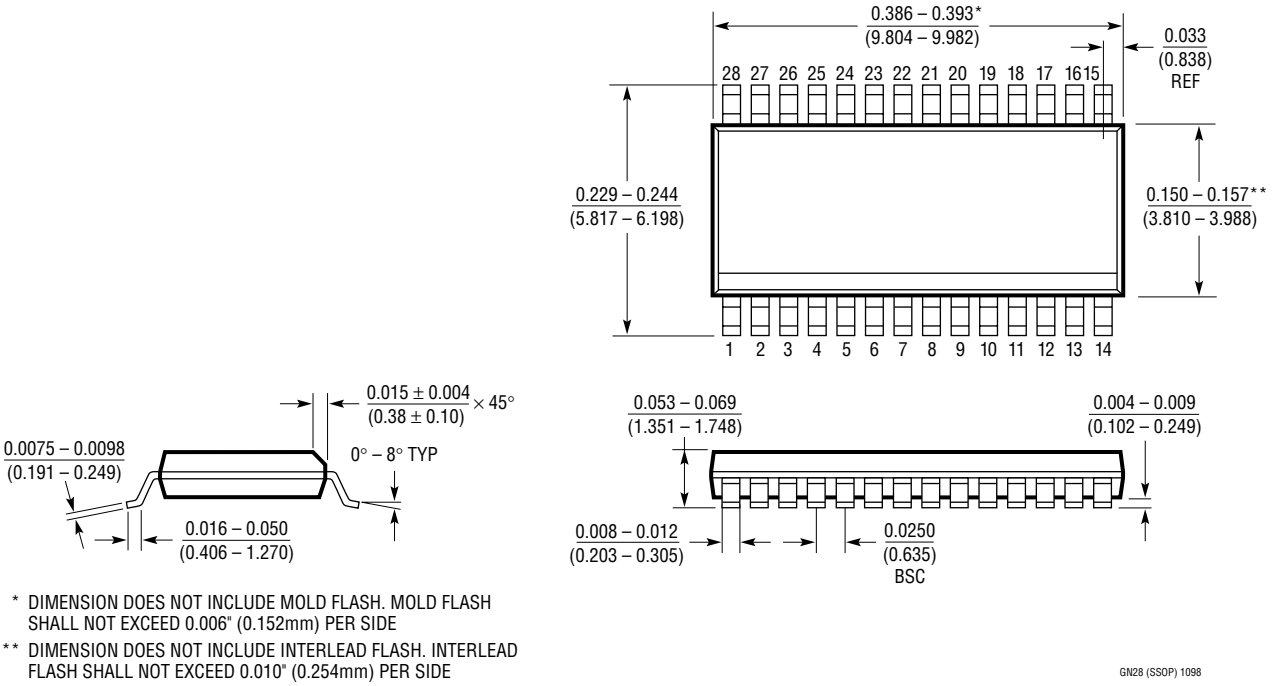
TYPICAL APPLICATION



Laser Temperature Control Loop Achieving Set Point Stability of 0.01°C

PACKAGE DESCRIPTION

GN Package
28-Lead Plastic SSOP (Narrow .150 Inch)
(Reference LTC DWG # 05-08-1641)



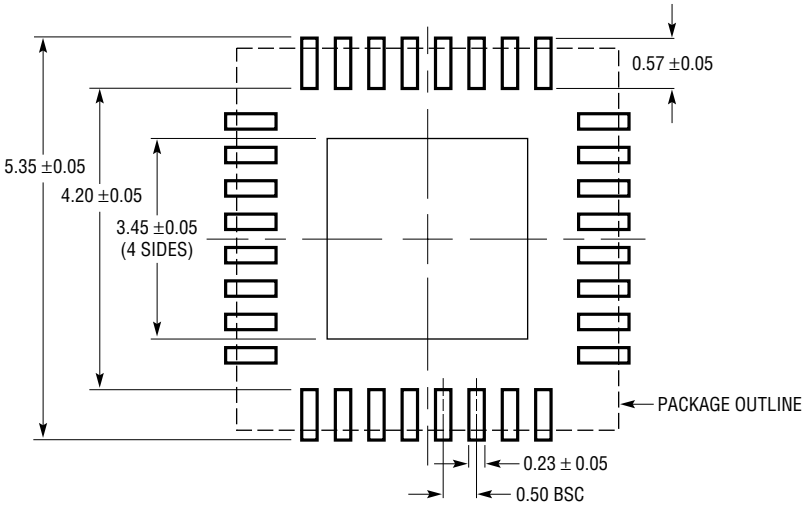
* DIMENSION DOES NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED 0.006" (0.152mm) PER SIDE

** DIMENSION DOES NOT INCLUDE INTERLEAD FLASH. INTERLEAD FLASH SHALL NOT EXCEED 0.010" (0.254mm) PER SIDE

GN28 (SSOP) 1098

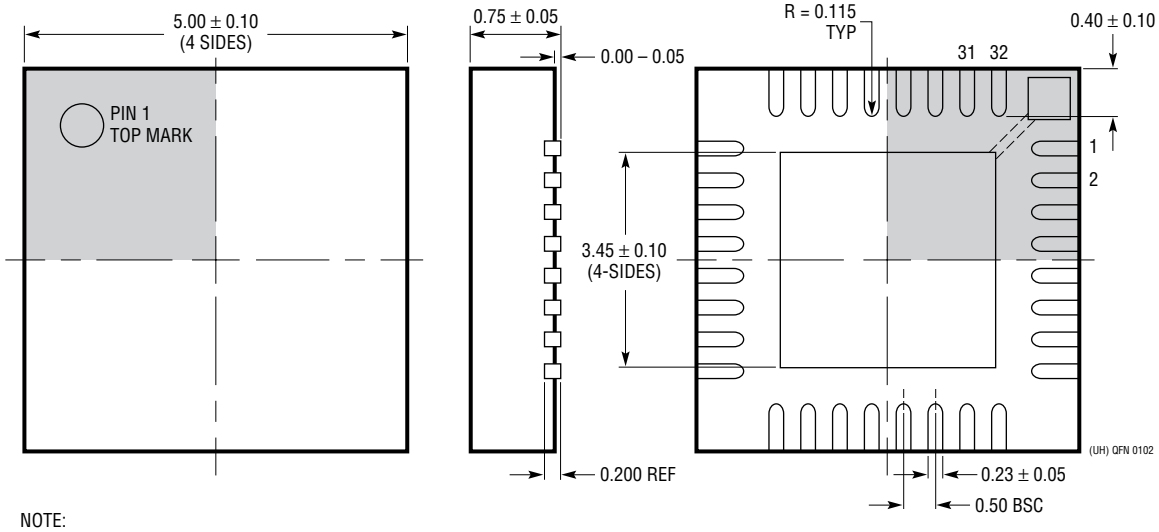
PACKAGE DESCRIPTION

UH Package
32-Lead Plastic QFN (5mm × 5mm)
(Reference LTC DWG # 05-08-1693)



RECOMMENDED SOLDER PAD LAYOUT

BOTTOM VIEW—EXPOSED PAD



NOTE:
1. DRAWING PROPOSED TO INCLUDE JEDEC PACKAGE OUTLINE
   M0-220 VARIATION WHHD-(X) (TO BE APPROVED)
2. DRAWING NOT TO SCALE
3. ALL DIMENSIONS ARE IN MILLIMETERS
4. DIMENSIONS OF EXPOSED PAD ON BOTTOM OF PACKAGE DO NOT INCLUDE
   MOLD FLASH. MOLD FLASH, IF PRESENT, SHALL NOT EXCEED 0.20mm ON ANY SIDE
5. EXPOSED PAD SHALL BE SOLDER PLATED

RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LTC1658	14-Bit Rail-to-Rail Micropower DAC	3V or 5V Single Supply Operation, I_{CC} = 270µA, 8-Lead MSOP Package
LTC1693-1	High Speed Dual N-Channel MOSFET Driver	1.5A Peak Output Current, 1GΩ Electrical Isolation, SO-8 Package
LTC2053	Zero Drift Instrumentation Amp	Max Gain Error 0.01%, Input Offset Drift of 50nV/°C, Input Offset Voltage of 10µV

Linear Technology Corporation
1630 McCarthy Blvd., Milpitas, CA 95035-7417
(408) 432-1900 • FAX: (408) 434-0507 • www.linear.com

LT/TP 0502 2K • PRINTED IN USA