LONTIUM SEMICONDUCTOR CORPORATION

ClearedEdge™ Technology

LT86102SX HDMI/DVI 1:2 Splitter Data Sheet

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Revision History

Date	Owner	Notes	**Version**
02/10/2014	Y.Shen	Initial data sheet creation	Preliminary
05/12/2014	XH.Guo	Update power consumption	1.0
07/14/2014	N.Wang	Check package information	1.1
02/2/2015	WJ.Liu	Update temperature range	1.2

Table of Contents

1. General Description

The LT86102SX is Lontium's 4th generation 2-port HDMI/DVI splitter which can repeat one HDMI/DVI signal to 2 HDMI/DVI signal sets, support up to 2 different HDMI/DVI receiving/display terminals. Based on ClearedEdge™ technology, it supports up to 3.4Gbps data rate per channel, compliant with the HDMI 1.4/DVI 1.0 specifications.

The device incorporates a pair of ODTs, an adaptive equalizer and a CDR circuit on each data channel of receiver side, and a de-emphasis driver with optional back terminations on each data channel of transmitter side. The clock channel feeds a high-performance PLL that regenerates a low jitter output clock for data recovery. The LT86102SX process HDCP decryption/encryption and transmits the data to 2 HDMI/DVI ports.

The HDCP repeater engine in LT86102SX handles all the processing required by authentication, decryption and encryption in hardware. This greatly reduces the external MCU overhead and firmware complexity. However, for more flexibility, the LT86102SX also provides an option of software-controlled mode in which HDCP operations are entirely controlled by external MCU.

Pre-programmed HDCP key sets ease the use of HDCP function and reduce the BOM cost. However, users can also use external key sets through the ESCL/ESDA port. The LT86102SX integrates EDID shadow RAM for better compatibility and reduced system complexity. Embedded EDID is accessible to the upstream port before the real EDID is loaded by the external MCU.

Fabricated in an advanced CMOS process, the LT86102SX is provided in a 80-lead LQFP package and is specified over the -40° C to +85° C temperature range.

1.1 FEATURES

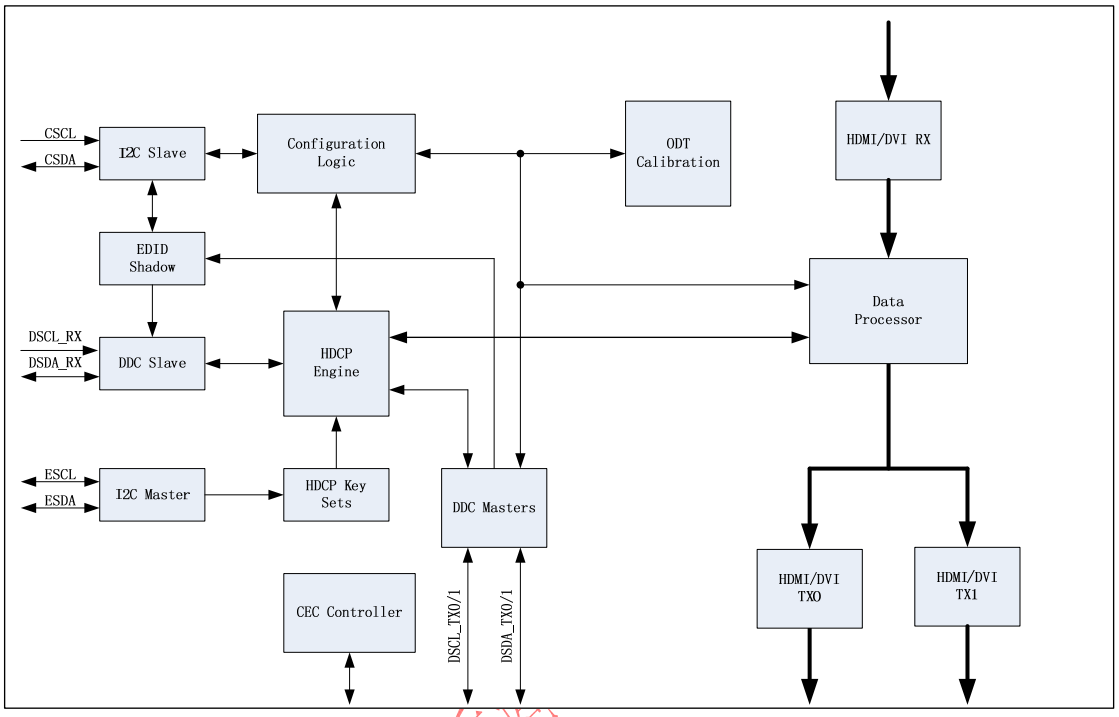
- HDMI 1.4/DVI 1.0 specifications compliant
- Support 3D video formats and 4Kx2K extended resolution formats up to 3.4Gbps data rate
- Adaptive equalization and de-emphasis to compensate long cable losses
- ODTs and calibration
- Integrated HDCP repeater engine compliant with HDCP 1.4 specification
- Fully hardware-controlled or optional software-controlled HDCP operations
- Pre-programmed HDCP key sets or external EEPROM stored key sets
- Integrated CEC controller
- Integrated EDID shadow RAM and embedded EDID
- 5V-tolerant DDC interfaces
- 1 HDMI/DVI input port, up to 2 HDMI/DVI output ports
- Unlimited cascading for more output ports or signal repeating
- 80-pin LQFP package

1.2 APPLICATIONS

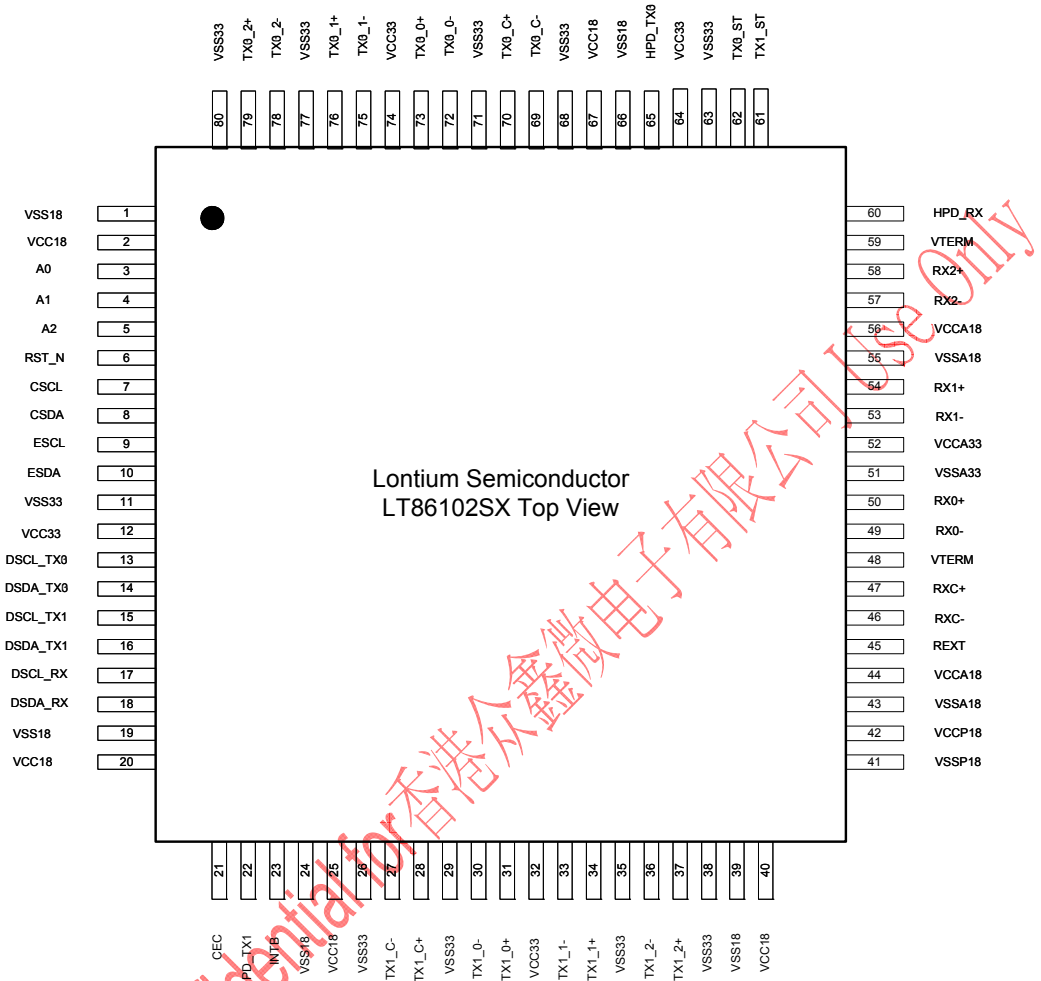
- Multiple display/TV support
- HDMI/DVI signal splitting/repeating

2. Function Description

2.1 FUNCTION BLOCK DIAGRAM



2.2 PIN CONFIGURATION



2.3 PIN DESCRIPTIONS

PIN	NAME	FUNCTION	NOTES
11，26，29，35，38，63，68，71，77，80	VSS33	I/O Ground	
12，32，64，74	VCC33	I/O Power, 3.3V	
1，19，24，39，66	VSS18	Core Ground	
2，20，25，40，67	VCC18	Core Power, 1.8V	
51	VSSA33	Analog Ground	
52	VCCA33	Analog Power, 3.3V	
43，55	VSSA18	Analog Ground	

44，56	VCCA18	Analog Power, 1.8V	
41	VSSP18	PLL Ground	
42	VCCP18	PLL Power, 1.8V	
48，59	VTERM	Termination Power, 3.3V nominal	
46，47， 49，50， 53，54， 57，58	RXC-，RXC+， RX0-，RX0+， RX1-，RX1+， RX2-，RX2+	HDMI/DVI RX Port	CML input
69，70， 72，73， 75，76， 78，79	TX0_C-，TX0_C+， TX0_0-，TX0_0+， TX0_1-，TX0_1+， TX0_2-，TX0_2+	HDMI/DVI TX Port 0	CML Output
27，28， 30，31， 33，34， 36，37	TX1_C-，TX1_C+， TX1_0-，TX1_0+， TX1_1-，TX1_1+， TX1_2-，TX1_2+	HDMI/DVI TX Port 1	CML Output
17，18	DSCL_RX, DSDA_RX	RX-Side DDC I2C Port. This port supports both HDCP and EDID access.	5V Tolerant I/O (Internal Weak Pull-Up)
9，10	ESCL, ESDA	EEPROM I2C Port. This port is dedicated to loading HDCP Key Sets.	5V Tolerant I/O (Internal Weak Pull-Up)
7，8	CSCL, CSDA	Configuration I2C Port	5V Tolerant I/O (Internal Weak Pull-Up)
15，16， 13，14，	DSCL_TX1，DSDA_TX1， DSCL_TX0，DSDA_TX0，	TX-Side DDC I2C Ports. These ports support both HDCP and EDID access.	5V Tolerant I/O (Internal Weak Pull-Up)
6	RST_N	External Reset (Active Low)	LVTTL Input (Internal Weak Pull-Up)
21	CEC	CEC Port	3.3V Tolerant I/O (Internal Weak Pull-Up)
60	HPD_RX	RX-Side HPD Port	5V Tolerant Output(Internal Weak Pull-Down)
65，22	HPD_TX0, HPD_TX1,	TX-Side HPD Ports	5V Tolerant Input (Internal Weak Pull-Down)
3，4，5	A0,A1,A2	Lowest 3 bits of the I2C slave device address for configuration I2C port (CSCL, CSDA) 0 1 1 1 A2 A1 A0 R/W	LVTTL Input (Internal Weak Pull-Down)
62，61	TX0_ST, TX1_ST	TX Ports Status. A HIGH status indicates the corresponding TX Port works fine, while a LOW status denotes a bad working status or no connection.	LVTTL Output (LED-Driving Ability)
45	REXT	External Resistor of 2KΩ (1%) should tie this pin to VSSA33.	Analog I/O
23	INTB	Interrupt output. This pin can be configured as either push-pull or open-drain type. Its polarity can be positive (active high) or negative (active low).	

Note: HIGH = VCC33, LOW = VSS33

2.4 ELECTRICAL CHARACTERISTICS

Absolute maximum conditions

Symbol	Parameter	Min	Typ	Max	Unit
VCCA33 VCC33	3.3V Supply	-0.3		4.0	V
VCCA18 VCC18 VCCP18	1.8V Supply	-0.3		2.5	V
Vin	Input Voltage	-0.3		VCC33+0.3	V
Vo	Output Voltage	-0.3		VCC33+0.3	V
Va	Ambient Temperature	-40		85	℃
Vstg	Storage Temperature	-55		125	℃
θja	Thermal Resistance		29		℃/W
Ppd	Package Power Dissipation			2.6	W

Notes:

1. Permanent device damage may occur if absolute maximum conditions are exceeded.
2. Function operation should be restricted to the conditions described under Normal Operating Conditions.

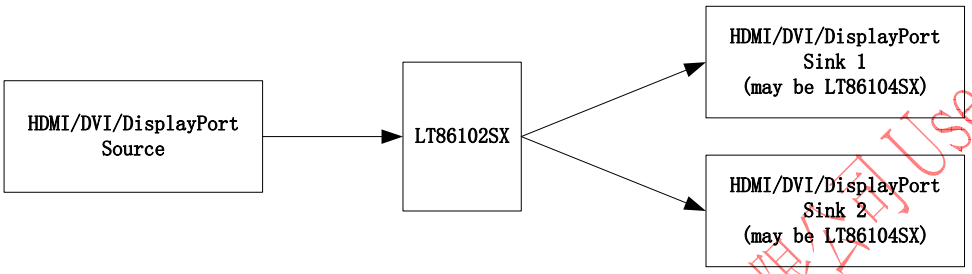
Normal operating conditions

PARAMETER	CONDITION	MIN	TYP	MAX	UNITS
3.3V Power Supply	DC	3.0	3.3	3.6	V
1.8V Power Supply	DC	1.62	1.8	1.98	V
Supply-Noise Tolerance	DC to 500kHz		200		mVp-p
CML INPUTS					
Differential Input Voltage Swing		150		1200	mVp-p
Common-Mode Input Voltage		VCCA33-0.5		VCCA33+0.1	V
Input Resistance	Single-ended	45	50	55	Ω
CML OUTPUTS					
Differential Output-Voltage Swing	50 ohm load, each side to VCCA33	800	1000	1200	mVp-p
Output-Voltage High	Single-ended		VCCA33		mV
Output-Voltage Low	Single-ended	VCCA33-600		VCCA33-400	mV
Output Voltage During Power-Down	Single-ended	VCCA33-10		VCCA33+10	mV
Common-Mode Output Voltage	50 ohm load, each side to VCCA33	VCC33-0.25			V
Rise /Fall Time	20% to 80%	100	150	200	ps
LVTTL CONTROL AND STATUS INTERFACE					
LVTTL Input High Voltage		2.0			V
LVTTL Input Low Voltage				0.8	V
LVTTL Input High Current	VIH(MIN) < VIN < VCC33			-50	μA
LVTTL Input Low Current	GND < VIN < VIL(MAX)			-100	μA
Open-Drain Output High	RLOAD 10k to VCC33	2.4			V

Open- Drain Output Low	RLOAD 2k to VCC33	0.4	V
Open- Drain Output Sink		5	mA
Supply Current			
4Kx2K	3.3v	79	mA
	1.8v	412	mA
1080p 12bit	3.3v	56	mA
	1.8v	356	mA
1080p 10bit	3.3v	56	mA
	1.8v	319	mA
1080p 8bit	3.3v	56	mA
	1.8v	282	mA
720p 12bit	3.3v	56	mA
	1.8v	244	mA
720p 10bit	3.3v	56	mA
	1.8v	226	mA
720p 8bit	3.3v	62	mA
	1.8v	208	mA
480p 12bit	3.3v	62	mA
	1.8v	176	mA
480p 10bit	3.3v	62	mA
	1.8v	169	mA
480p 8bit	3.3v	62	mA
	1.8v	162	mA

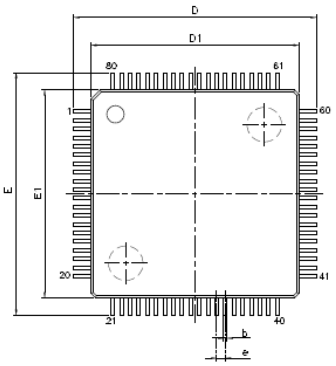
2.5 TYPICAL APPLICATIONS

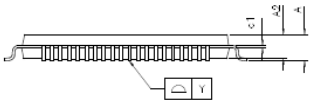
The following picture shows the typical application of LT86102SX. It can receive HDMI/DVI signals from an upstream source device and split it up to 2 paths feeding into 2 independent sink devices respectively. The HDMI/DVI Sink devices could alternatively be splitters (LT86102SX itself) to form a cascade network for more device connections. This application provides a convenient and efficient scheme for multiple displays situation.

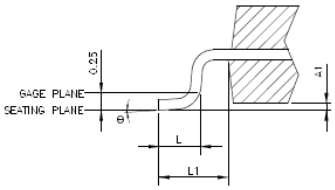


3. Packaging

The LT86102SX is packaged in an 80-pin LQFP package.







VARIATIONS (ALL DIMENSIONS SHOWN IN MM)

SYMBOLS	MIN.	MAX.
A	--	1.6
A1	0.05	0.15
A2	1.35	1.45
c1	0.09	0.16
D	14 BSC	
D1	12 BSC	
E	14 BSC	
E1	12 BSC	
e	0.5 BSC	
b	0.17	0.27
L	0.45	0.75
L1	1 REF	
Y	—	0.08
θ	0°	7°

NOTES:
1.JEDEC OUTLINE:MS-026 BDD
2.DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25mm PER SIDE. D1 AND E1 ARE MAXIMUM PLASTIC BODY SIZE DIMENSIONS INCLUDING MOLD MISMATCH.
3.DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION.ALLOWABLE DAMBAR PROTRUSION SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED THE MAXIMUM b DIMENSION BY MORE THAN 0.08mm.

References

Standards Documents

The abbreviations shown in column one of table below is used elsewhere in this data sheet. Please contact the responsible standards bodies here for more information on these specifications.

HDMI	*High Definition Multimedia Interface*, Revision 1.1, HDMI Consortium; March 2004.
HCTS	*HDMI Compliance Test Specification*, Revision 1.1, HDMI Consortium, Junu 2004.
HDCP	*High-bandwidth Digital Content Protection*, Revision 1.1, Digital-CP, LLP; June 2003.
DVI	*Digital Visual Interface*, Revision 1.0, Digital Display Working Group; April 1999.
E-EDID	*Enhanced Extended Display Identification Data Standard*, Release A Revision 1, VESA; Feb. 2000.
EDIDUG	*VESA EDID Implementation Guide*, VESA; March 2001.
CEA861	*A DTV Profile for Uncompressed High Speed Digital Interfaces*, EIA/CEA; January 2001.
CEA861B	*A DTV Profile For Uncomp. High Speed Digital Interfaces*, Draft 020328, EIA/CEA; March 2002.
EDDC	*Enhanced Display Data Channel Standard*, Version 1, VESA; September 1999.

These documents are available from the following standards groups:
ANSI/EIA/CEA Standards:
http://global.l.com or by e-mail to global@l.com, or telephone at 800-854-7179.
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