TECHNICAL MANUAL

LSI53CF92A
Fast SCSI Controller

April 2002

Version 2.1

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Preface

This book is the primary reference and technical manual for the LSI53CF92A Fast SCSI Controller. It contains a complete functional description and includes complete physical and electrical specifications.

Audience

This document assumes that you have some familiarity with current and proposed SCSI standards. The people who benefit from this book are:

- Engineers and managers who are evaluating the controller for possible use in a system
- Engineers who are designing the controller into a system

Organization

This document has the following chapters and appendixes:

- Chapter 1, **Introduction**
- Chapter 2, **Functional Description**
- Chapter 3, **Signal Descriptions**
- Chapter 4, **Registers**
- Chapter 5, **Command Set**
- Chapter 6, **Electrical Specifications**
- Appendix A, **Register Map**
- Appendix B, **Wiring Diagram**

Related Publications

ANSI
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Prentice Hall
113 Sylvan Avenue
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(800) 947-7700
SCSI: Understanding the Small Computer System Interface,
ISBN 0-13-796855-8

LSI Logic World Wide Web Home Page
www.lsil.com

SCSI SCRIPTS™ Processors Programming Guide,
Order No. S14044.A

SCAM specification X3T9.2/93-109r5

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2575 N. E. Katherine
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Conventions Used in This Manual

The word *assert* means to drive a signal true or active. The word *deassert* means to drive a signal false or inactive.

Hexadecimal numbers are indicated by the prefix “0x” —for example, 0x32CF. Binary numbers are indicated by the prefix “0b” —for example, 0b0011.0010.1100.1111.

Revision Record

Revision	Date	Remarks
1.0	12/97	First version.
1.1	4/99	Miscellaneous edits, reformat.
2.0	11/00	All product names changed from SYM® to LSI.
2.1	12/01	Updated Tables 6.7, 6.13, and 6.15 and Figures 6.9, 6.12, and 6.16.

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Figures

Tables

Chapter 1
Introduction

This chapter is divided into the following sections:

1.1 General Description

The LSI53CF92A Fast SCSI Controller (FSC) is a high performance CMOS device designed to maximize SCSI transfer rates. This device conforms to American National Standards Institute (ANSI) standards X3.131-1986 (SCSI-1) and X3.131-199X (SCSI-2). The FSC includes the basic functionality of earlier SCSI devices, plus additional features including Fast SCSI, a 24-bit transfer counter, a part-unique ID code, and SCSI-Configured AutoMatically (SCAM) Level 1 and 2 capability.

The LSI53CF92A is a second generation SCSI controller that reduces protocol overhead by performing common SCSI sequences in hardware, in response to a single command. The LSI53CF92A operates at sustained data transfer rates up to 10 Mbytes/s in synchronous mode and 5 Mbytes/s in asynchronous mode. The LSI53CF92A has on-chip 48 mA drivers for Single-Ended (SE) transmission and is offered in a 64-pin Plastic Quad Flat Pack (PQFP) or a 64-pin Thin Quad Flat Pack (TQFP) package.

The microprocessor and DMA bus widths are eight bits. The FSC microprocessor bus can operate in either a multiplexed or nonmultiplexed mode, depending on the state of the MODE pin. See Figures 1.2 and 1.3 for more details.

1.2 SCSI-Configured AutoMatically (SCAM) Capability

The LSI53CF92A differs from other members of the 53Cx9x family in that SCAM capability has been incorporated into the device. SCAM requires the ability to manipulate the SCSI control and data lines individually. To provide this capability, a low-level SCSI programming mode has been added along with hardware assist for some SCAM operations. The LSI53CF92A now contains an additional register addressing mode, permitting access to two register banks, one for normal operation and one for SCAM operation. Refer to Section 2.8, “SCAM Capabilities,” on page 2-17, for more information.

1.3 TolerANT® Technology

The FSC features TolerANT technology, which includes active negation on the SCSI drivers and input signal filtering on the SCSI receivers. Active negation causes the SCSI REQ/, ACK/, Data, and Parity signals to be actively deasserted.

TolerANT receiver technology improves data integrity in unreliable cabling environments, where other devices would be subject to data corruption. TolerANT technology receivers filter the SCSI bus signal to eliminate unwanted transitions without the long signal delay associated with RC-type input filters. This improved driver and receiver technology helps to eliminate the double clocking of data, which is the single biggest data reliability issue with SCSI operations. The benefits of TolerANT technology include increased immunity to noise when the signal is going HIGH, increased performance due to balanced duty cycles, and improved Fast SCSI transfer rates. TolerANT technology is compatible with both the Alternative One and Alternative Two termination schemes proposed by the ANSI.

1.4 Features

- SCSI-2 compatible
- Ideal for target applications such as CD-ROMs
- Up to 5 Mbytes/s sustained asynchronous SCSI transfer rate
- Up to 10 Mbytes/s sustained synchronous SCSI transfer rate
- TolerANT technology provides:
  - Active negation pad cells on the SCSI Data, Parity, REQ/, and ACK/ pins to improve Fast SCSI-2 performance
  - Input signal conditioning on the REQ/ and ACK/ lines
- SCAM Level 1 and 2 capability
- On-chip 48 mA drivers
- Latch-up protection greater than 100 mA
- Typical 300 mV SCSI bus hysteresis
- Voltage feed-through protection
- A 24-bit transfer counter that eliminates intersector transfer delays and allows single transfers up to 16 Mbytes
- Up to 13.3 Mbytes/s DMA interface
- SCSI-2 tagged-queuing
- Single-pin, SE SCSI bus operation
- Combination commands implemented with on-chip sequential logic
- Host intervention minimized using combination commands
- Enhanced hot-plugability
- An 8-bit, split µP/DMA architecture
- Parity generation, optional checking
- Parity pass-through
- Supports clock frequencies from 10 to 40 MHz
- Low power CMOS
- Ordering Information:
  - LSI53CF92A: 64-pin PQFP or TQFP

Figure 1.1 illustrates the functional block diagram for the LSI53CF92A.

Figure 1.1 Functional Block Diagram

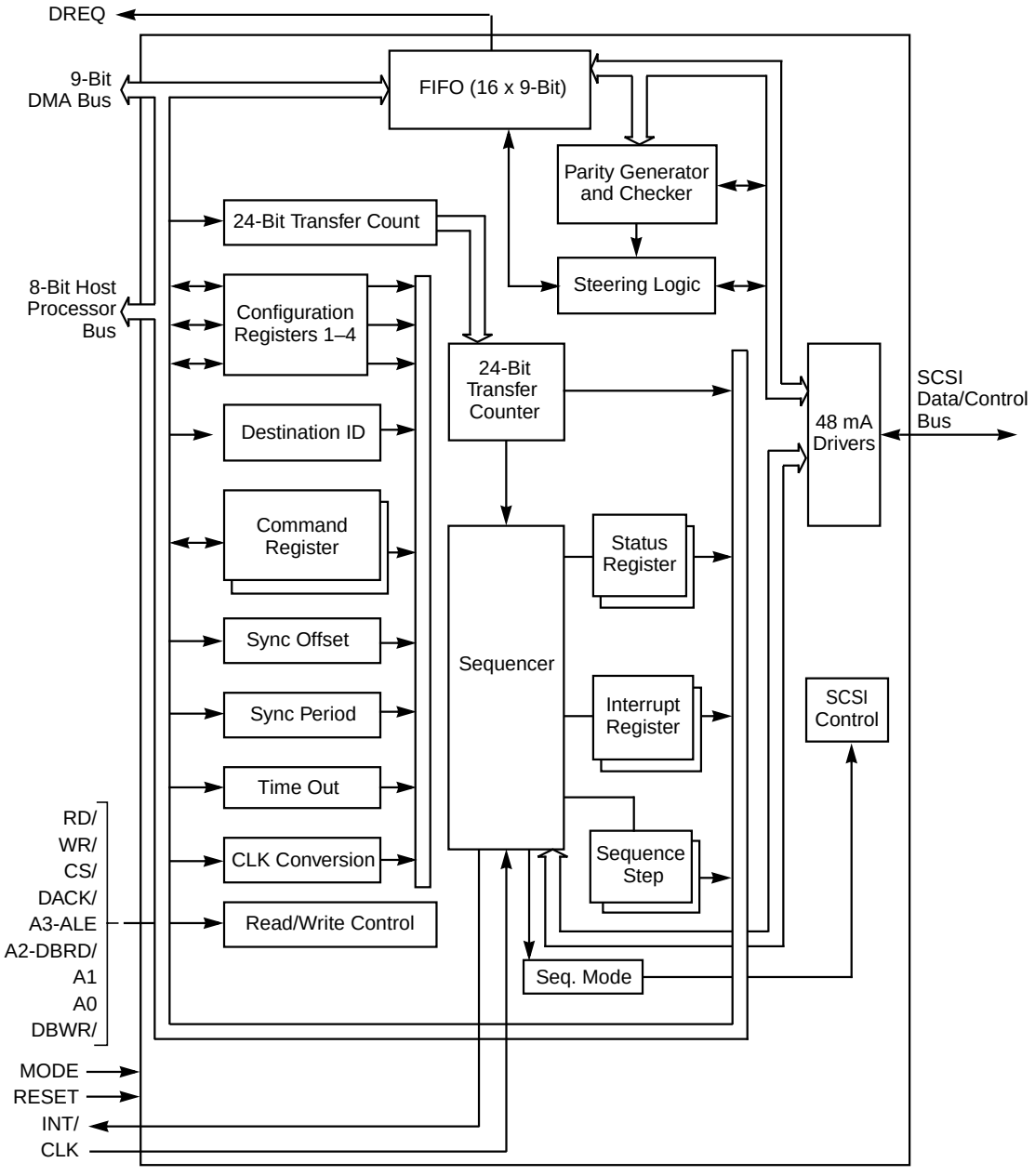


Figure 1.2 Bus Configuration, Multiplexed Mode (Dual Bus, 8-Bit DMA Bus and 8-Bit Multiplexed Processor Address/Data Bus)

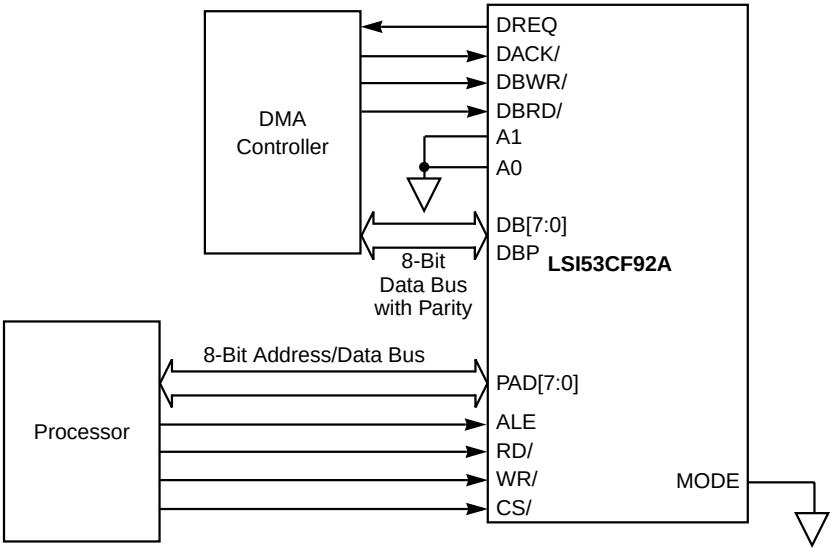
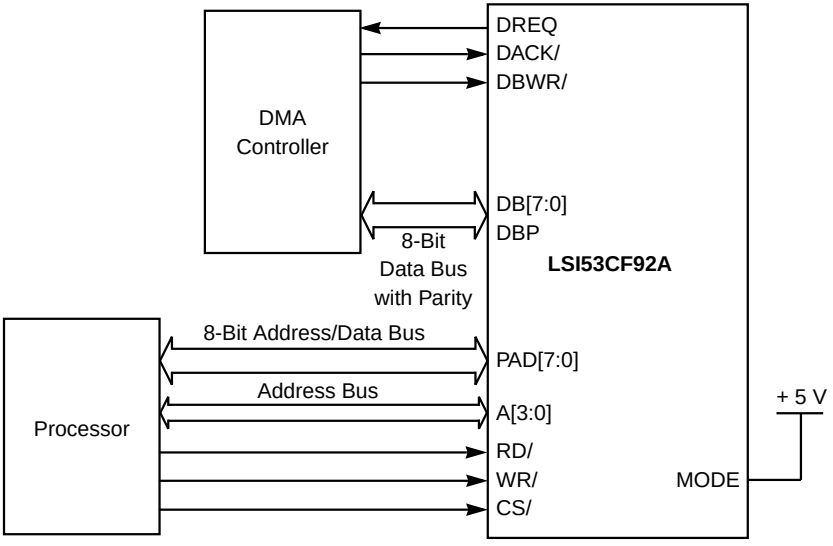


Figure 1.3 Bus Configuration, Nonmultiplexed Mode (Dual Bus, 8-Bit DMA Bus and 8-Bit Processor Bus)



Chapter 2
Functional Description

This chapter is divided into the following sections:

The FSC has a command set that allows it to perform common SCSI sequences at hardware speed without host intervention. Its on-chip FIFO may be accessed simultaneously by the SCSI bus and either the microprocessor or the host DMA controller. All command, data, status, and message bytes pass through the FIFO on the way to or from the SCSI bus. Most FSC commands have two versions: DMA and non-DMA. When DMA instructions are used, data passes between memory and the SCSI bus with the FIFO acting as temporary storage when the DMA channel is temporarily shut down by a higher priority event, such as DRAM refresh.

The FIFO also helps speed execution during non-DMA transfers. For example, in initiator mode, the microprocessor loads the Command Descriptor Block (CDB) and optionally, one or three message bytes into the FIFO. It then issues one of several selection commands and wait for an interrupt. The FSC waits for bus free, arbitrates for the bus until it acquires it, sends the message bytes followed by the CDB, then generates an interrupt. Meanwhile, a multitasking host may continue with other tasks.

The LSI53CF92A is the newest member of the LSI53C90 family, with additional features such as Fast SCSI transfer rates, single-pin SE SCSI, 8-bit DMA mode, and TolerANT Active Negation Technology.

2.1 Typical SCSI Operation

In target mode, the microprocessor enables selection and then waits for an interrupt. Eventually an initiator selects the FSC. It then automatically steps through the selection and command phases before generating an interrupt. When the interrupt occurs, the entire CDB is in the FIFO along with any message bytes sent by the initiator.

After the selection phase has been successfully completed, the FSC may transfer bytes in any SCSI information phase whether it is operating in initiator or target mode. The FSC supports disconnect/reselect in both initiator and target modes, making high performance multithreaded systems easy to implement.

The FSC may transfer data phase bytes across the bus synchronously, at speeds up to 10 Mbytes/s, or asynchronously, at speeds up to 5 Mbytes/s. Refer to Section 2.6, “SCSI Data Transfer Rates,” on page 2-14, for more information. The difference between asynchronous and synchronous operation is transparent to the user except that the synchronous offset and the synchronous transfer period registers must be programmed prior to synchronous data transfer. The default, after hardware or software reset, is asynchronous transmission.

Data phase bytes are usually transferred using DMA. The microprocessor programs an external DMA controller, programs the FSC transfer count register, issues one of several FSC data transfer commands, then waits for an interrupt. The DMA controller and the FSC transfer all the data without microprocessor intervention.

To end the SCSI transaction, the FSC target places a status byte and a message byte in the FIFO. It then issues one of two single commands which causes the FSC first to assert Status phase, send the first byte, assert Message In phase, send the second byte, disconnect from the SCSI bus (after the initiator releases ACK/ [Acknowledge]) and interrupt the microprocessor.

The end of a SCSI transaction is similar for an FSC initiator except that it receives two bytes into its FIFO. The initiator prevents the target from disconnecting by holding ACK/ asserted on the bus while the microprocessor examines the status and message bytes. If both bytes are acceptable, the Message Accepted command instructs the FSC to release ACK/, which allows the target to disconnect and causes the initiator to interrupt its host and report the disconnect. If the status and message bytes are not acceptable, the host could first issue the Set ATN (Attention) command before issuing the Message Accepted command. This instructs the FSC to assert ATN/ before releasing ACK/, which should cause the target to request Message Out phase rather than disconnect.

2.2 Bus-Initiated Sequences

- Selection
- Reselection
- SCSI bus reset

Selection or reselection sequences occur in the disconnected state when the FSC is selected or reselected by another initiator or target, if the Enable Selection or Reselection command has previously been received by the FSC.

In addition to responding to bus-initiated events, the FSC may initiate a bus event by using one of several selection or reselection commands. If one of these commands starts executing, the Enable Selection or Reselection command is cleared after another device has been selected, preventing the FSC from responding to a Select or Reselect command. Normally the microprocessor has 250 ms (ANSI recommended selection time-out period) after the chip disconnects from the bus to re-enable bus-initiated events. If the time-out period is exceeded, an initiator or target which is attempting to connect to the FSC may time-out and abort.

If, on the other hand, the bus-initiated event occurs before the command starts executing, the FIFO and command register is cleared and any further writes by the microprocessor are ignored until the Interrupt register is read. Because a selection or reselection command requires placing something in the FIFO, these bytes are lost, as is any command written to the Command register. The interrupt handler that services a selection or reselection command has to examine the bits in the Interrupt register

to determine if the FSC selected another device, or if it was selected by another device. The former case causes a Function Complete Interrupt, the latter case causes a Selection or Reselection interrupt.

2.2.1 Bus-Initiated Selection

When the FSC has been selected as a target, the following data is in its FIFO:

- Bus ID
- Identify message
- Optional two-byte command queuing message
- Command Descriptor Block (CDB)

The bus ID is always present and is always one byte. It is an unencoded version of the state of the bus during Selection phase. Any SCSI data bits that were true during Selection phase are set. The target ID must always be set. In arbitrating systems, the initiator ID must also be set. The initiator ID is optional in nonarbitrating systems. If parity checking is enabled, parity must be valid during the bus-initiated selection. If parity is not valid, the FSC does not respond to bus-initiated selection.

The identify message, if sent, is also be placed in the FIFO. The identify message is optional in SCSI-1 systems but is always one byte if it is used. In SCSI-2 systems a one or three byte message is sent, consisting of the one-byte identify message and an optional two-byte command queuing message. If the FSC is selected with ATN/ false, it stores a null byte (00) in the FIFO behind the bus ID, then begins requesting command phase bytes. A detected parity error causes the FSC to interrupt and stop, if parity checking is enabled.

If the FSC is selected with ATN/ true and the SCSI-2 bit is not set, it requests one message byte and places it in the FIFO behind the bus ID. Then it requests Command phase bytes unless the message byte is not a valid identify message, bit 7 in the Configuration 3 (Config 3) register is not set, or a parity error is detected, which causes the FSC to interrupt and stop. The Sequence Step register can then be examined to determine what events have been completed.

If the FSC is selected with ATN/ true and the SCSI-2 bit set, the FSC examines both the message byte and the ATN/ signal to determine how many bytes to request. If the first byte is a valid identify message and if ATN/ goes false after receiving the first byte, the FSC changes to Command phase. If the first byte is a valid identify message byte (0x80–0xFF) and ATN/ is still true, it requests two more message bytes. After requesting the message bytes, the FSC requests Command phase bytes unless one of the following situations occurs:

- The first byte is not a valid identify message
- A parity error is detected
- ATN/ goes false between the second and third bytes
- ATN/ remains true but the SCSI-2 bit is false.

All of these conditions cause the FSC to interrupt and stop.

To determine if one of these conditions has occurred, examine the Sequence Step register.

The CDB always begins at the third or fifth byte in the FIFO, assuming selection completed normally. The CDB may be 6, 10 or 12 bytes long. Thus, in SCSI-2, the entire FIFO may be filled if a tagged-queuing, 12-byte command is used.

2.2.2 Bus-Initiated Reselection

The FSC allows itself to be reselected as an initiator by a target if it has previously received the Enable Selection/Reselection command. If the sequence completes normally, the FIFO has the following information:

- Bus ID
- Identify message

The bus ID is always present and is always one byte. It is an unencoded version of the state of the bus during Reselection phase.

The identify message is always present and is always one byte.

The FSC prevents the target from disconnecting by holding ACK/ asserted on the bus while the microprocessor examines the Bus ID and Identify message bytes. The Message Accept command causes the FSC to release ACK/. Any further message bytes can be received with the Transfer Information command.

Note: The settings of the SCSI-2 or Queue Tag Enable bits do not affect this operation.

2.2.3 Bus-Initiated Reset

A SCSI bus-initiated reset is recognized by the FSC at any time. When SCSI RST/ pulses true, the FSC disconnects from the bus and resets its internal sequencer. If bit 6 in Configuration 1 (Config 1) register is not set, the FSC generates a SCSI reset-detected interrupt.

2.2.4 Stacked Commands

The Command register is a two-deep, eight-bit read/write register that gives commands to the FSC. If DMA commands are to be stacked, the Transfer Count must be loaded prior to loading the respective command. Command stacking should only be used during Data In and Data Out. If stacked commands are used in Initiator mode, it is recommended that the Features Enable bit in the Configuration 2 (Config 2) register be set. This causes the SCSI phase lines to be latched at the end of a command.

2.3 Parity Checking and Generation

The FSC has three bits that control parity generation and checking. These three bits can be accessed by the user and are described in Table 2.1. If parity checking is disabled, the FSC does not check for parity errors. In this document, the word detected in conjunction with parity error should be understood to imply that parity checking has previously been enabled.

In Target role, detected parity errors set the Parity Error bit (bit 5 in the Status register) and clear the Command register without causing an interrupt. In Initiator role, detected parity errors set the Parity Error bit and, if receiving SCSI bytes, assert ATN/ (Attention) prior to releasing

ACK/ (Acknowledge). Parity errors occurring after a phase change to Synchronous Data In are handled differently in Initiator mode. Refer to Chapter 5, “Command Set,” for more information on initiator commands.

Table 2.1 Parity Control

Control Bit	Data Direction	Bit Set	Bit Not Set
Parity Checking, Configuration 1 (Config 1), bit 4	SCSI to FIFO	Enable parity checking and error reporting. SDP loaded into FIFO.	Disable parity checking and error reporting. Parity generator to FIFO.
Test parity, Configuration 1 (Config 1), bit 5	FIFO to SCSI FIFO to memory	SDP is a replica of SD7. DBP is a replica of DB7.	FIFO to SDP. FIFO to DBP.
DMA parity, Configuration 2 (Config 2), bit 0	DACK/ to FIFO FIFO to SCSI	DBP to FIFO. Enable parity checking and error reporting.	Parity generator to FIFO. Disable parity checking and error reporting.

Configuration 2 (Config 2) register bit 2, the Target Bad Parity Abort bit, allows special handling for parity errors. When this bit is set, the chip aborts a Receive command or Receive Data command if bad parity is received from the SCSI bus. If a parity error occurs when the Target Bad Parity Abort bit is set, the Status register Parity Error bit (bit 5) is set, but no additional bits are set in the Interrupt or Status registers after bad parity is detected. The Transfer Counter and FIFO Flags registers contain a record of how many bytes were transferred before the command was aborted.

For additional information on the parity bits, refer to Chapter 4, “Registers.”

The LSI53CF92A has one parity pin (DBP). In both the Multiplexed Bus Configuration mode and in the Nonmultiplexed Bus Configuration mode, the processor connects to the FIFO on an 8-bit bus only. In both of these modes, the internal parity generator creates parity to send to the SCSI bus.

When the DBP pin is enabled, parity may pass between the SCSI and host DMA bus without change or may be generated by the FSC from the data byte. Whether generated internally or externally, the parity bit is always loaded into the FIFO along with the data byte. From there on, it moves through the FIFO along with the data byte. The FIFO may be accessed by three buses: SCSI bus, microprocessor bus, or host DMA bus.

If parity test mode is enabled during a DMA transfer, DBP is a duplicate of DB7. This is true both for data flowing from the FIFO to the SCSI Data Bus (SDB) pins or data flowing from the FIFO to the Host Data Bus (DB) pins.

The FSC flags parity errors as data comes into the FIFO from the SCSI bus, or as it leaves the FIFO on its way out to the SCSI bus.

2.4 Host Bus Configuration

The DMA and microprocessor buses may be configured in one of the two following ways.

2.4.1 Mode Description

Multiplexed Dual bus; 8-bit DMA bus and 8-bit multiplexed processor address/data bus.

Nonmultiplexed Dual bus; 8-bit DMA bus and 8-bit nonmultiplexed processor bus.

The operating mode is selected by the Mode strapping pin; refer to Chapter 3, “Signal Descriptions,” for the setting of either mode. The two operating modes are labeled Multiplexed mode and Nonmultiplexed mode. Refer to Chapter 1, “Introduction,” Figure 1.2, and Figure 1.3 for configuration diagrams. Both of these dual bus modes have separate data buses for DMA and microprocessor, which may be active simultaneously provided CS/ is not accessing the FIFO.

2.4.2 Multiplexed Bus Configuration Mode

In this dual-bus mode, 8-bit operations are supported by the DMA Data bus. The microprocessor interface is supported by the PAD bus. FIFO parity is not available for data transfers over the PAD bus. The direction of transfer is determined by the RD/ and WR/ lines. CS/ must be active during PAD bus accesses.

In the Multiplexed Bus Configuration mode, register addresses and register data are multiplexed on the PAD bus. The register address on the PAD[3:0] lines is latched into the chip on the HIGH to LOW transition of ALE (A3).

In this bus configuration mode, the Data bus configuration is for 8-bit DMA transfers. Pin A2 functions as the Data bus read signal (DBRD/), which drives the DMA read data. A1 and A0 must be tied to ground.

2.4.3 Nonmultiplexed Bus Configuration Mode

Like the Multiplexed Bus Configuration mode, this dual bus mode is configured for 8-bit transfers.

In this dual bus mode interface, DMA operations are supported by the DB bus, and the microprocessor interface is supported by the PAD bus. FIFO parity is not available for data transfers over the PAD bus. The direction of transfer is determined by the RD/ and WR/ lines. CS/ must be active during PAD bus accesses.

In the Nonmultiplexed Bus Configuration mode, transfers occur on the microprocessor interface over the PAD bus, which operates as a nonmultiplexed data only bus. The register address is carried by the A[3:0] lines and is latched into the chip on the HIGH to LOW transition of CS/.

2.5 DMA Operation

The FSC supports 8-bit DMA transfers. The on-chip FIFO allows the FSC to support normal and burst mode transfers. The DMA interface protocol runs asynchronous to the chip clock. The DMA Request signal (DREQ) is asserted when the DMA is ready for a transfer to or from the DMA channel. DREQ is asserted only when the DMA Acknowledge signal (DACK/) is inactive, and is released on the leading edge of DACK/. DREQ remains asserted until the chip receives as many DACK/s as it needs or can handle.

2.5.1 DMA Threshold

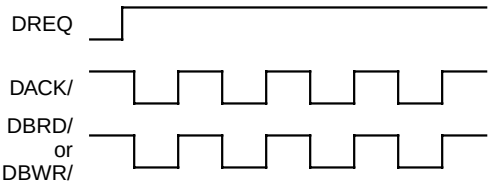
The threshold is the number of bytes in the FIFO that trigger DREQ. For DMA read, DREQ is asserted when the FIFO contains at least the threshold number of bytes. For DMA write, the FIFO must be able to accept this number of bytes. For 8-bit DMA operation the normal threshold is one byte.

2.5.2 Normal DMA Mode

In normal operation, DREQ remains true until the FIFO empties or fills, depending on the direction of the transfer. Figure 2.1 illustrates the case where the threshold is always exceeded. This is typical of a DMA interface that is slower than the SCSI device to which the system is connected.

Normal DMA mode tends to monopolize the DMA bus, and slows the entire system down to the performance level of the SCSI device to which the chip is connected. In single-threaded systems, however, this remains the most efficient method of transferring data as long as important events, like DRAM refresh, can interrupt the DMA transfer.

Figure 2.1 Normal DMA Mode



2.5.3 Threshold Eight Mode

Threshold Eight mode causes the FSC to wait until eight bytes or more can be transferred before it requests service from the external DMA controller. Because the DMA bus can operate at speeds five to ten times greater than typical SCSI devices, this mode allows SCSI operations to run effectively in parallel with other processes.

The Threshold Eight bit in Configuration 3 (Config 3) register changes the threshold to eight bytes. Refer to the description for the Configuration 3 (Config 3) register in Chapter 4, “Registers.” Threshold Eight mode is enabled by setting bit 0 in the Configuration 3 (Config 3) register and is valid in both bus configurations. Threshold Eight mode operates only during SCSI Data In or Data Out phase.

Note: When enabling this mode, the synchronous data offset can only be set to seven or less.

Threshold Eight mode causes DREQ to remain false until the FIFO can accommodate an eight-byte transfer. This improves DMA bus efficiency by keeping the chip off this bus until it can transfer at least eight bytes. With Threshold Eight enabled, the chip retains control of the DMA channel as long as one transfer can be accommodated. The transfer continues in normal mode whenever the Transfer Counter drops below eight bytes and the threshold drops to one transfer.

The following conditions must be true for a DMA Threshold Eight transfer to occur:

- Threshold Eight mode is enabled.
- Transfer Counter indicates eight or more bytes.
- The FIFO can accommodate an 8-byte transfer as follows:
  - The FIFO contains at least eight bytes of data to transfer to memory, or
  - At least the top eight bytes of the FIFO are empty to receive the eight-byte transfer from memory.

Because the Threshold Eight mode is enabled during DMA burst mode, the DMA burst is limited to eight transfers. This feature forces the chip to periodically relinquish control of the DMA channel, allowing other devices to gain access to the bus to perform such operations as memory refresh.

2.5.4 DMA Burst Mode

Burst mode, or Alternate DMA mode, is a special mode devised to maximize data throughput using most DMA controllers. DMA burst mode is enabled by setting both the Threshold Eight and the Alternate DMA mode bits in the Configuration 3 (Config 3) register. Threshold Eight causes the FSC to delay assertion of DREQ until it can transfer eight bytes. Alternate DMA mode causes the FSC to deassert DREQ after the byte transfers, causing the DMA controller to relinquish the bus.

This regular surrendering of the DMA channel has benefits for two common DMA interface problems. For DMA controllers that do not recognize higher priority requests until the current device finishes, the FSC can periodically force DMA arbitration. This allows DRAM refresh and other operations to occur during SCSI operations. For DMA controllers that are much faster than the SCSI host or peripheral to which the system is connected, bus efficiency is improved by ensuring that the FSC has data to transfer while the DMA controller is controlling the bus.

DMA Burst mode can be enabled in both bus configurations. DMA Burst mode affects the deassertion of DREQ and assertion of DACK/ for DMA reads and writes.

In the Multiplexed Bus Configuration mode, the FSC is designed to operate with a DMA controller that has timings similar to an 8237. Because many systems use one of the 8237 channels for DRAM refresh and because the 8237 does not recognize a higher priority request until it finishes its current transfer, Burst mode gives the best transfer rate without sacrificing memory integrity.

2.5.4.1 Deassertion of DREQ

The FSC remains in Burst mode as long as more than eight bytes remain to be transferred. However, if the Transfer Counter drops below eight, then the FSC switches out of Burst mode for the last one to seven bytes. The last bytes are transferred in Normal DMA mode where DREQ goes true and stays true as long as the FIFO is able to transfer data; DACK/ cycles true then false for each transfer. Because DACK/ must cycle true then false for every DMA transfer in this mode, Normal mode is sometimes referred to as Single Transfer mode.

- **Single Transfer Mode***:* DREQ goes true and stays true as long as the FIFO is able to transfer data. DACK/ cycles true then false for every transfer.
- **Multiple DMA Transfers per DREQ***:* In the Multiplexed Bus Configuration mode, DREQ is deasserted after the trailing edge of DBWR/ or DBRD/. DACK/ remains asserted throughout multiple transfers. In the Nonmultiplexed Bus Configuration mode, DREQ is deasserted after the trailing edge of DACK/ of the next-to-last DMA transfer. In the Nonmultiplexed Bus Configuration mode, DACK/ toggles for each DMA read cycle.

2.5.4.2 DMA Read

When DMA Burst mode is enabled, the method by which DMA read data is transferred to the system bus depends on the bus configuration mode. The DMA read data is enabled onto the DB bus by DACK/ and either the RD/ or DBRD/ input signal, as follows.

- **Multiplexed Bus Configuration Mode**: Data is enabled when both DBRD/ and DACK/ are true. For multiple DMA transfers, DACK/ remains asserted throughout the multiple transfers and DBRD/ toggles for each transfer.
- **Nonmultiplexed Bus Configuration Mode**: Data is enabled when DACK/ is true. DACK/ toggles for each DMA transfer.

2.5.4.3 DMA Write

In DMA Burst mode, the functionality of DACK/ and DBWR/ is unchanged for single DMA transfers per DREQ. For multiple DMA transfers per DREQ, DACK/ remains asserted throughout the multiple transfers and DBWR/ toggles for each transfer.

Figure 2.2 illustrates the DMA Burst mode, Multiplexed mode and Nonmultiplexed mode writes.

Figure 2.2 DMA Burst Mode (Multiplexed Mode and Nonmultiplexed Mode Writes)

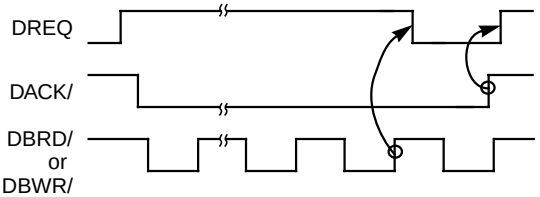
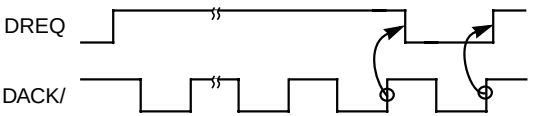


Figure 2.3 illustrates the DMA Burst mode, Nonmultiplexed mode reads.

Figure 2.3 DMA Burst Mode (Nonmultiplexed Mode Reads)



2.5.5 Single-Pin, SE SCSI

The LSI53CF92A improves fast, SE SCSI performance by reducing capacitance of the SCSI input and output signals. Single pin SCSI provides the best performance for fast, SE SCSI, and reduces signal attenuation at SCSI-1 transfer rates.

2.6 SCSI Data Transfer Rates

Performance numbers for the FSC are based on SE connection to the SCSI bus with no external transceivers.

2.6.1 Asynchronous Operation

The asynchronous transmission rate varies with cable length and the CLK period. The FSC can reach sustained transfer rates of 5 Mbytes/s on short (1 foot) cables using typical devices operating at or near nominal voltage and temperature. The typical transfer rate on a 6-meter cable is 4 Mbytes/s using two typical FSCs talking to each other. The worst case asynchronous transmission rate, over voltage, temperature, and process variations is 3 Mbytes/s on a maximum length (6 meters), SE cable and 4 Mbytes/s on a 1-foot cable.

The asynchronous transmission rate is only slightly affected by the CLK frequency when sending data. The FSC drives the data bus for a minimum of one CLK period (plus any additional time required to meet the ANSI required 55 ns setup time) before asserting REQ/ or ACK/. The CLK frequency does not affect the asynchronous transfer rate when receiving data. When the Enable Active Negation bit is set, Configuration 4 (Config 4) bit 2, the LSI53CF92A can transfer data asynchronously at up to 5 Mbytes/s.

2.6.2 Synchronous Operation

The synchronous data transmission period is equal to the CLK input frequency multiplied by the encoded value in the Synchronous Transfer Period register. Sustained synchronous transfer rates of 10 Mbytes/s are attainable across the commercial voltage and temperature range.

The LSI53CF92A can transfer synchronous SCSI data in both initiator and target modes at transfer rates up to 10 Mbytes/s, using an input clock frequency of 40 MHz. The SCSI-1 and Fast SCSI-2 minimum timing requirements are in Table 2.2.

Table 2.2 Minimum Timing Requirements

Mode	Setup	Hold	Assert/Negate
SCSI-1	55 ns	100 ns	90 ns
SE Fast SCSI-2	25 ns	35 ns	30 ns

To support maximum Fast SCSI transfer rates and SCSI-1 transfer requirements, the FASTSCSI (bit 4) and FASTCLK (bit 3) bits have been added to the Configuration 3 (Config 3) register. They modify the SCSI state machine to provide fast and normal synchronous timings depending upon the clock frequency. A full description of the operations of these bits and the required clock frequencies are provided in the Configuration 3 (Config 3) register description in Chapter 4, “Registers.”

During synchronous SCSI transfers, the assertion and deassertion of the REQ/ and ACK/ signals is programmable using the FASTCLK bit and other bits in the Synchronous Offset register. The input clock duty cycle affects the half clock assertion/deassertion delays. For more information, see the Synchronous Offset register description in Chapter 4, “Registers.”

2.7 Chip Reset

The FSC has the following three levels of reset:

- Hard
- Soft
- Disconnect

2.7.1 Hard Reset

A hard reset is executed, when using the Reset Chip command, or when the RESET pin is asserted by external hardware. It stops all chip operations, resets all functions in the chip, and returns the chip to a disconnected state. The Reset Chip command remains at the top of the Command register FIFO, which locks the chip and all registers in a reset state until a NOP command is issued. At power up, the RESET pin must be asserted as V_{DD} first becomes stable.

2.7.2 Soft Reset

A soft reset is applied when the SCSI Bus reset condition is received through the RST/ pin, or when the Reset SCSI Bus command is issued, which asserts the RST/ pin. This condition resets the following subset of the functions reset by the hard reset:

- Resets DMA interface
- Resets bus-initiated selection/reselection module
- Resets command sequence module
- Resets Sequence Step and clears Sequencer Mode bits (Enable Select/Reselect = 0, Target = 0, Initiator = 0)
- Initializes Command register FIFO to empty
- Releases all SCSI signals except RST/
- Resets disconnect, initiator, and target command modules

The Reset SCSI Bus command causes the RST/ signal to be asserted. See Chapter 5, “Command Set,” for further description of this command.

A SCSI Bus reset may occur in any mode. The RST/ signal is asserted by another SCSI device on the bus, and returns the chip to a disconnected state. The chip generates a SCSI Reset interrupt to the microprocessor if the interrupt is not disabled by bit 6 of the Configuration 1 (Config 1) register. If the SCSI bus reset is still active when the microprocessor clears the interrupt, a new interrupt is generated. This new interrupt must be serviced.

The Reset SCSI Bus command asserts the SCSI RST/ pin for approximately 25 µs and returns the chip to disconnected status. A SCSI reset interrupt is generated if the interrupt is not disabled by Bit 6 of the Configuration 1 (Config 1) register.

2.7.3 Disconnect Reset

The disconnect reset is caused by various circumstances that result in the chip becoming disconnected from the SCSI bus, as follows:

- The Target Mode Disconnect, Disconnect Sequence, or Terminate Sequence command is issued to the chip.
- The chip is in initiator mode and the SCSI bus changes to the bus free state.
- The Select or Reselect command terminates with a selection time-out.

A disconnect reset resets the following subset of the functions reset by the Soft Reset:

- Sequencer Mode bits are cleared (target = 0 and initiator = 0).
- Initializes Command register FIFO to empty.
- Releases all SCSI signals except RST/.
- Resets disconnect, initiator, and target command modules.

2.8 SCAM Capabilities

This section defines how SCAM functionality is accommodated within the LSI53CF92A SCSI protocol chip. The SCAM terminology and functionality presented within this section is consistent with definitions provided within the SCAM specification X3T9.2/93-109r5. The SCAM additions to the LSI53CF92A allow the chip to be a Level 1 or Level 2 SCAM Master or Slave device.

To provide SCAM functionality, SCSI interface chips must be able to control individual SCSI control and data lines and be able to disable active negation of signals. The LSI53CF92A uses hardware sequencers to control all SCSI interface activity. The general strategy for SCAM implementation in the LSI53CF92A is to provide a low-level SCSI programming mode along with hardware support for some of the SCAM operations.

2.8.1 SCSI Low-Level Programming

The LSI53CF92A design provides SCAM capability with a generic low-level SCSI programming mode. Low-level access to the SCSI bus is controlled by the Low Level bit, SCSI Control (SCONTROL) register, bit 0. When the Low Level bit is set, all SCSI bus sequences are performed using software control. Arbitration may be performed purely in software or by using the ARB bit, SCSI Control (SCONTROL) register, bit 1. See Section 2.8.2, "SCAM Operations,", for details. During low-level operation, no relational restrictions exist between SCSI signals; data bits may be driven without respect to the I/O control line, and there is no distinction between target/initiator signals.

2.8.2 SCAM Operations

The following categories describe the different SCAM operations:

- Section 2.8.2.1, "Arbitration With or Without an ID"
- Section 2.8.2.2, "SCAM Selection"
- Section 2.8.2.3, "Response to SCAM Selection"
- Section 2.8.2.4, "Response to Normal Selection"
- Section 2.8.2.5, "SCAM Protocol and Transfer Cycles"
- Section 2.8.2.6, "Limitations"

2.8.2.1 Arbitration With or Without an ID

Arbitration with or without an ID is possible through low-level control by utilizing the SCSI Output Data Latch and the ARB bit, SCSI Control (SCONTROL) register, bit 1. During arbitration, the contents of the SCSI Output Data Latch (SODL) are asserted onto the SCSI bus in a direct bit-mapped fashion. During arbitration, legal values for the SCSI Output Data Latch (SODL) are {0x01, 0x02, 0x04, 0x08, 0x10, 0x20, 0x40, 0x80}. Arbitration without an ID is accomplished by setting the SODL to {0x00} prior to the start of arbitration. The following steps should be performed by software to arbitrate for the SCSI bus in low-level mode:

Step 1. Set the Low Level bit in the SCSI Control register.

Step 2. Write bit-mapped ID (normal arbitration) or 00 (no ID) to the SCSI Output Data Latch (SODL) register.

Step 3. Set the ARB bit.

Step 4. Wait for the ARB1 status bit (normal arbitration) or the ARB4 status bit (SCAM, no ID).

Examine the bus (read SCSI Bus Data Lines (SBDL))

```
IF (any device with higher ID is present) then
another device has won arbitration
turn off ARB and Low Level
goto Step 1
ELSE
arbitration has been won
assert BSY, SEL using SOCL register
turn off ARB bit
ENDIF
```

Note: If another device wins arbitration and asserts SEL/, the FSC deasserts BSY/ and rearbitrates the next time a bus free condition is detected. The FSC continues arbitrating until either it wins (ARB1, ARB4 set and no higher IDs on the bus) or until the ARB bit is reset.

2.8.2.2 SCAM Selection

After arbitration is complete as described in Section 2.8.2.1, BSY/ and SEL/ are asserted on the bus. The following steps should be performed by software to generate a SCAM selection:

Step 1. Assert MSG/ using the SCSI Output Control Latch (SOCL) register.

Step 2. Delay at least two de-skew delays, then release BSY/ using the SCSI Output Control Latch (SOCL) register.

Step 3. Maintain SEL/ and MSG/ asserted with BSY/ released for a minimum of a SCAM selection response time, then release MSG/.

Note: The SCAM specification provides for two distinctly different SCAM selection response times; the long SCAM selection response time (250 ms), and the short SCAM selection response time (1 ms). Many Level 2 SCAM systems can accommodate the 1 ms SCAM selection response time.

Step 4. Wait until MSG/ has been released by all other devices (examine the SCSI Bus Control Lines (SBCL) register), using wired-OR glitch filtering in software.

Step 5. Assert BSY/ using the SCSI Output Data Latch (SODL) register.

Step 6. Wait two de-skew delays.

Step 7. Assert SEL/ and I/O while maintaining BSY/ asserted. At this time, if the device is a SCAM master, C/D should also be asserted.

Step 8. Assert DB6 and DB7 by first writing them in the SCSI Output Data Latch (SODL) register, then enabling their drivers with bit 2 of the SCSI Control (SCONTROL) register.

Step 9. Wait two de-skew delays.

Step 10. Release SEL/ and wait until SEL/ has been deasserted, using wired-OR glitch filtering in software.

Step 11. Release DB6 and examine the SCSI bus signals. If C/D is not asserted, then there are no SCAM master devices participating, and the slave devices release all signals. If C/D is asserted, wait for DB6 to be released by all devices, using wired-OR glitch filtering, then assert SEL/. This completes initiation of the SCAM selection protocol.

2.8.2.3 Response to SCAM Selection

When response to SCAM selection is enabled (ENSS bit set in the SCSI Control (SCONTROL) register), the FSC monitors the SCSI bus for SCAM selection attempts (SEL/ and MSG/ asserted when BSY/ released). Upon detection of a SCAM selection, the FSC responds by asserting SEL/ and MSG/, and then interrupting the processor. A SCAM selection interrupt is indicated when both bits 1 and 0 of the Interrupt register are set (normally mutually exclusive events). Following a SCAM selection interrupt, software must enter the low-level programming mode and participate in the SCAM protocol. The following minimal steps must be taken by software in preparation for and response to the SCAM selection interrupt:

Step 1. In the SCSI Control (SCONTROL) set the ENSS (bit 3) and Low Level (bit 0).

Step 2. Wait for SCAM Selection Interrupt.

Step 3. In the SCSI Output Control Latch (SOCL) set MSG (bit 2).

Step 4. In the SCSI Control (SCONTROL) register reset ENSS (bit 3).

Step 5. Release MSG/.

Step 6. Wait until MSG/ has been released by all other devices (examine the SCSI Bus Control Lines (SBCL) register), using wired-OR glitch filtering in software.

Step 7. Assert BSY/ using the SCSI Output Data Latch (SODL) register.

Step 8. Wait two de-skew delays.

Step 9. Assert SEL/ and I/O while maintaining BSY/ asserted. At this time, if the device is a SCAM master, C/D should also be asserted.

Step 10. Assert DB6 and DB7 by first writing them in the SCSI Output Data Latch (SODL) register, then enabling their drivers with bit 2 of the SCSI Control (SCONTROL) register.

Step 11. Wait two de-skew delays.

Step 12. Release SEL/ and wait until SEL/ has been deasserted, using wired-OR glitch filtering in software.

Step 13. Release DB6 and examine the SCSI bus signals. If C/D is not asserted, then there are no SCAM master devices participating, and the slave devices releases all signals. If C/D is asserted, wait for DB6 to be released by all devices, using wired-OR glitch filtering, then assert SEL/. This completes initiation of the protocol for response to SCAM selection.

2.8.2.4 Response to Normal Selection

The response to normal selection attempts is determined by the state of the ENDR bit (bit 4 in the SCSI Control (SCONTROL) register). SCAM slave devices with unconfirmed default IDs may not respond to selection until a SCAM default ID selection response time period elapses. Setting the ENDR bit causes the FSC to delay its response to selection, using the select/reselect Time-Out register to control the delay period. After the delay period elapses, the FSC responds by asserting BSY/ and continues to process the selection as described elsewhere in this technical manual. When this bit is cleared, the FSC responds to normal selection attempts as soon as it detects that it is being selected (within a SCAM-tolerant selection response time).

2.8.2.5 SCAM Protocol and Transfer Cycles

The SCAM protocol functions through a sequence of transfer cycles. During each cycle, certain devices send data to all participating SCAM devices. The actual data received is the logical-OR of the data sent by all sending devices. Each transfer cycle is fully interlocked in the same sense that asynchronous data transfers are interlocked. Completion of each step of the transfer is explicitly acknowledged, and the transfer rate adapts automatically to the speed of the nodes involved.

Transfer cycles use DB[7:5] as handshake lines and DB[4:0] as data lines. At the beginning and end of each cycle, DB7 is asserted while DB6 and DB5 are released. Each device sequences through the following steps for each transfer cycle:

Step 1. Use the SCSI Output Data Latch (SODL) register to place data on DB[4:0], if the device is sending data, and assert DB5. Use bit 2 of the SCSI Control (SCONTROL) register to drive the data onto the SCSI bus.

Step 2. Release DB7 using the SCSI Output Data Latch (SODL) register.

Step 3. Wait until DB7 is released by all other devices (examine the SCSI Bus Data Lines (SBDL) register), using wired-OR glitch filtering in software.

Step 4. Read and latch data from DB[4:0], and assert DB6.

Step 5. Release DB5.

Step 6. Wait until DB5 is released by all other devices, using wired-OR glitch filtering in software.

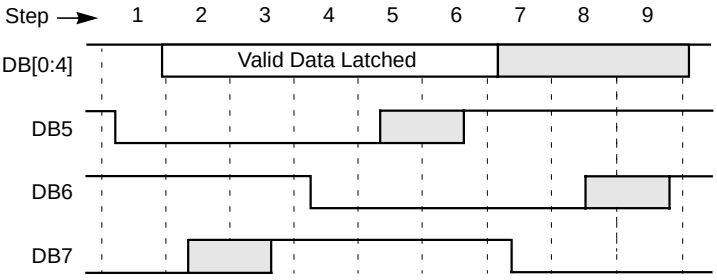
Step 7. Release or change DB[4:0], and assert DB7.

Step 8. Release DB6.

Step 9. Wait until DB6 is released by all other devices, using wired-OR glitch filtering in software.

Figure 2.4 illustrates the SCAM Transfer Cycles.

Figure 2.4 SCAM Transfer Cycles



Note: Signals are shown asserted LOW.

The SCAM protocol continues through successive transfer cycles until the master device(s) choose to terminate it by releasing C/D and all other signals. Slave devices notes the release of C/D and release all other signals.

2.8.2.6 Limitations

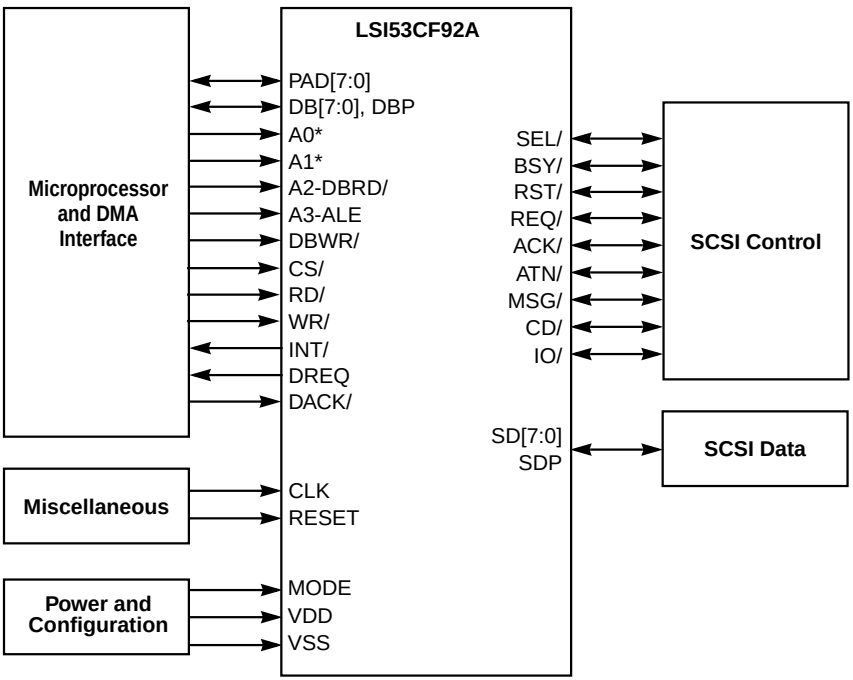
Low-level mode allows independent control of all SCSI bus signals with the following two limitations:

- The SCSI Reset signal cannot be directly controlled using low-level mode; however, the Reset SCSI Bus command may be issued during low-level mode, which asserts SCSI Reset as described in Section 2.7.2, “Soft Reset,” on page 2-16.
- The SCSI Parity signal cannot be directly controlled using low-level mode; however, when the Assert Data Bus (ADB) bit is set, the FSC generates parity for the SCSI bus using the Low Level Parity Control (LPC) bit to select even or odd parity.

Chapter 3
Signal Descriptions

This chapter contains signal descriptions and pin diagrams for the 64-pin PQFP and the 64-pin TQFP packages. A slash (/) indicates an active LOW signal; B = bidirectional signal; I = input signal; and O = output signal. Figure 3.1 is the Functional Signal Grouping and Figure 3.2 is the pin configuration for the chip.

Figure 3.1 Functional Signal Grouping



Note: * In Multiplexed mode, these two pins must be tied to VSS. See the signal description on page 3-2 for details.

Table 3.1 lists the Microprocessor and DMA Interface Signals group.

Table 3.1 Microprocessor and DMA Interface Signals

Name	Bump	Type	Description
PAD[7:0]	63–60 58–55	B	Bidirectional, active HIGH processor address-data bus with internal 200 µA pull-ups. These pins allow the processor to access the internal registers of the chip at the same time the DMA bus is active. In multiplexed mode, address and data share this bus. In nonmultiplexed mode, these pins are for data only.
DB[7:0]	15–14 12–10 8-6	B	Bidirectional, active HIGH data bus with internal 200 µA pull-ups. These pins are the 8-bit DMA data bus.
DBP	16	B	Odd parity for DB[7:0].
A0 A1 A2-DBRD/ A3-ALE	49 50 52 53	I	In nonmultiplexed mode, these TTL-compatible inputs are address bits [3:0]. In multiplexed mode, they become A0, A1, DBRD/, and ALE. The address on the PAD bus is internally latched when ALE switches from HIGH to LOW. DBRD/ is the read signal for the DB bus. Also, in multiplexed mode, A1 and A0 must be tied to V_{SS} to transfer data on DB[7:0].
DBWR/	4	I	Active LOW, DMA write signal which strobes DB[7:0] data into the FIFO when DACK/ is true.
CS/	47	I	Active LOW chip select. This TTL-compatible input enables eight-bit access to internal registers during read or write. CS/ uses the address inputs to access any register (including the FIFO) while DACK/ accesses only the FIFO. CS/ and DACK/ may both be true at the same time, provided that CS/ is not accessing the FIFO.
RD/	46	I	Active LOW register read signal. This TTL-compatible input allows internal registers to drive the data bus when CS/ is also true.

Table 3.1 Microprocessor and DMA Interface Signals (Cont.)

Name	Bump	Type	Description
WR/	45	I	Active LOW register write signal. This TTL-compatible input causes the FSC to write data into its internal registers when CS/ is also true.
INT/	42	O	Active LOW, open drain interrupt signal to the microprocessor. It is asserted on the rising edge of CLK. It may be cleared by reading the interrupt register, by a host hardware reset, or the Reset command (but not by a SCSI reset). This output cannot be masked by the user. An external pull-up is required. See Figure B.1 for details.
DREQ	2	O	3-state, active HIGH DMA request signal to the DMA controller. DREQ remains true as long as the FIFO either: • contains at least one byte to send to memory DMA read, • has room for one more byte during DMA write. If Threshold Eight mode is enabled, DREQ is not asserted until the FIFO can accommodate an eight-byte transfer. When the TESTIN/ pin is enabled, DREQ is the output of the “AND” tree (see the TESTIN/ pin description on page 3-5).
DACK/	3	I	Active LOW DMA acknowledge from the DMA controller. DACK/ accesses the FIFO only, while CS/ accesses any register, including the FIFO.
CLK	48	I	Square wave clock input that generates internal chip timing. The maximum frequency is 40 MHz. The minimum frequency for asynchronous SCSI is 10 MHz. The minimum frequency for synchronous SCSI is 12 MHz. The synchronous transmission period is equal to the CLK period multiplied by the value in the synchronous transfer period register. The asynchronous transmission rate is indirectly affected by the CLK period.
RESET	44	I	Active HIGH chip reset. Reset must be asserted for at least two CLK periods after the voltage on the power pins has reached minimum VDD.

Table 3.2 lists the SCSI Signals group.

Table 3.2 SCSI Signals

Name	Bump	Type	Description
SD[7:0] SDP	27, 25–22, 20–18 28	B	48 mA, SCSI data/parity output bus. These pins are active LOW SCSI data signals. These signals are actively deasserted when Active Negation is enabled and the chip is active on the SCSI bus; otherwise, these are open drain SCSI outputs.
SEL/, BSY/, RST/	35 30 33	B	48 mA, open drain SCSI I/Os, active LOW. The Reset SCSI Bus command that causes the FSC to drive RST/ true for 25–40 µs, depending on the CLK frequency and clock conversion factor.
REQ/	38	B	48 mA, SCSI I/O. Asserted only in target mode. This signal is actively deasserted when Active Negation is enabled and the chip is active as a target on the SCSI bus; otherwise, this is an open drain SCSI output.
ACK/	32	B	48 mA, SCSI I/O. Driven by the FSC in initiator mode only. This signal is actively deasserted when Active Negation is enabled and the chip is active as an initiator on the SCSI bus; otherwise, this is an open drain SCSI output.
ATN/	29	B	48 mA, open drain output, Schmitt trigger input. In initiator mode it is an output, and is automatically asserted when the FSC detects an incoming parity error, or may be asserted by certain FSC commands. In target mode, this signal is an input.
MSG/, CD/, IO/	34 37 39	B	SCSI phase signals. They are 48 mA outputs in target mode, and Schmitt trigger inputs in initiator mode.

Table 3.3 lists the Configuration and Test Signals group.

Table 3.3 Configuration and Test Signals

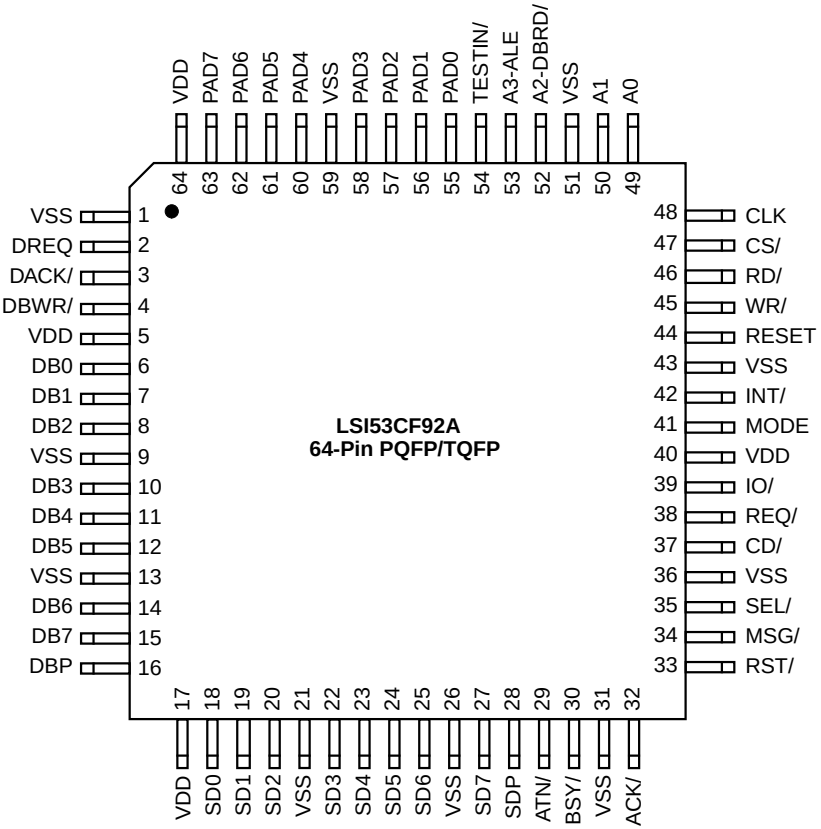
Name	Bump	Type	Description
MODE	41	I	This TTL-compatible input pin configures the PAD bus and the address control bus (A3-ALE, A2-DBRD/, A1, A0) for multiplexed bus operation when LOW, and for nonmultiplexed bus operation when HIGH.
TESTIN/	54	I	Test In. When this pin is driven LOW, the LSI53CF92A connects all inputs and outputs to an “AND” tree. The SCSI control signals and data lines are not connected to the “AND” tree. The output of the “AND” tree is connected to the DREQ pin. This allows the user to verify chip connectivity to the board and to determine exactly which pins are not properly attached. When the TESTIN/ input is driven LOW, internal pull-ups are enabled on all input, output, and bidirectional pins, all output and bidirectional signals are high impedance, and the DREQ pin is enabled. Connectivity can be tested by driving one of the LSI53CF92A pins LOW. The DREQ pin should respond by driving LOW.

Table 3.4 lists the Power and Ground Signals group.

Table 3.4 Power and Ground Signals

Name	Bump	Description
VDD-core	5, 40	+5 V power input.
VDD-DB and SCSI	17	N/A
VDD-PAD	64	N/A
VSS-core	1, 43, 51	Ground. LSI Logic recommends using a ground plane.
VSS-SCSI	21, 26, 31, 36	N/A
VSS-DB	9, 13	N/A
VSS-PAD	59	N/A

Figure 3.2 LSI53CF92A 64-Pin Plastic QFP and Thin QFP Pin Configuration[1]



1. See Figure 6.27 and Figure 6.28.

Chapter 4
Registers

This chapter contains descriptions of all FSC registers. A register map is provided in Appendix A, “Register Map.” All register values are given in hexadecimal. The terms set and assert refer to bits that are programmed to binary one. Similarly, the terms reset, clear, or deassert refer to bits that are programmed to binary zero. Some FSC registers have different meanings during reads than writes. When CS/ is true, the register being accessed is determined by either RD/ or WR/ together with the address pins A[3:0] and the state of the Register Bank Select bit (bit 3 in the Configuration 4 (Config 4) register). The FIFO may be accessed using either CS/ or DACK/ together with RD/ or WR/. Address pins A[3:0] are ignored when DACK/ is active, but must be driven when CS/ is active. The FSC registers must not be read while they are in transition, especially the FIFO, FIFO Flags, and Transfer Counter registers.

This chapter contains the following sections:

- Section 4.1, “Standard Register Set”
- Section 4.2, “SCAM Register Set”

Reserved bits should be masked when read. All register bits in the LSI53CF92A are cleared to zero after a hard reset, except as noted in Table 4.1. The shaded area in Table 4.2 contains the SCAM register set.

Table 4.1 Register Reset Values

Register	Bit(s)	Reset Value
Transfer Count	All	Indeterminate
Transfer Counter High/ID Register	All	10010100
Destination Bus ID	[2:0]	Indeterminate
Status	[2:0]	Indeterminate
Clock Conversion Factor	[2:0]	010
Synchronous Transfer Period	[4:0]	00101

Table 4.2 Register Set

Register Address	Configuration Register 4, Bit 3 = 0		Configuration Register 4, Bit 3 = 1	
	Register Bank 0 Read	Register Bank 0 Write	Register Bank 1 Read	Register Bank 1 Write
0x00	Transfer Counter Low	Transfer Counter Low	Transfer Counter Low	Transfer Counter Low
0x01	Transfer Counter Middle	Transfer Counter Middle	Transfer Counter Middle	Transfer Counter Middle
0x02	FIFO	FIFO	FIFO	FIFO
0x03	Command	Command	Command	Command
0x04	Status	Destination Bus ID	Status	Destination Bus ID
0x05	Interrupt	Time-Out	Interrupt	Time-Out
0x06	Sequence Step	Synchronous Transfer Period	Sequence Step	Synchronous Transfer Period
0x07	FIFO Flags	Synchronous Offset	FIFO Flags	Synchronous Offset
0x08	Configuration 1 (Config 1)	Configuration 1 (Config 1)	SCSI Control (SCONTROL)	SCSI Control (SCONTROL)
0x09	Reserved	Clock Conversion	SCSI Status (SSTATUS)	Reserved
0x0A	Reserved	Test	SCSI Output Control Latch (SOCL)	SCSI Output Control Latch (SOCL)
0x0B	Configuration 2 (Config 2)	Configuration 2 (Config 2)	SCSI Bus Control Lines (SBCL)	Reserved
0x0C	Configuration 3 (Config 3)	Configuration 3 (Config 3)	Reserved	Reserved
0x0D	Configuration 4 (Config 4)	Configuration 4 (Config 4)	Configuration 4 (Config 4)	Configuration 4 (Config 4)
0x0E	Transfer Counter High/ID	Transfer Counter High/ID	SCSI Output Data Latch (SODL)	SCSI Output Data Latch (SODL)
0x0F	Reserved	Reserved	SCSI Bus Data Lines (SBDL)	Reserved

4.1 Standard Register Set

The Standard Register Set can be accessed when CS/ is true. The specific register being accessed is determined by the states of the RD/ and WR/ signals together with the address pins A[3:0]. The state of bit 3 of Configuration 4 (Config 4) selects between two banks of registers. Registers 0x00 through 0x07 of the Standard Register Set are accessible with either register bank setting. Registers 0x08 through 0x0F of the Standard Register Set are accessible when bank 0 is selected, and the SCAM Register Set is accessible in registers 0x08 through 0x0F when register bank 1 is selected. The complete register map, including SCAM registers, is shown in Table 4.2 on page 4-3.

Register: 0x00–0x01

Transfer Counter
Write Only

Register Bank 0 or 1

7	6	5	4	3	2	1	0
Default							
x	x	x	x	x	x	x	x

These two registers, together with the Transfer Counter High/ID register (0x0E), form a 24-bit register which stores the Transfer Count value for DMA operations. They specify the number of bytes that are to be transferred over the SCSI bus. Values written to these two registers are stored internally and loaded into the transfer count by any DMA command. These values remain unchanged while the transfer counter decrements. Thus, successive blocks of equal size may be transferred without reprogramming the count. They may be reprogrammed any time after the previous DMA operation has started, whether it has finished or not. When the Features Enable bit is clear (which disables the Transfer Counter High/ID register), a zero value in registers 00 and 01 specifies a maximum length count of 64 Kbytes. When the Features Enable bit is set, and the Transfer Counter High/ID register is enabled, zeros specify a maximum length count of 16 Mbytes. These registers are not changed by any reset. Their states are unpredictable after power-up.

Register: 0x00–0x01

Transfer Counter
Read Only

Register Bank 0 or 1

7	6	5	4	3	2	1	0
Default							
0	0	0	0	0	0	0	0

These registers combine with the Transfer Counter High/ID register (0x0E) to form a 24-bit transfer counter. A read from these addresses returns the value currently in the counter. DMA commands use the counter to terminate a transfer. When the counter decrements to zero, the Terminal Count bit in the Status register is set, indicating the current transfer is complete. Any DMA command loads the transfer count into the counter. A DMA NOP (0x80) loads the counter while the non-DMA NOP (0x00) does not.

During SCSI Data phases, the transfer counter decrements on the leading edge of the following:

- Target Decremented by
  - Data In phase DACK/ *
  - Data Out phase REQ/
- Initiator Decremented by
  - Synchronous Data In DACK/ *
  - Asynchronous Data In ACK/
  - Data Out DACK/ *
- Target Decremented by
  - Message In, Status DACK/ *
  - Message Out, Command REQ/
- Initiator Decremented by
  - Message In, Status ACK/
  - Message Out, Command DACK/ *

* In DMA Burst mode, the transfer counter decrements on the leading edge of RD/, DBRD/, DBWR/, and DACK/ as follows:

- Target Decremented by
  - Data In phase
    - ◊ DMA Write, Multiplex Bus Mode DBWR/
    - ◊ DMA Write, Nonmultiplex Bus Mode DACK/
- Initiator Decremented by
  - Synchronous Data In
    - ◊ DMA Read, Multiplex Bus Mode DBRD/
    - ◊ DMA Read, Nonmultiplex Bus Mode DACK/
  - Data Out
    - ◊ DMA Write, Multiplex Bus Mode DBWR/
    - ◊ DMA Write, Nonmultiplex Bus Mode DACK/

Note: DACK/ can decrement the counter even if RD/ or WR/ do not go true. False DACK/s can cause the counter to get out of sync with the data stream, leading to subtle errors that are difficult to trace. When false DACK/s are expected to interfere with a temporarily suspended DMA operation, the DREQ HIGH-Z bit in Configuration 2 (Config 2) should be set while the DMA is suspended.

With two exceptions, non-DMA commands do not use the counter. During bus-initiated selection and during the Target Receive Command sequence, the FSC decodes the group code field of the Command Descriptor Block (CDB), loads the counter with the number of bytes in the CDB, then decrements once for every byte received.

Register: 0x02
FIFO
Read/Write

Register Bank 0 or 1

7	6	5	4	3	2	1	0
Default							
0	0	0	0	0	0	0	0

This register is a 16-by-9-bit, First-In-First-Out buffer between the SCSI bus and memory. Read Chapter 2, “Functional Description,” to understand its use during SCSI transactions.

The SCSI bus may transfer 8- or 9-bit bytes to the FIFO, depending on the parity control bit settings (refer to Table 2.1 on page 2-7 for details). The microprocessor may transfer 8-bit bytes to or from the FIFO using CS/ and RD/ or WR/, and the address bits. An external DMA controller may transfer 8 or 9-bit bytes to the FIFO using DACK/ and RD/ or WR/. When accessed by CS/, the address bits must be valid. When accessed by DACK/, the address bits are ignored.

The bottom FIFO element and the FIFO flags are initialized to zero after hardware reset, Chip Reset command, or Flush FIFO command and at the beginning of bus-initiated selection or reselection. The contents of the rest of the FIFO are not changed by any reset but when the flags are zero, successive FIFO reads access the bottom register. This register changes during any DMA or SCSI bus activity. The default value of this register is 0x00.

Register: 0x03
Command
Read/Write

Register Bank 0 or 1

7	6						0
ENDMA	Command Code (CC)						
Default							
0	0	0	0	0	0	0	0

This register is a two-deep, 8-bit read/write register that gives commands to the FSC. Up to two commands may be stacked in the Command register. The second command may be written before the FSC completes (or even starts) the first. Reset Chip, Reset SCSI Bus, set Attention Immediate, and Target Stop DMA execute immediately (within four cycles of being loaded); all others wait for the previous command to complete. The last executed (or executing) command remains in the Command register and may be read by the microprocessor. Reading the Command register has no effect on its contents. The internal sequencer maintains a working copy of the bottom of the command FIFO. Certain conditions cause the working copy to be cleared, allowing the next command to fall through into the sequencer. If an interrupt was pending prior to these conditions occurring, the command sequencer remains reset until the Interrupt register is read. These conditions are as follows:

- Hardware reset
- Software reset
- SCSI bus reset
- SCSI bus disconnect
- Bus-initiated selection or reselection
- Select command
- Reconnect command if ATN/ is set
- Select or Reselect time-out
- Target Terminate command
- Parity error detected in target mode
- Assertion of ATN/ in target mode

- Any phase change in initiator mode (except when issuing a sequence command)
- Illegal command

Notes:

- Non-DMA Send commands should not be stacked.
- Commands that transfer data in one direction should not be stacked with commands that transfer data in the opposite direction.
- After a hardware reset or Reset Chip command, a NOP is required to fill the Command register.

If two commands are placed in the command register, two interrupts may result. If the first interrupt is not serviced before the second finishes, the second interrupt is placed behind the first. The first interrupt must be serviced before issuing a third command. When the Interrupt register is read by the host to service the first interrupt, the contents of the Status register, Sequence Step register, and Interrupt register change to describe the second interrupt. When using stacked commands, the Features Enable bit (Configuration 2 (Config 2), bit 6) should be set to latch the SCSI phase bit in the Status register at the completion of each stacked command.

ENDMA **Enable DMA** **7**

When bit 7 is set, the command is a DMA instruction. When it is not set, the command is a non-DMA instruction. DMA instructions load the internal byte counter with the value in the Transfer Count register, without changing the count register. If the transfer terminates prematurely, the bits in the Status, Sequence Step, and Interrupt registers indicate why.

CC **Command Code** **[6:0]**

The FSC commands are shown in Table 5.1. Bits 6, 5, and 4 specify a mode group, as shown in the following illustration. Commands from the miscellaneous group may be issued at any time. Commands from the disconnected target or initiator groups are only accepted by the FSC if it is in the same mode as the command when it falls to the bottom of the command FIFO. Otherwise, an illegal command interrupt is generated. For example, after a hardware or software reset, the FSC is in the

disconnected state. A command from either the target group or the initiator group causes an Illegal Command interrupt. An Enable Selection/Reselection command by itself does not change modes. However, if another SCSI device then selects the FSC, it is in the target state; if another device reselects the FSC, it is then in the initiator state. Similarly, any select command places the FSC in Initiator mode, while the Reselect Sequence command places the FSC in Target mode.

Bits			
6	**5**	**4**	**Command Mode**
0	0	0	Miscellaneous
0	0	1	Initiator
0	1	0	Target
1	0	0	Disconnected State

Register: 0x04

Status

Read Only

Register Bank 0 or 1

7	6	5	4	3	2	1	0
INT	GE	PE	TC	VOC	MSG	C/D	I/O
Default							
0	0	0	0	0	x	x	x

This register contains important flags that indicate certain events have occurred. Bits [7:3] are latched until the interrupt register is read, and are reset by a hard reset, but not by a SCSI reset. The phase bits are not normally latched. They may be latched (for stacked commands) by setting Configuration 2 (Config 2), bit 6.

INT **Interrupt** **7**

This bit is set whenever the FSC drives the INT/ output true. It may be polled. It is buffered from the actual output so that in wired-OR (shared interrupt) designs, this bit indicates whether the FSC is attempting to interrupt the microprocessor. Hardware reset, the Reset command, or a read from the Interrupt register releases an active INT/ signal and also clears this bit.

GE **Gross Error** **6**

This bit is set when one of the following occurs:

- The top of the FIFO is overwritten
- The top of the Command register has been overwritten
- Direction of DMA transfer is opposite to the direction of the SCSI transfer
- An unexpected phase change in initiator role during Synchronous Data phase when the offset has not been reconciled

These conditions do not cause an interrupt; a gross error may be detected only while servicing another interrupt. This bit is cleared by reading the interrupt register if the interrupt output is asserted. It is also cleared by a hardware reset or the Reset command, but not SCSI reset.

PE **Parity Error** **5**

This bit is set if parity checking is enabled in the Configuration 1 (Config 1) register and the FSC detects a SCSI parity error on command, data, status or message bytes. Detected parity errors do not cause an interrupt; they are merely reported with other interrupt-causing events. If a parity error is detected during an initiator Information In phase, ATN/ is automatically asserted on the SCSI bus.

This bit is cleared by reading the Interrupt register if the interrupt output is asserted. Hardware reset or the Reset Chip command clears this bit, but not SCSI reset.

TC **Terminal Count** **4**

This bit is set when the transfer counter decrements to zero. It is not set by loading a zero into the Transfer Counter register, but resets when the transfer count is loaded. Because a DMA NOP (0x80) command loads the Transfer Counter, it also clears this bit. A non-DMA NOP (00) does not load the counter and does not clear this bit. Reading the Interrupt register does not clear this bit. Hardware reset or the Reset Chip command clears it, but SCSI reset does not.

VOC **Valid Group Code** **3**

When the FSC is selected, this bit decodes the group code field in the first byte of the Command Descriptor Block (CDB). If the group code matches one defined in ANSI X3.131-1986, this bit is set. An undefined group code (designated reserved by the ANSI committee) leaves it not set. If the SCSI-2 bit is set in the Configuration 2 (Config 2) register, Group 2 commands are recognized as ten-byte commands and this bit is set. If the SCSI-2 bit is cleared, Group 2 commands are treated as reserved commands. Groups 3 and 4 are always treated as reserved commands. A reserved group command causes the FSC to request six command bytes and does not set this bit. Group 5 commands are recognized as twelve-byte commands and this bit is set. The FSC recognizes Group 6 as six-byte vendor unique commands and Group 7 as ten-byte vendor unique commands. The Valid Group Code bit is cleared by reading the Interrupt register if the interrupt output is asserted. It is also cleared by a hardware reset or the Reset Chip command, but not by a SCSI reset.

MSG, C/D, I/O

Phase Bits **[2:0]**

These bits indicate the phase on the SCSI bus. They may be latched or unlatched, depending on Configuration 2 (Config 2), bit 6.

When not latched, they indicate the phase at the time the Status register was read. In keeping with the ANSI definition of the phase signals, these bits must be stable during any Status register read that follows an interrupt generated by the FSC.

The phase bits may be latched to permit stacking FSC commands. When the latch is enabled, the SCSI phase is latched upon command completion. These values are

latched only if the Features Enable bit (bit 6) is set in the Configuration 2 (Config 2) register. The transparent latch is reopened when the Interrupt register is read.

Bits			
2	**1**	**0**	**SCSI Bus Phase**
0	0	0	Data Out
0	0	1	Data In
0	1	0	Command
0	1	1	Status
1	0	0	Reserved
1	0	1	Reserved
1	1	0	Message Out
1	1	1	Message In

Register: 0x04

Destination Bus ID
Write Only

Register Bank 0 or 1

7					3	2	1	0
R						ID2	ID1	ID0
Default								
x	x	x	x	x		x	x	x

The least significant three bits of this register specify the encoded destination bus ID for a selection or reselection command. These bits are binary encoded, with 000 0111 representing device ID 7, which appears as 0x80 on the SCSI bus. The most significant five bits are reserved. The destination ID is not changed by any reset; the states of these bits are unpredictable after power-up.

Register: 0x05
Interrupt
Read Only

Register Bank 0 or 1

7	6	5	4	3	2	1	0
SRST	ILCMD	DIS	BS	FC	RESEL	SI	
Default							
0	0	0	0	0	0	0	0

This 8-bit register is used in conjunction with the Status register and Sequence Step register to determine the cause of an interrupt. Reading this register when the interrupt output is true clears all three registers. The entire Interrupt register is cleared (0x00) by a hardware reset or the Reset command, but not SCSI reset. The default value of this register is 0x00.

Note: This register should only be read when an interrupt is pending. The Sequence Step and Status registers should be read prior to reading this register.

SRST **SCSI Reset Detected** **7**
This bit is set if SCSI Reset Reporting is enabled in the Configuration 1 (Config 1) register and the chip detects a reset on the SCSI bus.

ILCMD **Illegal Command** **6**
This bit is set when a reserved code is placed in the Command register or when the command is from a mode group different than the mode the FSC is currently in. Refer to the Command register definition. An interrupt is generated when this bit is set.

DIS **Disconnect** **5**
In initiator mode, this bit is set when the target disconnects or a Selection or Reselection time-out occurs. When the FSC is in target mode, this bit is set if a Terminate Sequence or Command Complete Sequence command causes the FSC to disconnect from the bus.

BS **Bus Service** **4**

This bit indicates that another device is requesting service. In target mode, it is set whenever the initiator asserts ATN/ (Attention). In initiator mode, it is set whenever the target is requesting an Information Transfer phase.

FC **Function Complete** **3**

This bit is set after any target mode command has completed. In initiator mode, it is set after a target has been selected (before transferring any command phase bytes), after Command Complete finishes, or after a Transfer Information command when the target is requesting Message In phase.

RESEL **Reselected** **2**

This bit is set during Reselection phase to indicate that the FSC has been reselected as an initiator.

SI **Selection Interrupt** **[1:0]**

These two bits distinguish and report three different types of selections as follows:

Bit 1	Bit 0	Indication
0	0	No selection interrupt
0	1	Selected without ATN/; FSC has been selected as a Target with ATN/ false
1	0	Selected with ATN/; FSC has been selected as a Target with ATN/ true
1	1	SCAM selection. FSC has detected a SCAM selection

Register: 0x05
Time-Out
Write Only

Register Bank 0 or 1

7	6	5	4	3	2	1	0
Default							
x	x	x	x	x	x	x	x

Under normal operation [when the Enable Delayed Response to Selection (ENDR) bit, bit 4 of the SCSI Control (SCONTROL) register, is cleared], this 8-bit, write only register specifies the amount of time the FSC waits for a response during selection or reselection. (The FSC has no way to time-out if it never wins arbitration; it keeps trying indefinitely until it wins.) The Time-Out register is normally loaded to specify a time-out period of 250 ms to comply with the ANSI standard.

When ENDR is set, the FSC delays its response to selection based on the value of this register. In either case, the register value (RV) may be calculated from:

$$RV = \frac{\text{(time-out period) (CLK frequency)}}{8192\ \text{(clock conversion factor)}}$$

For example, at 40 MHz, the register value that gives a 250 ms time-out period is 153 decimal or 0x99. The clock conversion factor is defined in the description of write address 0x09. To compute the register value using this formula when the clock conversion factor is zero, use eight, the number of clocks, rather than zero. The Time-Out register remains unchanged by any reset, and the states of these bits are unpredictable after power-up.

Register: 0x06
Sequence Step
Read Only

Register Bank 0 or 1

7			4	3	2		0
R				SOM	SS[2:0]		
Default							
1	1	0	0	0	0	0	0

The lower three bits of this register indicate how far the internal sequencer was able to proceed in executing a sequenced command. This counter is incremented at certain points in sequenced commands to aid in error recovery if the command does not complete normally. This register is cleared by a hard reset, SCSI reset, and by reading the Interrupt register when an interrupt is pending.

R **Reserved** **[7:4]**

SOM **Synchronous Offset Max** **3**
This bit is zero for asynchronous data transfers. For synchronous transfers, this bit is set. When this bit is clear, the synchronous offset counter has reached its maximum value.

SS[2:0] **Sequence Step** **[2:0]**
The sequence step counter is set to zero at the beginning of certain commands. The counter is then incremented at specific points in the various algorithms to aid in error recovery. The possible states are described in Chapter 5, “Command Set.”

Register: 0x06

Synchronous Transfer Period
Write Only

Register Bank 0 or 1

7		5	4	3	2	1	0
R			Clocks Per Byte				
Default							
0	0	0	0	0	1	0	1

Bits [4:0] of this register specify the minimum time between leading edges of successive REQ/ (Request) or ACK/ (Acknowledge) pulses. Synchronous data is transmitted or received at the rate of one byte every “n” Clocks (CLK). The variable “n” is related to the register value and the data transfer rate as shown in Table 4.3 and Table 4.4.

Table 4.3 Transfer Rate with 40 MHz Clock (FASTCLK Bit Set)

FAST SCSI Bit Value	Register Value	Clocks per Byte	Transfer Rate (Mbytes/s)
1	0x4	4	10.0
1	0x5	5	8.0
1	0x6	6	6.6
1	0x7	7	5.7
x	0x8	8	5.0
0	0x9	9	4.4
0	0xA	10	4.0
0	0xB	11	3.6
0	0xC	12	3.3
0	0xD	13	3.0
0	0xE	14	2.8
0	0xF	15	2.6
0	0x10	16	2.5
0	0x11	17	2.3
0	0x12	18	2.2
0	0x13	19	2.1
0	0x14	20	2.0

Table 4.4 Transfer Rate with 25 MHz Clock (FASTCLK Bit Clear)

FAST SCSI Bit Value	Register Value	Clocks per Byte	Transfer Rate (Mbytes/s)
0	0x5	5	5.0
0	0x6	6	4.2
0	0x7	7	3.6
0	0x8	8	3.1
0	0x9	9	2.8
0	0xA	10	2.5
0	0xB	11	2.3
0	0xC	12	2.1
0	0xD	13	1.9

The upper three bits are reserved by LSI Logic. This register defaults to 0x55 after hardware reset or the Reset Chip command (but not SCSI reset). Refer to the descriptions for the FASTCLK and FASTSCSI bits, Configuration 3 (Config 3), bits 3 and 4, for information on Fast SCSI operation.

Note: Any combination not listed in the above tables violates ANSI standards, and should not be used.

Register: 0x07
FIFO Flags
Read Only

Register Bank 0 or 1

7	6	5	4	3	2	1	0
SS2	SS1	SS0	FF4	FF3	FF2	FF1	FF0
Default							
0	0	0	0	0	0	0	0

The least significant five bits of this register indicate how many bytes are currently in the FIFO. The value is binary encoded. The flags should not be polled while transferring data because they are not stable while the SCSI interface is changing the contents of the FIFO.

The upper three bits are duplicates of the Sequence Step register bits in normal mode. If Test Mode is enabled, bit 5 is set to indicate that the offset counter is not zero. Not zero means that synchronous data may continue to be transferred. Zero means that the synchronous offset count has expired, and the FSC does not transfer any more data until it receives an acknowledge.

Register: 0x07
Synchronous Offset
Write Only

Register Bank 0 or 1

7	6	5	4	3	2	1	0
Deassertion Delay		Assertion Delay		Synchronous/Asynchronous			
0	0	0	0	0	0	0	0

Bits [7:6] of this register control when the REQ/ and ACK/ signals deassert by selecting one of four input clock edges. These bits only affect a Synchronous Data In or Synchronous Data Out phase. The control over deassertion of these signals is measured in input clock cycles and is dependent on the status of the FASTCLK bit, Configuration 3 (Config 3), bit 3, as shown in Table 4.5.

Table 4.5 REQ/ ACK/ Deassertion Delay Selection

FASTCLK Status	Synchronous Offset Register Bits [7:6]	REQ/ ACK/ Deassertion Delay (Input Clock Cycles)
1	00	No Delay (Default)
1	01	1/2 Clock
1	10	1 Clock
1	11	1 1/2 Clocks
0	00	No Delay
0	01	1/2 Clock Early
0	10	1 Clock
0	11	1/2 Clock

Bits 5 and 4 control when REQ/ or ACK/ asserts by selecting one of four input clock edges. Assertion of the REQ/ and ACK/ signals is not dependent on the FASTCLK bit. The assertion delay is shown in Table 4.6.

Table 4.6 REQ/ ACK/ Assertion Delay Selection

Synchronous Offset Register Bits [5:4]	REQ/ ACK/ Assertion Delay (In Input Clock Cycles)
00	0 (Default)
01	1/2 Clock
10	1 Clock
11	1 1/2 Clocks

The least significant four bits of this register specify whether the FSC transfers data phase bytes synchronously or asynchronously. Zero specifies asynchronous transfer. Any other value specifies the synchronous offset, the number of data phase bytes that may be sent synchronously without an acknowledge (either REQ/ or ACK/), depending on whether the FSC is in initiator or target mode.

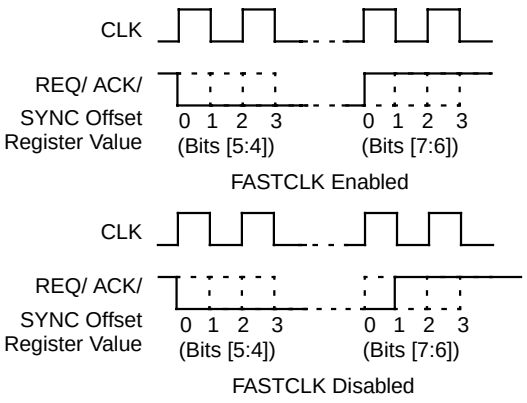
When transmitting to the SCSI bus, the FSC stops sending bytes when it reaches this offset, and thereafter sends one byte for every acknowledge it receives from the other SCSI device(s).

When receiving from the SCSI bus, the FSC sends an acknowledge every time a byte is removed from its FIFO on the DMA interface. The maximum offset of 15 allows a receiving FSC to store data in its FIFO while the external DMA controller gains control of the memory bus. The maximum offset is 15 for nonburst mode operation, and 7 for burst mode.

The synchronous offset is cleared (00) by hardware reset or a software chip reset, but not SCSI reset.

Figure 4.1 illustrates the REQ/ ACK/ deassertion delay.

Figure 4.1 REQ/ ACK/ Deassertion Delay



Note: The input clock duty cycle affects the half clock assertion/deassertion delays.

Register: 0x08
Configuration 1 (Config 1)
Read/Write

Register Bank 0

7	6	5	4	3	2		0
Slow	SRD	PTest	PChk	CTEST	MBID		
Default							
0	0	0	0	0	0	0	0

This 8-bit read/write register specifies various operating conditions for the FSC. Any bit pattern written to this register may be read back and should be identical. The default value of this register is 0x00.

Slow — **Slow Cable Mode** — **7**

Slow cable mode is needed when cabling conditions cause SCSI bus violations. It compensates for excessive capacitive loading on the SCSI data signals by inserting an extra CLK period between data being asserted on the bus and REQ/ or ACK/ being driven true. This bit is cleared (0) by hardware reset or the Reset command, but not SCSI reset.

SRD — **SCSI Reset Reporting Interrupt Disable** — **6**

This bit disables the reporting of a SCSI reset. If the SCSI reset signal goes true when this bit is set, the FSC disconnects from the SCSI bus and remains idle in the disconnected state without interrupting the host. If the bit is not set, the FSC responds to the SCSI reset by first interrupting the host. This bit is cleared by hardware reset or the Chip Reset command, but not SCSI reset.

PTest — **Parity Test Mode** — **5**

With this bit set, the parity bit equals bit 7 when unloading the FIFO to the SCSI bus and using a DMA command. For non-DMA commands, standard odd parity is generated on the SCSI bus. This allows parity errors to be created so that hardware and software may be tested. This bit must not be set during normal operation. Refer to Section 2.3, “Parity Checking and Generation,” on page 2-6. This bit is cleared by hardware reset or the Chip Reset command, but not SCSI reset.

PChk **Enable Parity Checking** **4**

When this bit is set, the FSC checks parity on SCSI bytes during any information transfer phase except when receiving pad bytes. Detected parity errors causes the Parity Error bit to be set in the Status register but does not cause an interrupt. In initiator role, bad parity on incoming SCSI bytes also sets ATN/ (Attention) on the SCSI bus. When this bit is not set, parity is not checked, the bit in the Status register is not set, and ATN/ is not asserted. Refer to Section 2.3, “Parity Checking and Generation,” on page 2-6. This bit is cleared by hardware reset or the Reset command, but not by a SCSI reset.

CTEST **Chip Test Mode Enable** **3**

When this bit is set, the chip is placed in a special test mode which enables the Test register at address 0x0A. After it has been set, the chip must be reset (hard or soft but not SCSI) before normal operation can begin. This bit should not be set during normal operation. This bit is cleared by hardware reset or the Reset command, but not SCSI reset.

MBID **My Bus ID** **[2:0]**

This bit field is the bus ID of this device. It is the ID to which the FSC responds during bus-initiated selection or reselection, and the ID that the FSC uses to arbitrate for the bus. This three-bit field is binary encoded. It is reset by hard reset but not by SCSI reset; after power-up the states of these bits are unpredictable.

Register: 0x09
Clock Conversion
Write Only

Register Bank 0

7					3	2		0
R						Clock Conversion Bits		
Default								
x	x	x	x	x		0	1	0

This register must be set according to the CLK (Clock) input frequency. All timings longer than 400 ns depend on this register correctly agreeing with the CLK frequency. The clock conversion factor is equal to the binary encoded version of the least significant three bits. It should be set to one of the seven values shown in Table 4.7.

Table 4.7 CLK Frequency vs. Clock Conversion Factor

CLK Frequency (MHz)	Clock Conversion Factor
10	0b010
10.01 to 15	0b011
15.01 to 20	0b100
20.01 to 25	0b101
25.01 to 30	0b110
30.01 to 35	0b111
35.01 to 40	0b000

Note: A Clock Conversion factor of 0b000 indicates eight clocks.

These bits must never be loaded with a binary 0b001. Hardware Reset or the Reset command sets the Clock Conversion Factor to a binary 0b010. The upper five bits of this register are reserved.

Register: 0x0A

Test
Write Only

Register Bank 0

7				3	2	1	0
R					HIGH-Z	Init	Tar
Default							
0	0	0	0	0	0	0	0

This register is enabled by setting the special test mode bit in Configuration 1 (Config 1) register at address 0x08. After test mode has been entered, a hardware reset or the Reset command must occur before normal operation can begin. These bits must not be set during normal chip operation.

R **Reserved** **[7:5]**

R **Reserved** **[4:3]**
These bits must be set to 0.

HIGH-Z **All Outputs to High Impedance** **2**
When this bit is set, all bidirectional and all output pins go to high impedance and do not significantly load a TTL or compatible device.

Init **Initiator Mode** **1**
When this bit is set, the FSC is artificially forced into initiator mode. Any initiator command is accepted by the FSC. For example, a Set ATN command causes ATN/ to be driven on the SCSI bus even if the FSC is disconnected.

Tar **Target Mode** **0**
When this bit is set, the FSC is artificially forced into target mode. Any target command is accepted by the FSC. For example, a DMA command loads or unloads the FIFO and sets the SCSI phase, Data, and REQ/ signals even if arbitration and selection have not occurred.

Register: 0x0B
Configuration 2 (Config 2)
Read/Write

Register Bank 0

7	6	5	4	3	2	1	0
R	FE	R	DHZ	SCSI2	BPA	R	DPE
Default							
0	0	0	0	0	0	0	0

After hardware reset or the Reset command, the bits in this register are all cleared, which makes the chip compatible with LSI53C90 family software. Any bit pattern written to this register may be read back and should be identical. The default value of this register is 0x20.

R **Reserved** **7**
This bit must be set to 0.

FE **Features Enable** **6**
This bit is cleared by hardware reset or the software Reset command, and is not affected by SCSI reset. When set, this bit enables all of the following features:

- The SCSI phase is latched at each command completion. This permits simpler software routines for stacked commands. When this bit is not set, the phase bits reported in the Status register are live indicators of the state of the SCSI phase lines.
- The Transfer Counter High/ID (0x0E) register is enabled, which extends the transfer counter from 16 to 24 bits. If other conditions are met, setting this bit also allows the chip revision code to be read (see the Transfer Counter High/ID register description for more information on this feature).

R **Reserved** **5**
This bit must be set to 0.

DHZ **DREQ High Impedance** **4**
When this bit is set, the DREQ output (DMA request) goes to high impedance and does not significantly load a TTL-compatible device. This is useful when several

devices share the DMA request line (known as wired-OR). When this bit is set, the FSC ignores any activity on the DACK/ (DMA acknowledge) input.

When this bit is cleared, the DREQ output is driven to TTL high or low voltages. When this bit is cleared, DACK/ is able to decrement the transfer counter and load or unload the FIFO, depending on WR/ or RD/. DACK/ should not pulse true without RD/ or WR/ because the transfer counter may decrement without transferring any data. Refer to the Transfer Counter register description.

SCSI2 **SCSI-2** **3**

Setting this bit allows the FSC to support two new features adopted in SCSI-2: the 3-byte message exchange for Tagged-Queuing and Group 2 commands. Similar features also can be set independently in the Configuration 3 (Config 3) register.

Tagged-Queuing

When this bit is set and the FSC is selected with ATN/ (Attention), it requests either one or three message bytes depending on whether ATN/ remains true or goes false. If ATN/ is still true after the first byte has been received, the FSC may request two more message bytes before switching to Command phase. If ATN/ goes false, it switches to Command phase after the first message byte. When the bit is not set, it requests a single message byte (as a target) when selected with ATN/, and aborts the selection sequence (as an initiator) if the target does not switch to Command phase after one message byte has been transferred. Refer to Section 2.2, “Bus-Initiated Sequences,” on page 2-3 for details.

Group 2 Commands

When the SCSI-2 bit is set, Group 2 commands are recognized as 10-byte commands. Receiving a Group 2 command with this bit set sets the Valid Group Code bit in the Status register. If the SCSI-2 bit is not set, the FSC treats Group 2 commands as reserved commands, it requests only six bytes in Command phase, and does not set the Valid Group Code status bit.

BPA **Target Bad Parity Abort** **2**

When this bit is set, the FSC aborts a Receive command or Receive Data Sequence command when the FSC detects a parity error.

R **Reserved** **1**

This bit should be set to 0. If this bit is set to 1, then incorrect parity may result when moving data from the FIFO to the SCSI bus.

DPE **DMA Parity Enable** **0**

When this bit is set, parity from the host DBP pins is loaded into the FIFO when DACK/ and WR/ are both true. When this bit is not set, the FSC generates parity from the host data bus when DACK/ and WR/ are both true and places it in the FIFO along with the data from which it was generated.

When the FSC is moving data from the FIFO to the SCSI bus, it flags outgoing parity errors only if this bit is set.

Register: 0x0C

Configuration 3 (Config 3)
Read/Write

Register Bank 0

7	6	5	4	3	2	1	0
IMRC	QTE	CDB10	FSCSI	FCLK	R	ADMA	T8
Default							
0	0	0	0	0	0	0	0

After a hardware reset or a software Chip Reset, the bits in this register are all cleared, which makes the chip compatible with LSI53C90 family software. Any bit pattern written to this register may be read back and should be identical, except that bit 2 remains low.

IMRC **ID Message Reserved Check** **7**

This bit allows a second level of checking for the validity of an ID message. The most significant bit of an ID Message byte is always checked, and must be one, or the chip interrupts. When this bit is set, bits [5:3] of the ID Message are also checked and must be zero, or the

chip interrupts. This check occurs if the chip is selected with ATN/ true. If the validation check fails, the selection sequence halts and the chip generates an interrupt.

QTE **Queue Tag Enable** **6**

When this bit is set, the LSI53CF92A can receive 3-byte messages during bus-initiated Select With ATN. A similar feature is also enabled by setting bit 3 in the Configuration 2 (Config 2) register. The message bytes consist of a one-byte identify message and a two-byte queue tag message. The middle byte is the tagged queue message itself and the last byte is the tag value (0 to 255). When this bit or the SCSI-2 bit is set, the second byte is checked to see if it is a valid queue tagging message. If the value of the byte is not 0x20, 0x21, or 0x22, the sequence halts and an interrupt is generated. When this bit is not set, the chip aborts the Select with ATN sequence after it receives one Identify Message byte, if ATN/ is still asserted.

CDB10 **CDB10** **5**

When this bit is set, 10-byte Group 2 commands are recognized as valid Command Descriptor Blocks (CDB). The Target command sequence receives ten Group 2 command bytes and sets the Valid Group Code bit (Status register, bit 3). When this bit and the SCSI-2 bit are not set, the Target command sequence receives only six Group 2 command bytes and does not set the Valid Group Code bit. The group code defines how many bytes are in the CDB, and determines how many bytes to request while driving Command Phase. This feature is also enabled or disabled by setting or clearing bit 3 in the Configuration 2 (Config 2) register.

FSCSI **FASTSCSI** **4**

Bits 4 and 3 of this register inform the device that it is connected to a fast clock, and to select between Fast SCSI timings and SCSI-1 timings. See Table 4.8 for transfer rates based on these bits. Also, the SCSI REQ/ and ACK/ input filtering period is determined by the state of this bit. When this bit is set, the filtering period is 30 ns. When it is reset, the period is 60 ns. See Figure 6.2 on page 6-5 for details.

FCLK **FASTCLK** **3**

Along with bit 4, this bit informs the device that it is connected to a fast clock, and to select between Fast SCSI timings and SCSI-1 timings. Fast SCSI operation requires a 40 MHz clock. A fast clock is one with a frequency greater than 25 MHz. The FASTCLK bit also controls the deassertion delay of the REQ/ and ACK/ signals. See register 0x07 Synchronous Offset, page 4-21. Bits 4 and 3 of this register affect the SCSI transfer rate as shown in Table 4.8.

Table 4.8 Synchronous Transfer Rate and Minimum Clocks/Byte

Bit 4	Bit 3	Minimum Clocks/Byte asynch	Minimum Clocks/Byte synch	Sync Transfer (Mbytes/s)
x	0	2	5	5
0	1	3	8	5
1	1	3	4	10

R **Reserved** **2**

This bit must be set to 0**.**

ADMA **Alternate DMA Mode** **1**

This bit may be set only when the Threshold Eight bit (bit 0) in this register is set. All possible combinations for using bits 1 and 0 of this register are shown in Table 4.9:

Table 4.9 DMA Modes

Bit 1	Bit 0	Function
0	0	Normal DMA Mode
0	1	Threshold Eight Mode
1	0	Reserved
1	1	DMA Burst Mode

Setting this bit modifies the DMA interface to take advantage of the demand mode using a DMA controller when the Threshold Eight bit is also set. Refer to the description for Section 2.5.4, “DMA Burst Mode,” on page 2-11 for details. When this bit is set, DMA data is strobed into or out of the FSC during DMA reads and writes as follows:

- DMA Write

  For multiple DMA writes per DREQ, DACK/ remains asserted while DBWR/ toggles for each write. The functionality of DACK/ and DREQ are unchanged for single DMA writes per DREQ.

- DMA Read

  In the Multiplexed Bus Configuration mode, during multiple DMA transfers, DACK/ remains asserted while DBRD/ toggles for each transfer. The FSC outputs data when both DACK/ and DBRD/ are true.

  In the Nonmultiplexed Bus Configuration mode, DACK/ must toggle for each DMA read. The FSC outputs data when DACK/ is true.

Note: RD/ is not used in this mode.

If the burst consists of one transfer, DREQ obeys the nonburst timings. If the burst consists of two or more transfers, DREQ obeys the Burst mode timings. If the FSC is operating as an initiator and a phase change occurs before the first DREQ has been acknowledged, DREQ obeys the nonburst timings. Otherwise, DREQ obeys the burst mode timings. Refer to Figures 2.2 and 2.3 for Burst mode timing relationships.

If less than eight bytes remain as a burst begins at the end of a transfer, the FSC switches out of Burst mode for the last one to seven bytes; these bytes are transferred in normal DMA mode.

TB **Threshold Eight** **0**

Setting this bit causes the FSC to delay assertion of DREQ (DMA Request) until it can transfer eight bytes. This higher threshold applies only to SCSI data phases. The threshold for all other SCSI phases is one byte. This bit must be set if using Alternate DMA mode.

When Threshold Eight is set, the maximum synchronous offset is limited to seven. DREQ goes true during DMA reads and writes as follows.

- DMA Write to FIFO

  DREQ is true whenever the top eight bytes of the FIFO are empty.

- DMA Read from FIFO
- End of transfer

  Target mode: DREQ is set when the transfer counter is zero or ATN/ is set.

  Initiator Synchronous Data In: DREQ is true when the transfer counter is less than eight.

  Initiator mode, not Synchronous Data In: DREQ is true when the transfer counter is zero, or after any phase change.

- Not end of transfer

  Initiator Synchronous Data In: DREQ is true if the transfer counter is greater than seven and the bottom eight bytes of the FIFO are full.

  Not Initiator Synchronous Data In: DREQ is true whenever the bottom eight bytes of the FIFO are full.

Register: 0x0D

Configuration 4 (Config 4)

Read/Write

Register Bank 0 or 1

7			4	3	2	1	0
R				RBS	EAN	R	
Default							
1	0	0	0	0	0	1	1

The reserved bits in this register are ignored on writes. This register is reset to zero on power-up or chip reset, but not on SCSI reset.

Note: This register is accessible in either Register Bank 0 or 1.

R **Reserved** **7**
This bit is set to 1 as soon as the chip is enabled.

R **Reserved** **[6:4]**
These bits remain set to 0.

RBS	**Register Bank Select** When this bit is set, access to Register Bank 1 (SCAM registers) is enabled. When this bit is clear, access to Register Bank 0 (Normal registers) is enabled.	**3**
EAN	**Enable Active Negation** When enabled, the SCSI data, parity, REQ/, and ACK/ outputs actively drive to both high and low logic levels. Refer to Section 1.3, "TolerANT® Technology," on page 1-2 for details. This bit should be set when transferring data at fast SCSI rates.	**2**
R	**Reserved** These bits remain set to 1.	**[1:0]**

Register: 0x0E

Transfer Counter High/ID
Read/Write

Register Bank 0

7				3	2		0
CFID					RL		
Default							
1	0	0	1	0	1	0	0

This register extends the Transfer Counter to 24 bits. This register is only enabled when the Features Enable bit is set. Refer to the descriptions for Registers 0x00–0x01 for additional information on the Transfer Counter.

Reading this register can also provide the chip revision code when the following conditions are met:

- A hard reset has occurred; and
- The register has not been loaded with a transfer count.

The following bit descriptions apply when the previous conditions are met.

CFID **Chip Family ID** **[7:3]**
These bits identify the chip family, and are currently fixed at 0b10010.

RL **Chip Revision Level** **[2:0]**
These bits identify the current revision level of the chip, and are currently set to 0x96.

Register: 0x0F
Reserved

Register Bank 0

7							0
R							
x	x	x	x	x	x	x	x

4.2 SCAM Register Set

To provide register structures for directly controlling and observing SCSI bus activity thus providing SCAM functionality, an additional addressing mode was created for the LSI53CF92A to allow access to the new registers. This is because the original address map for the LSI53CF92A was limited to 16 registers and only two read only addresses were available. The address map is extended to 24 locations through a bank-select mechanism whereby two sets of registers are mapped to addresses 0x08–0x0F. The control bit for selecting the SCAM Register Set is bit 3 in the Configuration 4 (Config 4) register, and is visible in either register bank. The complete register map including SCAM registers is shown in Table 4.2 and in Appendix A, “Register Map.”

Register: 0x08
SCSI Control (SCONTROL)
Read/Write

Register Bank 1

7	6	5	4	3	2	1	0
R	TOTest	LPC	ENDR	ENSS	ADB	ARB	LL
Default							
0	0	0	0	0	0	0	0

This register controls FSC actions and response in low-level mode. This register is cleared by the Reset Chip command, assertion of the RESET pin, SCSI Bus reset, or chip power-up.

R **Reserved** **7**

TOTest **Time-out Test** **6**
When this bit is set, the internal counter, which controls selection and delayed SCAM selection time-out delays, is loaded with a shorter time-out value (8 as opposed to the normal value of 480). This bit is for test purposes only and should not be used for normal chip operation.

LPC **Low Level Parity Control** **5**
During low-level SCSI programming (Low Level true), parity is generated from the contents of the SCSI Output Data Latch (SODL) register. When this bit is set, the generated parity is even. When this bit is cleared, odd parity is generated.

ENDR **Enable Delayed Response to Selection** **4**
When this bit is set, the FSC delays its response to selection based on the value programmed in the select/reselect Time-Out register. The FSC, upon detecting that it is being selected, waits for the specified time, then asserts BSY/ and continues its normal response to selection. If the initiator drops BSY/ before the delay period expires, the FSC ignores the selection attempt. This functionality allows a SCAM Master to scan the SCSI bus for SCAM tolerant (“old”) devices using short selection time-outs. Unassigned SCAM slaves do

not respond to this initial bus scan because of their delayed response. After a SCAM slave has been assigned an ID, this bit should be cleared to enable normal selection response.

ENSS **Enable SCAM Selection Response** **3**

When this bit is set, the FSC monitors the SCSI bus for SCAM selections. When the FSC detects a valid SCAM selection, it asserts SEL/ and MSG/, sets both the SEL and SATN bits in the Interrupt register, and asserts the interrupt pin.

ADB **Assert Data Bus** **2**

When set, this bit allows the contents of the SCSI Output Data Latch (SODL) register to be enabled as chip outputs. Parity is also generated and asserted onto the SCSI data bus. The Low Level Parity Control bit determines whether the generated parity is even or odd.

ARB **Arbitrate** **1**

When set, this bit starts the arbitration process when a bus-free condition has been detected. Prior to setting this bit, the SCSI Output Data Latch (SODL) register should contain the proper SCSI ID value. One SCSI ID bit should be set for normal low-level arbitration; no ID bits should be set for SCAM arbitration without an ID. The chip waits for a bus-free condition before entering the arbitration phase. The status of the arbitration phase may be determined by reading the SCSI Status register, bits [1:0].

LL **Low Level** **0**

Setting this bit places the FSC into low-level mode. In this mode, direct control of the SCSI bus is possible. SCSI bus arbitration, selection, and data transfers are performed by manually asserting and monitoring SCS bus signals. When this bit is cleared, both the SCSI Output Control Latch (SOCL) and SCSI Output Data Latch (SODL) registers are held reset. The current bus status using the SCSI Bus Control Lines (SBCL) and SCSI Bus Data Lines (SBDL) registers is available regardless of the state of this bit.

Register: 0x09
SCSI Status (SSTATUS)
Read Only

Register Bank 1

7			4	3	2	1	0
R				SDP	SRST	ARB4	ARB1
Default							
0	0	0	0	x	x	0	0

This register provides SCSI status information for use during low-level mode.

R **Reserved** **[7:4]**

SDP **SCSI Parity Status** **3**
This bit indicates the state of the SCSI data parity signal (bit set = SCSI parity asserted). This bit is not latched; it provides a true representation of what is on the SCSI bus at the time this register is read.

SRST **SCSI Reset Status** **2**
This bit indicates the state of the SCSI reset signal (bit set = SCSI reset asserted). This bit is sampled; it provides a representation of what was on the SCSI bus one synchronization delay prior to the time this register is read.

ARB4 **Arbitration Delay4** **1**
This bit is set when four arbitration delays have passed since the FSC detected bus-free and started arbitrating for the SCSI bus.

ARB1 **Arbitration Delay1** **0**
This bit is set when one arbitration delay has passed since the FSC detected bus-free and started arbitrating for the SCSI bus.

Register: 0x0A

SCSI Output Control Latch (SOCL)
Read/Write

Register Bank 1

7	6	5	4	3	2	1	0
REQ	ACK	BSY	SEL	ATN	MSG	C/D	I/O
Default							
0	0	0	0	0	0	0	0

This register provides low-level control of the SCSI bus control signals. This register is cleared by the Reset Chip command, assertion of the RESET pin, a SCSI Bus reset, chip power-up, and held reset whenever the Low Level mode bit is cleared.

REQ **(Bit set = assert SCSI REQ/)** **7**

ACK **(Bit set = assert SCSI ACK/)** **6**

BSY **(Bit set = assert SCSI BSY/)** **5**

SEL **(Bit set = assert SCSI SEL/)** **4**

ATN **(Bit set = assert SCSI ATN/)** **3**

MSG **(Bit set = assert SCSI MSG/)** **2**

C/D **(Bit set = assert SCSI C/D/)** **1**

I/O **(Bit set = assert SCSI I/O/)** **0**

Register: 0x0B

SCSI Bus Control Lines (SBCL)
Read Only

Register Bank 1

7	6	5	4	3	2	1	0
REQ	ACK	BSY	SEL	ATN	MSG	C/D	I/O
Default							
0	0	0	0	0	0	0	0

This read only register provides status of the SCSI bus control signals. These bits are sampled; they are a representation of what was on the SCSI bus one synchronization delay prior to the time this register is read.

REQ **(Bit Set = SCSI REQ/ Asserted)** **7**

ACK **(Bit Set = SCSI ACK/ Asserted)** **6**

BSY **(Bit Set = SCSI BSY/ Asserted)** **5**

SEL **(Bit Set = SCSI SEL/ Asserted)** **4**

ATN **(Bit Set = SCSI ATN/ Asserted)** **3**

MSG **(Bit Set = SCSI MSG/ Asserted)** **2**

C/D **(Bit Set = SCSI C/D/ Asserted)** **1**

I/O **(Bit Set = SCSI I/O/ Asserted)** **0**

Register: 0x0E
SCSI Output Data Latch (SODL)
Read/Write

Register Bank 1

7							0
SD7	SD6	SD5	SD4	SD3	SD2	SD1	SD0
Default							
0	0	0	0	0	0	0	0

SD[7:0] **(Bit Set = Assert SCSI Data Bit)** **[7:0]**
This register provides low-level control of the SCSI bus data signals. This register is cleared by the Reset Chip command, assertion of the RESET pin, a SCSI Bus reset, chip power-up, and held reset whenever the Low Level mode bit is cleared. The contents of this register are placed onto the SCSI bus during low-level arbitration (ARB bit set) or by setting the Assert Data Bus bit in the SCSI Control (SCONTROL) register.

Register: 0x0F
SCSI Bus Data Lines (SBDL)
Read Only

Register Bank 1

7							0
SD7	SD6	SD5	SD4	SD3	SD2	SD1	SD0
Default							
x	x	x	x	x	x	x	x

SD[7:0] **(SCSI Data Bits, Active High)** **[7:0]**
This read only register provides status of the SCSI bus data signals. These bits are not latched; they are a true representation of what is on the SCSI bus at the time this register is read.

Chapter 5
Command Set

All LSI53CF92A instructions may be issued in two forms: DMA and non-DMA. DMA commands move data between memory and the SCSI bus, while non-DMA commands move data between the FIFO and the SCSI bus. Non-DMA commands require the microprocessor to move data between the FIFO and memory. DMA commands require an external DMA controller to move data between the FIFO and memory. A command that is issued to the Command register with bit 7 of the Command register set is a DMA command. A command that is issued with bit 7 not set is a non-DMA command. DMA commands load the transfer counter with the value in the Transfer Counter register, so the Transfer Counter register must be loaded before any DMA command is issued. The word “sequence” in the command name indicates that the Sequence Step register is affected by executing the command. Check the Sequence Step register after using these commands to verify the command completed normally or to aid in data recovery if the command did not complete normally.

This chapter contains the following sections:

Table 5.1 lists the Command Set.

Table 5.1 Command Set

Non-DMA	DMA[1]	Command Register [7:0]	Command	Interrupt
		7 6 5 4 3 2 1 0	**Miscellaneous Group**	
0x00	0x80	x 0 0 0 0 0 0 0	NOP	No
0x01	–	0 0 0 0 0 0 0 1	Flush FIFO	No
0x02	–	0 0 0 0 0 0 1 0	Reset Chip	No
0x03	–	0 0 0 0 0 0 1 1	Reset SCSI Bus	Yes[2]
0x45	–	0 1 0 0 0 1 0 1	Disable Selection/Reselection	Yes
		7 6 5 4 3 2 1 0	**Disconnected State Group**	
0x40	0xC0	x 1 0 0 0 0 0 0	Reselect Sequence	Yes
0x41	0xC1	x 1 0 0 0 0 0 1	Select without ATN Sequence	Yes
0x42	0xC2	x 1 0 0 0 0 1 0	Select with ATN Sequence	Yes
0x43	0xC3	x 1 0 0 0 0 1 1	Select with ATN and Stop Sequence	Yes
0x44	0xC4	x 1 0 0 0 1 0 0	Enable Selection/Reselection	No
0x46	0xC6	x 1 0 0 0 1 1 0	Select with ATN3 Sequence	Yes
0x47	0xC7	x 1 0 0 0 1 1 1	Reselect3 Sequence	Yes
		7 6 5 4 3 2 1 0	**Initiator Group**	
0x10	0x90	x 0 0 1 0 0 0 0	Transfer Information	Yes
0x11	0x91	x 0 0 1 0 0 0 1	Initiator Command Complete Sequence	Yes
0x12	–	0 0 0 1 0 0 1 0	Message Accepted	Yes
0x18	0x98	x 0 0 1 1 0 0 0	Transfer Pad	Yes
0x1A	–	0 0 0 1 1 0 1 0	Set ATN	No
0x1B	–	0 0 0 1 1 0 1 1	Reset ATN	No
0x1E	–	0 0 0 1 1 1 1 0	Set ATN Immediate	No
		7 6 5 4 3 2 1 0	**Target Group**	
0x20	0xA0	x 0 1 0 0 0 0 0	Send Message	Yes
0x21	0xA1	x 0 1 0 0 0 0 1	Send Status	Yes
0x22	0xA2	x 0 1 0 0 0 1 0	Send Data	Yes
0x23	0xA3	x 0 1 0 0 0 1 1	Disconnect Sequence	Yes
0x24	0xA4	x 0 1 0 0 1 0 0	Terminate Sequence	Yes
0x25	0xA5	x 0 1 0 0 1 0 1	Target Command Complete Sequence	Yes

Table 5.1 Command Set (Cont.)

Non-DMA	DMA[1]	Command Register [7:0]	Command	Interrupt
		7 6 5 4 3 2 1 0	**Target Group**	
0x27	–	0 0 1 0 0 1 1 1	Disconnect	No
0x28	0xA8	x 0 1 0 1 0 0 0	Receive Message	Yes
0x29	0xA9	x 0 1 0 1 0 0 1	Receive Command	Yes
0x2A	0xAA	x 0 1 0 1 0 1 0	Receive Data	Yes
0x2B	0xAB	x 0 1 0 1 0 1 1	Receive Command Sequence	Yes
0x04	–	0 0 0 0 0 1 0 0	Target Abort DMA	No[3]

1. A dash (–) in the DMA column means that the transfer counter is loaded but no DMA operation occurs.
2. The command causes an interrupt if the SCSI Reset Reporting is not disabled in Configuration 1 (Config 1) register.
3. The command itself does not cause an interrupt. However, it may allow a stalled command to finish and generate an interrupt.

5.1 Illegal Commands

Writing an illegal command to the Command register causes an illegal command interrupt to be generated. An illegal command is any command outside of the specified mode commands or any unsupported command. An illegal command interrupt must be cleared prior to writing another command to the command register.

5.1.1 Stacked Commands

The Command register is a two-deep, eight-bit read/write register that gives commands to the FSC. If DMA commands are to be stacked, the transfer count must be loaded prior to loading the respective command. Command stacking should only be used during Data In and Data Out phase. If stacking is used in initiator mode, it is recommended that the Features Enable bit in Configuration 2 (Config 2) be set. This causes the SCSI phase lines to be latched at the end of a command.

5.2 Miscellaneous Command Group

Miscellaneous commands can be executed and are valid in any mode. Table 5.2 lists the Miscellaneous commands.

Table 5.2 Miscellaneous Commands

Non-DMA	DMA	Mnemonic
0x00	0x80	No Operation (NOP)
0x01	–	Flush FIFO
0x02	–	Reset chip
0x03	–	Reset SCSI bus
0x45	–	Disable selection/reselection

5.2.1 No-Operation (NOP)

The FSC requires this command only after hardware reset or the Reset Chip command to free the Command register. A DMA NOP (0x80) may load the transfer counter with the value in the Transfer Counter register. No interrupt is generated from this command.

5.2.2 Flush FIFO

This command initializes the FIFO to the empty condition by resetting the FIFO flags and setting the bottom byte of the FIFO to zero.

5.2.3 Reset Chip

This command resets all functions in the chip and returns it to a disconnected state. The command has the same effect as a hardware reset.

5.2.4 Reset SCSI Bus

This command asserts the RST/ (SCSI Reset Output) signal for T2 µs, where:

T2 = 130 (CLK period) (CCF)

CCF = Clock Conversion Factor. Refer to the description of Write Register 0x09 in Chapter 4, "Registers." For CCF = 0, indicating 8 clocks, substitute 8 for 0 in this calculation. CLK is the clock input to the FSC. An interrupt is generated unless it is disabled in the Config 1 register.

5.2.5 Disable Selection/Reselection

This command disables an earlier Enable Selection/Reselection command. If bus-initiated selection or reselection has not begun when this command is received by the FSC, it generates a Function Complete interrupt. If bus-initiated selection or reselection has begun, this command (and all other commands) is ignored. Refer to Section 2.2.1, "Bus-Initiated Selection," on page 2-4, and Section 2.2.2, "Bus-Initiated Reselection," on page 2-5, for details.

When this command is loaded into the Command register, any bus-initiated selection or reselection that is already requested begins immediately. Because there is no delay in execution of the selection or reselection, the Function Complete Interrupt bit is not set inadvertently if the selection or reselection sequence continues after this command has been loaded.

5.3 Disconnected State Command Group

If any of the disconnected state commands are received by the FSC when it is not in the disconnected state, the command is ignored, the Command register is cleared, and the FSC generates an illegal command interrupt.

Table 5.3 lists the Disconnected State commands.

Table 5.3 Disconnected State Commands

Non-DMA	DMA	Mnemonic
0x40	0dxC0	Reselect Sequence
0x41	0xC1	Select without ATN Sequence
0x42	0xC2	Select with ATN Sequence
0x43	0xC3	Select with ATN and Stop Sequence
0x44	0xC4	Enable Selection and Reselection
0x45	–	Disable Selection and Reselection
0x46	0xC6	Select with ATN3 Sequence
0x47	0xC7	Reselect3 Sequence

5.3.1 Reselect Sequence

This command causes the FSC target to arbitrate for the bus and then enter the Reselection phase when it wins arbitration. The Identify message, required by SCSI protocol, must either be placed in the FIFO by the microprocessor before issuing the command; or must be transferred by DMA, which involves setting the transfer count to one and setting up the external DMA controller. In either case, the Time-Out and Destination Bus ID registers must have been programmed previously. The sequence terminates early if a Reselect time-out occurs. If it terminates normally, a Function Complete interrupt occurs.

5.3.2 Select without ATN Sequence

This command causes the FSC initiator to arbitrate for the bus, enter the Selection phase when it wins, and send the Command Descriptor Block (CDB). The 6-, 10-, or 12-byte CDB must have either been placed in the FIFO previously by the microprocessor, or must be transferred by DMA, which involves setting the transfer count to 6, 10, or 12 and programming the external DMA controller. In either case, the Time-Out and Destination Bus ID registers must have been programmed previously. This command terminates early if a reselection time-out occurs, the target does not assert Command phase or the target removes Command phase too early. If it terminates normally, a Function Complete and Bus Service interrupt is generated.

5.3.3 Select with ATN Sequence

This command causes the FSC initiator to arbitrate for the bus, select a device with ATN/ true, then send one message phase byte followed by 6, 10, or 12 Command phase bytes. The message and command bytes must have either been placed in the FIFO by the microprocessor or must be transferred by DMA, which involves setting the transfer count to 7, 11, or 13 and programming the external DMA controller. In either case, the Time-Out and Destination Bus ID registers must have previously been programmed. This command terminates early if a select time-out occurs, the target does not assert Message Out phase followed by Command phase, or the target removes Command phase early. If it completes normally, a Function Complete and Bus Service interrupt are generated.

5.3.4 Select with ATN and Stop Sequence

This command should be used in place of Select with ATN when multiple message phase bytes are to be sent (for example, a synchronous negotiation message). The command selects a target with ATN/ asserted, sends one message phase byte that had previously been stored in the FIFO, generates a Bus Service interrupt and a Function Complete interrupt, and stops. After the interrupt, the FIFO may be filled with other message bytes. A Transfer Information command then transfers bytes with ATN/ true until the FIFO empties. If a DMA Transfer Information command is used, ATN/ remains true until the transfer counter decrements to zero.

Table 5.4 lists the Target Selected without ATN sequence.

Table 5.4 Target Selected without ATN Sequence

Sequence Step [2:0]	Interrupt Register [7:0]	Interpretation
0 0 0	0 0 0 0 0 0 0 1	Selected, loaded bus ID into FIFO, loaded null-byte message into FIFO.
0 0 1	0 0 0 0 0 0 0 1	Stopped in Command phase due to parity error; some command descriptor block bytes may not have been received; check FIFO flags.
0 0 1	0 0 0 1 0 0 0 1	Same as previous; initiator asserted ATN/ during Command phase.
0 1 0	0 0 0 0 0 0 0 1	Selected, received entire command descriptor block; check Valid Group Code bit.
0 1 0	0 0 0 1 0 0 0 1	Same as previous; initiator asserted ATN/ during Command phase.

Table 5.5 lists the Target Selected with ATN sequence, SCSI-2 bit not set.

Table 5.5 Target Selected with ATN Sequence (SCSI-2 Bit Not Set)

Sequence Step [2:0]	Interrupt Register [7:0]	Interpretation
0 0 0	0 0 0 0 0 0 1 0	Selected with ATN/, stored bus ID and one message byte; stopped due to either parity error or invalid ID message.
0 0 0	0 0 0 1 0 0 1 0	Selected with ATN/, stored bus ID and one message byte; stopped because ATN/ remained true after first message byte.
0 0 1	0 0 0 0 0 0 1 0	Stopped in Command phase due to parity error; some CDB bytes not received; check Valid Group Code bit and FIFO flags.
0 0 1	0 0 0 1 0 0 1 0	Stopped in Command phase; parity error and ATN/ true.
0 1 0	0 0 0 0 0 0 1 0	Selection complete; received one message byte and the entire command descriptor block.
0 1 0	0 0 0 1 0 0 1 0	Same as previous; initiator asserted ATN/ during Command phase.

Table 5.6 lists the Target Selected with ATN Sequence, SCSI-2 Bit or Queue Tag Enable Bit set.

Table 5.6 Target Selected with ATN Sequence (SCSI-2 Bit or Queue Tag Enable Bit Set)

Sequence Step [2:0]	Interrupt Register [7:0]	Interpretation
0 0 0	0 0 0 0 0 0 1 0	Selected with ATN/, stored bus ID and one message byte; stopped due to either parity error or invalid ID message.
0 0 1	0 0 0 0 0 0 1 0	Initiator released ATN/ after one message byte received. Stopped in Command phase due to parity error; some CDB bytes not received; check Valid Group Code bit and FIFO flags.
0 0 1	0 0 0 1 0 0 1 0	Initiator released ATN/ after one message byte received. Stopped in Command phase; parity error and ATN/ true.
0 1 0	0 0 0 0 0 0 1 0	Initiator released ATN/ after one message byte received. Selection complete; received one message byte and the entire command descriptor block.
0 1 0	0 0 0 1 0 0 1 0	Same as previous, initiator asserted ATN/ during Command phase.
1 0 0	0 0 0 0 0 0 1 0	Parity error during second or third message byte.
1 0 0	0 0 0 1 0 0 1 0	ATN/ remained true after third message byte, or ATN/ remained true and invalid Queue tagged message (if Queue Tagged Enable bit is set).
1 0 1	0 0 0 0 0 0 1 0	Received three message bytes, then stopped in Command phase due to parity error; some CDB bytes not received; check Valid Group Code bit and FIFO flags.
1 0 1	0 0 0 1 0 0 1 0	Stopped in Command phase; parity error and ATN/ true.
1 1 0	0 0 0 0 0 0 1 0	Selection complete; received three message bytes and the entire command descriptor block.

Table 5.7 lists the Initiator Select without ATN sequence.

Table 5.7 Initiator Select without ATN Sequence

Sequence Step [2:0]	Interrupt Register [7:0]	Interpretation
0 0 0	0 0 1 0 0 0 0 0	Arbitration complete; selection time-out; disconnected.
0 1 0	0 0 0 1 1 0 0 0	Arbitration and selection complete; stopped because target did not assert command phase.
0 1 1	0 0 0 1 1 0 0 0	Stopped during command transfer because target prematurely changed phase.
1 0 0	0 0 0 1 1 0 0 0	Select sequence complete.

Table 5.8 lists the Initiator Select with ATN sequence.

Table 5.8 Initiator Select with ATN Sequence

Sequence Step [2:0]	Interrupt Register [7:0]	Interpretation
0 0 0	0 0 1 0 0 0 0 0	Arbitration complete; selection time-out; disconnected.
0 0 0	0 0 0 1 1 0 0 0	Arbitration and selection complete; stopped because target did not assert Message Out phase; ATN/ still asserted by FSC.
0 1 0	0 0 0 1 1 0 0 0	Arbitration, selection, and Message out complete; sent one message byte with ATN/ true, then released ATN/; stopped because target did not assert Command phase after message byte was sent.
0 1 1	0 0 0 1 1 0 0 0	Stopped during command transfer due to premature phase change. Some CDB bytes may not have been sent; check FIFO flags.
1 0 0	0 0 0 1 1 0 0 0	Selection with ATN Sequence complete. One message byte and all command bytes have been sent.

Table 5.9 lists the Initiator Select with ATN and Stop sequence.

Table 5.9 Initiator Select with ATN and Stop Sequence

Sequence Step [2:0]	Interrupt Register [7:0]	Interpretation
0 0 0	0 0 1 0 0 0 0 0	Arbitration complete; selection time-out; disconnected.
0 0 0	0 0 0 1 1 0 0 0	Arbitration and selection complete; stopped because target did not assert Message Out phase; ATN/ still asserted by FSC.
0 0 1	0 0 0 1 1 0 0 0	Message out complete; sent one message byte; ATN/ on.

5.3.5 Enable Selection/Reselection

After receiving this command, the FSC responds to bus-initiated selection or reselection. A command that causes the FSC to select or reselect cancels this command. This command must be reissued within 250 ms after the FSC disconnects to preserve ANSI-recommended timings. If DMA is enabled, incoming information is placed in memory. If DMA is not enabled, incoming information remains in the FIFO.

5.3.6 Select with ATN3 Sequence

This command is similar to the Select with ATN command, but sends three message bytes instead of one. It causes the FSC initiator to arbitrate for the bus, select a device with ATN/ true, send three Message phase bytes, deassert ATN/, then send 6, 10, or 12 command phase bytes. The message and command bytes must have either been placed in the FIFO by the microprocessor or must be transferred by DMA. This involves setting the transfer count to 9, 13, or 15 and programming the external DMA controller. In either case, the Time-Out and Destination Bus ID registers must have previously been programmed. This command terminates early if a selection time-out occurs; the target does not assert the Message Out phase followed by the Command phase, or the target removes Command phase early. If it completes normally, a Function Complete and Bus Service interrupt are generated.

5.3.7 Reselect3 Sequence

This command reselects an initiator and sends three message bytes: a one-byte Identify Message and a two-byte Queue Tag message. If DMA is not enabled, the three message bytes must be loaded into the FIFO before this command is issued.

Table 5.10 lists the Initiator Select with ATN3 sequence.

Table 5.10 Initiator Select with ATN3 Sequence

Sequence Step [2:0]	Interrupt Register [7:0]	Interpretation
0 0 0	0 0 1 0 0 0 0 0	Arbitration complete; selection time-out; disconnected.
0 0 0	0 0 0 1 1 0 0 0	Arbitration and selection complete; stopped because target did not assert Message Out phase; ATN/ still asserted by FSC.
0 1 0	0 0 0 1 1 0 0 0	Sent 1, 2, or 3 message bytes; stopped because target prematurely changed from Message Out phase or did not assert Command phase after third message byte; ATN/ released only if third message byte was sent.
0 1 1	0 0 0 1 1 0 0 0	Stopped during command transfer due to premature phase change; some CDB bytes may not have been sent; check FIFO flags.
1 0 0	0 0 0 1 1 0 0 0	Selection with ATN3 Sequence complete. Three message bytes and all command bytes were sent.

5.4 Initiator Command Group

If the FSC is not in initiator state when it receives one of these commands, the command is ignored, an Illegal Command interrupt is generated, and the Command register is cleared. Refer to the description of the Command register on page 4-8.

If BSY/ goes false while the FSC is connected as an initiator, it generates a disconnected interrupt. The interrupt output occurs 1.5 to 3.5 CLK cycles after BSY/ goes false.

When the FSC receives the last byte of a Message In phase, it leaves ACK/ (Acknowledge) asserted on the bus to prevent the target from sending any more bytes until the initiator decides to accept or reject the message. If the initiator accepts the command, it issues a Message Accepted command. If the initiator does not accept the message, a Set ATN command should be issued before the Message Accepted command, causing the target to change to Message Out phase. For non-DMA commands, an empty FIFO means that the last byte has been sent. For DMA commands, the transfer counter signals the last byte.

If parity checking is enabled and the FSC detects a parity error on an incoming SCSI byte while in Initiator mode, it automatically asserts ATN/ prior to deasserting ACK/ for the byte that has the error. The one exception is after a phase change to Synchronous Data In, and is described as follows.

If the Synchronous Offset register is non-zero (synchronous) and the phase changes to Data In, the DMA interface is immediately disabled and the reporting of a parity error during Data In phase is delayed. The phase change to Data In latches the FIFO flags to indicate how many bytes were in the FIFO (these bytes are lost); clears the FIFO; loads the FIFO with the first Data In byte; generates an interrupt; and continues to load the FIFO with incoming Data In bytes as long as the target sends them, but not more than the specified offset. To continue receiving Data In bytes, the microprocessor would normally issue the Transfer Information command to re-enable the DMA interface. If parity checking is enabled and a parity error occurred on a previous input phase (Message In or Status), then the parity error flag is set in the Status register and ATN/ is set on the SCSI bus. If a parity error occurred during the Data In phase, the parity bit is not set nor is ATN/ asserted until after the FSC receives the subsequent Transfer Information command.

Table 5.11 lists the Initiator commands.

Table 5.11 Initiator Commands

Non-DMA	DMA	Mnemonic
0x10	0x90	Transfer Information
0x11	0x91	Initiator Command Complete Sequence
0x12	–	Message Accepted
0x18	0x98	Transfer Pad
0x1A	–	Set ATN
0x1B	–	Reset ATN
0x1E	–	Set ATN Immediate

5.4.1 Transfer Information

This command can send or receive any Information phase bytes, but is most often used for data transfer.

Note: For synchronous transfer, DMA must be used. The FSC continues to transfer information until one of the following terminating events occurs:

- Transfer is complete. Successful completion generates a Bus Service interrupt. For DMA Transfer Information, the transfer is complete when the transfer counter decrements to zero, the FIFO is empty and the target asserts REQ/ for the next byte. For non-DMA Transfer Information in which the FSC is sending bytes to the SCSI bus, the transfer is complete when the FIFO empties and the target asserts REQ/ for the next byte. For non-DMA Transfer Information in which the FSC is receiving bytes from the SCSI bus, transfer is complete after one byte is received and the target asserts REQ/ for the next byte. Thus non-DMA Transfer Information commands generate an interrupt for every byte received.

- If the phase is Message Out, the FSC removes ATN/ prior to asserting ACK/ for the last byte of the message. For non-DMA, the FIFO flags indicate the last byte. For DMA, the transfer counter indicates the last byte.
- Target changes phase. The FSC clears the Command register and generates a Bus Service interrupt after the target asserts REQ/ for the next byte.
- Target releases BSY/ (Busy). The FSC generates a Disconnected interrupt.
- The FSC receives the last byte of a Message In phase. (For non-DMA, every byte is assumed to be the last byte. For DMA, the transfer counter signals the last byte.) The FSC leaves ACK/ asserted and generates a Function Complete interrupt.

  All Message In and Status phase transfers are handled one byte at a time. If DMA is enabled, the next byte is not received until the current byte has been written to buffer memory and the FIFO is empty. If DMA is not enabled, each byte creates an interrupt.

5.4.2 Initiator Command Complete Sequence

This command causes the FSC to receive a status byte followed by a message byte. It terminates early if the target does not assert the Message In phase, or if the target disconnects. After receiving the message byte, the FSC leaves ACK/ asserted on the bus to allow the initiator to assert ATN/ if the message is unacceptable.

5.4.3 Message Accepted

This command deasserts the ACK/ signal on the SCSI bus. Any of the commands that receive bytes during message phase leave ACK/ asserted after receiving the last message byte. To accept the message, issue this command. To reject the message, set ATN/ and then issue this command.

5.4.4 Transfer Pad

Transfer Pad is usually an error recovery technique. It is useful when a target requests more bytes than an initiator has to send, or when an initiator must receive and discard a number of bytes from a target.

When transmitting to the SCSI bus, Transfer Pad fills the FIFO with null bytes and sends them to the SCSI bus. When receiving from the SCSI bus, Transfer Pad receives bytes, places them on the top of the FIFO, and discards them from the bottom of the FIFO.

When sending pad bytes to the SCSI bus, DMA must be enabled. No DMA requests are actually made, but the FSC uses the transfer counter to end the transfer.

The command terminates under the same conditions as the Section 5.4.1, “Transfer Information,” command, except that the FSC does not leave ACK/ asserted on the last byte of a Message In phase. If the command terminates before the transfer counter reaches zero (due to phase change or disconnect) the FIFO may contain pad bytes.

5.4.5 Set ATN

This command asserts attention on the SCSI bus. No interrupt is generated from this command. ATN/ stays asserted until the last byte of a message out phase. This command does not pre-empt a command in progress; attention is asserted after the current command is completed.

DMA commands use the transfer counter to indicate the last byte. For non-DMA commands, the last byte means that the FIFO is empty. For DMA transfers, the last byte means that the transfer counter is zero. ATN/ is also released if the target disconnects prematurely.

5.4.6 Reset ATN

This command causes ATN/ to be released. It does not cause an interrupt.

This command must not be used when connected to a device supporting the Common Command Set (CCS). The FSC obeys CCS protocol by releasing ATN/ on the last byte of a Message Out phase. The Reset ATN command is provided for older devices that do not respond properly to the ATN/ condition.

5.4.7 Set ATN Immediate

This command asserts attention on the SCSI bus while another command is in progress. This command does not terminate a currently executing command, but allows the FSC as initiator to alert the target to go to Message Out phase at the earliest convenience. ATN/ deasserts at the last Message Out byte or when a Reset ATN command is issued.

5.5 Target Command Group

If the FSC receives any of these commands when it is not in target state, it ignores the command, clears the Command register, and generates an Illegal Command interrupt. Refer to the Command register description on page 4-8 for details.

Normal completion of these commands causes a Function Complete interrupt. If ATN is asserted, the Bus Service bit is set in the Status register and an interrupt is generated. If the FSC was idle when ATN was asserted, a Bus Service interrupt is generated, the Function Complete bit is zero, and the Command register is cleared.

Table 5.12 lists the Target commands.

Table 5.12 Target Commands

Non-DMA	DMA	Mnemonic
0x20	0xA0	Send Message
0x21	0xA1	Send Status
0x22	0xA2	Send Data
0x23	0xA3	Disconnect Sequence
0x24	0xA4	Terminate Sequence
0x25	0xA5	Target Command Complete Sequence
0x27	–	Disconnect
0x28	0xA8	Receive Message
0x29	0xA9	Receive Command
0x2A	0xAA	Receive Data
0x2B	0xAB	Receive Command Sequence
0x04	–	Target Abort DMA

5.5.1 Send Message

This command causes the FSC to assert Message In phase and sends bytes until the FIFO is empty or the transfer counter is zero (if DMA).

5.5.2 Send Status

This command causes the FSC to assert Status phase and sends bytes until the FIFO is empty or the transfer counter is zero (if DMA).

5.5.3 Send Data

This command causes the FSC to assert Data In phase and sends bytes until the FIFO is empty, or the transfer counter is zero and the FIFO is empty (if DMA). DMA must be used for synchronous transfers.

5.5.4 Disconnect Sequence

This command causes the FSC to assert Message In phase, send two bytes, then disconnect from the SCSI bus. Normally, the first byte is a Save Data Pointers message, and the second byte is a Disconnect message. These bytes must be loaded into the FIFO by the microprocessor, or may be loaded by DMA. If ATN/ is asserted by the initiator, the Bus Service and Function Complete bits are set and an interrupt is generated, but the FSC does not disconnect.

Table 5.13 lists the Target Disconnect sequence.

Table 5.13 Target Disconnect Sequence

Sequence Step [2:0]	Interrupt Register [7:0]	Interpretation
0 0 0	0 0 0 1 1 0 0 0	Sent one message byte; stopped because initiator set ATN/.
0 0 1	0 0 0 1 1 0 0 0	Sent two message bytes; stopped because initiator set ATN/.
0 1 0	0 0 1 0 1 0 0 0	Disconnect Sequence complete; disconnected, bus is free.

5.5.5 Terminate Sequence

This command causes the FSC first to assert Status phase, send one byte; then assert Message In phase, send one more byte, and disconnect. These bytes must be loaded into the FIFO by the microprocessor, or may be loaded by DMA. If ATN/ is asserted by the initiator, the Bus Service and Function Complete bits are set and an interrupt is generated, but the FSC does not disconnect. If ATN/ is not asserted by the initiator, a disconnect interrupt is generated.

Table 5.14 lists the Target Terminate sequence.

Table 5.14 Target Terminate Sequence

Sequence Step [2:0]	Interrupt Register [7:0]	Interpretation
0 0 0	0 0 0 1 1 0 0 0	Sent one status byte; stopped because initiator set ATN/.
0 0 1	0 0 0 1 1 0 0 0	Sent status and message bytes; stopped because initiator set ATN/.
0 1 0	0 0 1 0 1 0 0 0	Terminate Sequence complete; disconnected, bus is free.

5.5.6 Target Command Complete Sequence

This command is similar to Terminate Sequence, but is used for linked commands. It causes the FSC first to assert Status phase, send one byte, then assert Message In phase and send one more byte. The message byte is normally a Command Complete message. If ATN/ is asserted by the initiator, the Bus Service and Function Complete bits are set and an interrupt is generated. If ATN/ is not asserted by the initiator, a function complete interrupt is generated. In either case, the FSC does not disconnect.

Table 5.15 lists the Target Command Complete sequence.

Table 5.15 Target Command Complete Sequence

Sequence Step [2:0]	Interrupt Register [7:0]	Interpretation
0 0 0	0 0 0 1 1 0 0 0	Sent one status byte; stopped because initiator set ATN/.
0 0 1	0 0 0 1 1 0 0 0	Sent status and message bytes; stopped because initiator set ATN/.
0 1 0	0 0 0 0 1 0 0 0	Command Complete Sequence complete.

5.5.7 Disconnect

This command causes the FSC to release all SCSI bus signals except RST/ (when triggered, RST/ is driven true for approximately 25 µs, depending on CLK frequency and the clock conversion factor). The FSC returns to the Disconnected state without generating an interrupt.

5.5.8 Receive Message

This command causes the FSC to assert Message Out phase and receive bytes from the initiator. For a non-DMA command, only one byte per interrupt may be received. A DMA command interrupts after the transfer counter decrements to zero. This command terminates by generating a function complete interrupt.

5.5.9 Receive Command

This command causes the FSC to assert Command phase and receive bytes from the initiator. For non-DMA Receive command, only one byte per interrupt may be received. DMA Receive command interrupts after the transfer counter decrements to zero. This command terminates by generating a function complete interrupt.

5.5.10 Receive Data

This command causes the FSC to assert Data Out phase and receive bytes from the initiator. For non-DMA Receive Data, only one byte per interrupt may be received. DMA Receive Data interrupts after the transfer counter decrements to zero and the FIFO is empty. This command terminates by generating a function complete interrupt. DMA must be used for synchronous transfers.

5.5.11 Receive Command Sequence

This command causes the FSC to assert Command phase and receive a number of bytes, which vary according to the group code field of the first byte. If the SCSI-2 bit is set in the Configuration 2 (Config 2) register, Group 2 commands are recognized as 10-byte commands. If the SCSI-2 bit is cleared, Group 2 commands are recognized as reserved commands. Groups 3 and 4 are always reserved. The FSC requests six bytes for reserved commands, six bytes for Group 6 vendor unique commands, 10 bytes for Group 7 vendor unique commands, and 12 bytes for Group 5 commands.

Table 5.16 lists the Target Receive Command sequence.

Table 5.16 Target Receive Command Sequence

Sequence Step [2:0]	Interrupt Register [7:0]	Interpretation
0 0 1	0 0 0 0 1 0 0 0	Stopped during command transfer due to parity error; check FIFO flags.
0 0 1	0 0 0 1 1 0 0 0	Stopped during command transfer due to parity error; ATN/ asserted by initiator.
0 1 0	0 0 0 0 1 0 0 0	Received entire command descriptor block.
0 1 0	0 0 0 1 1 0 0 0	Received entire CDB; initiator asserted ATN/.

5.5.12 Target Abort DMA

The Target Abort DMA command allows the microprocessor to stop a target data transfer command whose progress has been halted due to inactivity on the DMA channel. One potential application is a system containing a microprocessor and an intelligent buffer controller that handles buffer management. The microprocessor sets up the buffer controller and overprograms the transfer counter prior to issuing a SCSI transfer command to the chip. When the buffer controller runs out of buffers, it interrupts the microprocessor. The microprocessor stops the chip and commands it to disconnect from the SCSI bus.

Note: The Target Abort DMA command should be used with extreme caution. Before using this command, verify that the removal of DREQ by this command does not confuse the system's DMA controller.

The abort DMA command executes from the top of the command FIFO. If there is a stacked command waiting to execute, it is overwritten and the Gross Error bit 6 (Status register) is set. The abort DMA command clears itself from the command stack after being decoded.

The abort DMA command can only be used when all of the following conditions are true:

- Either the Target Send Data or Target Receive Data command is operating
- The DMA controller has halted

- The chip is in a steady state:

  Send Data – the DMA FIFO is empty

  Receive Asynchronous Data – The FIFO is full (FIFO Flags Register = 0x10), or the Transfer Counter is zero (Status register bit 4 = 1)

  Receive Synchronous Data – The Transfer Counter is zero, or the Offset Counter is at maximum value (Sequence Step register bit 3 = 0)

When these conditions are true, the chip halts with DREQ asserted. If the chip is in Synchronous Transfer mode when halted, some ACK/ responses from the SCSI bus may not have been received and remain outstanding. Upon receiving the Abort DMA command, the chip resets the DMA interface, including the DREQ output pin, and terminates the command in progress. The chip completes any ongoing SCSI process. Send Asynchronous Data transfers complete immediately. Send Synchronous Data transfers complete when the offset counter is zero. Receive Asynchronous Data transfers complete immediately. Data left in the FIFO should be removed by the microprocessor. Receive Synchronous Data operations complete when all outstanding SCSI ACK/s have been received. No extra bits are set in the Interrupt or Status registers. The microprocessor receives the interrupt from the command that was in progress, and the command FIFO is cleared.

Chapter 6 Electrical Specifications

This chapter is divided into the following sections:

6.1 DC Electrical Characteristics

Tables 6.1 through 6.5 describe the LSI53CF92A DC electrical characteristics.

Table 6.1 Absolute Maximum Stress Ratings

Symbol	Parameter	Pins	Min	Max	Unit	Test Conditions
T_{STG}	Storage temperature	–	–55	150	C	–
V_{DD}	Supply voltage	–	–0.5	7.0	V	–
V_{IN}	Input voltage	–	V_{SS} –0.5	V_{DD} +0.5	V	–
I_{LU}	Latch-up current	–	±100	–	mA	–2 V < V_{PIN} < +8 V

Stresses beyond those listed in Table 6.1 may cause permanent damage to the device. These are stress ratings only; functional operation of the device at these or any other conditions beyond those indicated in the Recommended Operating Conditions section of this specification is not implied.

Table 6.2 Recommended Operating Conditions

Symbol	Parameter	Pins	Min	Max	Unit	Test Conditions
V_{DD}	Supply voltage	–	4.75	5.25	V	–
I_{DD}	Supply current	–	–	1	mA	Static[1]
I_{DD}	Supply current	–	–	50	mA	Dynamic
T_A	Ambient temperature	–	0	70	C	–
Θ_{JA}	Thermal resistance, junction/ambient		–	54	C/W	–
t_r	Rise Time	[2]	1	–	V/ns	–
t_f	Fall Time	[2]	1	–	V/ns	–

1. Static means all inputs are deasserted, all outputs floating, and all bidirectional pins configured as inputs.
2. The timing data applies to all pins without Schmitt triggers.

Table 6.3 Inputs

Symbol	Parameter	Pins	Min	Max	Unit	Test Conditions
V_{IH}	Input high voltage	–	2.0	V_{DD} +0.5	V	–
V_{IL}	Input low voltage	–	V_{SS} –0.5	0.8	V	–
I_{IN}	Input leakage current	Non-SCSI	–10	10	µA	$0 < V_{IN} < V_{DD}$
V_H	Hysteresis	SCSI	300	400	mV	–
I_{IL}	Input leakage current	SCSI	–10	10	µA	$0 < V_{IN} < V_{DD}$
C_{IN}	Capacitance	–	–	10	pF	–

Table 6.4 Outputs

Symbol	Parameter	Pins	Min	Max	Unit	Test Conditions
V_{OH}	Output high voltage	DREQ	2.4	V_{DD}	V	I_{OH} = –2 mA
V_{OL}	Output low voltage	DREQ, INT/	V_{SS}	0.4	V	I_{OL} = 4 mA
V_{OL}	Output low voltage[1]	RST/, SEL/, ACK/, REQ/, BSY/, SDP, SD[7:0]	V_{SS}	0.5	V	I_{OL} = 48 mA
I_{OZ}	HIGH-Z state leakage	–	–10	10	µA	$0 < V_{OUT} < V_{DD}$
T_F	Fall Time	SCSI pins	5.2	14.7	ns	SCSI termination
C_{OUT}	Capacitance	–	–	10	pF	–

1. TolerANT active negation not enabled.

Table 6.5 Bidirectional Pins

Symbol	Parameter	Pins	Min	Max	Unit	Test Conditions
V_{IH}	Input high voltage	–	2.0	V_{DD} +0.5	V	–
V_{IL}	Input low voltage	–	V_{SS} –0.5	0.8	V	–
V_{OH}	Output high voltage[1]	SCSI inputs	2.4	V_{DD}	V	I_{OH} = –2 mA
V_{OL}	Output low voltage	SCSI inputs	V_{SS}	0.4	V	I_{OL} = 4 mA
V_{OL}	Output low voltage[1]	SD[7:0], SDP, REQ/, ACK/	V_{SS}	0.5	V	I_{OL} = 48 mA
V_H	Hysteresis	SCSI	300	400	mV	–
I_I	Input leakage	SCSI	–10	10	µA	$0 < V_{IN} < V_{DD}$
I_{IL}	Input current, low	DB[7:0], DBP, PAD[7:0]	–200	–50	µA	V_{IN} = 0
I_{IH}	Input current, high	DB[7:0], DBP, PAD[7:0]	0	10	µA	$V_{IN} = V_{DD}$
I_{PU}	HIGH-Z pull-up current	DB[7:0], DBP, PAD[7:0]	–200	–50	µA	V_{IN} = 0
C_{IO}	Capacitance	–	–	10	pF	–

1. TolerANT active negation not enabled.

6.2 TolerANT Active Negation Technology Specifications

Table 6.6 provides electrical characteristics for SE SCSI signals. Figures 6.1 through 6.5 provide reference information for testing SCSI signals.

Table 6.6 TolerANT Active Negation Technology Electrical Characteristics[1]

Symbol	Parameter	Min	Type	Max	Unit	Test Conditions
V_{OH}[2]	Output high voltage	2.5	3.1	3.5	V	I_{OH} = 2.5 mA
V_{OL}	Output low voltage	0.1	0.2	0.5	V	I_{OL} = 48 mA
V_{IH}	Input high voltage	2.0		7.0	V	–
V_{IL}	Input low voltage	–0.5		0.8	V	Referenced to V_{SS}
V_{IK}	Input clamp voltage	–0.66	–0.74	–0.77	V	V_{DD} = min; I_I = –20 mA
V_{TH}	Threshold, HIGH to LOW	1.1	1.2	1.3	V	–
V_{TL}	Threshold, LOW to HIGH	1.5	1.6	1.7	V	–
V_{TH}–V_{TL}	Hysteresis	300	350	400	mV	–
I_{OH}[2]	Output high current	2.5	15	24	mA	V_{OH} = 2.5 V
I_{OL}	Output low current	100	150	200	mA	V_{OL} = 0.5 V
I_{OSH}[2]	Short-circuit output high current	–	–	625	mA	Output driving low, pin shorted to V_{DD} supply[3]
I_{OSL}	Short-circuit output low current	–	–	95	mA	Output driving high, pin shorted to V_{SS} supply
I_{LH}	Input high leakage	–	0.05	10	µA	–0.5 < V_{DD} < 5.25 V_{PIN} = 2.7 V
I_{LL}	Input low leakage	–	–0.05	–10	µA	–0.5 < V_{DD} < 5.25 V_{PIN} = 0.5V
R_I	Input resistance	–	20	–	MΩ	SCSI pins [4]
C_P	Capacitance per pin	6	8	10	pF	Quad Flat Pack Package
t_R[2]	Rise time, 10% to 90%	9.7	15.0	18.5	ns	Figure 6.1
t_F	Fall time, 90% to 10%	5.2	8.1	14.7	ns	Figure 6.1
dV_H/dt	Slew rate, LOW to HIGH	0.15	0.23	0.49	V/ns	Figure 6.1
dV_L/dt	Slew rate, HIGH to LOW	0.19	0.37	0.67	V/ns	Figure 6.1
I_{LU}	Latch-up	100	–	–	mA	–
t_1	Filter Delay	20	25	30	ns	Figure 6.2
t_1	Extended Filter Delay	40	50	60	ns	Figure 6.2

1. These values are guaranteed by periodic characterization.
2. Active Negation outputs only: Data, Parity, REQ/, ACK/.
3. Single pin only; irreversible damage may occur if sustained for one second.
4. SCSI RESET pin as 10 kΩ pull-up resistor.

Figure 6.1 Rise and Fall Time Test Conditions

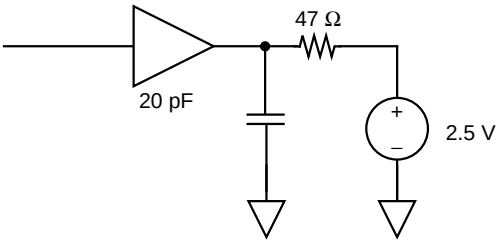
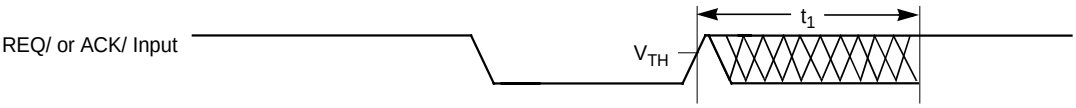


Figure 6.2 SCSI Input Filtering



Note: t_1 is the input filtering period, register programmable (Bit 4 of the Configuration 3 (Config 3) register 0x0C to either 30 or 60 ns.

Figure 6.3 Hysteresis of SCSI Receivers

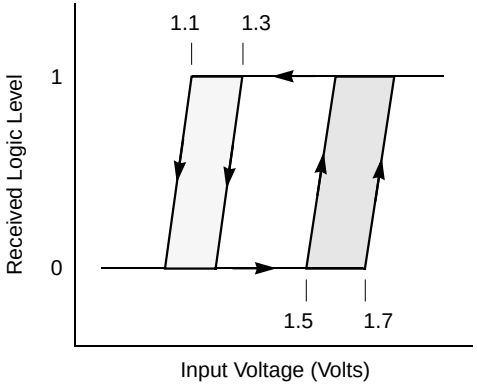


Figure 6.4 Input Current as a Function of Input Voltage

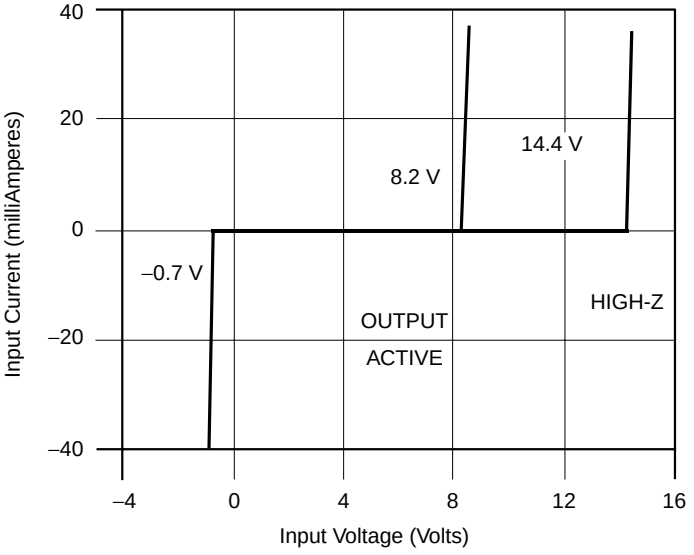
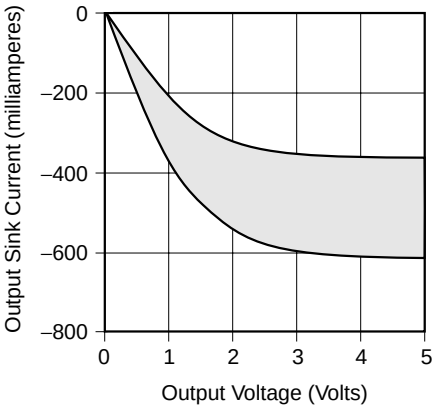
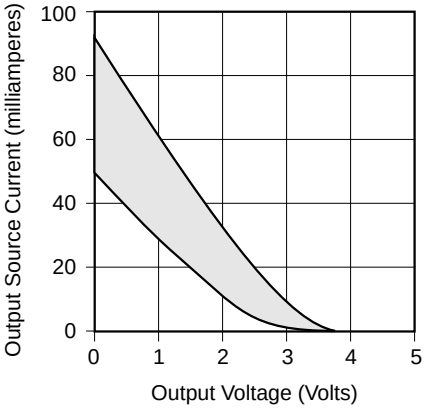


Figure 6.5 Output Current as a Function of Output Voltage





6.3 AC Electrical Characteristics

The AC characteristics described in this section apply over the operating voltage and temperature range, 4.75 V ≥ V_{DD} ≥ 5.25 V and 0 ˚C ≥ T_A ≥ 70 ˚C. Output timing is based on simulation under worst-case conditions (4.75 V, 70 ˚C) and worst-case processing using the following termination. All timing data in this specification is taken from the 10% and 90% points with respect to the specified V_{OL} and V_{OH} of the waveforms.

Note: Performance numbers are based upon the FSC operating with a 40 MHz clock. Other clock inputs also allow for increased transfer rates in proportion to their frequencies.

Table 6.7 lists the pin terminations.

Table 6.7 Pin Terminations

Pin	Termination
DREQ, PAD[7:0]	50 pF
INT/	50 pF, 2.2 kΩ pull-up
DB[7:0], DBP	80 pF
SDP, SD[7:0], RST/, SEL/, BSY/, ATN/, MSG/, CD/, IO/, REQ/, ACK/	200 pF, 110 Ω pull-up, 165 Ω pull-down

Figure 6.6 illustrates the clock input. Table 6.8 lists the Clock Timing with the FASTCLK bit cleared, and Table 6.9 lists the Clock Timing with the FASTCLK bit set.

Figure 6.6 Clock Input

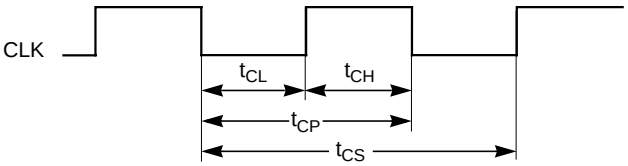


Table 6.8 Clock Timing (FASTCLK Bit Cleared)

Symbol	Parameter	Min	Max	Unit	Notes
t_{CPA}	Clock frequency, asynchronous SCSI	10	25	MHz	1
t_{CPS}	Clock frequency, synchronous SCSI	12	25	MHz	1
t_{CH}	Clock HIGH time	0.4 t_{CP}	0.6 t_{CP}	ns	–
t_{CL}	Clock LOW time	0.4 t_{CP}	0.6 t_{CP}	ns	–
t_{CP}	Clock period	40	100	ns	–
t_{CS}	Synchronization latency = t_{CP} + t_{CL}	t_{CP}	t_{CL} + t_{CP}	–	–

1. Minimum frequencies to meet ANSI timing specifications.

Table 6.9 Clock Timing (FASTCLK Bit Set)

Symbol	Parameter	Min	Max	Unit	Notes
t_{CPA}	Clock frequency, asynchronous SCSI	25	40	MHz	1
t_{CPS}	Clock frequency, synchronous SCSI	25	40	MHz	1
t_{CH}	Clock HIGH time	0.4 * t_{CP}	0.6 * t_{CP}	ns	–
t_{CL}	Clock LOW time	0.4 * t_{CP}	0.6 * t_{CP}	ns	–
t_{CP}	Clock period	25	40	ns	–
t_{CS}	Synchronization latency = t_{CP} + t_{CL}	t_{CP}	t_{CL} + t_{CP}	–	–

1. Minimum frequencies to meet ANSI timing specifications.

Figure 6.7 and Table 6.10 provide Reset timing data.

Figure 6.7 Reset Input

Table 6.10 Reset Timing

Symbol	Parameter	Min	Max	Unit	Notes
t_{RST}	RESET pulse width	3 t_{CP}	–	ns	1

1. At power-up, the RESET pin must be asserted as V_{DD} first becomes stable.

Figure 6.8 and Table 6.11 provide Interrupt timing data.

Figure 6.8 Interrupt Output

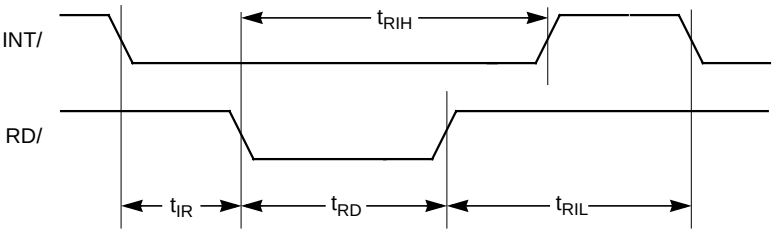


Table 6.11 Interrupt Timing

Symbol	Parameter	Min	Max	Unit	Notes
t_{IR}	INT/ LOW to Interrupt register read	0	–	ns	1
t_{RD}	RD/ pulse width	30	–	ns	2
t_{RIH}	RD/ LOW to INT/ HIGH	0	3 t_{CP} + 30	ns	–
t_{RIL}	RD/ HIGH to INT/ LOW	t_{CS}	–	ns	–

1. The Interrupt register should not be read when INT/ is false.
2. Refer to the register read specifications for the timing requirements of CS/, RD/, and address for reading the Interrupt register.

6.3.1 Register Interface, Nonmultiplexed PAD Bus

Figure 6.9 illustrates the Register Read, Nonmultiplexed PAD bus.

Figure 6.9 Register Read, Nonmultiplexed PAD Bus

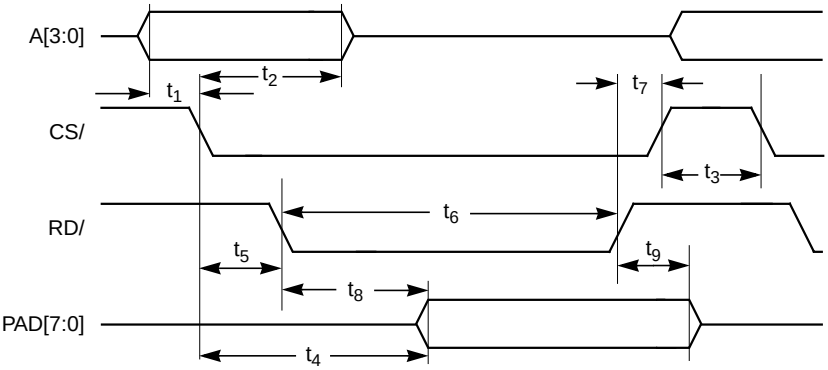


Figure 6.10 illustrates the Register Write, Nonmultiplexed PAD bus.

Figure 6.10 Register Write, Nonmultiplexed PAD Bus

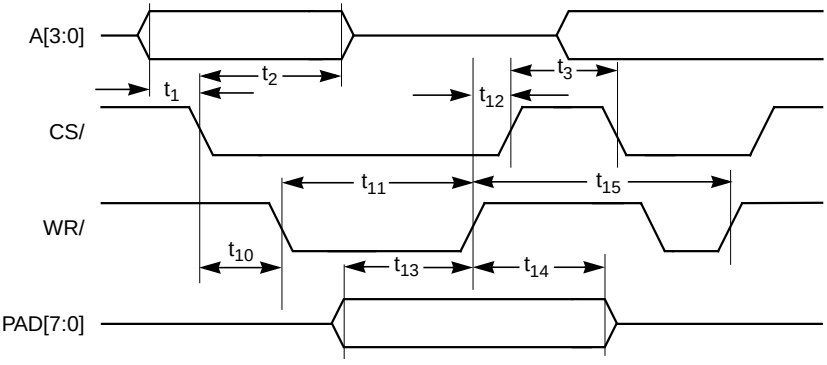


Table 6.12 lists the Register Interface, Nonmultiplexed PAD bus.

Table 6.12 Register Interface, Nonmultiplexed PAD Bus

Symbol	Parameter	Min	Max	Unit	Notes
t_1	Address setup to CS/ LOW	3	–	ns	1
t_2	Address hold from CS/ LOW	20	–	ns	–
t_3	CS/ HIGH to CS/ LOW	t_{CP} +5	–	ns	2
t_4	CS/ LOW to read data valid	–	t_{CP} +30	ns	3
t_5	CS/ setup to RD/ LOW	0	–	ns	4, 5
t_6	RD/ pulse width	30	–	ns	–
t_7	RD/ HIGH to CS/ HIGH	0	–	ns	4
t_8	RD/ LOW to data valid	–	30	ns	6
t_9	RD/ HIGH to data bus disable	2	30	ns	–
t_{10}	CS/ setup to WR/ LOW	0	–	ns	5, 7
t_{11}	WR/ pulse width	30	–	ns	–
t_{12}	WR/ HIGH to CS/ HIGH	0	–	ns	7
t_{13}	Data setup to WR/ HIGH	15	–	ns	–
t_{14}	Data hold after WR/ HIGH	4	–	ns	–
t_{15}	CS/ or WR/ HIGH to CS/ or WR/ HIGH	3 t_{CP}	–	ns	–

1. CS/ must make a HIGH to LOW transition to latch a new register address.
2. t_3 minimum is (2 * 3 t_{CP} + 5) for successive FIFO reads or a FIFO write/read followed by a read of the FIFO Flags register.
3. t_8 must also be satisfied.
4. If RD/ is held LOW, the time from CS/ LOW to stable data is t_4 and the output disable time from CS/ HIGH is t_9.
5. If DMA is active, the FIFO must not be accessed.
6. t_4 must also be satisfied.
7. If WR/ is held LOW, the data setup to CS/ HIGH is t_{13} minimum; data hold from CS/ HIGH is t_{13} minimum.

6.3.2 Register Interface, Multiplexed PAD Bus

Figure 6.11 illustrates the Register Read, Multiplexed PAD bus.

Figure 6.11 Register Read, Multiplexed PAD Bus

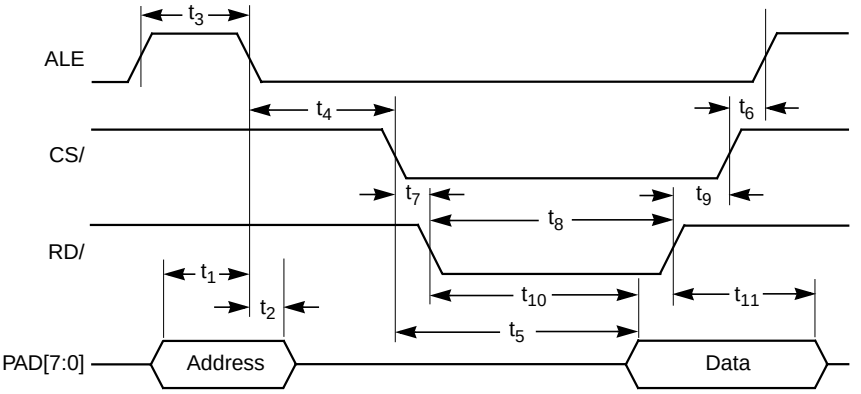


Figure 6.12 illustrates the Register Write, Multiplexed PAD bus.

Figure 6.12 Register Write, Multiplexed PAD Bus

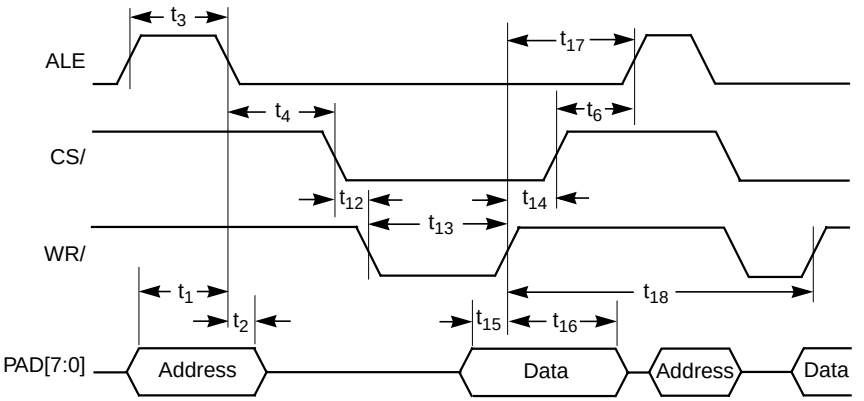


Table 6.13 lists the Register Interface, Multiplexed PAD bus.

Table 6.13 Register Interface, Multiplexed PAD Bus

Symbol	Parameter	Min	Max	Unit	Notes
t_1	Address setup to ALE LOW	10	–	ns	–
t_2	Address hold from ALE LOW	10	–	ns	–
t_3	ALE pulse width	20	–	ns	1
t_4	ALE LOW to CS/ LOW	10	–	ns	–
t_5	CS/ LOW to data valid	–	t_{CP} +30	ns	2
t_6	CS/ HIGH to ALE HIGH	0	–	ns	
t_7	CS/ setup to RD/ LOW	0	–	ns	3, 4
t_8	RD/ pulse width	30	–	ns	–
t_9	RD/ HIGH to CS/ HIGH	0	–	ns	4
t_{10}	RD/ LOW to data valid	–	30	ns	5
t_{11}	RD/ HIGH to data bus disable	2	30	ns	–
t_{12}	CS/ setup to WR/ LOW	0	–	ns	3, 6
t_{13}	WR/ pulse width	30	–	ns	–
t_{14}	WR/ HIGH to CS/ HIGH	0	–	ns	6
t_{15}	Data setup to WR/ HIGH	15	–	ns	–
t_{16}	Data hold from WR/ HIGH	4	–	ns	–
t_{17}	WR/ HIGH to ALE HIGH	t_{CP} +5	–	ns	7
t_{18}	CS/ or WR/ HIGH to CS/ or WR/ HIGH	3 t_{CP}	–	ns	–

1. ALE must pulse to capture a new register address.
2. t_{10} must also be satisfied.
3. IF DMA is active, the FIFO register must not be accessed.
4. If RD/ is held LOW, the time from CS/ LOW to stable data is t_5 and the data release time from CS/ HIGH is t_{11}.
5. t_5 must also be satisfied.
6. If WR/ is held LOW, data setup to CS/ HIGH is t_{15} and data hold from CS/ HIGH is t_{16} minimum.
7. t_{17} minimum is (2 *3 t_{CP} + 5) for successive FIFO reads or a FIFO write/read followed by a read of the FIFO Flags register.

6.3.3 DMA Interface (Nonmultiplexed Mode Only)

Figure 6.13 illustrates the DMA Read, Nonmultiplexed Mode only.

Figure 6.13 DMA Read, Nonmultiplexed Mode Only

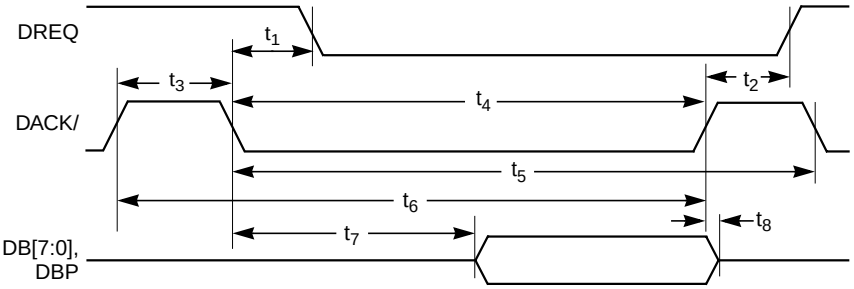


Figure 6.14 illustrates the DMA Write, Nonmultiplexed Mode only.

Figure 6.14 DMA Write, Nonmultiplexed Mode Only

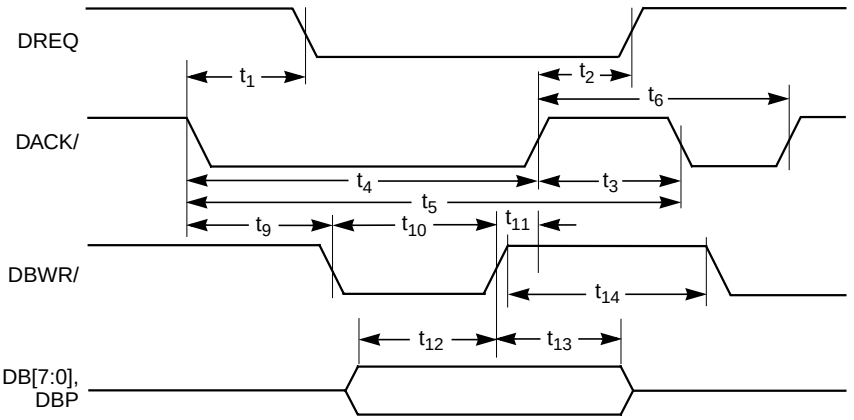


Table 6.14 lists the DMA Interface, Nonmultiplexed Mode only.

Table 6.14 DMA Interface (Nonmultiplexed Mode Only)[1]

Symbol	Parameter	Min	Max	Unit	Notes
t_1	DACK/ LOW to DREQ LOW	–	30	ns	2
t_2	DACK/ HIGH to DREQ HIGH	30	–	ns	–
t_3	DACK/ HIGH to DACK/ LOW	t_{CP} +5	–	ns	3, 4
t_4	DACK/ pulse width	t_{CP} +5	–	ns	–
t_5	DACK/ period (LOW to LOW)	3 t_{CP}	–	ns	–
t_6	DACK/ period (HIGH to HIGH)	3 t_{CP}	–	ns	–
t_7	DACK/ LOW to data valid	–	30	ns	–
t_8	DACK/ HIGH to data bus disable	2	30	ns	–
t_9	DACK/ LOW to DBWR/ LOW	0	–	ns	4
t_{10}	DBWR/ pulse width	30	–	ns	–
t_{11}	DBWR/ HIGH to DACK/ HIGH	0	–	ns	4
t_{12}	Data setup to DBWR/	15	–	ns	–
t_{13}	Data hold from DBWR/	4	–	ns	–
t_{14}	DBWR/ HIGH to DBWR/ LOW	30	–	ns	–

1. Alternate DMA is disabled.
2. DREQ may stay HIGH if the FIFO has room to accept another byte during DMA write, or send another byte during DMA read. If the current DMA acknowledge cycle fills the FIFO (write) or empties the FIFO (read), then DREQ goes LOW.
3. DACK/ must toggle once for each access.
4. DBWR/ edges may precede or follow DACK/ edges. Recommended values are: $t_9 \geq 0$ and $t_{11} \geq 0$. If DBWR/ is held LOW, the data setup to DACK/ HIGH is 15 ns minimum; data hold from DACK/ HIGH is 4 ns minimum.

6.3.4 DMA Interface (Multiplexed Mode Only)

Figure 6.15 illustrates the DMA Read, Multiplexed Mode only.

Figure 6.15 DMA Read, Multiplexed Mode Only

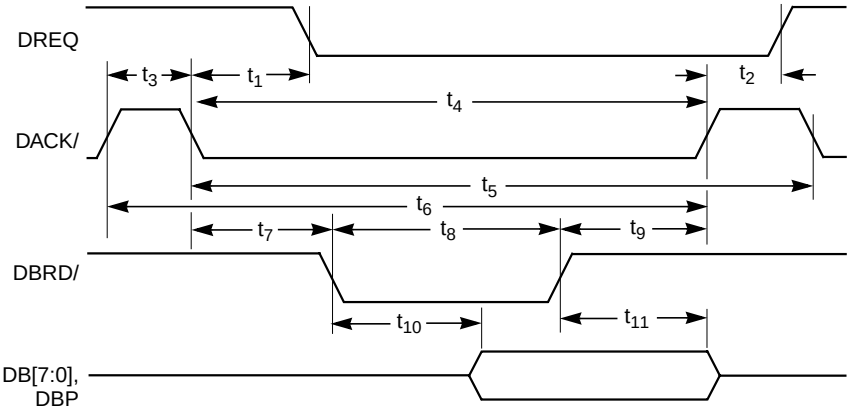


Figure 6.16 illustrates the DMA Write, Multiplexed Mode only.

Figure 6.16 DMA Write, Multiplexed Mode Only

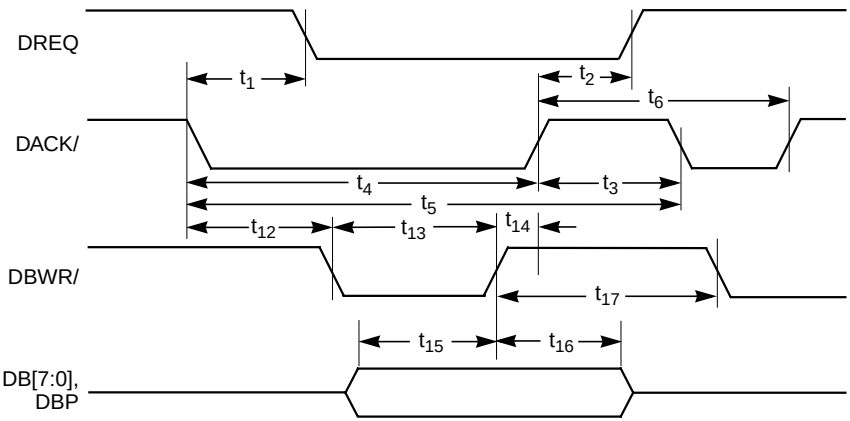


Table 6.15 lists the DMA Interface, Multiplexed Mode only.

Table 6.15 DMA Interface (Multiplexed Mode Only)[1]

Symbol	Parameter	Min	Max	Unit	Notes
t_1	DACK/ LOW to DREQ LOW	–	30	ns	2
t_2	DACK/ HIGH to DREQ HIGH	30	–	ns	2
t_3	DACK/ HIGH to DACK/ LOW	t_{CP} +5	–	ns	3
t_4	DACK/ pulse width	t_{CP} +5	–	ns	–
t_5	DACK/ period (LOW to LOW)	3 t_{CP}	–	ns	–
t_6	DACK/ period (HIGH to HIGH)	3 t_{CP}	–	ns	–
t_7	DACK/ LOW to DBRD/ LOW	0	–	ns	4
t_8	DBRD/ pulse width	30	–	ns	–
t_9	DBRD/ HIGH to DACK/ HIGH	0	–	ns	4
t_{10}	DBRD/ to data valid	0	30	ns	–
t_{11}	DBRD/ HIGH to data bus disable	2	30	ns	–
t_{12}	DACK/ LOW to DBWR/ LOW	0	–	ns	5
t_{13}	DBWR/ pulse width	30	–	ns	–
t_{14}	DBWR/ HIGH to DACK/ HIGH	0	–	ns	5
t_{15}	Data setup to DBWR/ HIGH	15	–	ns	–
t_{16}	Data hold from DBWR/ HIGH	4	–	ns	–
t_{17}	DBWR/ HIGH to DBWR/ LOW	30	–	ns	–

1. Alternate DMA is disabled.
2. DREQ may stay HIGH if the FIFO has room to accept another byte during DMA write, or send another byte during DMA read. If the current DMA acknowledge cycle fills the FIFO (write) or empties the FIFO (read), then DREQ goes LOW.
3. DACK/ must toggle once for each access.
4. DBRD/ trailing edge may precede or follow DACK/ trailing edge. The recommended value is: $t_9 \geq 0$. If DBRD/ is held LOW past DACK/, the time from DACK/ LOW to stable data is 30 ns maximum, and the time from DACK/ HIGH to data bus disable is 2 ns minimum and 25 ns maximum.
5. DBWR/ trailing edge may precede or follow DACK/ trailing edge. The recommended value is: $t_{14} \geq 0$. If DBWR/ is past DACK/, the data setup to DACK/ HIGH is 10 ns minimum; data hold from DACK/ HIGH is 10 ns minimum.

6.3.5 Burst Mode DMA Interface (Multiplexed Mode)

Figure 6.17 illustrates the Burst Mode DMA Read, Multiplexed Mode only.

Figure 6.17 Burst Mode DMA Read, Multiplexed Mode Only

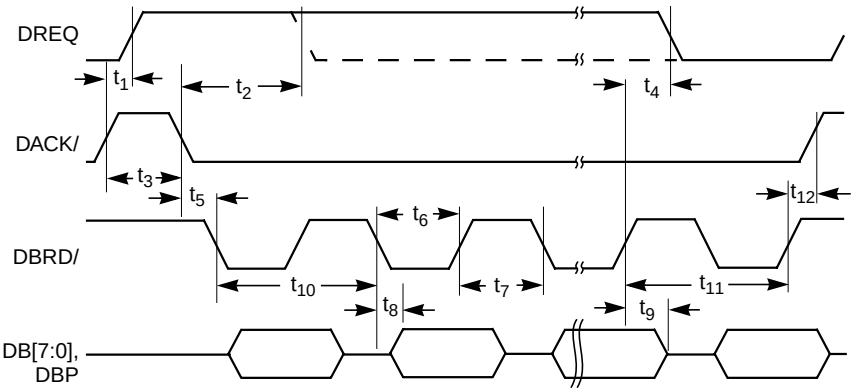


Figure 6.18 illustrates Burst Mode DMA Write, Multiplexed Mode only.

Figure 6.18 Burst Mode DMA Write, Multiplexed Mode Only

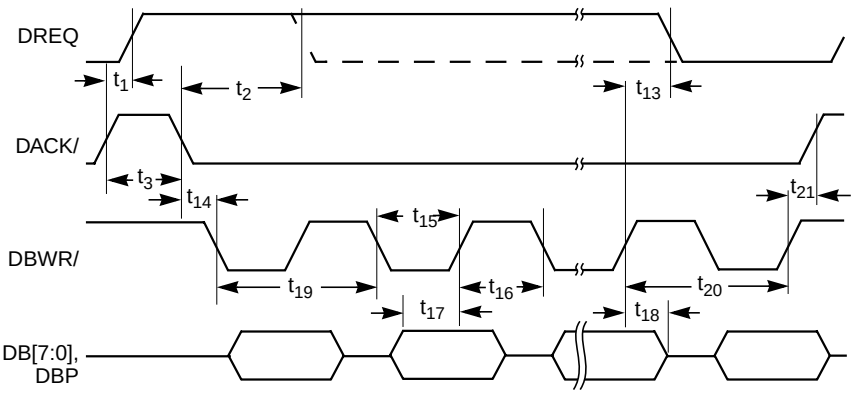


Table 6.16 lists the Burst Mode DMA Interface, Multiplexed Mode.

Table 6.16 Burst Mode DMA Interface (Multiplexed Mode)

Symbol	Parameter	Min	Max	Unit	Notes
t_1	DACK/ HIGH to DREQ HIGH	30	–	ns	1
t_2	DACK/ LOW to DREQ LOW	–	30	ns	2
t_3	DACK/ HIGH to DACK/ LOW	t_{CP} +5	–	ns	–
t_4	DBRD/ HIGH to DREQ LOW	–	2 t_{CP} + t_{CL} +30	ns	3
t_5	DACK/ LOW to DBRD/ LOW	0	–	ns	–
t_6	DBRD/ pulse width	t_{CP} +5	–	ns	–
t_7	DBRD/ HIGH to DBRD/ LOW	t_{CP} +5	–	ns	–
t_8	DBRD/ LOW to data valid	–	30	ns	–
t_9	DBRD/ HIGH to data bus disable	–	30	ns	–
t_{10}	DBRD/ LOW to DBRD/ LOW	3 t_{CP}	–	ns	–
t_{11}	DBRD/ HIGH to DBRD/ HIGH	3 t_{CP}	–	ns	–
t_{12}	DBRD/ HIGH to DACK/ HIGH	0	–	ns	–
t_{13}	DBWR/ HIGH to DREQ LOW	–	2 t_{CP} + t_{CL} +30	ns	3
t_{14}	DACK/ LOW to DBWR/ LOW	0	–	ns	–
t_{15}	DBWR/ pulse width	t_{CP} +5	–	ns	–
t_{16}	DBWR/ HIGH to DBWR/ LOW	t_{CP} +5	–	ns	–
t_{17}	Data setup to DBWR/ HIGH	10	–	ns	–
t_{18}	Data hold from DBWR/ HIGH	4	–	ns	–
t_{19}	DBWR/ LOW to DBWR/ LOW	3 t_{CP}	–	ns	–
t_{20}	DBWR/ HIGH to DBWR/ HIGH	3 t_{CP}	–	ns	–
t_{21}	DBWR/ HIGH to DACK/ HIGH	0	–	ns	–

1. Assertion pending. If the FIFO is empty during DMA read, or full during DMA write, then assertion is not pending.
2. Single DMA transfer only.
3. Multiple DMA transfers only.

6.3.6 Burst Mode DMA Interface (Nonmultiplexed Mode)

Figure 6.19 illustrates the Burst Mode DMA Read, Nonmultiplexed Mode only.

Figure 6.19 Burst Mode DMA Read, Nonmultiplexed Mode Only

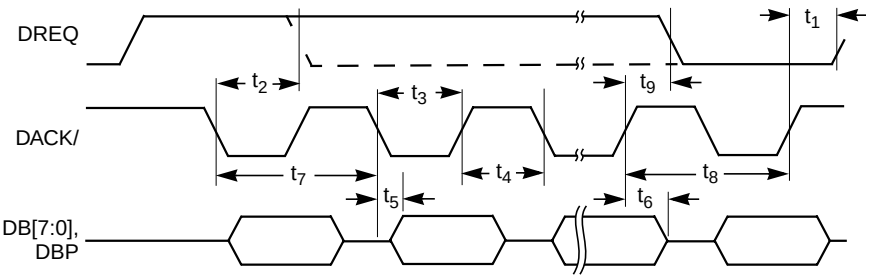


Figure 6.20 illustrates the Burst Mode DMA Write, Nonmultiplexed Mode only.

Figure 6.20 Burst Mode DMA Write, Nonmultiplexed Mode Only

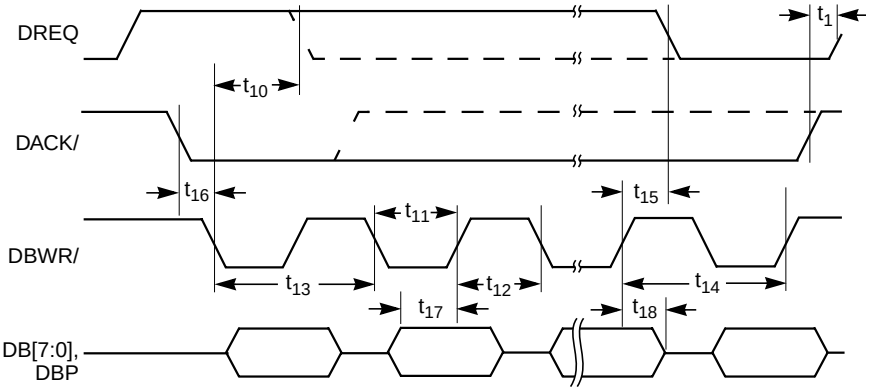


Table 6.17 lists the Burst Mode DMA Interface, Nonmultiplexed Mode.

Table 6.17 Burst Mode DMA Interface (Nonmultiplexed Mode)

Symbol	Parameter	Min	Max	Unit	Notes
t_1	DACK/ HIGH to DREQ HIGH	30	–	ns	1
t_2	DACK/ LOW to DREQ LOW	–	30	ns	2
t_3	DACK/ pulse width	t_{CP} +5	–	ns	3
t_4	DACK/ HIGH to DACK/ LOW	t_{CP} +5	–	ns	–
t_5	DACK/ LOW to data valid	–	30	ns	–
t_6	DACK/ HIGH to data bus disable	–	30	ns	–
t_7	DACK/ LOW to DACK/ LOW	3 t_{CP}	–	ns	3
t_8	DACK/ HIGH to DACK/ HIGH	3 t_{CP}	–	ns	3
t_9	DACK/ HIGH to DREQ LOW	–	2 t_{CP} + t_{CL} +30	ns	4
t_{10}	DBWR/ LOW to DREQ LOW	–	30	ns	2, 5
t_{11}	DBWR/ pulse width	t_{CP} +5	–	ns	5
t_{12}	DBWR/ HIGH to DBWR/ LOW	t_{CP} +5	–	ns	5
t_{13}	DBWR/ LOW to DBWR/ LOW	3 t_{CP}	–	ns	5
t_{14}	DBWR/ HIGH to DBWR/ HIGH	3 t_{CP}	–	ns	5
t_{15}	DBWR/ HIGH to DREQ LOW	–	2 t_{CP} + t_{CL} +30	ns	4, 5
t_{16}	DACK/ LOW to DBWR/ LOW	0	–	ns	5, 6
t_{17}	Data setup to DBWR/ HIGH	15	–	ns	5
t_{18}	Data hold from DBWR/ HIGH	4	–	ns	5

1. Assertion pending. If the FIFO is empty during DMA read, or full during DMA write, then assertion is not pending.
2. Single DMA transfer only.
3. DACK/ is used for DMA reads and writes. For DMA reads, DACK/ must toggle, and is assumed to be coincident with an external read signal.
4. Multiple DMA transfers only.
5. Either DACK/ or DBWR/ may toggle during a burst write. Timings are shown for DBWR/ toggling; however, DACK/ and DBWR/ may be interchanged in Figure 6.20 and Table 6.17.
6. DBWR/ LOW may precede DACK/ LOW.

6.4 SCSI Timing Diagrams

Figures 6.21 through 6.26 and tables 6.18 through 6.23 describe the LSI53CF92A SCSI timing.

Figure 6.21 Initiator Asynchronous Send

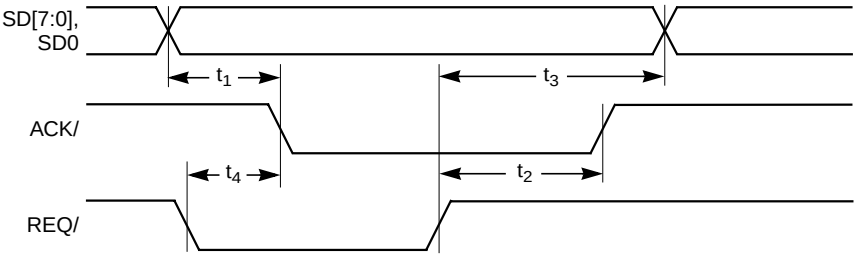


Table 6.18 Initiator Asynchronous Send Timings

Symbol	Parameter	Min	Max	Unit
t_1	Data setup to ACK/ LOW	60	–	ns
t_2	ACK/ HIGH from REQ/ HIGH	10	–	ns
t_3	Data hold from REQ/ HIGH	5	–	ns
t_4	ACK/ LOW from REQ/ LOW	10	–	ns

Figure 6.22 Initiator Asynchronous Receive

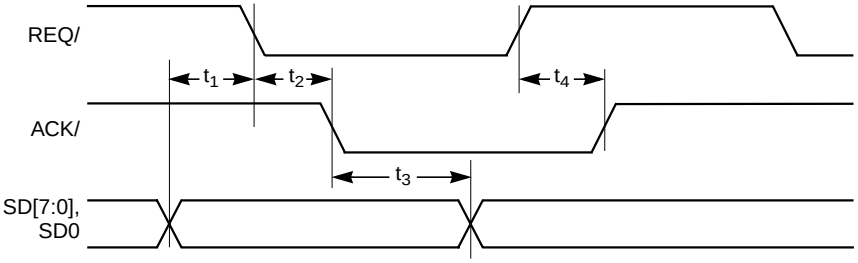


Table 6.19 Initiator Asynchronous Receive Timings

Symbol	Parameter	Min	Max	Unit
t_1	Data setup to REQ/ LOW	0	–	ns
t_2	ACK/ LOW from REQ/ LOW	10	–	ns
t_3	Data hold from ACK/ LOW	0	–	ns
t_4	ACK/ HIGH from REQ/ HIGH	10	–	ns

Figure 6.23 Target Asynchronous Send

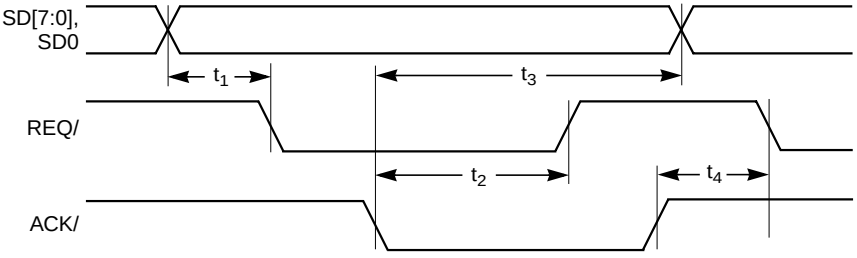


Table 6.20 Target Asynchronous Send Timings

Symbol	Parameter	Min	Max	Unit
t_1	Data setup to REQ/ LOW	60	–	ns
t_2	REQ/ HIGH from ACK/ LOW	10	–	ns
t_3	Data hold from ACK/ LOW	5	–	ns
t_4	REQ/ LOW from ACK/ HIGH	10	–	ns

Figure 6.24 Target Asynchronous Receive

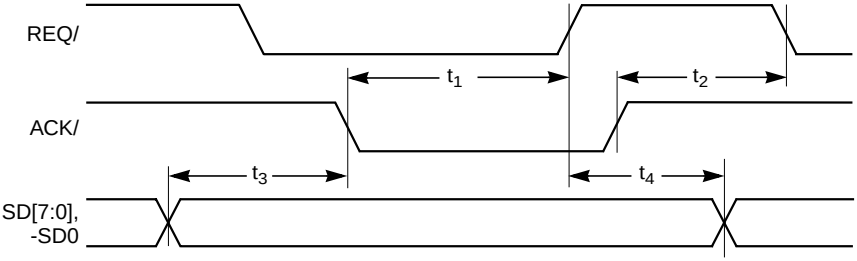


Table 6.21 Target Asynchronous Receive Timings

Symbol	Parameter	Min	Max	Unit
t_1	REQ/ HIGH from ACK/ LOW	10	–	ns
t_2	REQ/ LOW from ACK/ HIGH	10	–	ns
t_3	Data setup to ACK/ LOW	0	–	ns
t_4	Data hold from REQ/ HIGH	0	–	ns

Figure 6.25 Target and Initiator Synchronous Output

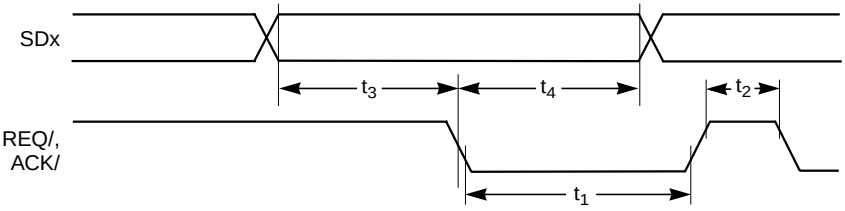


Figure 6.26 Target and Initiator Synchronous Input

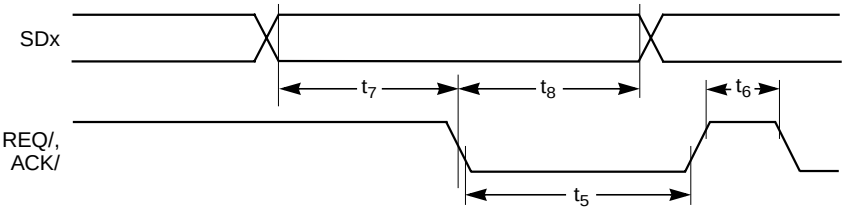


Table 6.22 SCSI-1 SE Transfers (5 Mbytes/s)

Symbol	Parameter	Min	Max	Unit
t_1	REQ/ or ACK/ assertion period	90	–	ns
t_2	REQ/ or ACK/ negation period	90	–	ns
t_3	Data setup to REQ/ or ACK/ LOW	65	–	ns
t_4	Data hold from ACK/ or REQ/ LOW	100	–	ns
t_5	REQ/ or ACK/ assertion period	90	–	ns
t_6	REQ/ or ACK/ negation period	90	–	ns
t_7	Data setup to REQ/ LOW or ACK/ LOW	0	–	ns
t_8	Data hold from REQ/ LOW or ACK/ LOW	45	–	ns

Table 6.23 Fast SCSI-2 SE Transfers (10 Mbytes/s)

Symbol	Parameter	Min	Max	Unit
t_1	REQ/ or ACK/ assertion period	32	–	ns
t_2	REQ/ or ACK/ negation period	32	–	ns
t_3	Data setup to REQ/ or ACK/ LOW	25	–	ns
t_4	Data hold from REQ/ or ACK/ LOW	35	–	ns
t_5	REQ/ or ACK/ assertion period	20	–	ns
t_6	REQ/ or ACK/ negation period	20	–	ns
t_7	Data setup to REQ/ LOW or ACK/ LOW	0	–	ns
t_8	Data hold from REQ/ LOW or ACK/ LOW	10	–	ns

6.5 Package Drawings

Figure 6.27 is the 64-Pin Plastic Quad Flat Pack package drawing and Figure 6.28 is the 64-Pin Thin Quad Flat Pack drawing for the LSI53CF92A.

Figure 6.27 64-Pin Plastic Quad Flat Pack

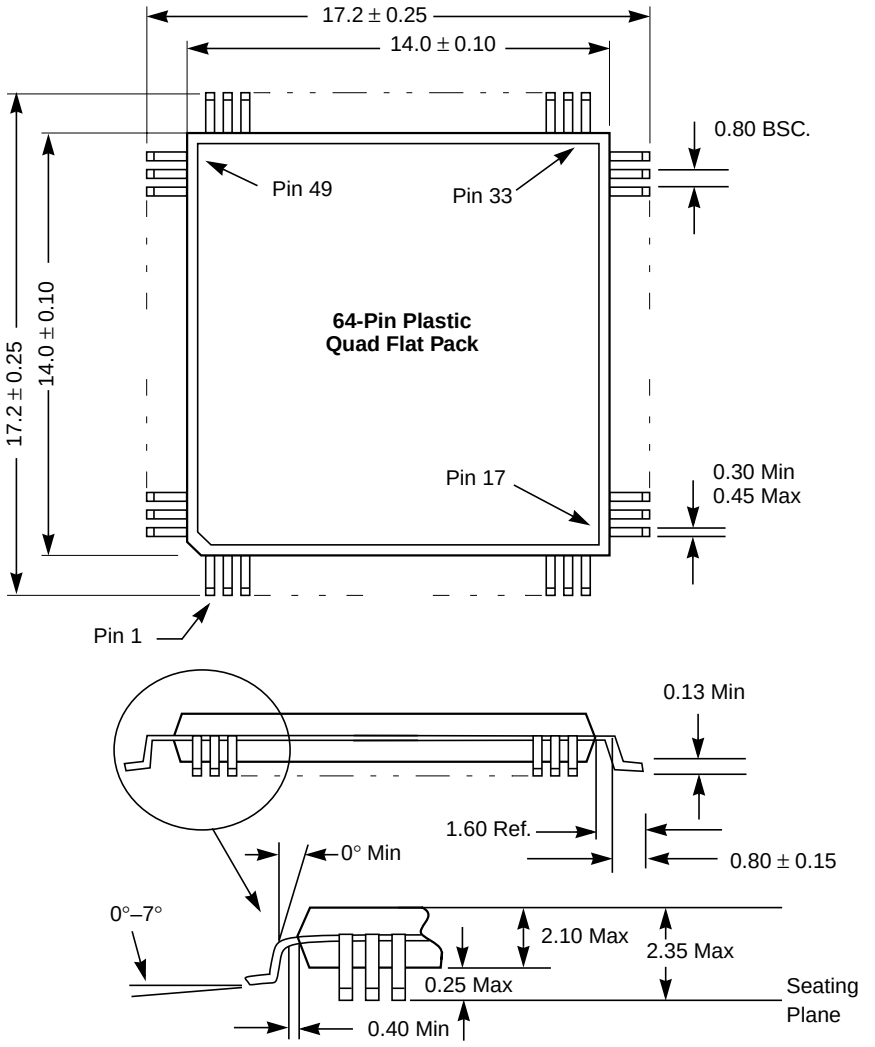
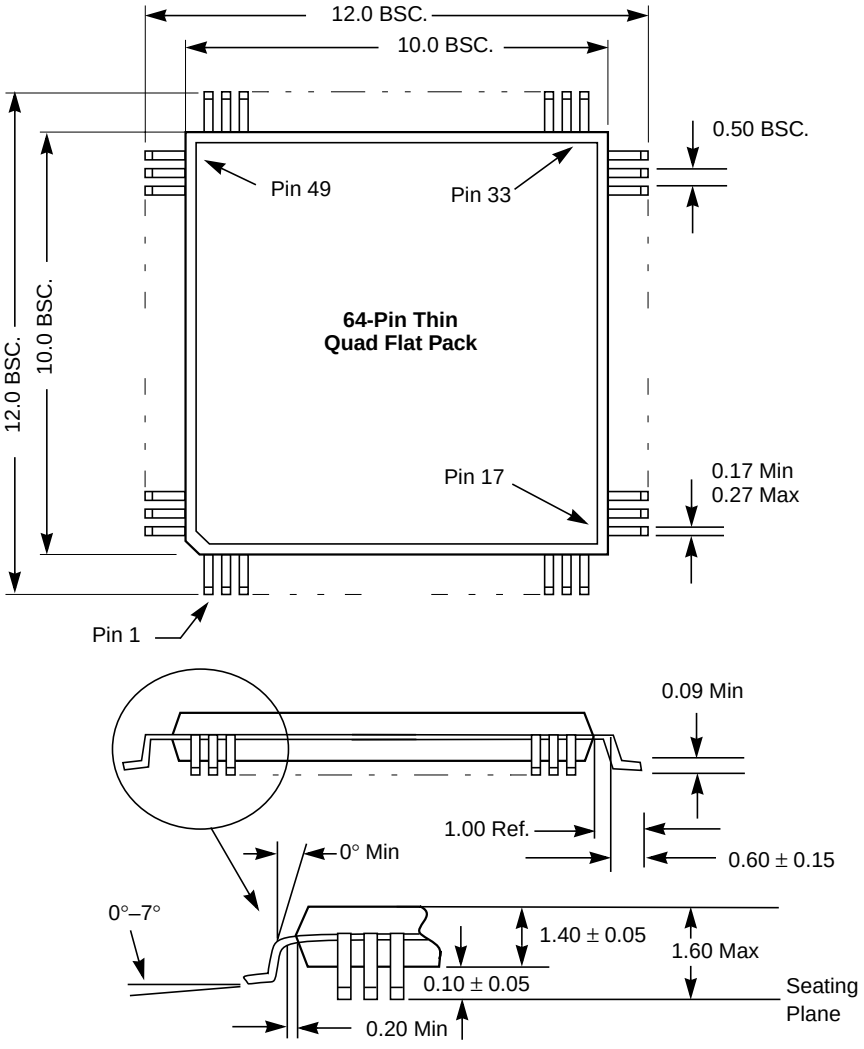


Figure 6.28 64-Pin Thin Quad Flat Pack



Appendix A
Register Map

This is the register map for the registers in Chapter 4, “Registers.”

Table A.1 Register Map

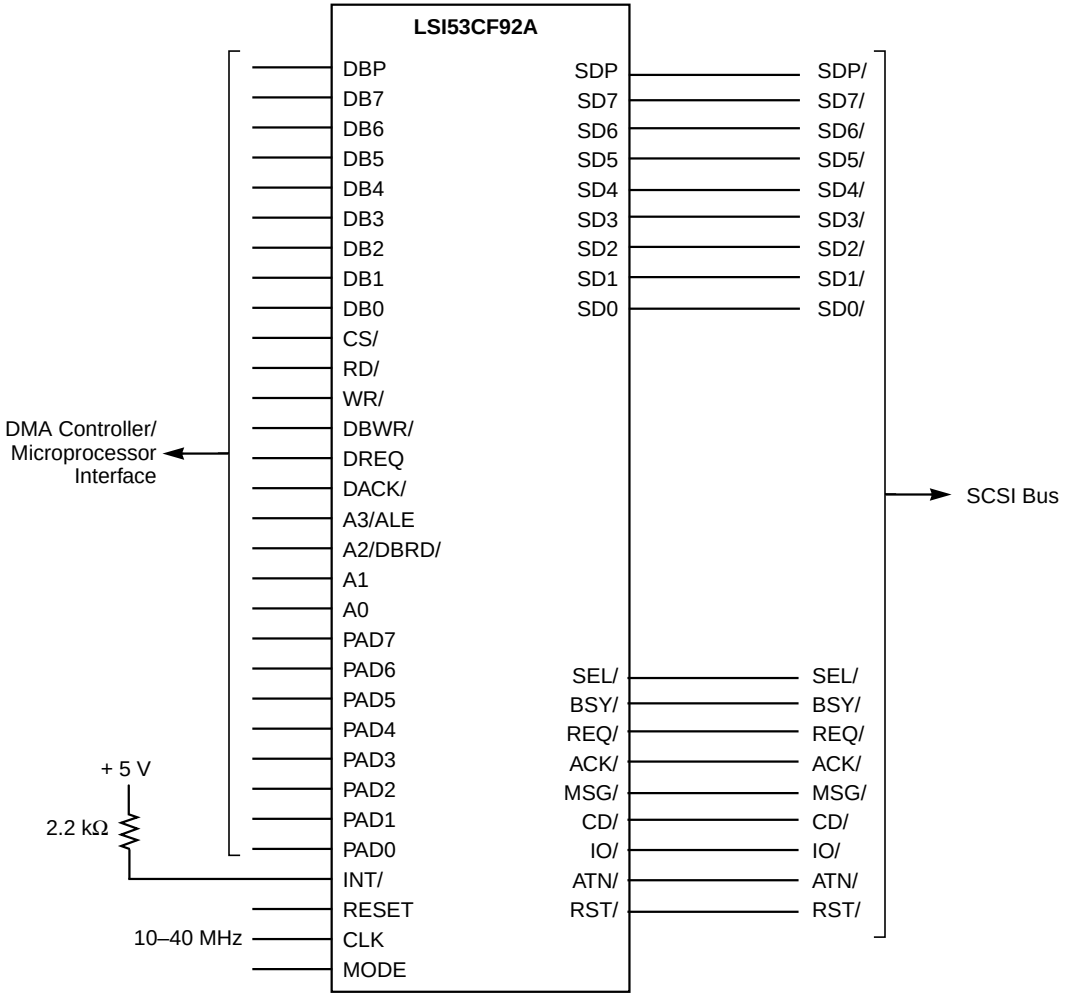
Register Name	Address	Read/Write	Page
Clock Conversion	0x09	Write Only	4-26
Command	0x03	Read/Write	4-8
Configuration 1 (Config 1)	0x08	Read/Write	4-24
Configuration 2 (Config 2)	0x0B	Read/Write	4-28
Configuration 3 (Config 3)	0x0C	Read/Write	4-30
Configuration 4 (Config 4)	0x0D	Read/Write	4-34
Destination Bus ID	0x04	Write Only	4-13
FIFO	0x02	Read/Write	4-7
FIFO Flags	0x07	Read Only	4-21
Interrupt	0x05	Read Only	4-14
Reserved	0x0F	–	4-36
Sequence Step	0x06	Read Only	4-17
Status	0x04	Read Only	4-10
Synchronous Offset	0x07	Write Only	4-21
Synchronous Transfer Period	0x06	Write Only	4-18
Test	0x0A	Write Only	4-27
Time-Out	0x05	Write Only	4-16
Transfer Counter	0x00–0x01	Write Only	4-4

Table A.1 Register Map (Cont.)

Register Name	Address	Read/Write	Page
Transfer Counter	0x00–0x01	Read Only	4-5
Transfer Counter High/ID	0x0E	Read/Write	4-35
SCAM Register Set			
SCSI Bus Control Lines (SBCL)	0x0B	Read Only	4-41
SCSI Bus Data Lines (SBDL)	0x0F	Read Only	4-42
SCSI Control (SCONTROL)	0x08	Read/Write	4-37
SCSI Output Control Latch (SOCL)	0x0A	Read/Write	4-40
SCSI Output Data Latch (SODL)	0x0E	Read/Write	4-42
SCSI Status (SSTATUS)	0x09	Read Only	4-39

Appendix B
Wiring Diagram

Figure B.1 Single-Pin, SE SCSI Bus Interface Wiring Diagram



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