

Linear Systems Ultra Low Leakage Low Drift Monolithic Dual JFET

The LS840 is a high-performance monolithic dual JFET featuring extremely low noise, tight offset voltage and low drift over temperature specifications, and is targeted for use in a wide range of precision instrumentation applications. The LS840 features a 5-mV offset and 5- $\mu\text{V}/^\circ\text{C}$ drift.

The 8 Pin P-DIP and 8 Pin SOIC provide ease of manufacturing, and the symmetrical pinout prevents improper orientation.

(See Packaging Information).

LS840 Applications:

- Wideband Differential Amps
- High-Speed, Temp-Compensated Single-Ended Input Amps
- High-Speed Comparators
- Impedance Converters and vibrations detectors.

FEATURES

LOW DRIFT	$ V_{GS1-2}/T \leq 5\mu\text{V}/^\circ\text{C}$
LOW LEAKAGE	$I_G = 10\text{pA TYP.}$
LOW NOISE	$e_n = 8\text{nV}/\sqrt{\text{Hz}}$ TYP.
LOW OFFSET VOLTAGE	$ V_{GS1-2} = 2\text{mV TYP.}$

ABSOLUTE MAXIMUM RATINGS @ 25°C (unless otherwise noted)

Maximum Temperatures

Storage Temperature	-65°C to +150°C
Operating Junction Temperature	+150°C

Maximum Voltage and Current for Each Transistor – Note 1

-V _{GSS}	Gate Voltage to Drain or Source	60V
-V _{DSO}	Drain to Source Voltage	60V
-I _{G(f)}	Gate Forward Current	50mA

Maximum Power Dissipation

Device Dissipation @ Free Air – Total	400mW @ +125°C
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MATCHING CHARACTERISTICS @ 25°C UNLESS OTHERWISE NOTED

SYMBOL	CHARACTERISTICS	VALUE	UNITS	CONDITIONS
$ V_{GS1-2}/T \text{ max.}$	DRIFT VS. TEMPERATURE	5	$\mu\text{V}/^\circ\text{C}$	$V_{DG}=20\text{V}, I_D=200\mu\text{A}$ $T_A=-55^\circ\text{C}$ to $+125^\circ\text{C}$
$ V_{GS1-2} \text{ max.}$	OFFSET VOLTAGE	5	mV	$V_{DG}=20\text{V}, I_D=200\mu\text{A}$

ELECTRICAL CHARACTERISTICS @ 25°C (unless otherwise noted)

SYMBOL	CHARACTERISTICS	MIN.	TYP.	MAX.	UNITS	CONDITIONS
BV _{GSS}	Breakdown Voltage	60	60	--	V	V _{DS} = 0 I _D =1nA
BV _{GGO}	Gate-To-Gate Breakdown	60	--	--	V	I _G = 1nA I _D = 0 I _S = 0
TRANSCONDUCTANCE						
Y _{FSS}	Full Conduction	1000	--	4000	μmho	V _{DG} = 20V V _{GS} = 0V f = 1kHz
Y _{FS}	Typical Operation	500	--	1000	μmho	V _{DG} = 20V I _D = 200μA
Y _{FS1-2} / Y _{FS}	Mismatch	--	0.6	3	%	
DRAIN CURRENT						
I _{DSS}	Full Conduction	0.5	2	5	mA	V _{DG} = 20V V _{GS} = 0V
I _{DSS1-2} / I _{DSS}	Mismatch at Full Conduction	--	1	5	%	
GATE VOLTAGE						
V _{GS(off)} or V _p	Pinchoff voltage	1	2	4.5	V	V _{DS} = 20V I _D = 1nA
V _{GS(on)}	Operating Range	0.5	--	4	V	V _{DS} =20V I _D =200μA
GATE CURRENT						
-I _G max.	Operating	--	10	50	pA	V _{DG} = 20V I _D = 200μA
-I _G max.	High Temperature	--	--	50	nA	T _A = +125°C
-I _G max.	Reduced V _{DG}	--	5	--	pA	V _{DG} = 10V I _D = 200μA
-I _{GSS} max.	At Full Conduction	--	--	100	pA	V _{DG} = 20V , V _{DS} =0
OUTPUT CONDUCTANCE						
Y _{OSS}	Full Conduction	--	--	10	μmho	V _{DG} = 20V V _{GS} = 0V
Y _{OS}	Operating	--	0.1	1	μmho	V _{DG} = 20V I _D = 200μA
Y _{OS1-2}	Differential	--	0.01	0.1	μmho	
CMR	COMMON MODE REJECTION -20 log V _{GS1-2} / V _{DS}	--	100	--	dB	ΔV _{DS} = 10 to 20V I _D =200μA
	-20 log V _{GS1-2} / V _{DS}	--	75	--		ΔV _{DS} = 5 to 10V I _D =200μA
NF	NOISE Figure	--	--	0.5	dB	V _{DS} = 20V V _{GS} = 0V R _G = 10MΩ f= 100Hz NBW= 6Hz
e _n	Voltage	--	--	10	nV/√Hz	V _{DS} =20V I _D =200μA f=1kHz NBW=1Hz
		--	--	15		V _{DS} =20V I _D =200μA f=10Hz NBW=1Hz
CAPACITANCE						
C _{ISS}	Input	--	4	10	pF	V _{DS} = 20V, I _D =200μA
C _{RSS}	Reverse Transfer	--	1.2	5		
C _{DD}	Drain-to-Drain	--	0.1	--		

Note 1 – These ratings are limiting values above which the serviceability of any semiconductor may be impaired

Available Packages:

LS840 / LS840 in PDIP & SOIC
LS840 / LS840 available as bare die
Please contact [Micross](http://www.micross.com) for full package and die dimensions

PDIP & SOIC (Top View)

