

Linear Systems Ultra Low Leakage Low Drift Monolithic Dual JFET

The LS832 is a high-performance monolithic dual JFET featuring extremely low noise, tight offset voltage and low drift over temperature specifications, and is targeted for use in a wide range of precision instrumentation applications. The LS832 features a 25-mV offset and 20- $\mu\text{V}/^\circ\text{C}$ drift.

The 8 Pin P-DIP and 8 Pin SOIC provide ease of manufacturing, and the symmetrical pinout prevents improper orientation.

(See Packaging Information).

LS832 Applications:

- Wideband Differential Amps
- High-Speed, Temp-Compensated Single-Ended Input Amps
- High-Speed Comparators
- Impedance Converters and vibrations detectors.

FEATURES

ULTRA LOW DRIFT	$ V_{GS1-2}/T \leq 20\mu\text{V}/^\circ\text{C}$
ULTRA LOW LEAKAGE	$I_G = 80\text{fA TYP.}$
LOW NOISE	$e_n = 70\text{nV}/\sqrt{\text{Hz}}$ TYP.
LOW CAPACITANCE	$C_{ISS} = 3\text{pF MAX.}$

ABSOLUTE MAXIMUM RATINGS @ 25°C (unless otherwise noted)

Maximum Temperatures

Storage Temperature	-65°C to +150°C
Operating Junction Temperature	+150°C

Maximum Voltage and Current for Each Transistor – Note 1

$-V_{GSS}$	Gate Voltage to Drain or Source	40V
$-V_{DSO}$	Drain to Source Voltage	40V
$-I_{G(f)}$	Gate Forward Current	10mA
$-I_G$	Gate Reverse Current	10 μA

Maximum Power Dissipation

Device Dissipation @ Free Air – Total	400mW @ +125°C
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MATCHING CHARACTERISTICS @ 25°C UNLESS OTHERWISE NOTED

SYMBOL	CHARACTERISTICS	VALUE	UNITS	CONDITIONS
$ V_{GS1-2}/T \text{ max.}$	DRIFT VS. TEMPERATURE	20	$\mu\text{V}/^\circ\text{C}$	$V_{DG}=10\text{V}$, $I_D=30\mu\text{A}$ $T_A=-55^\circ\text{C}$ to $+125^\circ\text{C}$
$ V_{GS1-2} \text{ max.}$	OFFSET VOLTAGE	25	mV	$V_{DG}=10\text{V}$, $I_D=30\mu\text{A}$

ELECTRICAL CHARACTERISTICS @ 25°C (unless otherwise noted)

SYMBOL	CHARACTERISTICS	MIN.	TYP.	MAX.	UNITS	CONDITIONS
BV_{GSS}	Breakdown Voltage	40	60	--	V	$V_{DS} = 0$ $I_D=1\text{nA}$
BV_{GGO}	Gate-To-Gate Breakdown	40	--	--	V	$I_G = 1\text{nA}$ $I_D = 0$ $I_S = 0$
TRANSCONDUCTANCE						
Y_{fss}	Full Conduction	70	300	500	μmho	$V_{DG}=10\text{V}$ $V_{GS}=0\text{V}$ $f=1\text{kHz}$
Y_{fs}	Typical Operation	50	100	200	μmho	$V_{DG}=10\text{V}$ $I_D=30\mu\text{A}$ $f=1\text{kHz}$
$ Y_{FS1-2}/Y_{FS} $	Mismatch	--	0.6	3	%	
DRAIN CURRENT						
I_{DSS}	Full Conduction	0.5	--	10	mA	$V_{DG}=10\text{V}$ $V_{GS}=0\text{V}$
$ I_{DSS1-2}/I_{DSS} $	Mismatch at Full Conduction	--	1	5	%	
GATE VOLTAGE						
$V_{GS(off)}$ or V_p	Pinchoff voltage	0.6	2	4.5	V	$V_{DS}=10\text{V}$ $I_D=1\text{nA}$
$V_{GS(on)}$	Operating Range	--	--	4	V	$V_{DS}=10\text{V}$ $I_D=30\mu\text{A}$
GATE CURRENT						
$-I_{Gmax.}$	Operating	--	--	0.1	pA	$V_{DG}=10\text{V}$ $I_D=30\mu\text{A}$
$-I_{Gmax.}$	High Temperature	--	--	0.1	nA	$T_A=+125^\circ\text{C}$
$-I_{GSSmax.}$	At Full Conduction	--	--	0.2	pA	$V_{DS}=0$
$-I_{GSSmax.}$	High Temperature	5	5	0.5	nA	$V_{GS}=0\text{V}$, $V_{GS}=-20\text{V}$, $T_A=+125^\circ\text{C}$
I_{GGO}	Gate-to-Gate Leakage	--	1	--	pA	$V_{GG}=20\text{V}$
OUTPUT CONDUCTANCE						
Y_{OSS}	Full Conduction	--	--	5	μmho	$V_{DG}=10\text{V}$ $V_{GS}=0\text{V}$
Y_{OS}	Operating	--	--	0.5	μmho	$V_{DG}=10\text{V}$ $I_D=30\mu\text{A}$
COMMON MODE REJECTION						
CMR	$-20 \log V_{GS1-2}/V_{DS} $	--	90	--	dB	$\Delta V_{DS}=10$ to 20V $I_D=30\mu\text{A}$
	$-20 \log V_{GS1-2}/V_{DS} $	--	90	--	dB	$\Delta V_{DS}=5$ to 10V $I_D=30\mu\text{A}$
NOISE						
NF	Figure	--	--	1	dB	$V_{DS}=10\text{V}$ $V_{GS}=0\text{V}$ $R_G=10\text{M}\Omega$ $f=100\text{Hz}$ $\text{NBW}=6\text{Hz}$
e_n	Voltage	--	20	70	nV/ $\sqrt{\text{Hz}}$	$V_{DS}=10\text{V}$ $I_D=30\mu\text{A}$ $f=10\text{Hz}$ $\text{NBW}=1\text{Hz}$
CAPACITANCE						
C_{ISS}	Input	--	--	3	pF	$V_{DS}=10\text{V}$, $V_{GS}=0\text{V}$, $f=1\text{MHz}$
C_{RSS}	Reverse Transfer	--	--	1.5	pF	$V_{DS}=10\text{V}$, $V_{GS}=0\text{V}$, $f=1\text{MHz}$
C_{DD}	Drain-to-Drain	--	--	0.1	pF	$V_{DS}=10\text{V}$, $I_D=30\mu\text{A}$

Note 1 – These ratings are limiting values above which the serviceability of any semiconductor may be impaired

Available Packages:

LS832 / LS832 in PDIP & SOIC
LS832 / LS832 available as bare die
Please contact [Micross](http://www.micross.com) for full package and die dimensions

PDIP & SOIC (Top View)

