PRELIMINARY PRODUCT SPECIFICATIONS

SHARP®

Integrated Circuits Group

LRS1B07

Stacked Chip

128M (x16) Flash and 64M (x16) SCRAM and 8M (×16) SRAM

(Model No.: LRS1B07)

Spec No.: MFM2-J14109B
Issue Date: October 18, 2002

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SPEC No.	MFM2-J14109B

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To; ______________

PRELIMINARY

SPECIFICATIONS

Product Type 64M (x16) Flash Memory +64M (x16) Flash Memory
64M (x16) Smartcombo RAM +8M (x16) SRAM

LRS1B07

Model No. (LRS1B07)

This device specification is subject to change without notice.

*This specifications contains 88 pages including the cover and appendix.
*Refer to LH28F320BF, LH28F640BF, LH28F128BF Series Appendix (FUM00701).

CUSTOMERS ACCEPTANCE

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- Audiovisual equipment
- Home appliance
- Communication equipment other than for trunk lines

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- Please direct all queries regarding the products covered herein to a sales representative of the company.

Contents

1. Description

The LRS1B07 is a combination memory organized as 4,194,304 x16 bit flash memory, 4,194,304 x16 bit flash memory, 4,194,304 x16 bit Smartcombo RAM and 524,288 x16 bit static RAM in one package.

Features

- -Power supply • • • • 2.7V to 3.1V
- -Operating temperature • • • • -25°C to +85°C
- -Not designed or rated as radiation hardened
- -72 pin CSP(LCSP072-P-0811) plastic package
- -Flash memory has P-type bulk silicon, and Smartcombo RAM has P-type bulk silicon, and SRAM has P-type bulk silicon
- -Flash memory and Smartcombo RAM share one power supply pin (F/SC-V_{CC})
- -For specifications of Flash memory, Smartcombo RAM and SRAM, refer to specification of each chip

Standby current of Flash memory and Smartcombo RAM

- -Power supply current • • • • 250 µA (Max.)

Flash Memory 1 (F_1: 64M (x16) bit Flash Memory)

- -Access Time (Address) • • • • 65 ns (Max.)
- -Power supply current (The current for F/SC-V_{CC} pin and V_{PP} pin)
  - Read • • • • 25 mA (Max. t_{CYCLE} = 200ns, CMOS Input)
  - Word write • • • • 60 mA (Max.)
  - Block erase • • • • 30 mA (Max.)

Flash Memory 2 (F_2: 64M (x16) bit Flash Memory)

- -Access Time (Address) • • • • 65 ns (Max.)
- -Power supply current (The current for F/SC-V_{CC} pin and V_{PP} pin)
  - Read • • • • 25 mA (Max. t_{CYCLE} = 200ns, CMOS Input)
  - Word write • • • • 60 mA (Max.)
  - Block erase • • • • 30 mA (Max.)

Smartcombo RAM (64M (x16) bit Smartcombo RAM)

- -Access Time (Address) • • • • 65 ns (Max.)
- -Cycle time • • • • 65 ns (Min.)
- -Power Supply current
  - Operating current • • • • 50 mA (Max. t_{RC}, t_{WC} = Min.)

SRAM (8M (x16) bit SRAM)

- -Access Time (Address) • • • • 65 ns (Max.)
- -Power Supply current
  - Operating current • • • • 45 mA (Max. t_{RC}, t_{WC} = Min.)
  - Standby current • • • • 15 µA (Max.)

2. Pin Configuration

INDEX (TOP View)

	1	2	3	4	5	6	7	8	9	10	11	12
A	NC	NC	A_{20}	A_{11}	A_{15}	A_{14}	A_{13}	A_{12}	GND	NC	NC	NC
B			A_{16}	A_{8}	A_{10}	A_{9}	DQ_{15}	S-$\overline{WE}$	DQ_{14}	DQ_{7}		
C			F-$\overline{WE}$	RY/$\overline{BY}$	A_{21}	S-A_{17}	DQ_{13}	DQ_{6}	DQ_{4}	DQ_{5}		
D			GND	$\overline{RST}$	T_{1}	T_{2}	DQ_{12}	CE_{2}	S-V_{CC}	F/SC-V_{CC}		
E			$\overline{WP}$	V_{PP}	A_{19}	DQ_{11}	F/SC-V_{CC}	DQ_{10}	DQ_{2}	DQ_{3}		
F			$\overline{LB}$	$\overline{UB}$	S-$\overline{OE}$	T_{3}	DQ_{9}	DQ_{8}	DQ_{0}	DQ_{1}		
G			A_{18}	F-A_{17}	A_{7}	A_{6}	A_{3}	A_{2}	A_{1}	SC-$\overline{CE}_{1}$		
H	NC	NC	F_{2}-$\overline{CE}$	A_{5}	A_{4}	A_{0}	F_{1}-$\overline{CE}$	GND	F-$\overline{OE}$	S-$\overline{CE}_{1}$	NC	NC

Note) From T_1 to T_3 pins are needed to be open.
Two NC pins at the corner are connected.
Do not float any GND pins.

Pin	Description	Type
A_0 to A_{16}, A_{18}	Address Inputs (Common)	Input
A_{19} to A_{21}	Address Inputs (Flash, Smartcombo RAM)	Input
F-A_{17}	Address Inputs (Flash)	Input
S-A_{17}	Address Input (SRAM, Smartcombo RAM)	Input
F_1-$\overline{CE}$	Chip Enable Input (Flash - F_1 Selected)	Input
F_2-$\overline{CE}$	Chip Enable Input (Flash - F_2 Selected)	Input
SC-$\overline{CE}_1$	Chip Enable Input (Smartcombo RAM)	Input
S-$\overline{CE}_1$	Chip Enable Input (SRAM)	Input
CE_2	Chip Enable Input (SRAM), Sleep State Input (Smartcombo RAM)	Input
F-$\overline{WE}$	Write Enable Input (Flash)	Input
S-$\overline{WE}$	Write Enable Input (SRAM, Smartcombo RAM)	Input
F-$\overline{OE}$	Output Enable Input (Flash)	Input
S-$\overline{OE}$	Output Enable Input (SRAM, Smartcombo RAM)	Input
$\overline{LB}$	SRAM, Smartcombo RAM Byte Enable Input (DQ_0 to DQ_7)	Input
$\overline{UB}$	SRAM, Smartcombo RAM Byte Enable Input (DQ_8 to DQ_{15})	Input
$\overline{RST}$	Reset Power Down Input (Flash) Block erase and Write : V_{IH} Read : V_{IH} Reset Power Down : V_{IL}	Input
$\overline{WP}$	Write Protect Input (Flash) When $\overline{WP}$ is V_{IL}, locked-down blocks cannot be unlocked. Erase or program operation can be executed to the blocks which are not locked and locked-down. When $\overline{WP}$ is V_{IH}, lock-down is disabled.	Input
RY/$\overline{BY}$	Ready/Busy Output (Flash) During an Erase or Write operation : V_{OL} Block Erase and Write Suspend : High-Z (High impedance)	Open Drain Output
DQ_0 to DQ_{15}	Data Inputs and Outputs (Common)	Input / Output
F/SC-V_{CC}	Power Supply (Flash, Smartcombo RAM)	Power
S-V_{CC}	Power Supply (SRAM)	Power
V_{PP}	Monitoring Power Supply Voltage (Flash) Block Erase and Write : $V_{PP} = V_{PPH}$ All Blocks Locked : $V_{PP} < V_{PPLK}$	Input
GND	GND (Common)	Power
NC	Non Connection	-
T_1 to T_3	Test pins (Should be all open)	-

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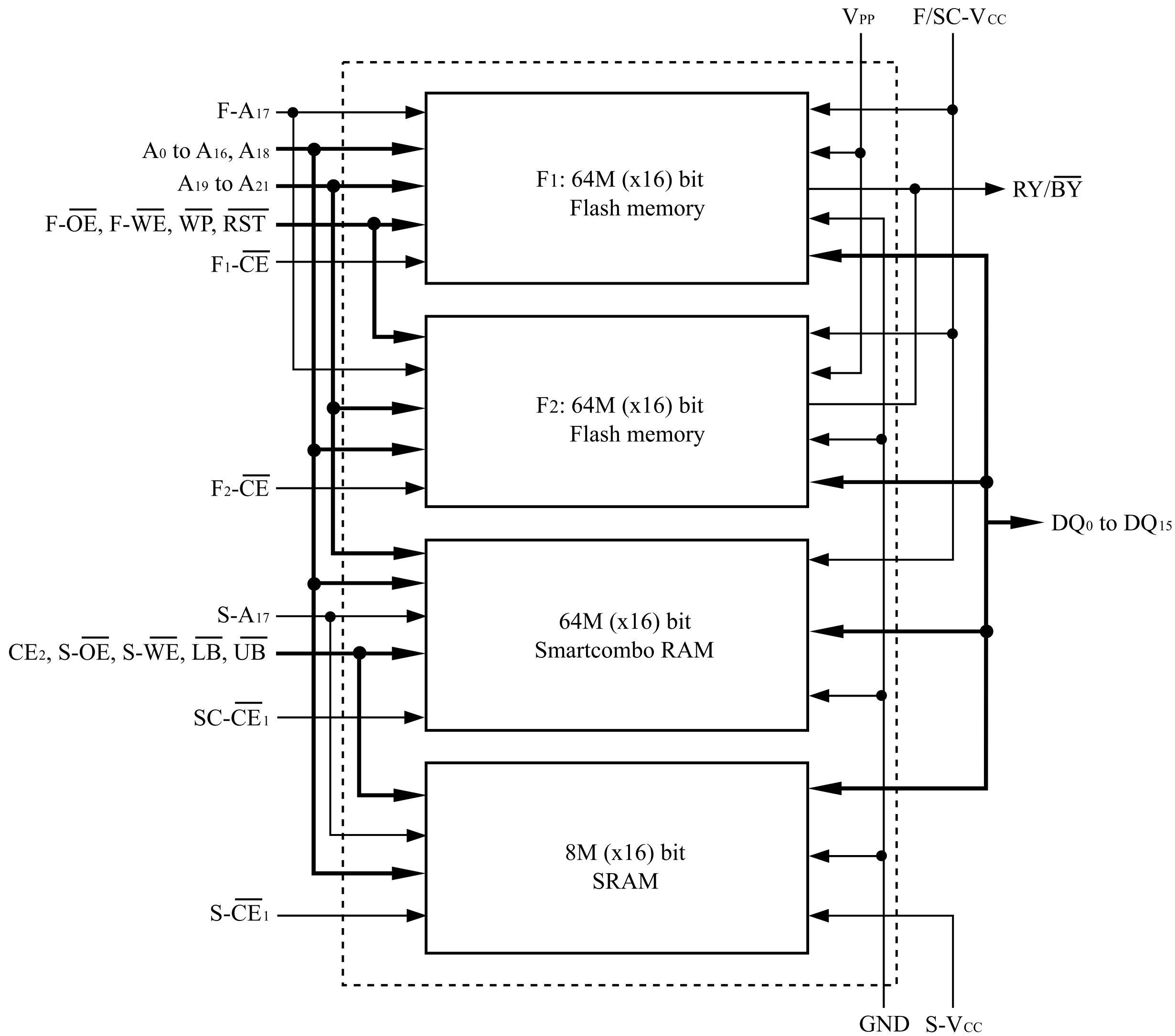
3. Block Diagram



Note: Only one among F1-CE, F2-CE, SC-CE1 and S-CE1 can be "low".
Two or more should not be "low".

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4. Absolute Maximum Ratings

Symbol	Parameter	Notes	Ratings	Unit
V_{CC}	Supply Voltage	1	-0.2 to +3.6	V
V_{IN}	Input Voltage	1,2,3	-0.2 to V_{CC} +0.3	V
T_A	Operating Temperature		-25 to +85	°C
T_{STG}	Storage Temperature		-55 to +125	°C
V_{PP}	V_{PP} Voltage	1,2	-0.2 to +3.6	V

Notes:

1. The maximum applicable voltage on any pins with respect to GND.
2. -1.0V undershoot is allowed when the pulse width is less than 5 nsec.
3. V_{IN} should not be over V_{CC} +0.3V.

5. Recommended DC Operating Conditions

(T_A = -25°C to +85°C)

Symbol	Parameter	Notes	Min.	Typ.	Max.	Unit
V_{CC}	Supply Voltage	3	2.7		3.1	V
V_{PP}	V_{PP} Voltage (Write Operation)		1.65		3.1	V
	V_{PP} Voltage (Read Operation)		0		3.1	V
V_{IH}	Input Voltage		VCC -0.4 (2)		VCC +0.2 (1)	V
V_{IL}	Input Voltage		-0.2		0.4	V

Notes:

1. V_{CC} is the lower of F/SC-V_{CC} or S-V_{CC}.
2. V_{CC} is the higher of F/SC-V_{CC} or S-V_{CC}.
3. V_{CC} includes both F/SC-V_{CC} and S-V_{CC}.

6. Flash Memory 1

6.1 Truth Table

6.1.1 Bus Operation [1]

<table>
<tr><th>Flash</th><th>Notes</th><th>F_1-$\overline{CE}$</th><th>$\overline{RST}$</th><th>F-$\overline{OE}$</th><th>F-$\overline{WE}$</th><th>DQ_0 to DQ_{15}</th></tr>
<tr><td>Read</td><td>3,5</td><td rowspan="3">L</td><td rowspan="3">H</td><td>L</td><td rowspan="2">H</td><td>(7)</td></tr>
<tr><td>Output Disable</td><td>5</td><td rowspan="2">H</td><td>High - Z</td></tr>
<tr><td>Write</td><td>2,3,4,5</td><td>L</td><td>D_{IN}</td></tr>
<tr><td>Standby</td><td>5</td><td>H</td><td>H</td><td rowspan="2">X</td><td rowspan="2">X</td><td rowspan="2">High - Z</td></tr>
<tr><td>Reset Power Down</td><td>5,6</td><td>X</td><td>L</td></tr>
</table>

Notes:

1. L = V_{IL}, H = V_{IH}, X = H or L, High-Z = High impedance. Refer to the DC Characteristics.
2. Command writes involving block erase, full chip erase, (page buffer) program are reliably executed when $V_{PP} = V_{PPH}$ and V_{CC} = 2.7V to 3.1V.
   Block erase, full chip erase, (page buffer) program with $V_{PP} < V_{PPH}$ (Min.) produce spurious results and should not be attempted.
3. Never hold F-$\overline{OE}$ low and F-$\overline{WE}$ low at the same timing.
4. Refer to Section 6.2 Command Definitions for Flash Memory valid D_{IN} during a write operation.
5. $\overline{WP}$ set to V_{IL} or V_{IH}.
6. Electricity consumption of Flash Memory is lowest when $\overline{RST}$ = GND ±0.2V.
7. Flash Read Mode

Mode	Address	DQ_0 to DQ_{15}
Read Array	X	D_{OUT}
Read Identifier Codes	See 6.2.2	See 6.2.2
Read Query	Refer to the Appendix	Refer to the Appendix

6.1.2 Simultaneous Operation Modes Allowed with Four Planes [1,2]

IF ONE PARTITION IS:	THEN THE MODES ALLOWED IN THE OTHER PARTITION IS:									
	Read Array	Read ID	Read Status	Read Query	Word Program	Page Buffer Program	Block Erase	Full Chip Erase	Program Suspend	Block Erase Suspend
Read Array	X	X	X	X	X	X	X		X	X
Read ID	X	X	X	X	X	X	X		X	X
Read Status	X	X	X	X	X	X	X	X	X	X
Read Query	X	X	X	X	X	X	X		X	X
Word Program	X	X	X	X						X
Page Buffer Program	X	X	X	X						X
Block Erase	X	X	X	X						
Full Chip Erase			X							
Program Suspend	X	X	X	X						X
Block Erase Suspend	X	X	X	X	X	X			X	

Notes:

1. “X” denotes the operation available.
2. Configurative Partition Dual Work Restrictions:
   Status register reflects partition state, not WSM (Write State Machine) state - this allows a status register for each partition.
   Only one partition can be erased or programmed at a time - no command queuing.
   Commands must be written to an address within the block targeted by that command.

6.2 Command Definitions for Flash Memory (11)

6.2.1 Command Definitions

Command	Bus Cycles Req'd	Notes	First Bus Cycle			Second Bus Cycle		
			Oper (1)	Address (2)	Data	Oper (1)	Address (2)	Data (3)
Read Array	1		Write	PA	FFH			
Read Identifier Codes	≥ 2	4	Write	PA	90H	Read	IA	ID
Read Query	≥ 2	4	Write	PA	98H	Read	QA	QD
Read Status Register	2		Write	PA	70H	Read	PA	SRD
Clear Status Register	1		Write	PA	50H			
Block Erase	2	5	Write	BA	20H	Write	BA	D0H
Full Chip Erase	2	5, 9	Write	X	30H	Write	X	D0H
Program	2	5, 6	Write	WA	40H or 10H	Write	WA	WD
Page Buffer Program	≥ 4	5, 7	Write	WA	E8H	Write	WA	N-1
Block Erase and (Page Buffer) Program Suspend	1	8, 9	Write	PA	B0H			
Block Erase and (Page Buffer) Program Resume	1	8, 9	Write	PA	D0H			
Set Block Lock Bit	2		Write	BA	60H	Write	BA	01H
Clear Block Lock Bit	2	10	Write	BA	60H	Write	BA	D0H
Set Block Lock-down Bit	2		Write	BA	60H	Write	BA	2FH
Set Partition Configuration Register	2		Write	PCRC	60H	Write	PCRC	04H

Notes:

1. Bus operations are defined in 6.1.1 Bus Operation.
2. All addresses which are written at the first bus cycle should be the same as the addresses which are written at the second bus cycle.
   X=Any valid address within the device.
   PA=Address within the selected partition.
   IA=Identifier codes address (See 6.2.2 Identifier Codes for Read Operation).
   QA=Query codes address. Refer to the LH28F320BF, LH28F640BF, LH28F128BF series Appendix for details.
   BA=Address within the block being erased, set/cleared block lock bit or set block lock-down bit.
   WA=Address of memory location for the Program command or the first address for the Page Buffer Program command.
   PCRC=Partition configuration register code presented on the address A_0-A_{15}.
3. ID=Data read from identifier codes (See 6.2.2 Identifier Codes for Read Operation).
   QD=Data read from query database. Refer to the LH28F320BF, LH28F640BF, LH28F128BF series Appendix for details.
   SRD=Data read from status register. See 6.3 Register Definition for a description of the status register bits.
   WD=Data to be programmed at location WA. Data is latched on the rising edge of F-$\overline{WE}$ or F_1-$\overline{CE}$ (whichever goes high first) during command write cycles.
   N-1=N is the number of the words to be loaded into a page buffer.
4. Following the Read Identifier Codes command, read operations access manufacturer code, device code, block lock configuration code, partition configuration register code (See 6.2.2 Identifier Codes for Read Operation).
   The Read Query command is available for reading CFI (Common Flash Interface) information.
5. Block erase, full chip erase or (page buffer) program cannot be executed when the selected block is locked. Unlocked block can be erased or programmed when $\overline{RST}$ is V_{IH}.
6. Either 40H or 10H are recognized by the CUI (Command User Interface) as the program setup.
7. Following the third bus cycle, input the program sequential address and write data of "N" times. Finally, input the any valid address within the target block to be programmed and the confirm command (D0H). Refer to the LH28F320BF, LH28F640BF, LH28F128BF series Appendix for details.

8. If the program operation in one partition is suspended and the erase operation in other partition is also suspended, the suspended program operation should be resumed first, and then the suspended erase operation should be resumed next.
9. Full chip erase operation can not be suspended.
10. Following the Clear Block Lock Bit command, block which is not locked-down is unlocked when $\overline{WP}$ is V_{IL}.
    When $\overline{WP}$ is V_{IH}, lock-down bit is disabled and the selected block is unlocked regardless of lock-down configuration.
11. Commands other than those shown above are reserved by SHARP for future device implementations and should not be used.

6.2.2 Identifier Codes for Read Operation

	Code	Address [A_{15}-A_0]	Data [DQ_{15}-DQ_0]	Notes
Manufacturer Code	Manufacturer Code	0000H	00B0H	4
Device Code	64M (x16) Top Parameter Device Code	0001H	00B0H	1, 4
Block Lock Configuration Code	Block is Unlocked	Block Address + 2	DQ_0 = 0	2
	Block is Locked		DQ_0 = 1	2
	Block is not Locked-Down		DQ_1 = 0	2
	Block is Locked-Down		DQ_1 = 1	2
Device Configuration Code	Partition Configuration Register	0006H	PCRC	3, 4

Notes:

1. Top parameter device has its parameter blocks in the plane 3 (The highest address).
2. Block Address = The beginning location of a block address within the partition to which the Read Identifier Codes command (90H) has been written.
   DQ_{15}-DQ_2 is reserved for future implementation.
3. PCRC = Partition Configuration Register Code.
4. The address A_{21}-A_{16} are shown in below table for reading the manufacturer, device, device configuration code.
   The address to read the identifier codes is dependent on the partition which is selected when writing the Read Identifier Codes command (90H).
   See Section 6.3 Partition Configuration Register Definition (P.17) for the partition configuration register.

Identifier Codes for Read Operation on Partition Configuration (64M (x16)-bit device)

Partition Configuration Register			Address (64M (x16)-bit device)
PCR.10	PCR.9	PCR.8	[A_{21}-A_{16}]
0	0	0	00H
0	0	1	00H or 10H
0	1	0	00H or 20H
1	0	0	00H or 30H
0	1	1	00H or 10H or 20H
1	1	0	00H or 20H or 30H
1	0	1	00H or 10H or 30H
1	1	1	00H or 10H or 20H or 30H

6.2.3 Functions of Block Lock and Block Lock-Down

Current State					Erase/Program Allowed (2)
State	$\overline{WP}$	DQ_1 (1)	DQ_0 (1)	State Name	
[000]	0	0	0	Unlocked	Yes
[001](3)	0	0	1	Locked	No
[011]	0	1	1	Locked-down	No
[100]	1	0	0	Unlocked	Yes
[101](3)	1	0	1	Locked	No
[110](4)	1	1	0	Lock-down Disable	Yes
[111]	1	1	1	Lock-down Disable	No

Notes:

1. DQ_0 = 1: a block is locked; DQ_0 = 0: a block is unlocked.
   DQ_1 = 1: a block is locked-down; DQ_1 = 0: a block is not locked-down.
2. Erase and program are general terms, respectively, to express: block erase, full chip erase and (page buffer) program operations.
3. At power-up or device reset, all blocks default to locked state and are not locked-down, that is, [001] ($\overline{WP}$ = 0) or [101] ($\overline{WP}$ = 1), regardless of the states before power-off or reset operation.
4. When $\overline{WP}$ is driven to V_{IL} in [110] state, the state changes to [011] and the blocks are automatically locked.

6.2.4 Block Locking State Transitions upon Command Write (4)

Current State				Result after Lock Command Written (Next State)		
State	$\overline{WP}$	DQ_1	DQ_0	Set Lock (1)	Clear Lock (1)	Set Lock-down (1)
[000]	0	0	0	[001]	No Change	[011] (2)
[001]	0	0	1	No Change (3)	[000]	[011]
[011]	0	1	1	No Change	No Change	No Change
[100]	1	0	0	[101]	No Change	[111] (2)
[101]	1	0	1	No Change	[100]	[111]
[110]	1	1	0	[111]	No Change	[111] (2)
[111]	1	1	1	No Change	[110]	No Change

Notes:

1. "Set Lock" means Set Block Lock Bit command, "Clear Lock" means Clear Block Lock Bit command and "Set Lock-down" means Set Block Lock-Down Bit command.
2. When the Set Block Lock-Down Bit command is written to the unlocked block (DQ_0 = 0), the corresponding block is locked-down and automatically locked at the same time.
3. "No Change" means that the state remains unchanged after the command written.
4. In this state transitions table, assumes that $\overline{WP}$ is not changed and fixed V_{IL} or V_{IH}.

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6.2.5 Block Locking State Transitions upon $\overline{WP}$ Transition (4)

Previous State	Current State				Result after $\overline{WP}$ Transition (Next State)	
	State	$\overline{WP}$	DQ_1	DQ_0	$\overline{WP}$ = 0→1 (1)	$\overline{WP}$ = 1→0 (1)
-	[000]	0	0	0	[100]	-
-	[001]	0	0	1	[101]	-
[110] (2)	[011]	0	1	1	[110]	-
Other than [110] (2)					[111]	-
-	[100]	1	0	0	-	[000]
-	[101]	1	0	1	-	[001]
-	[110]	1	1	0	-	[011] (3)
-	[111]	1	1	1	-	[011]

Notes:
1. "$\overline{WP}$ = 0→1" means that $\overline{WP}$ is driven to V_{IH} and "$\overline{WP}$ = 1→0" means that $\overline{WP}$ is driven to V_{IL}.
2. State transition from the current state [011] to the next state depends on the previous state.
3. When $\overline{WP}$ is driven to V_{IL} in [110] state, the state changes to [011] and the blocks are automatically locked.
4. In this state transitions table, assumes that lock configuration commands are not written in previous, current and next state.

6.3 Register Definition

Status Register Definition

R	R	R	R	R	R	R	R
15	14	13	12	11	10	9	8
WSMS	BESS	BEFCES	PBPS	VPPS	PBPSS	DPS	R
7	6	5	4	3	2	1	0

SR.15 - SR.8 = RESERVED FOR FUTURE ENHANCEMENTS (R)	Notes:
SR.7 = WRITE STATE MACHINE STATUS (WSMS) 1 = Ready 0 = Busy	Status Register indicates the status of the partition, not WSM (Write State Machine). Even if the SR.7 is "1", the WSM may be occupied by the other partition when the device is set to 2, 3 or 4 partitions configuration.
SR.6 = BLOCK ERASE SUSPEND STATUS (BESS) 1 = Block Erase Suspended 0 = Block Erase in Progress/Completed	Check SR.7 or RY/$\overline{\text{BY}}$ to determine block erase, full chip erase, (page buffer) program completion. SR.6 - SR.1 are invalid while SR.7= "0".
SR.5 = BLOCK ERASE AND FULL CHIP ERASE STATUS (BEFCES) 1 = Error in Block Erase or Full Chip Erase 0 = Successful Block Erase or Full Chip Erase	If both SR.5 and SR.4 are "1"s after a block erase, full chip erase, (page buffer) program, set/clear block lock bit, set block lock-down bit or set partition configuration register attempt, an improper command sequence was entered.
SR.4 = (PAGE BUFFER) PROGRAM STATUS (PBPS) 1 = Error in (Page Buffer) Program 0 = Successful (Page Buffer) Program	
SR.3 = V_{PP} STATUS (VPPS) 1 = V_{PP} LOW Detect, Operation Abort 0 = V_{PP} OK	SR.3 does not provide a continuous indication of V_{PP} level. The WSM interrogates and indicates the V_{PP} level only after Block Erase, Full Chip Erase, (Page Buffer) Program command sequences. SR.3 is not guaranteed to report accurate feedback when $V_{PP} \neq V_{PPH}$ or V_{PPLK}.
SR.2 = (PAGE BUFFER) PROGRAM SUSPEND STATUS (PBPSS) 1 = (Page Buffer) Program Suspended 0 = (Page Buffer) Program in Progress/Completed	
SR.1 = DEVICE PROTECT STATUS (DPS) 1 = Erase or Program Attempted on a Locked Block, Operation Abort 0 = Unlocked	SR.1 does not provide a continuous indication of block lock bit. The WSM interrogates the block lock bit only after Block Erase, Full Chip Erase, (Page Buffer) Program command sequences. It informs the system, depending on the attempted operation, if the block lock bit is set. Reading the block lock configuration codes after writing the Read Identifier Codes command indicates block lock bit status.
SR.0 =RESERVED FOR FUTURE ENHANCEMENTS (R)	SR.15 - SR.8 and SR.0 are reserved for future use and should be masked out when polling the status register.

Extended Status Register Definition

R	R	R	R	R	R	R	R
15	14	13	12	11	10	9	8
SMS	R	R	R	R	R	R	R
7	6	5	4	3	2	1	0

XSR.15-8 = RESERVED FOR FUTURE ENHANCEMENTS (R) XSR.7 = STATE MACHINE STATUS (SMS) 1 = Page Buffer Program available 0 = Page Buffer Program not available XSR.6-0 = RESERVED FOR FUTURE ENHANCEMENTS (R)	Notes: After issue a Page Buffer Program command (E8H), XSR.7="1" indicates that the entered command is accepted. If XSR.7 is "0", the command is not accepted and a next Page Buffer Program command (E8H) should be issued again to check if page buffer is available or not. XSR.15-8 and XSR.6-0 are reserved for future use and should be masked out when polling the extended status register.

Partition Configuration Register Definition

R	R	R	R	R	PC2	PC1	PC0
15	14	13	12	11	10	9	8
R	R	R	R	R	R	R	R
7	6	5	4	3	2	1	0

PCR.15-11 = RESERVED FOR FUTURE ENHANCEMENTS (R)

PCR.10-8 = PARTITION CONFIGURATION (PC2-0)

- 000 = No partitioning. Dual Work is not allowed.
- 001 = Plane1-3 are merged into one partition. (default in a bottom parameter device)
- 010 = Plane 0-1 and Plane 2-3 are merged into one partition respectively.
- 100 = Plane 0-2 are merged into one partition. (default in a top parameter device)
- 011 = Plane 2-3 are merged into one partition. There are three partitions in this configuration. Dual work operation is available between any two partitions.
- 110 = Plane 0-1 are merged into one partition. There are three partitions in this configuration. Dual work operation is available between any two partitions.
- 101 = Plane 1-2 are merged into one partition. There are three partitions in this configuration. Dual work operation is available between any two partitions.
- 111 = There are four partitions in this configuration. Each plane corresponds to each partition respectively. Dual work operation is available between any two partitions.

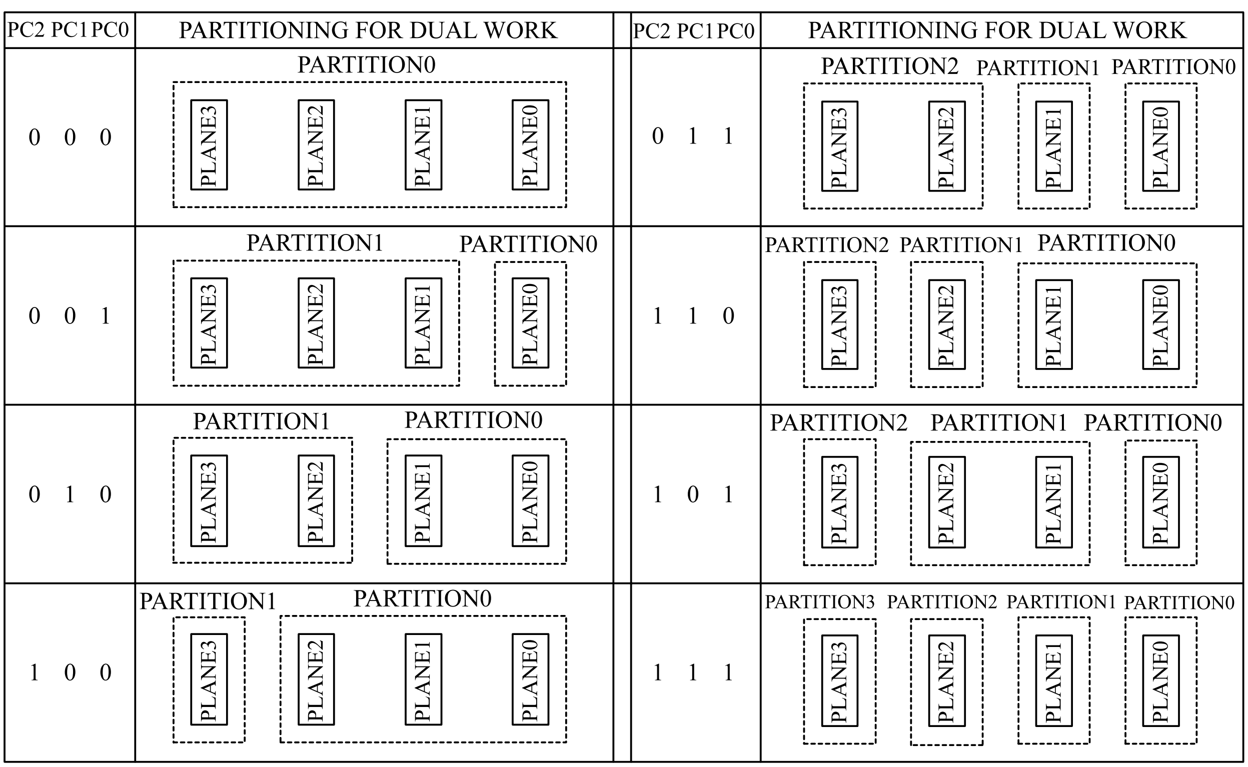
PCR.7-0 = RESERVED FOR FUTURE ENHANCEMENTS (R)

Notes:
After power-up or device reset, PCR 10-8 (PC2-0) is set to “001” in a bottom parameter device and “100” in a top parameter device.

See the table below for more details.

PCR.15-11 and PCR.7-0 are reserved for future use and should be masked out when checking the partition configuration register.

Partition Configuration



6.4 Memory Map for Flash Memory

Top Parameter

PLANE3 (PARAMETER PLANE)

BLOCK NUMBER		ADDRESS RANGE
134	4K-WORD	3FF000H - 3FFFFFH
133	4K-WORD	3FE000H - 3FEFFFH
132	4K-WORD	3FD000H - 3FDFFFH
131	4K-WORD	3FC000H - 3FCFFFH
130	4K-WORD	3FB000H - 3FBFFFH
129	4K-WORD	3FA000H - 3FAFFFH
128	4K-WORD	3F9000H - 3F9FFFH
127	4K-WORD	3F8000H - 3F8FFFH
126	32K-WORD	3F0000H - 3F7FFFH
125	32K-WORD	3E8000H - 3EFFFFH
124	32K-WORD	3E0000H - 3E7FFFH
123	32K-WORD	3D8000H - 3DFFFFH
122	32K-WORD	3D0000H - 3D7FFFH
121	32K-WORD	3C8000H - 3CFFFFH
120	32K-WORD	3C0000H - 3C7FFFH
119	32K-WORD	3B8000H - 3BFFFFH
118	32K-WORD	3B0000H - 3B7FFFH
117	32K-WORD	3A8000H - 3AFFFFH
116	32K-WORD	3A0000H - 3A7FFFH
115	32K-WORD	398000H - 39FFFFH
114	32K-WORD	390000H - 397FFFH
113	32K-WORD	388000H - 38FFFFH
112	32K-WORD	380000H - 387FFFH
111	32K-WORD	378000H - 37FFFFH
110	32K-WORD	370000H - 377FFFH
109	32K-WORD	368000H - 36FFFFH
108	32K-WORD	360000H - 367FFFH
107	32K-WORD	358000H - 35FFFFH
106	32K-WORD	350000H - 357FFFH
105	32K-WORD	348000H - 34FFFFH
104	32K-WORD	340000H - 347FFFH
103	32K-WORD	338000H - 33FFFFH
102	32K-WORD	330000H - 337FFFH
101	32K-WORD	328000H - 32FFFFH
100	32K-WORD	320000H - 327FFFH
99	32K-WORD	318000H - 31FFFFH
98	32K-WORD	310000H - 317FFFH
97	32K-WORD	308000H - 30FFFFH
96	32K-WORD	300000H - 307FFFH

PLANE2 (UNIFORM PLANE)

BLOCK NUMBER		ADDRESS RANGE
95	32K-WORD	2F8000H - 2FFFFFH
94	32K-WORD	2F0000H - 2F7FFFH
93	32K-WORD	2E8000H - 2EFFFFH
92	32K-WORD	2E0000H - 2E7FFFH
91	32K-WORD	2D8000H - 2DFFFFH
90	32K-WORD	2D0000H - 2D7FFFH
89	32K-WORD	2C8000H - 2CFFFFH
88	32K-WORD	2C0000H - 2C7FFFH
87	32K-WORD	2B8000H - 2BFFFFH
86	32K-WORD	2B0000H - 2B7FFFH
85	32K-WORD	2A8000H - 2AFFFFH
84	32K-WORD	2A0000H - 2A7FFFH
83	32K-WORD	298000H - 29FFFFH
82	32K-WORD	290000H - 297FFFH
81	32K-WORD	288000H - 28FFFFH
80	32K-WORD	280000H - 287FFFH
79	32K-WORD	278000H - 27FFFFH
78	32K-WORD	270000H - 277FFFH
77	32K-WORD	268000H - 26FFFFH
76	32K-WORD	260000H - 267FFFH
75	32K-WORD	258000H - 25FFFFH
74	32K-WORD	250000H - 257FFFH
73	32K-WORD	248000H - 24FFFFH
72	32K-WORD	240000H - 247FFFH
71	32K-WORD	238000H - 23FFFFH
70	32K-WORD	230000H - 237FFFH
69	32K-WORD	228000H - 22FFFFH
68	32K-WORD	220000H - 227FFFH
67	32K-WORD	218000H - 21FFFFH
66	32K-WORD	210000H - 217FFFH
65	32K-WORD	208000H - 20FFFFH
64	32K-WORD	200000H - 207FFFH

PLANE1 (UNIFORM PLANE)

BLOCK NUMBER		ADDRESS RANGE
63	32K-WORD	1F8000H - 1FFFFFH
62	32K-WORD	1F0000H - 1F7FFFH
61	32K-WORD	1E8000H - 1EFFFFH
60	32K-WORD	1E0000H - 1E7FFFH
59	32K-WORD	1D8000H - 1DFFFFH
58	32K-WORD	1D0000H - 1D7FFFH
57	32K-WORD	1C8000H - 1CFFFFH
56	32K-WORD	1C0000H - 1C7FFFH
55	32K-WORD	1B8000H - 1BFFFFH
54	32K-WORD	1B0000H - 1B7FFFH
53	32K-WORD	1A8000H - 1AFFFFH
52	32K-WORD	1A0000H - 1A7FFFH
51	32K-WORD	198000H - 19FFFFH
50	32K-WORD	190000H - 197FFFH
49	32K-WORD	188000H - 18FFFFH
48	32K-WORD	180000H - 187FFFH
47	32K-WORD	178000H - 17FFFFH
46	32K-WORD	170000H - 177FFFH
45	32K-WORD	168000H - 16FFFFH
44	32K-WORD	160000H - 167FFFH
43	32K-WORD	158000H - 15FFFFH
42	32K-WORD	150000H - 157FFFH
41	32K-WORD	148000H - 14FFFFH
40	32K-WORD	140000H - 147FFFH
39	32K-WORD	138000H - 13FFFFH
38	32K-WORD	130000H - 137FFFH
37	32K-WORD	128000H - 12FFFFH
36	32K-WORD	120000H - 127FFFH
35	32K-WORD	118000H - 11FFFFH
34	32K-WORD	110000H - 117FFFH
33	32K-WORD	108000H - 10FFFFH
32	32K-WORD	100000H - 107FFFH

PLANE0 (UNIFORM PLANE)

BLOCK NUMBER		ADDRESS RANGE
31	32K-WORD	0F8000H - 0FFFFFH
30	32K-WORD	0F0000H - 0F7FFFH
29	32K-WORD	0E8000H - 0EFFFFH
28	32K-WORD	0E0000H - 0E7FFFH
27	32K-WORD	0D8000H - 0DFFFFH
26	32K-WORD	0D0000H - 0D7FFFH
25	32K-WORD	0C8000H - 0CFFFFH
24	32K-WORD	0C0000H - 0C7FFFH
23	32K-WORD	0B8000H - 0BFFFFH
22	32K-WORD	0B0000H - 0B7FFFH
21	32K-WORD	0A8000H - 0AFFFFH
20	32K-WORD	0A0000H - 0A7FFFH
19	32K-WORD	098000H - 09FFFFH
18	32K-WORD	090000H - 097FFFH
17	32K-WORD	088000H - 08FFFFH
16	32K-WORD	080000H - 087FFFH
15	32K-WORD	078000H - 07FFFFH
14	32K-WORD	070000H - 077FFFH
13	32K-WORD	068000H - 06FFFFH
12	32K-WORD	060000H - 067FFFH
11	32K-WORD	058000H - 05FFFFH
10	32K-WORD	050000H - 057FFFH
9	32K-WORD	048000H - 04FFFFH
8	32K-WORD	040000H - 047FFFH
7	32K-WORD	038000H - 03FFFFH
6	32K-WORD	030000H - 037FFFH
5	32K-WORD	028000H - 02FFFFH
4	32K-WORD	020000H - 027FFFH
3	32K-WORD	018000H - 01FFFFH
2	32K-WORD	010000H - 017FFFH
1	32K-WORD	008000H - 00FFFFH
0	32K-WORD	000000H - 007FFFH

6.5 DC Electrical Characteristics for Flash Memory

DC Electrical Characteristics

(T_A = -25°C to +85°C, V_{CC} = 2.7V to 3.1V)

Symbol	Parameter		Notes	Min.	Typ.	Max.	Unit	Test Conditions
C_{IN}	Input Capacitance		5			7	pF	V_{IN} = 0V, f = 1MHz, T_A = 25°C
C_{IO}	I/O Capacitance		5			10	pF	$V_{I/O}$ = 0V, f = 1MHz, T_A = 25°C
I_{LI}	Input Leakage Current					±1	μA	V_{IN} = V_{CC} or GND
I_{LO}	Output Leakage Current					±1	μA	V_{OUT} = V_{CC} or GND
I_{CCS}	V_{CC} Standby Current		1, 8		4	20	μA	V_{CC} = V_{CC} Max., F_1-$\overline{CE}$ = $\overline{RST}$ = V_{CC} ±0.2V, $\overline{WP}$ = V_{CC} or GND
I_{CCAS}	V_{CC} Automatic Power Savings Current		1, 4		4	20	μA	V_{CC} = V_{CC} Max., F_1-$\overline{CE}$ = GND ±0.2V, $\overline{WP}$ = V_{CC} or GND
I_{CCD}	V_{CC} Reset Power-Down Current		1		4	20	μA	$\overline{RST}$ = GND ±0.2V I_{OUT} (RY/$\overline{BY}$) = 0mA
I_{CCR}	Average V_{CC} Read Current Normal Mode		1, 7		15	25	mA	V_{CC} = V_{CC} Max., F_1-$\overline{CE}$ = V_{IL}, F-$\overline{OE}$ = V_{IH}, f = 5MHz I_{OUT} = 0mA
	Average V_{CC} Read Current Page Mode	8 Word Read	1, 7		5	10	mA	
I_{CCW}	V_{CC} (Page Buffer) Program Current		1, 5, 7		20	60	mA	V_{PP} = V_{PPH}
I_{CCE}	V_{CC} Block Erase, Full Chip Erase Current		1, 5, 7		10	30	mA	V_{PP} = V_{PPH}
I_{CCWS} I_{CCES}	V_{CC} (Page Buffer) Program or Block Erase Suspend Current		1, 2, 7		10	200	μA	F_1-$\overline{CE}$ = V_{IH}
I_{PPS} I_{PPR}	V_{PP} Standby or Read Current		1, 6, 7		2	5	μA	V_{PP} ≤ V_{CC}
I_{PPW}	V_{PP} (Page Buffer) Program Current		1,5,6,7		2	5	μA	V_{PP} = V_{PPH}
I_{PPE}	V_{PP} Block Erase, Full Chip Erase Current		1,5,6,7		2	5	μA	V_{PP} = V_{PPH}
I_{PPWS}	V_{PP} (Page Buffer) Program Suspend Current		1, 6, 7		2	5	μA	V_{PP} = V_{PPH}
I_{PPES}	V_{PP} Block Erase Suspend Current		1, 6, 7		2	5	μA	V_{PP} = V_{PPH}

DC Electrical Characteristics (Continue)

(T_A = -25°C to +85°C, V_{CC} = 2.7V to 3.1V)

Symbol	Parameter	Notes	Min.	Typ.	Max.	Unit	Test Conditions
V_{IL}	Input Low Voltage	5	-0.2		0.4	V	
V_{IH}	Input High Voltage	5	VCC -0.4		VCC +0.2	V	
V_{OL}	Output Low Voltage	5, 8			0.2VCC	V	I_{OL} = 0.5mA
V_{OH}	Output High Voltage	5	0.8VCC			V	I_{OH} = -0.5mA
V_{PPLK}	V_{PP} Lockout during Normal Operations	3,5,6			0.4	V	
V_{PPH}	V_{PP} during Block Erase, Full Chip Erase, (Page Buffer) Program Operations	6	1.65	3	3.1	V	
V_{LKO}	V_{CC} Lockout Voltage		1.5			V	

Notes:

1. All currents are in RMS unless otherwise noted. Typical values are the reference values at V_{CC} = 3.0V and T_A = +25°C unless V_{CC} is specified.
2. I_{CCWS} and I_{CCES} are specified with the device de-selected. If read or (page buffer) program is executed while in block erase suspend mode, the device's current draw is the sum of I_{CCES} and I_{CCR} or I_{CCW}. If read is executed while in (page buffer) program suspend mode, the device's current draw is the sum of I_{CCWS} and I_{CCR}.
3. Block erase, full chip erase, (page buffer) program are inhibited when $V_{PP} \leq V_{PPLK}$, and not guaranteed outside the specified voltage.
4. The Automatic Power Savings (APS) feature automatically places the device in power save mode after read cycle completion. Standard address access timings (t_{AVQV}) provide new data when addresses are changed.
5. Sampled, not 100% tested.
6. V_{PP} is not used for power supply pin. With $V_{PP} \leq V_{PPLK}$, block erase, full chip erase, (page buffer) program cannot be executed and should not be attempted.
7. The operating current in dual work is the sum of the operating current (read, erase, program) in each plane.
8. Includes RY/$\overline{BY}$

6.6 AC Electrical Characteristics for Flash Memory

6.6.1 AC Test Conditions

Input Pulse Level	0 V to 2.7 V
Input Rise and Fall Time	5 ns
Input and Output Timing Ref. level	1.35 V
Output Load	1TTL +C_L (50pF)

6.6.2 Read Cycle

(T_A = -25°C to +85°C, V_{CC} = 2.7V to 3.1V)

Symbol	Parameter	Notes	Min.	Max.	Unit
t_{AVAV}	Read Cycle Time		65		ns
t_{AVQV}	Address to Output Delay			65	ns
t_{ELQV}	F_1-$\overline{CE}$ to Output Delay	2		65	ns
t_{APA}	Page Address Access Time			25	ns
t_{GLQV}	F-$\overline{OE}$ to Output Delay	2		20	ns
t_{PHQV}	$\overline{RST}$ High to Output Delay			150	ns
t_{EHQZ}, t_{GHQZ}	F_1-$\overline{CE}$ or F-$\overline{OE}$ to Output in High-Z, Whichever Occurs First	1		20	ns
t_{ELQX}	F_1-$\overline{CE}$ to Output in Low-Z	1	0		ns
t_{GLQX}	F-$\overline{OE}$ to Output in Low-Z	1	0		ns
t_{OH}	Output Hold from First Occurring Address, F_1-$\overline{CE}$ or F-$\overline{OE}$ Change	1	0		ns

Notes:

1. Sampled, not 100% tested.
2. F-$\overline{OE}$ may be delayed up to $t_{ELQV} - t_{GLQV}$ after the falling edge of F_1-$\overline{CE}$ without impact to t_{ELQV}.

6.6.3 Write Cycle (F-$\overline{WE}$ / F_1-$\overline{CE}$ Controlled) [1,2]

(T_A = -25°C to +85°C, V_{CC} = 2.7V to 3.1V)

Symbol	Parameter	Notes	Min.	Max.	Unit
t_{AVAV}	Write Cycle Time		65		ns
t_{PHWL} (t_{PHEL})	$\overline{RST}$ High Recovery to F-$\overline{WE}$ (F_1-$\overline{CE}$) Going Low	3	150		ns
t_{ELWL} (t_{WLEL})	F_1-$\overline{CE}$ (F-$\overline{WE}$) Setup to F-$\overline{WE}$ (F_1-$\overline{CE}$) Going Low		0		ns
t_{WLWH} (t_{ELEH})	F-$\overline{WE}$ (F_1-$\overline{CE}$) Pulse Width	4	50		ns
t_{DVWH} (t_{DVEH})	Data Setup to F-$\overline{WE}$ (F_1-$\overline{CE}$) Going High	8	40		ns
t_{AVWH} (t_{AVEH})	Address Setup to F-$\overline{WE}$ (F_1-$\overline{CE}$) Going High	8	50		ns
t_{WHEH} (t_{EHWH})	F_1-$\overline{CE}$ (F-$\overline{WE}$) Hold from F-$\overline{WE}$ (F_1-$\overline{CE}$) High		0		ns
t_{WHDX} (t_{EHDX})	Data Hold from F-$\overline{WE}$ (F_1-$\overline{CE}$) High		0		ns
t_{WHAX} (t_{EHAX})	Address Hold from F-$\overline{WE}$ (F_1-$\overline{CE}$) High		0		ns
t_{WHWL} (t_{EHEL})	F-$\overline{WE}$ (F_1-$\overline{CE}$) Pulse Width High	5	15		ns
t_{SHWH} (t_{SHEH})	$\overline{WP}$ High Setup to F-$\overline{WE}$ (F_1-$\overline{CE}$) Going High	3	0		ns
t_{VVWH} (t_{VVEH})	V_{PP} Setup to F-$\overline{WE}$ (F_1-$\overline{CE}$) Going High	3	200		ns
t_{WHGL} (t_{EHGL})	Write Recovery before Read		30		ns
t_{QVSL}	$\overline{WP}$ High Hold from Valid SRD, RY/$\overline{BY}$ High-Z	3, 6	0		ns
t_{QVVL}	V_{PP} Hold from Valid SRD, RY/$\overline{BY}$ High-Z	3, 6	0		ns
t_{WHR0} (t_{EHR0})	F-$\overline{WE}$ (F_1-$\overline{CE}$) High to SR.7 Going "0"	3, 7		t_{AVQV}+50	ns
t_{WHRL} (t_{EHRL})	F-$\overline{WE}$ (F_1-$\overline{CE}$) High to RY/$\overline{BY}$ Going Low	3		100	ns

Notes:

1. The timing characteristics for reading the status register during block erase, full chip erase, (page buffer) program operations are the same as during read-only operations. See the AC Characteristics for read cycle.
2. A write operation can be initiated and terminated with either F_1-$\overline{CE}$ or F-$\overline{WE}$.
3. Sampled, not 100% tested.
4. Write pulse width (t_{WP}) is defined from the falling edge of F_1-$\overline{CE}$ or F-$\overline{WE}$ (whichever goes low last) to the rising edge of F_1-$\overline{CE}$ or F-$\overline{WE}$ (whichever goes high first). Hence, $t_{WP}=t_{WLWH}=t_{ELEH}=t_{WLEH}=t_{ELWH}$.
5. Write pulse width high (t_{WPH}) is defined from the rising edge of F_1-$\overline{CE}$ or F-$\overline{WE}$ (whichever goes high first) to the falling edge of F_1-$\overline{CE}$ or F-$\overline{WE}$ (whichever goes low last). Hence, $t_{WPH}=t_{WHWL}=t_{EHEL}=t_{WHEL}=t_{EHWL}$.
6. V_{PP} should be held at $V_{PP}=V_{PPH}$ until determination of block erase, full chip erase, (page buffer) program success (SR.1/3/4/5=0).
7. t_{WHR0} (t_{EHR0}) after the Read Query or Read Identifier Codes command=t_{AVQV}+100ns.
8. See 6.2.1 Command Definitions for valid address and data for block erase, full chip erase, (page buffer) program or lock bit configuration.

6.6.4 Block Erase, Full Chip Erase, (Page Buffer) Program Performance [3]

(T_A = -25°C to +85°C, V_{CC} = 2.7V to 3.1V)

Symbol	Parameter	Notes	Page Buffer Command is Used or not Used	$V_{PP}=V_{PPH}$			Unit
				Min.	Typ. [1]	Max. [2]	
t_{WPB}	4K-Word Parameter Block Program Time	2	Not Used		0.05	0.3	s
		2	Used		0.03	0.12	s
t_{WMB}	32K-Word Main Block Program Time	2	Not Used		0.38	2.4	s
		2	Used		0.24	1	s
t_{WHQV1}/ t_{EHQV1}	Word Program Time	2	Not Used		11	200	µs
		2	Used		7	100	µs
t_{WHQV2}/ t_{EHQV2}	4K-Word Parameter Block Erase Time	2	-		0.3	4	s
t_{WHQV3}/ t_{EHQV3}	32K-Word Main Block Erase Time	2	-		0.6	5	s
	Full Chip Erase Time	2			80	700	s
t_{WHRH1}/ t_{EHRH1}	(Page Buffer) Program Suspend Latency Time to Read	4	-		5	10	µs
t_{WHRH2}/ t_{EHRH2}	Block Erase Suspend Latency Time to Read	4	-		5	20	µs
t_{ERES}	Latency Time from Block Erase Resume Command to Block Erase Suspend Command	5	-	500			µs

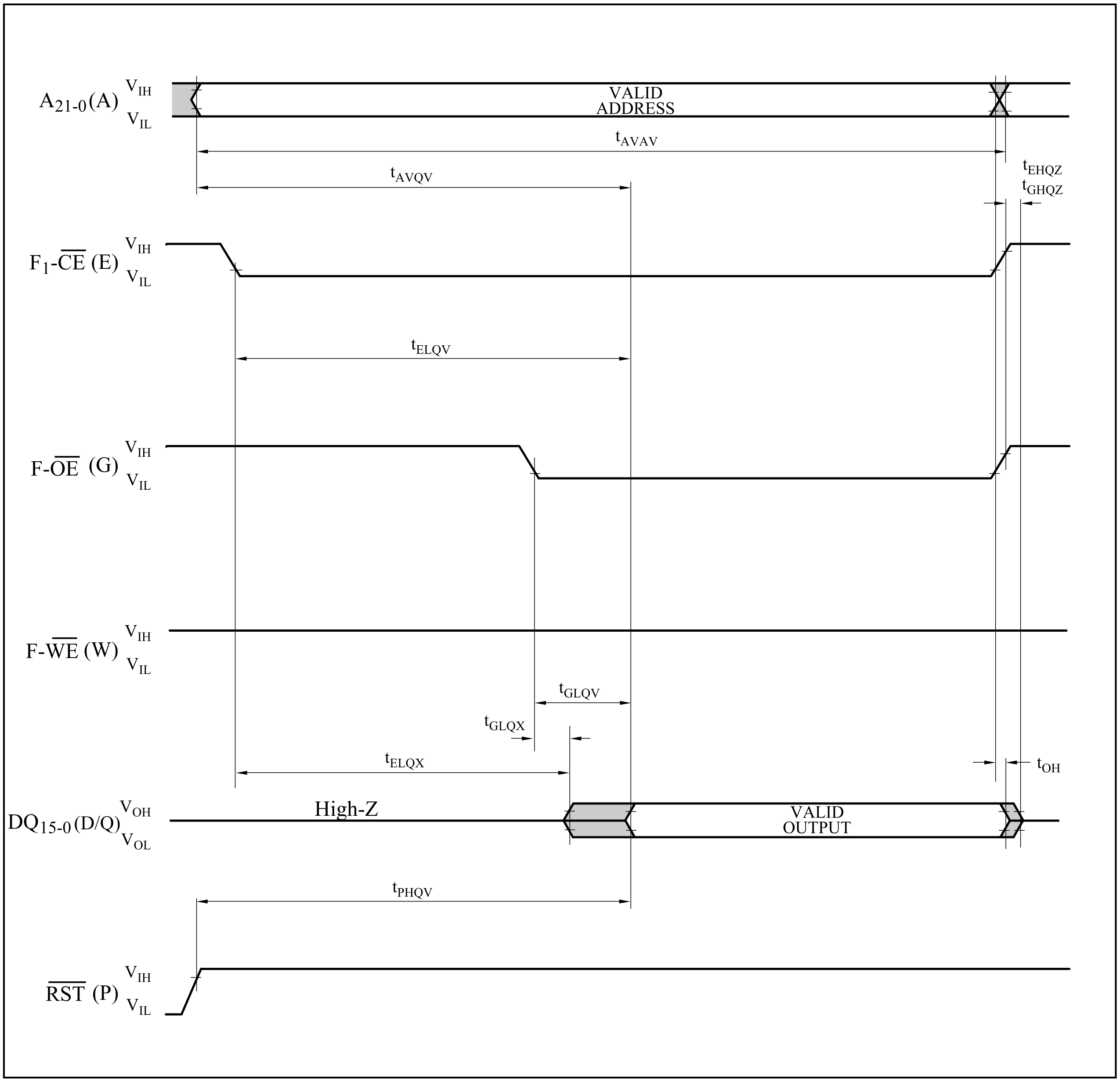
Notes:

1. Typical values measured at V_{CC} =3.0V, V_{PP} =3.0V, and T_A=+25°C. Assumes corresponding lock bits are not set. Subject to change based on device characterization.
2. Excludes external system-level overhead.
3. Sampled, but not 100% tested.
4. A latency time is required from writing suspend command (F-$\overline{WE}$ or F_1-$\overline{CE}$ going high) until SR.7 going “1” or RY/$\overline{BY}$ going High-Z.
5. If the interval time from a Block Erase Resume command to a subsequent Block Erase Suspend command is shorter than t_{ERES} and its sequence is repeated, the block erase operation may not be finished.

SHARP

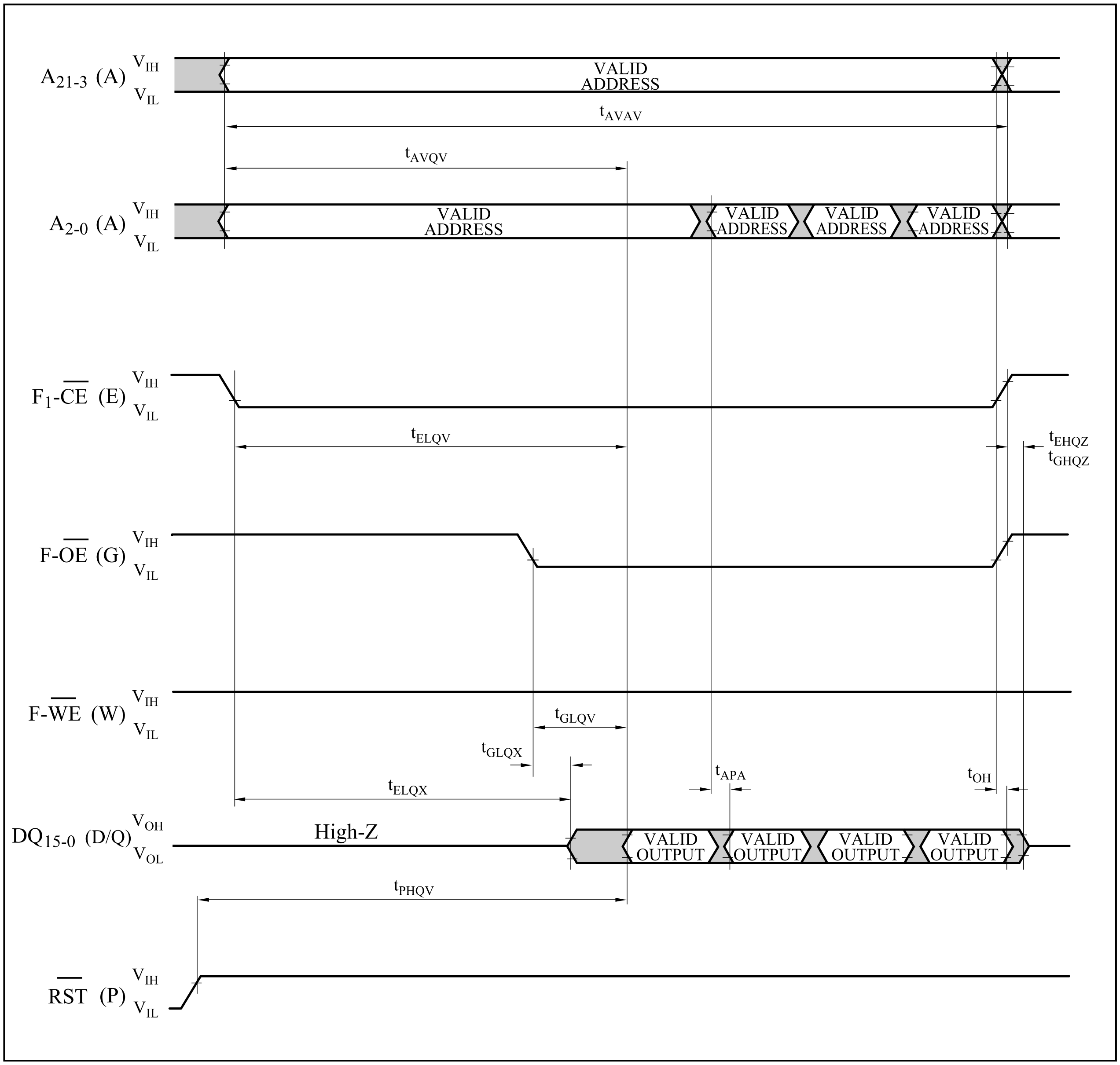
6.6.5 Flash Memory AC Characteristics Timing Chart

AC Waveform for Single Asynchronous Read Operations from Status Register, Identifier Codes or Query Code

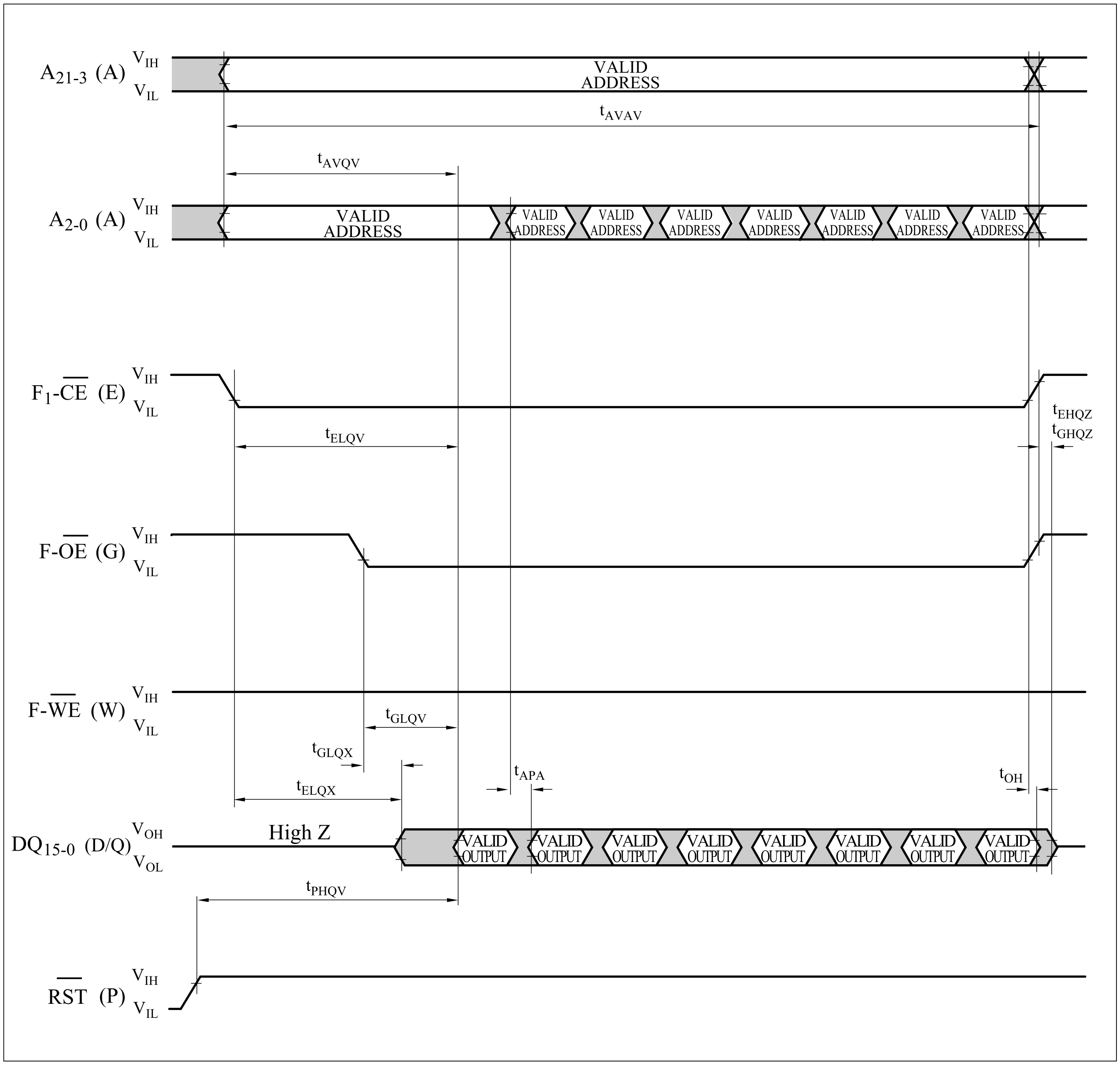


SHARP

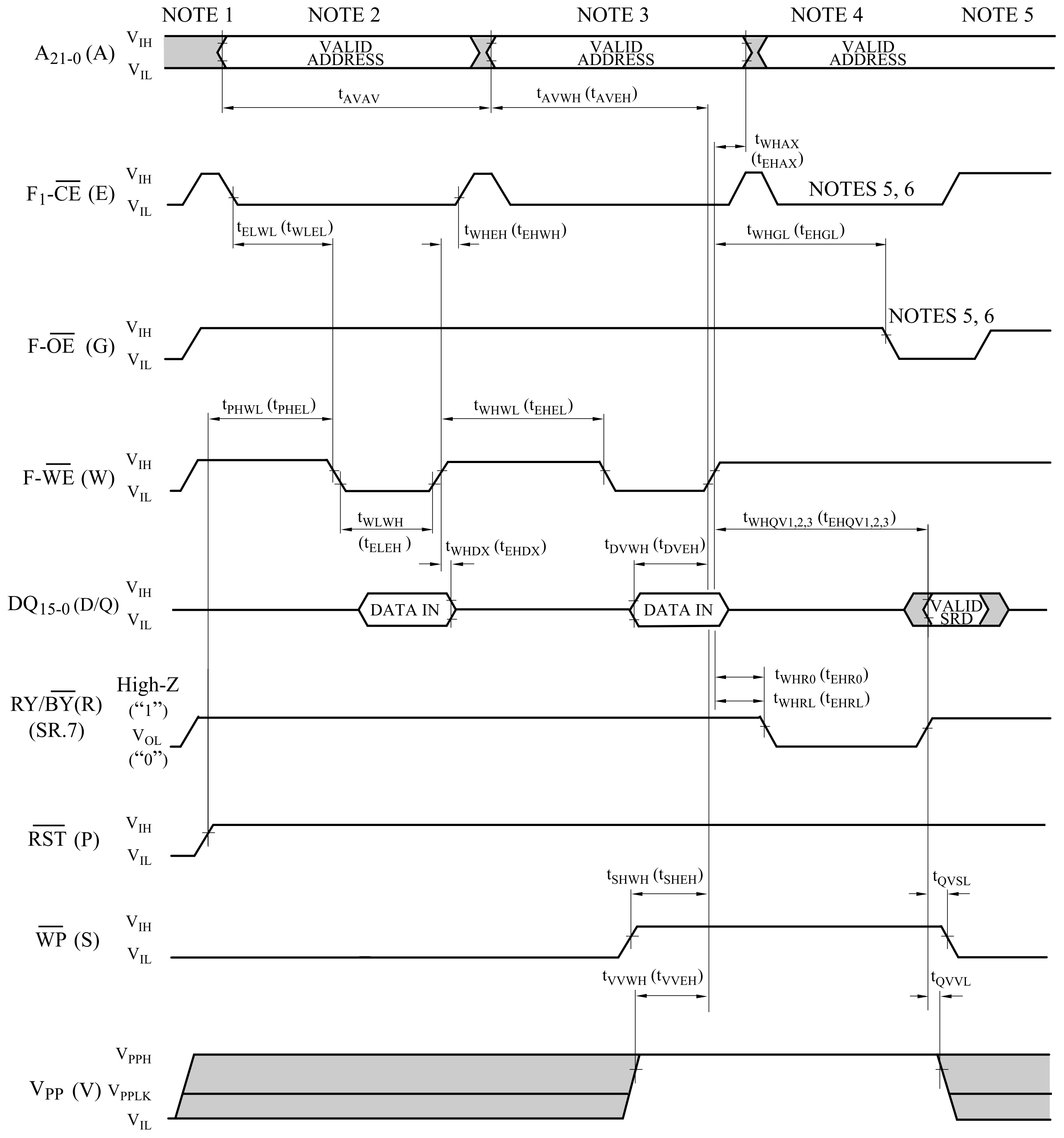
AC Waveform for Asynchronous 4-Word Page Mode Read Operations from Main Blocks or Parameter Blocks



AC Waveform for Asynchronous 8-Word Page Mode Read Operations from Main Blocks or Parameter Blocks



AC Waveform for Write Operations (F-$\overline{WE}$ / F1-$\overline{CE}$ Controlled)



Notes:
1. VCC power-up and standby.
2. Write each first cycle command.
3. Write each second cycle command or valid address and data.
4. Automated erase or program delay.
5. Read status register data.
6. For read operation, F-$\overline{OE}$ and F 1-$\overline{CE}$ must be driven active, and F-$\overline{WE}$ de-asserted.

6.6.6 Reset Operations

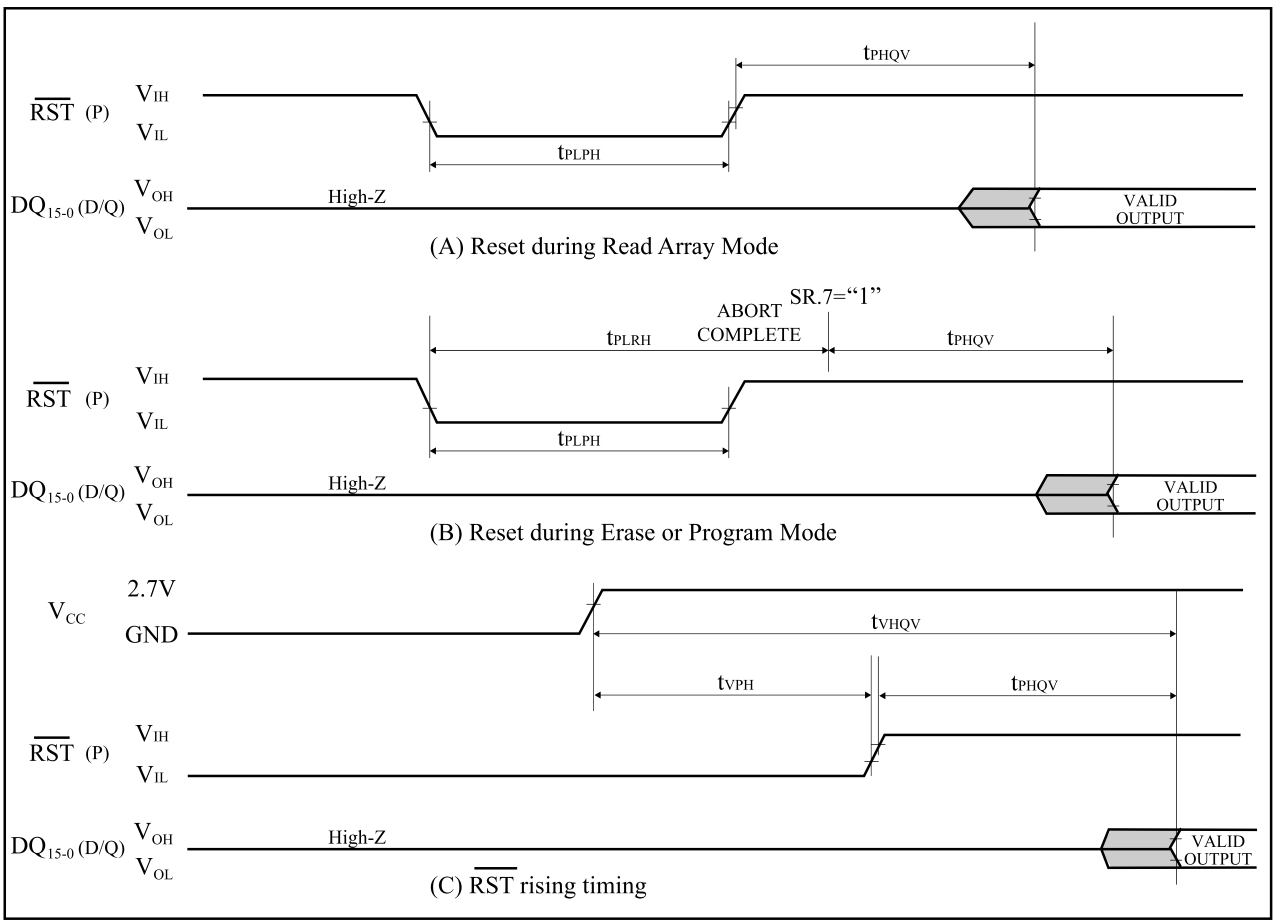
(T_A = -25°C to +85°C, V_{CC} = 2.7V to 3.1V)

Symbol	Parameter	Notes	Min.	Max.	Unit
t_{PLPH}	$\overline{RST}$ Low to Reset during Read ($\overline{RST}$ should be low during power-up.)	1, 2, 3	100		ns
t_{PLRH}	$\overline{RST}$ Low to Reset during Erase or Program	1, 3, 4		22	µs
t_{VPH}	V_{CC} = 2.7V to $\overline{RST}$ High	1, 3, 5	100		ns
t_{VHQV}	V_{CC} = 2.7V to Output Delay	3		1	ms

Notes:

1. A reset time, t_{PHQV}, is required from the later of SR.7 (RY/$\overline{BY}$) going "1" (High-Z) or $\overline{RST}$ going high until outputs are valid. See the AC Characteristics - read cycle for t_{PHQV}.
2. t_{PLPH} is <100ns the device may still reset but this is not guaranteed.
3. Sampled, not 100% tested.
4. If $\overline{RST}$ asserted while a block erase, full chip erase or (page buffer) program operation is not executing, the reset will complete within 100ns.
5. When the device power-up, holding $\overline{RST}$ low minimum 100ns is required after V_{CC} has been in predefined range and also has been in stable there.

AC Waveform for Reset Operation



7. Flash Memory 2

7.1 Truth Table

7.1.1 Bus Operation [1]

<table>
<tr><th>Flash</th><th>Notes</th><th>F_2-$\overline{CE}$</th><th>$\overline{RST}$</th><th>F-$\overline{OE}$</th><th>F-$\overline{WE}$</th><th>DQ_0 to DQ_{15}</th></tr>
<tr><td>Read</td><td>3,5</td><td rowspan="3">L</td><td rowspan="3">H</td><td>L</td><td rowspan="2">H</td><td>(7)</td></tr>
<tr><td>Output Disable</td><td>5</td><td rowspan="2">H</td><td>High - Z</td></tr>
<tr><td>Write</td><td>2,3,4,5</td><td>L</td><td>D_{IN}</td></tr>
<tr><td>Standby</td><td>5</td><td>H</td><td>H</td><td rowspan="2">X</td><td rowspan="2">X</td><td rowspan="2">High - Z</td></tr>
<tr><td>Reset Power Down</td><td>5,6</td><td>X</td><td>L</td></tr>
</table>

Notes:

1. L = V_{IL}, H = V_{IH}, X = H or L, High-Z = High impedance. Refer to the DC Characteristics.
2. Command writes involving block erase, full chip erase, (page buffer) program are reliably executed when $V_{PP} = V_{PPH}$ and V_{CC} = 2.7V to 3.1V.
   Block erase, full chip erase, (page buffer) program with $V_{PP} < V_{PPH}$ (Min.) produce spurious results and should not be attempted.
3. Never hold F-$\overline{OE}$ low and F-$\overline{WE}$ low at the same timing.
4. Refer to Section 7.2 Command Definitions for Flash Memory valid D_{IN} during a write operation.
5. $\overline{WP}$ set to V_{IL} or V_{IH}.
6. Electricity consumption of Flash Memory is lowest when $\overline{RST}$ = GND ±0.2V.
7. Flash Read Mode

Mode	Address	DQ_0 to DQ_{15}
Read Array	X	D_{OUT}
Read Identifier Codes	See 7.2.2	See 7.2.2
Read Query	Refer to the Appendix	Refer to the Appendix

7.1.2 Simultaneous Operation Modes Allowed with Four Planes [1,2]

IF ONE PARTITION IS:	THEN THE MODES ALLOWED IN THE OTHER PARTITION IS:									
	Read Array	Read ID	Read Status	Read Query	Word Program	Page Buffer Program	Block Erase	Full Chip Erase	Program Suspend	Block Erase Suspend
Read Array	X	X	X	X	X	X	X		X	X
Read ID	X	X	X	X	X	X	X		X	X
Read Status	X	X	X	X	X	X	X	X	X	X
Read Query	X	X	X	X	X	X	X		X	X
Word Program	X	X	X	X						X
Page Buffer Program	X	X	X	X						X
Block Erase	X	X	X	X						
Full Chip Erase			X							
Program Suspend	X	X	X	X						X
Block Erase Suspend	X	X	X	X	X	X			X	

Notes:
1. "X" denotes the operation available.
2. Configurative Partition Dual Work Restrictions:
Status register reflects partition state, not WSM (Write State Machine) state - this allows a status register for each partition.
Only one partition can be erased or programmed at a time - no command queuing.
Commands must be written to an address within the block targeted by that command.

7.2 Command Definitions for Flash Memory (11)

7.2.1 Command Definitions

Command	Bus Cycles Req'd	Notes	First Bus Cycle			Second Bus Cycle		
			Oper (1)	Address (2)	Data	Oper (1)	Address (2)	Data (3)
Read Array	1		Write	PA	FFH			
Read Identifier Codes	≥ 2	4	Write	PA	90H	Read	IA	ID
Read Query	≥ 2	4	Write	PA	98H	Read	QA	QD
Read Status Register	2		Write	PA	70H	Read	PA	SRD
Clear Status Register	1		Write	PA	50H			
Block Erase	2	5	Write	BA	20H	Write	BA	D0H
Full Chip Erase	2	5, 9	Write	X	30H	Write	X	D0H
Program	2	5, 6	Write	WA	40H or 10H	Write	WA	WD
Page Buffer Program	≥ 4	5, 7	Write	WA	E8H	Write	WA	N-1
Block Erase and (Page Buffer) Program Suspend	1	8, 9	Write	PA	B0H			
Block Erase and (Page Buffer) Program Resume	1	8, 9	Write	PA	D0H			
Set Block Lock Bit	2		Write	BA	60H	Write	BA	01H
Clear Block Lock Bit	2	10	Write	BA	60H	Write	BA	D0H
Set Block Lock-down Bit	2		Write	BA	60H	Write	BA	2FH
Set Partition Configuration Register	2		Write	PCRC	60H	Write	PCRC	04H

Notes:

1. Bus operations are defined in 7.1.1 Bus Operation.
2. All addresses which are written at the first bus cycle should be the same as the addresses which are written at the second bus cycle.
   X=Any valid address within the device.
   PA=Address within the selected partition.
   IA=Identifier codes address (See 7.2.2 Identifier Codes for Read Operation).
   QA=Query codes address. Refer to the LH28F320BF, LH28F640BF, LH28F128BF series Appendix for details.
   BA=Address within the block being erased, set/cleared block lock bit or set block lock-down bit.
   WA=Address of memory location for the Program command or the first address for the Page Buffer Program command.
   PCRC=Partition configuration register code presented on the address A_0-A_{15}.
3. ID=Data read from identifier codes (See 7.2.2 Identifier Codes for Read Operation).
   QD=Data read from query database. Refer to the LH28F320BF, LH28F640BF, LH28F128BF series Appendix for details.
   SRD=Data read from status register. See 7.3 Register Definition for a description of the status register bits.
   WD=Data to be programmed at location WA. Data is latched on the rising edge of F-$\overline{WE}$ or F_2-$\overline{CE}$ (whichever goes high first) during command write cycles.
   N-1=N is the number of the words to be loaded into a page buffer.
4. Following the Read Identifier Codes command, read operations access manufacturer code, device code, block lock configuration code, partition configuration register code (See 7.2.2 Identifier Codes for Read Operation).
   The Read Query command is available for reading CFI (Common Flash Interface) information.
5. Block erase, full chip erase or (page buffer) program cannot be executed when the selected block is locked. Unlocked block can be erased or programmed when $\overline{RST}$ is V_{IH}.
6. Either 40H or 10H are recognized by the CUI (Command User Interface) as the program setup.
7. Following the third bus cycle, input the program sequential address and write data of "N" times. Finally, input the any valid address within the target block to be programmed and the confirm command (D0H). Refer to the LH28F320BF, LH28F640BF, LH28F128BF series Appendix for details.

8. If the program operation in one partition is suspended and the erase operation in other partition is also suspended, the suspended program operation should be resumed first, and then the suspended erase operation should be resumed next.
9. Full chip erase operation can not be suspended.
10. Following the Clear Block Lock Bit command, block which is not locked-down is unlocked when $\overline{WP}$ is V_{IL}.
    When $\overline{WP}$ is V_{IH}, lock-down bit is disabled and the selected block is unlocked regardless of lock-down configuration.
11. Commands other than those shown above are reserved by SHARP for future device implementations and should not be used.

7.2.2 Identifier Codes for Read Operation

	Code	Address [A_{15}-A_0]	Data [DQ_{15}-DQ_0]	Notes
Manufacturer Code	Manufacturer Code	0000H	00B0H	4
Device Code	64M (x16) Top Parameter Device Code	0001H	00B0H	1, 4
Block Lock Configuration Code	Block is Unlocked	Block Address + 2	DQ_0 = 0	2
	Block is Locked		DQ_0 = 1	2
	Block is not Locked-Down		DQ_1 = 0	2
	Block is Locked-Down		DQ_1 = 1	2
Device Configuration Code	Partition Configuration Register	0006H	PCRC	3, 4

Notes:

1. Top parameter device has its parameter blocks in the plane 3 (The highest address).
2. Block Address = The beginning location of a block address within the partition to which the Read Identifier Codes command (90H) has been written.
   DQ_{15}-DQ_2 is reserved for future implementation.
3. PCRC = Partition Configuration Register Code.
4. The address A_{21}-A_{16} are shown in below table for reading the manufacturer, device, device configuration code.
   The address to read the identifier codes is dependent on the partition which is selected when writing the Read Identifier Codes command (90H).
   See Section 7.3 Partition Configuration Register Definition (P.38) for the partition configuration register.

Identifier Codes for Read Operation on Partition Configuration (64M (x16)-bit device)

Partition Configuration Register			Address (64M (x16)-bit device)
PCR.10	PCR.9	PCR.8	[A_{21}-A_{16}]
0	0	0	00H
0	0	1	00H or 10H
0	1	0	00H or 20H
1	0	0	00H or 30H
0	1	1	00H or 10H or 20H
1	1	0	00H or 20H or 30H
1	0	1	00H or 10H or 30H
1	1	1	00H or 10H or 20H or 30H

7.2.3 Functions of Block Lock and Block Lock-Down

Current State					Erase/Program Allowed (2)
State	$\overline{WP}$	DQ_1 (1)	DQ_0 (1)	State Name	
[000]	0	0	0	Unlocked	Yes
[001] (3)	0	0	1	Locked	No
[011]	0	1	1	Locked-down	No
[100]	1	0	0	Unlocked	Yes
[101] (3)	1	0	1	Locked	No
[110] (4)	1	1	0	Lock-down Disable	Yes
[111]	1	1	1	Lock-down Disable	No

Notes:

1. DQ_0 = 1: a block is locked; DQ_0 = 0: a block is unlocked.
   DQ_1 = 1: a block is locked-down; DQ_1 = 0: a block is not locked-down.
2. Erase and program are general terms, respectively, to express: block erase, full chip erase and (page buffer) program operations.
3. At power-up or device reset, all blocks default to locked state and are not locked-down, that is, [001] ($\overline{WP}$ = 0) or [101] ($\overline{WP}$ = 1), regardless of the states before power-off or reset operation.
4. When $\overline{WP}$ is driven to V_{IL} in [110] state, the state changes to [011] and the blocks are automatically locked.

7.2.4 Block Locking State Transitions upon Command Write (4)

Current State				Result after Lock Command Written (Next State)		
State	$\overline{WP}$	DQ_1	DQ_0	Set Lock (1)	Clear Lock (1)	Set Lock-down (1)
[000]	0	0	0	[001]	No Change	[011] (2)
[001]	0	0	1	No Change (3)	[000]	[011]
[011]	0	1	1	No Change	No Change	No Change
[100]	1	0	0	[101]	No Change	[111] (2)
[101]	1	0	1	No Change	[100]	[111]
[110]	1	1	0	[111]	No Change	[111] (2)
[111]	1	1	1	No Change	[110]	No Change

Notes:

1. "Set Lock" means Set Block Lock Bit command, "Clear Lock" means Clear Block Lock Bit command and "Set Lock-down" means Set Block Lock-Down Bit command.
2. When the Set Block Lock-Down Bit command is written to the unlocked block (DQ_0 = 0), the corresponding block is locked-down and automatically locked at the same time.
3. "No Change" means that the state remains unchanged after the command written.
4. In this state transitions table, assumes that $\overline{WP}$ is not changed and fixed V_{IL} or V_{IH}.

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7.2.5 Block Locking State Transitions upon $\overline{WP}$ Transition [4]

Previous State	Current State				Result after $\overline{WP}$ Transition (Next State)	
	State	$\overline{WP}$	DQ_1	DQ_0	$\overline{WP} = 0 \rightarrow 1$ [1]	$\overline{WP} = 1 \rightarrow 0$ [1]
-	[000]	0	0	0	[100]	-
-	[001]	0	0	1	[101]	-
[110] [2]	[011]	0	1	1	[110]	-
Other than [110] [2]					[111]	-
-	[100]	1	0	0	-	[000]
-	[101]	1	0	1	-	[001]
-	[110]	1	1	0	-	[011] [3]
-	[111]	1	1	1	-	[011]

Notes:

1. "$\overline{WP} = 0 \rightarrow 1$" means that $\overline{WP}$ is driven to V_{IH} and "$\overline{WP} = 1 \rightarrow 0$" means that $\overline{WP}$ is driven to V_{IL}.
2. State transition from the current state [011] to the next state depends on the previous state.
3. When $\overline{WP}$ is driven to V_{IL} in [110] state, the state changes to [011] and the blocks are automatically locked.
4. In this state transitions table, assumes that lock configuration commands are not written in previous, current and next state.

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7.3 Register Definition

Status Register Definition

R	R	R	R	R	R	R	R
15	14	13	12	11	10	9	8
WSMS	BESS	BEFCES	PBPS	VPPS	PBPSS	DPS	R
7	6	5	4	3	2	1	0

SR.15 - SR.8 = RESERVED FOR FUTURE ENHANCEMENTS (R)	Notes:
SR.7 = WRITE STATE MACHINE STATUS (WSMS) 1 = Ready 0 = Busy	Status Register indicates the status of the partition, not WSM (Write State Machine). Even if the SR.7 is “1”, the WSM may be occupied by the other partition when the device is set to 2, 3 or 4 partitions configuration.
SR.6 = BLOCK ERASE SUSPEND STATUS (BESS) 1 = Block Erase Suspended 0 = Block Erase in Progress/Completed	Check SR.7 or RY/$\overline{BY}$ to determine block erase, full chip erase, (page buffer) program completion. SR.6 - SR.1 are invalid while SR.7= “0”.
SR.5 = BLOCK ERASE AND FULL CHIP ERASE STATUS (BEFCES) 1 = Error in Block Erase or Full Chip Erase 0 = Successful Block Erase or Full Chip Erase	If both SR.5 and SR.4 are “1”s after a block erase, full chip erase, (page buffer) program, set/clear block lock bit, set block lock-down bit or set partition configuration register attempt, an improper command sequence was entered.
SR.4 = (PAGE BUFFER) PROGRAM STATUS (PBPS) 1 = Error in (Page Buffer) Program 0 = Successful (Page Buffer) Program	
SR.3 = V_{PP} STATUS (VPPS) 1 = V_{PP} LOW Detect, Operation Abort 0 = V_{PP} OK	SR.3 does not provide a continuous indication of V_{PP} level. The WSM interrogates and indicates the V_{PP} level only after Block Erase, Full Chip Erase, (Page Buffer) Program command sequences. SR.3 is not guaranteed to report accurate feedback when $V_{PP} \neq V_{PPH}$ or V_{PPLK}.
SR.2 = (PAGE BUFFER) PROGRAM SUSPEND STATUS (PBPSS) 1 = (Page Buffer) Program Suspended 0 = (Page Buffer) Program in Progress/Completed	
SR.1 = DEVICE PROTECT STATUS (DPS) 1 = Erase or Program Attempted on a Locked Block, Operation Abort 0 = Unlocked	SR.1 does not provide a continuous indication of block lock bit. The WSM interrogates the block lock bit only after Block Erase, Full Chip Erase, (Page Buffer) Program command sequences. It informs the system, depending on the attempted operation, if the block lock bit is set. Reading the block lock configuration codes after writing the Read Identifier Codes command indicates block lock bit status.
SR.0 =RESERVED FOR FUTURE ENHANCEMENTS (R)	SR.15 - SR.8 and SR.0 are reserved for future use and should be masked out when polling the status register.

Extended Status Register Definition

R	R	R	R	R	R	R	R
15	14	13	12	11	10	9	8
SMS	R	R	R	R	R	R	R
7	6	5	4	3	2	1	0

XSR.15-8 = RESERVED FOR FUTURE ENHANCEMENTS (R) XSR.7 = STATE MACHINE STATUS (SMS) 1 = Page Buffer Program available 0 = Page Buffer Program not available XSR.6-0 = RESERVED FOR FUTURE ENHANCEMENTS (R)	Notes: After issue a Page Buffer Program command (E8H), XSR.7="1" indicates that the entered command is accepted. If XSR.7 is "0", the command is not accepted and a next Page Buffer Program command (E8H) should be issued again to check if page buffer is available or not. XSR.15-8 and XSR.6-0 are reserved for future use and should be masked out when polling the extended status register.

Partition Configuration Register Definition

R	R	R	R	R	PC2	PC1	PC0
15	14	13	12	11	10	9	8
R	R	R	R	R	R	R	R
7	6	5	4	3	2	1	0

PCR.15-11 = RESERVED FOR FUTURE ENHANCEMENTS (R)

PCR.10-8 = PARTITION CONFIGURATION (PC2-0)

- 000 = No partitioning. Dual Work is not allowed.
- 001 = Plane1-3 are merged into one partition. (default in a bottom parameter device)
- 010 = Plane 0-1 and Plane 2-3 are merged into one partition respectively.
- 100 = Plane 0-2 are merged into one partition. (default in a top parameter device)
- 011 = Plane 2-3 are merged into one partition. There are three partitions in this configuration. Dual work operation is available between any two partitions.
- 110 = Plane 0-1 are merged into one partition. There are three partitions in this configuration. Dual work operation is available between any two partitions.
- 101 = Plane 1-2 are merged into one partition. There are three partitions in this configuration. Dual work operation is available between any two partitions.
- 111 = There are four partitions in this configuration. Each plane corresponds to each partition respectively. Dual work operation is available between any two partitions.

PCR.7-0 = RESERVED FOR FUTURE ENHANCEMENTS (R)

Notes:
After power-up or device reset, PCR 10-8 (PC2-0) is set to “001” in a bottom parameter device and “100” in a top parameter device.

See the table below for more details.

PCR.15-11 and PCR.7-0 are reserved for future use and should be masked out when checking the partition configuration register.

Partition Configuration

PC2 PC1 PC0	PARTITIONING FOR DUAL WORK	PC2 PC1 PC0	PARTITIONING FOR DUAL WORK
0 0 0	PARTITION0: PLANE3, PLANE2, PLANE1, PLANE0	0 1 1	PARTITION2: PLANE3, PLANE2; PARTITION1: PLANE1; PARTITION0: PLANE0
0 0 1	PARTITION1: PLANE3, PLANE2, PLANE1; PARTITION0: PLANE0	1 1 0	PARTITION2: PLANE3; PARTITION1: PLANE2; PARTITION0: PLANE1, PLANE0
0 1 0	PARTITION1: PLANE3, PLANE2; PARTITION0: PLANE1, PLANE0	1 0 1	PARTITION2: PLANE3; PARTITION1: PLANE2, PLANE1; PARTITION0: PLANE0
1 0 0	PARTITION1: PLANE3; PARTITION0: PLANE2, PLANE1, PLANE0	1 1 1	PARTITION3: PLANE3; PARTITION2: PLANE2; PARTITION1: PLANE1; PARTITION0: PLANE0

7.4 Memory Map for Flash Memory

Top Parameter

PLANE3 (PARAMETER PLANE)

BLOCK NUMBER		ADDRESS RANGE
134	4K-WORD	3FF000H - 3FFFFFH
133	4K-WORD	3FE000H - 3FEFFFH
132	4K-WORD	3FD000H - 3FDFFFH
131	4K-WORD	3FC000H - 3FCFFFH
130	4K-WORD	3FB000H - 3FBFFFH
129	4K-WORD	3FA000H - 3FAFFFH
128	4K-WORD	3F9000H - 3F9FFFH
127	4K-WORD	3F8000H - 3F8FFFH
126	32K-WORD	3F0000H - 3F7FFFH
125	32K-WORD	3E8000H - 3EFFFFH
124	32K-WORD	3E0000H - 3E7FFFH
123	32K-WORD	3D8000H - 3DFFFFH
122	32K-WORD	3D0000H - 3D7FFFH
121	32K-WORD	3C8000H - 3CFFFFH
120	32K-WORD	3C0000H - 3C7FFFH
119	32K-WORD	3B8000H - 3BFFFFH
118	32K-WORD	3B0000H - 3B7FFFH
117	32K-WORD	3A8000H - 3AFFFFH
116	32K-WORD	3A0000H - 3A7FFFH
115	32K-WORD	398000H - 39FFFFH
114	32K-WORD	390000H - 397FFFH
113	32K-WORD	388000H - 38FFFFH
112	32K-WORD	380000H - 387FFFH
111	32K-WORD	378000H - 37FFFFH
110	32K-WORD	370000H - 377FFFH
109	32K-WORD	368000H - 36FFFFH
108	32K-WORD	360000H - 367FFFH
107	32K-WORD	358000H - 35FFFFH
106	32K-WORD	350000H - 357FFFH
105	32K-WORD	348000H - 34FFFFH
104	32K-WORD	340000H - 347FFFH
103	32K-WORD	338000H - 33FFFFH
102	32K-WORD	330000H - 337FFFH
101	32K-WORD	328000H - 32FFFFH
100	32K-WORD	320000H - 327FFFH
99	32K-WORD	318000H - 31FFFFH
98	32K-WORD	310000H - 317FFFH
97	32K-WORD	308000H - 30FFFFH
96	32K-WORD	300000H - 307FFFH

PLANE2 (UNIFORM PLANE)

95	32K-WORD	2F8000H - 2FFFFFH
94	32K-WORD	2F0000H - 2F7FFFH
93	32K-WORD	2E8000H - 2EFFFFH
92	32K-WORD	2E0000H - 2E7FFFH
91	32K-WORD	2D8000H - 2DFFFFH
90	32K-WORD	2D0000H - 2D7FFFH
89	32K-WORD	2C8000H - 2CFFFFH
88	32K-WORD	2C0000H - 2C7FFFH
87	32K-WORD	2B8000H - 2BFFFFH
86	32K-WORD	2B0000H - 2B7FFFH
85	32K-WORD	2A8000H - 2AFFFFH
84	32K-WORD	2A0000H - 2A7FFFH
83	32K-WORD	298000H - 29FFFFH
82	32K-WORD	290000H - 297FFFH
81	32K-WORD	288000H - 28FFFFH
80	32K-WORD	280000H - 287FFFH
79	32K-WORD	278000H - 27FFFFH
78	32K-WORD	270000H - 277FFFH
77	32K-WORD	268000H - 26FFFFH
76	32K-WORD	260000H - 267FFFH
75	32K-WORD	258000H - 25FFFFH
74	32K-WORD	250000H - 257FFFH
73	32K-WORD	248000H - 24FFFFH
72	32K-WORD	240000H - 247FFFH
71	32K-WORD	238000H - 23FFFFH
70	32K-WORD	230000H - 237FFFH
69	32K-WORD	228000H - 22FFFFH
68	32K-WORD	220000H - 227FFFH
67	32K-WORD	218000H - 21FFFFH
66	32K-WORD	210000H - 217FFFH
65	32K-WORD	208000H - 20FFFFH
64	32K-WORD	200000H - 207FFFH

PLANE1 (UNIFORM PLANE)

BLOCK NUMBER		ADDRESS RANGE
63	32K-WORD	1F8000H - 1FFFFFH
62	32K-WORD	1F0000H - 1F7FFFH
61	32K-WORD	1E8000H - 1EFFFFH
60	32K-WORD	1E0000H - 1E7FFFH
59	32K-WORD	1D8000H - 1DFFFFH
58	32K-WORD	1D0000H - 1D7FFFH
57	32K-WORD	1C8000H - 1CFFFFH
56	32K-WORD	1C0000H - 1C7FFFH
55	32K-WORD	1B8000H - 1BFFFFH
54	32K-WORD	1B0000H - 1B7FFFH
53	32K-WORD	1A8000H - 1AFFFFH
52	32K-WORD	1A0000H - 1A7FFFH
51	32K-WORD	198000H - 19FFFFH
50	32K-WORD	190000H - 197FFFH
49	32K-WORD	188000H - 18FFFFH
48	32K-WORD	180000H - 187FFFH
47	32K-WORD	178000H - 17FFFFH
46	32K-WORD	170000H - 177FFFH
45	32K-WORD	168000H - 16FFFFH
44	32K-WORD	160000H - 167FFFH
43	32K-WORD	158000H - 15FFFFH
42	32K-WORD	150000H - 157FFFH
41	32K-WORD	148000H - 14FFFFH
40	32K-WORD	140000H - 147FFFH
39	32K-WORD	138000H - 13FFFFH
38	32K-WORD	130000H - 137FFFH
37	32K-WORD	128000H - 12FFFFH
36	32K-WORD	120000H - 127FFFH
35	32K-WORD	118000H - 11FFFFH
34	32K-WORD	110000H - 117FFFH
33	32K-WORD	108000H - 10FFFFH
32	32K-WORD	100000H - 107FFFH

PLANE0 (UNIFORM PLANE)

31	32K-WORD	0F8000H - 0FFFFFH
30	32K-WORD	0F0000H - 0F7FFFH
29	32K-WORD	0E8000H - 0EFFFFH
28	32K-WORD	0E0000H - 0E7FFFH
27	32K-WORD	0D8000H - 0DFFFFH
26	32K-WORD	0D0000H - 0D7FFFH
25	32K-WORD	0C8000H - 0CFFFFH
24	32K-WORD	0C0000H - 0C7FFFH
23	32K-WORD	0B8000H - 0BFFFFH
22	32K-WORD	0B0000H - 0B7FFFH
21	32K-WORD	0A8000H - 0AFFFFH
20	32K-WORD	0A0000H - 0A7FFFH
19	32K-WORD	098000H - 09FFFFH
18	32K-WORD	090000H - 097FFFH
17	32K-WORD	088000H - 08FFFFH
16	32K-WORD	080000H - 087FFFH
15	32K-WORD	078000H - 07FFFFH
14	32K-WORD	070000H - 077FFFH
13	32K-WORD	068000H - 06FFFFH
12	32K-WORD	060000H - 067FFFH
11	32K-WORD	058000H - 05FFFFH
10	32K-WORD	050000H - 057FFFH
9	32K-WORD	048000H - 04FFFFH
8	32K-WORD	040000H - 047FFFH
7	32K-WORD	038000H - 03FFFFH
6	32K-WORD	030000H - 037FFFH
5	32K-WORD	028000H - 02FFFFH
4	32K-WORD	020000H - 027FFFH
3	32K-WORD	018000H - 01FFFFH
2	32K-WORD	010000H - 017FFFH
1	32K-WORD	008000H - 00FFFFH
0	32K-WORD	000000H - 007FFFH

7.5 DC Electrical Characteristics for Flash Memory

DC Electrical Characteristics

(T_A = -25°C to +85°C, V_{CC} = 2.7V to 3.1V)

Symbol	Parameter	Notes	Min.	Typ.	Max.	Unit	Test Conditions
C_{IN}	Input Capacitance	5			7	pF	V_{IN} = 0V, f = 1MHz, T_A = 25°C
C_{IO}	I/O Capacitance	5			10	pF	$V_{I/O}$ = 0V, f = 1MHz, T_A = 25°C
I_{LI}	Input Leakage Current				±1	µA	$V_{IN} = V_{CC}$ or GND
I_{LO}	Output Leakage Current				±1	µA	$V_{OUT} = V_{CC}$ or GND
I_{CCS}	V_{CC} Standby Current	1, 8		4	20	µA	$V_{CC} = V_{CC}$ Max., F_2-$\overline{CE}$ = $\overline{RST}$ = V_{CC} ±0.2V, $\overline{WP}$ = V_{CC} or GND
I_{CCAS}	V_{CC} Automatic Power Savings Current	1, 4		4	20	µA	$V_{CC} = V_{CC}$ Max., F_2-$\overline{CE}$ = GND ±0.2V, $\overline{WP}$ = V_{CC} or GND
I_{CCD}	V_{CC} Reset Power-Down Current	1		4	20	µA	$\overline{RST}$ = GND ±0.2V I_{OUT} (RY/$\overline{BY}$) = 0mA
I_{CCR}	Average V_{CC} Read Current Normal Mode	1, 7		15	25	mA	$V_{CC} = V_{CC}$ Max., F_2-$\overline{CE}$ = V_{IL}, F-$\overline{OE}$ = V_{IH}, f = 5MHz I_{OUT} = 0mA
	Average V_{CC} Read Current Page Mode — 8 Word Read	1, 7		5	10	mA	
I_{CCW}	V_{CC} (Page Buffer) Program Current	1, 5, 7		20	60	mA	$V_{PP} = V_{PPH}$
I_{CCE}	V_{CC} Block Erase, Full Chip Erase Current	1, 5, 7		10	30	mA	$V_{PP} = V_{PPH}$
I_{CCWS} I_{CCES}	V_{CC} (Page Buffer) Program or Block Erase Suspend Current	1, 2, 7		10	200	µA	F_2-$\overline{CE}$ = V_{IH}
I_{PPS} I_{PPR}	V_{PP} Standby or Read Current	1, 6, 7		2	5	µA	$V_{PP} \leq V_{CC}$
I_{PPW}	V_{PP} (Page Buffer) Program Current	1,5,6,7		2	5	µA	$V_{PP} = V_{PPH}$
I_{PPE}	V_{PP} Block Erase, Full Chip Erase Current	1,5,6,7		2	5	µA	$V_{PP} = V_{PPH}$
I_{PPWS}	V_{PP} (Page Buffer) Program Suspend Current	1, 6, 7		2	5	µA	$V_{PP} = V_{PPH}$
I_{PPES}	V_{PP} Block Erase Suspend Current	1, 6, 7		2	5	µA	$V_{PP} = V_{PPH}$

DC Electrical Characteristics (Continue)

(T_A = -25°C to +85°C, V_{CC} = 2.7V to 3.1V)

Symbol	Parameter	Notes	Min.	Typ.	Max.	Unit	Test Conditions
V_{IL}	Input Low Voltage	5	-0.2		0.4	V	
V_{IH}	Input High Voltage	5	VCC -0.4		VCC +0.2	V	
V_{OL}	Output Low Voltage	5, 8			0.2VCC	V	I_{OL} = 0.5mA
V_{OH}	Output High Voltage	5	0.8VCC			V	I_{OH} = -0.5mA
V_{PPLK}	V_{PP} Lockout during Normal Operations	3,5,6			0.4	V	
V_{PPH}	V_{PP} during Block Erase, Full Chip Erase, (Page Buffer) Program Operations	6	1.65	3	3.1	V	
V_{LKO}	V_{CC} Lockout Voltage		1.5			V	

Notes:

1. All currents are in RMS unless otherwise noted. Typical values are the reference values at V_{CC} = 3.0V and T_A = +25°C unless V_{CC} is specified.
2. I_{CCWS} and I_{CCES} are specified with the device de-selected. If read or (page buffer) program is executed while in block erase suspend mode, the device's current draw is the sum of I_{CCES} and I_{CCR} or I_{CCW}. If read is executed while in (page buffer) program suspend mode, the device's current draw is the sum of I_{CCWS} and I_{CCR}.
3. Block erase, full chip erase, (page buffer) program are inhibited when $V_{PP} \leq V_{PPLK}$, and not guaranteed outside the specified voltage.
4. The Automatic Power Savings (APS) feature automatically places the device in power save mode after read cycle completion. Standard address access timings (t_{AVQV}) provide new data when addresses are changed.
5. Sampled, not 100% tested.
6. V_{PP} is not used for power supply pin. With $V_{PP} \leq V_{PPLK}$, block erase, full chip erase, (page buffer) program cannot be executed and should not be attempted.
7. The operating current in dual work is the sum of the operating current (read, erase, program) in each plane.
8. Includes RY/$\overline{BY}$

7.6 AC Electrical Characteristics for Flash Memory

7.6.1 AC Test Conditions

Input Pulse Level	0 V to 2.7 V
Input Rise and Fall Time	5 ns
Input and Output Timing Ref. level	1.35 V
Output Load	1TTL +C_L (50pF)

7.6.2 Read Cycle

(T_A = -25°C to +85°C, V_{CC} = 2.7V to 3.1V)

Symbol	Parameter	Notes	Min.	Max.	Unit
t_{AVAV}	Read Cycle Time		65		ns
t_{AVQV}	Address to Output Delay			65	ns
t_{ELQV}	F_2-$\overline{CE}$ to Output Delay	2		65	ns
t_{APA}	Page Address Access Time			25	ns
t_{GLQV}	F-$\overline{OE}$ to Output Delay	2		20	ns
t_{PHQV}	$\overline{RST}$ High to Output Delay			150	ns
t_{EHQZ}, t_{GHQZ}	F_2-$\overline{CE}$ or F-$\overline{OE}$ to Output in High-Z, Whichever Occurs First	1		20	ns
t_{ELQX}	F_2-$\overline{CE}$ to Output in Low-Z	1	0		ns
t_{GLQX}	F-$\overline{OE}$ to Output in Low-Z	1	0		ns
t_{OH}	Output Hold from First Occurring Address, F_2-$\overline{CE}$ or F-$\overline{OE}$ Change	1	0		ns

Notes:

1. Sampled, not 100% tested.
2. F-$\overline{OE}$ may be delayed up to $t_{ELQV} - t_{GLQV}$ after the falling edge of F_2-$\overline{CE}$ without impact to t_{ELQV}.

7.6.3 Write Cycle (F-$\overline{WE}$ / F_2-$\overline{CE}$ Controlled) [1,2]

(T_A = -25°C to +85°C, V_{CC} = 2.7V to 3.1V)

Symbol	Parameter	Notes	Min.	Max.	Unit
t_{AVAV}	Write Cycle Time		65		ns
t_{PHWL} (t_{PHEL})	$\overline{RST}$ High Recovery to F-$\overline{WE}$ (F_2-$\overline{CE}$) Going Low	3	150		ns
t_{ELWL} (t_{WLEL})	F_2-$\overline{CE}$ (F-$\overline{WE}$) Setup to F-$\overline{WE}$ (F_2-$\overline{CE}$) Going Low		0		ns
t_{WLWH} (t_{ELEH})	F-$\overline{WE}$ (F_2-$\overline{CE}$) Pulse Width	4	50		ns
t_{DVWH} (t_{DVEH})	Data Setup to F-$\overline{WE}$ (F_2-$\overline{CE}$) Going High	8	40		ns
t_{AVWH} (t_{AVEH})	Address Setup to F-$\overline{WE}$ (F_2-$\overline{CE}$) Going High	8	50		ns
t_{WHEH} (t_{EHWH})	F_2-$\overline{CE}$ (F-$\overline{WE}$) Hold from F-$\overline{WE}$ (F_2-$\overline{CE}$) High		0		ns
t_{WHDX} (t_{EHDX})	Data Hold from F-$\overline{WE}$ (F_2-$\overline{CE}$) High		0		ns
t_{WHAX} (t_{EHAX})	Address Hold from F-$\overline{WE}$ (F_2-$\overline{CE}$) High		0		ns
t_{WHWL} (t_{EHEL})	F-$\overline{WE}$ (F_2-$\overline{CE}$) Pulse Width High	5	15		ns
t_{SHWH} (t_{SHEH})	$\overline{WP}$ High Setup to F-$\overline{WE}$ (F_2-$\overline{CE}$) Going High	3	0		ns
t_{VVWH} (t_{VVEH})	V_{PP} Setup to F-$\overline{WE}$ (F_2-$\overline{CE}$) Going High	3	200		ns
t_{WHGL} (t_{EHGL})	Write Recovery before Read		30		ns
t_{QVSL}	$\overline{WP}$ High Hold from Valid SRD, RY/$\overline{BY}$ High-Z	3, 6	0		ns
t_{QVVL}	V_{PP} Hold from Valid SRD, RY/$\overline{BY}$ High-Z	3, 6	0		ns
t_{WHR0} (t_{EHR0})	F-$\overline{WE}$ (F_2-$\overline{CE}$) High to SR.7 Going "0"	3, 7		t_{AVQV}+50	ns
t_{WHRL} (t_{EHRL})	F-$\overline{WE}$ (F_2-$\overline{CE}$) High to RY/$\overline{BY}$ Going Low	3		100	ns

Notes:

1. The timing characteristics for reading the status register during block erase, full chip erase, (page buffer) program operations are the same as during read-only operations. See the AC Characteristics for read cycle.
2. A write operation can be initiated and terminated with either F_2-$\overline{CE}$ or F-$\overline{WE}$.
3. Sampled, not 100% tested.
4. Write pulse width (t_{WP}) is defined from the falling edge of F_2-$\overline{CE}$ or F-$\overline{WE}$ (whichever goes low last) to the rising edge of F_2-$\overline{CE}$ or F-$\overline{WE}$ (whichever goes high first). Hence, $t_{WP}=t_{WLWH}=t_{ELEH}=t_{WLEH}=t_{ELWH}$.
5. Write pulse width high (t_{WPH}) is defined from the rising edge of F_2-$\overline{CE}$ or F-$\overline{WE}$ (whichever goes high first) to the falling edge of F_2-$\overline{CE}$ or F-$\overline{WE}$ (whichever goes low last). Hence, $t_{WPH}=t_{WHWL}=t_{EHEL}=t_{WHEL}=t_{EHWL}$.
6. V_{PP} should be held at $V_{PP}=V_{PPH}$ until determination of block erase, full chip erase, (page buffer) program success (SR.1/3/4/5=0).
7. t_{WHR0} (t_{EHR0}) after the Read Query or Read Identifier Codes command=t_{AVQV}+100ns.
8. See 7.2.1 Command Definitions for valid address and data for block erase, full chip erase, (page buffer) program or lock bit configuration.

7.6.4 Block Erase, Full Chip Erase, (Page Buffer) Program Performance [3]

(T_A = -25°C to +85°C, V_{CC} = 2.7V to 3.1V)

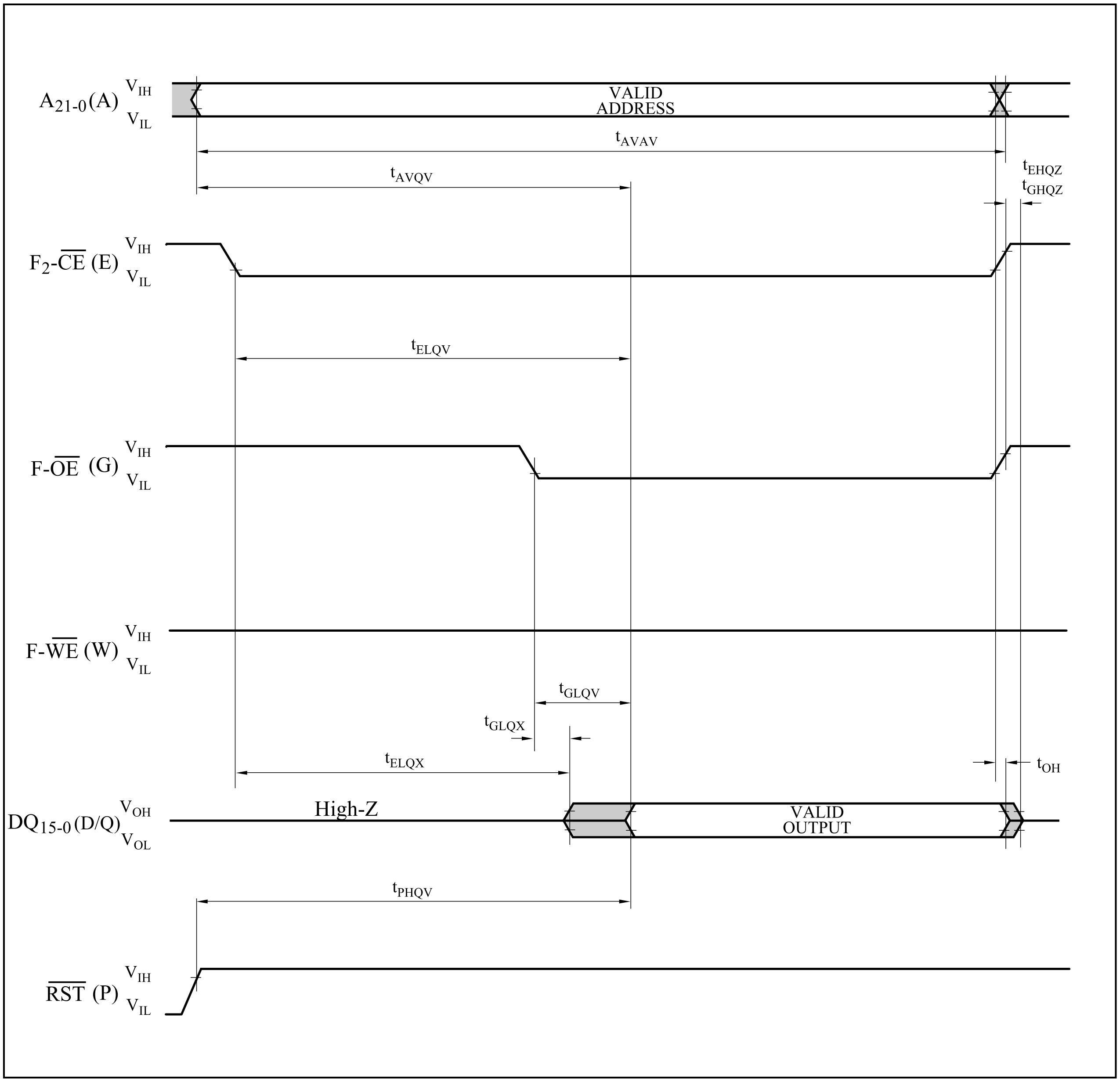
Symbol	Parameter	Notes	Page Buffer Command is Used or not Used	$V_{PP}=V_{PPH}$			Unit
				Min.	Typ. [1]	Max. [2]	
t_{WPB}	4K-Word Parameter Block Program Time	2	Not Used		0.05	0.3	s
		2	Used		0.03	0.12	s
t_{WMB}	32K-Word Main Block Program Time	2	Not Used		0.38	2.4	s
		2	Used		0.24	1	s
t_{WHQV1}/ t_{EHQV1}	Word Program Time	2	Not Used		11	200	µs
		2	Used		7	100	µs
t_{WHQV2}/ t_{EHQV2}	4K-Word Parameter Block Erase Time	2	-		0.3	4	s
t_{WHQV3}/ t_{EHQV3}	32K-Word Main Block Erase Time	2	-		0.6	5	s
	Full Chip Erase Time	2			80	700	s
t_{WHRH1}/ t_{EHRH1}	(Page Buffer) Program Suspend Latency Time to Read	4	-		5	10	µs
t_{WHRH2}/ t_{EHRH2}	Block Erase Suspend Latency Time to Read	4	-		5	20	µs
t_{ERES}	Latency Time from Block Erase Resume Command to Block Erase Suspend Command	5	-	500			µs

Notes:

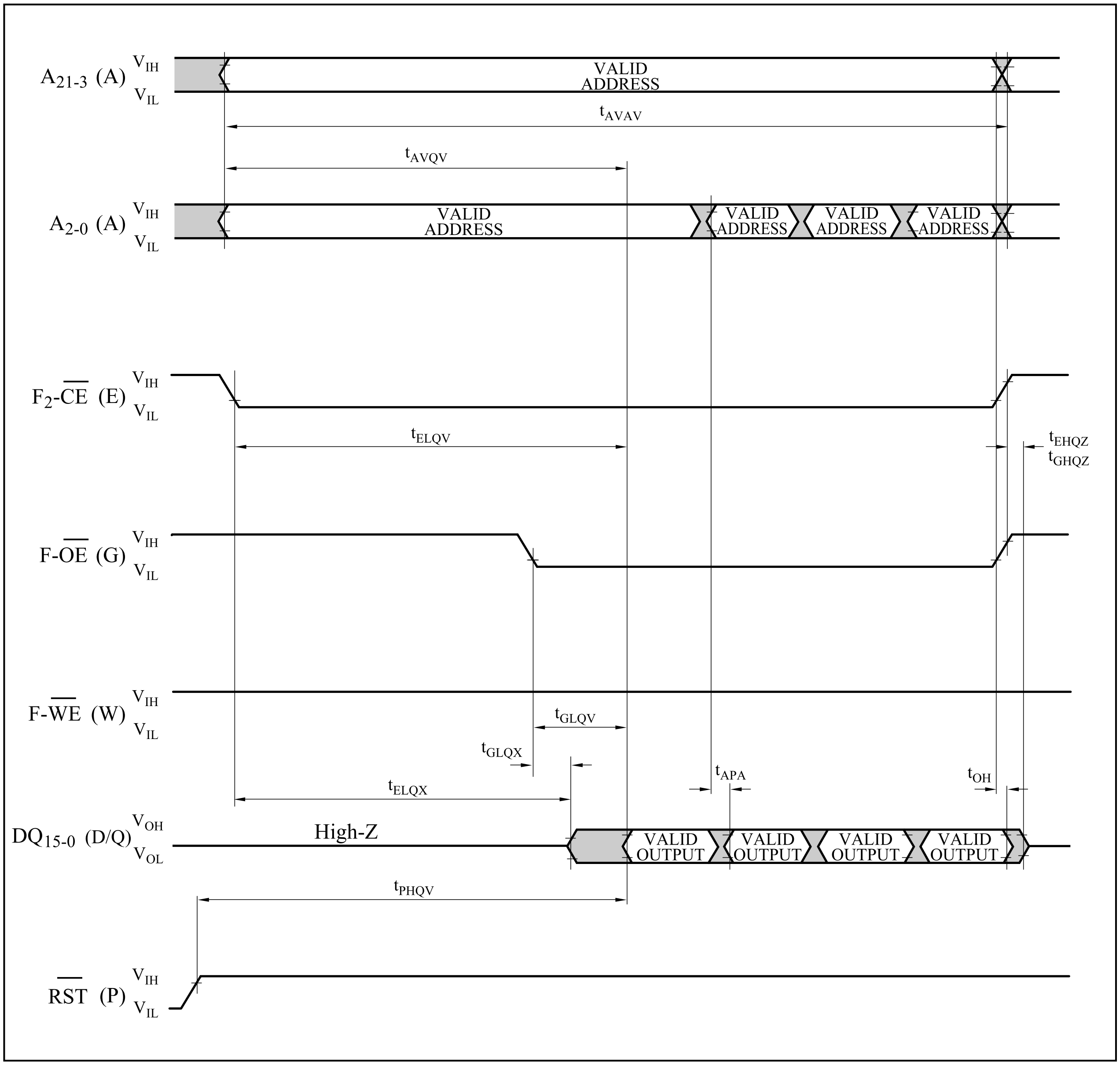
1. Typical values measured at V_{CC} =3.0V, V_{PP} =3.0V, and T_A=+25°C. Assumes corresponding lock bits are not set. Subject to change based on device characterization.
2. Excludes external system-level overhead.
3. Sampled, but not 100% tested.
4. A latency time is required from writing suspend command (F-$\overline{WE}$ or F_2-$\overline{CE}$ going high) until SR.7 going “1” or RY/$\overline{BY}$ going High-Z.
5. If the interval time from a Block Erase Resume command to a subsequent Block Erase Suspend command is shorter than t_{ERES} and its sequence is repeated, the block erase operation may not be finished.

7.6.5 Flash Memory AC Characteristics Timing Chart

AC Waveform for Single Asynchronous Read Operations from Status Register, Identifier Codes or Query Code



AC Waveform for Asynchronous 4-Word Page Mode Read Operations from Main Blocks or Parameter Blocks



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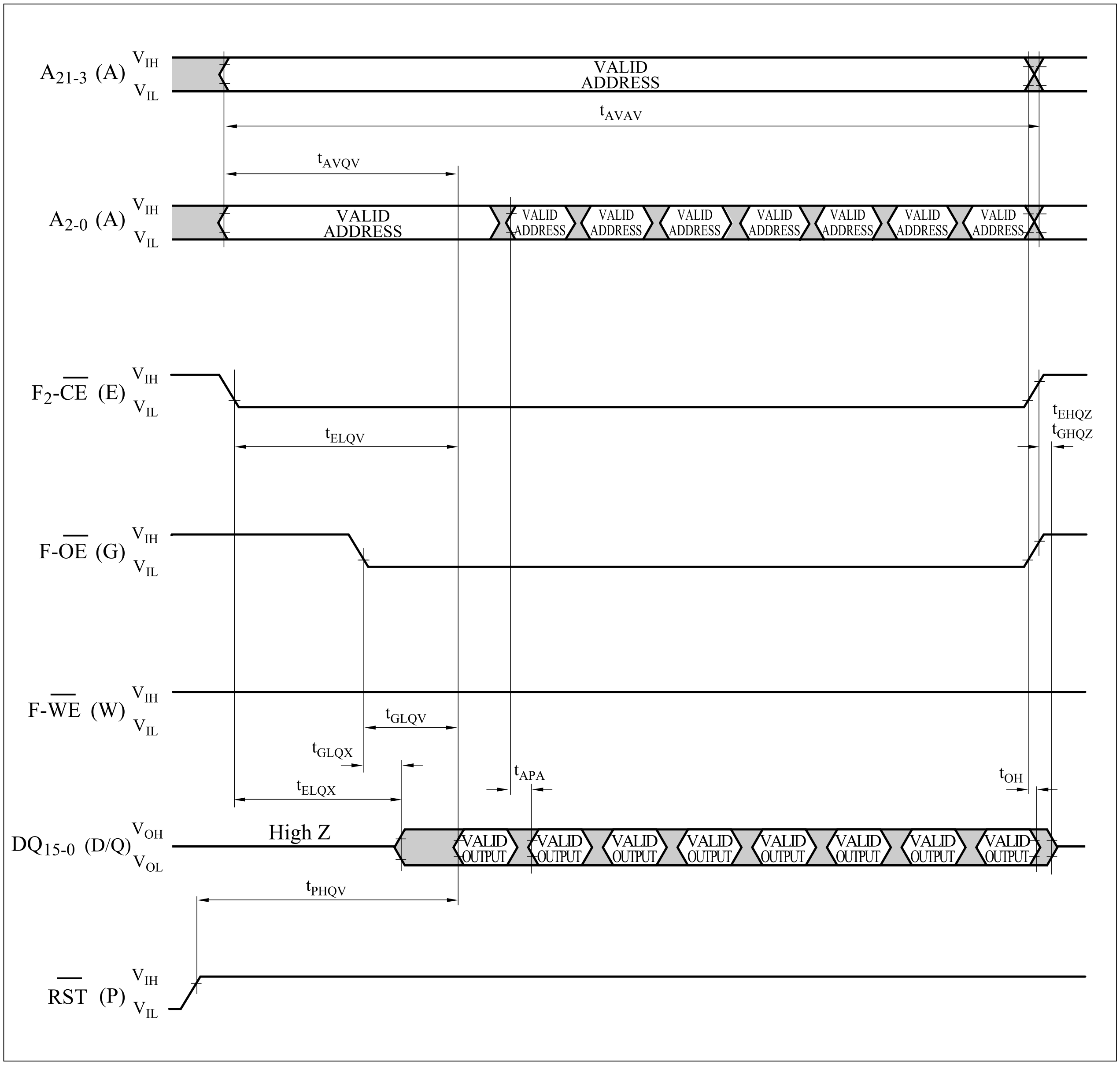
AC Waveform for Asynchronous 8-Word Page Mode Read Operations from Main Blocks or Parameter Blocks



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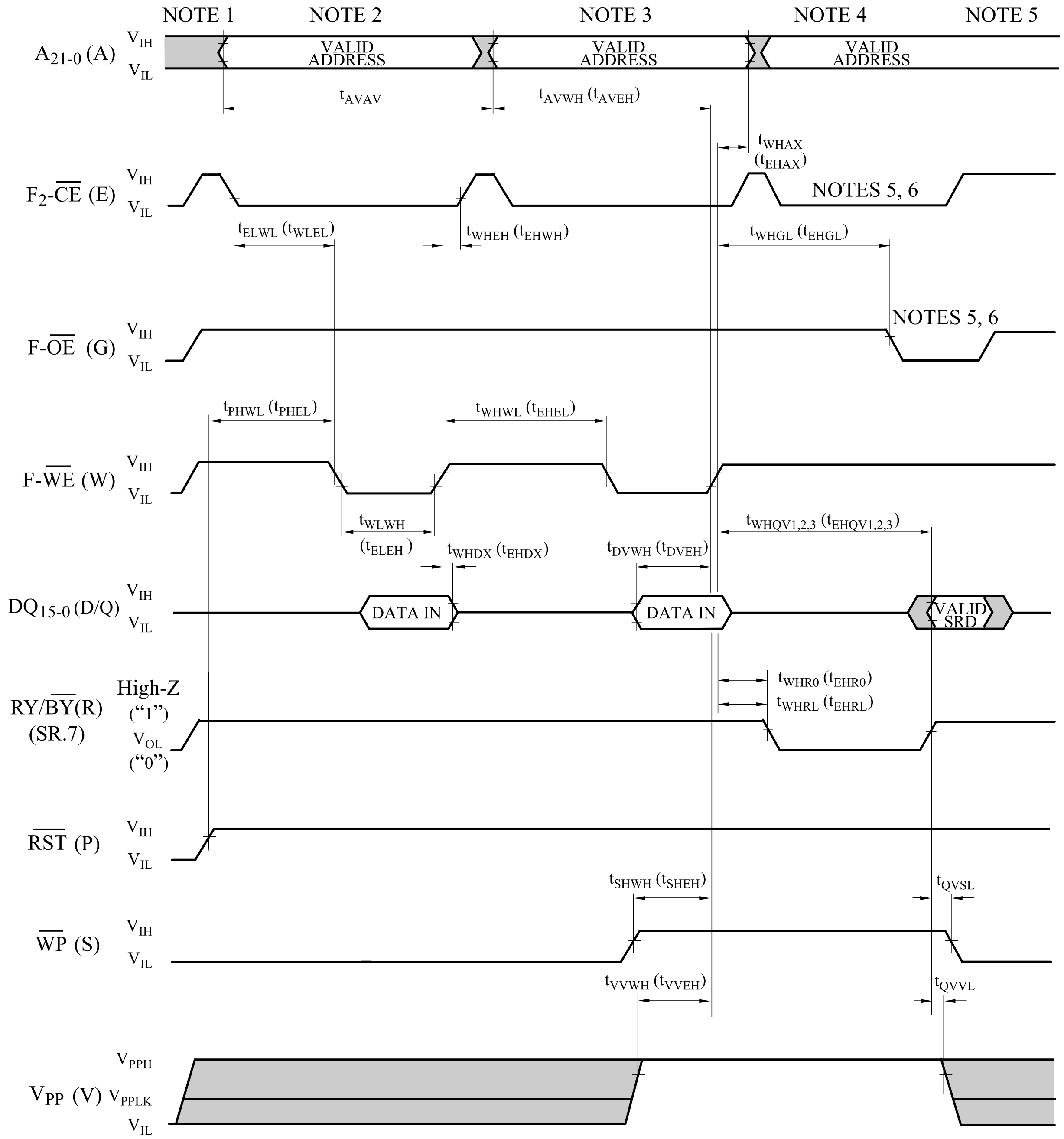
AC Waveform for Write Operations (F-$\overline{WE}$ / F2-$\overline{CE}$ Controlled)



Notes:
1. Vcc power-up and standby.
2. Write each first cycle command.
3. Write each second cycle command or valid address and data.
4. Automated erase or program delay.
5. Read status register data.
6. For read operation, F-$\overline{OE}$ and F 2-$\overline{CE}$ must be driven active, and F-$\overline{WE}$ de-asserted.

7.6.6 Reset Operations

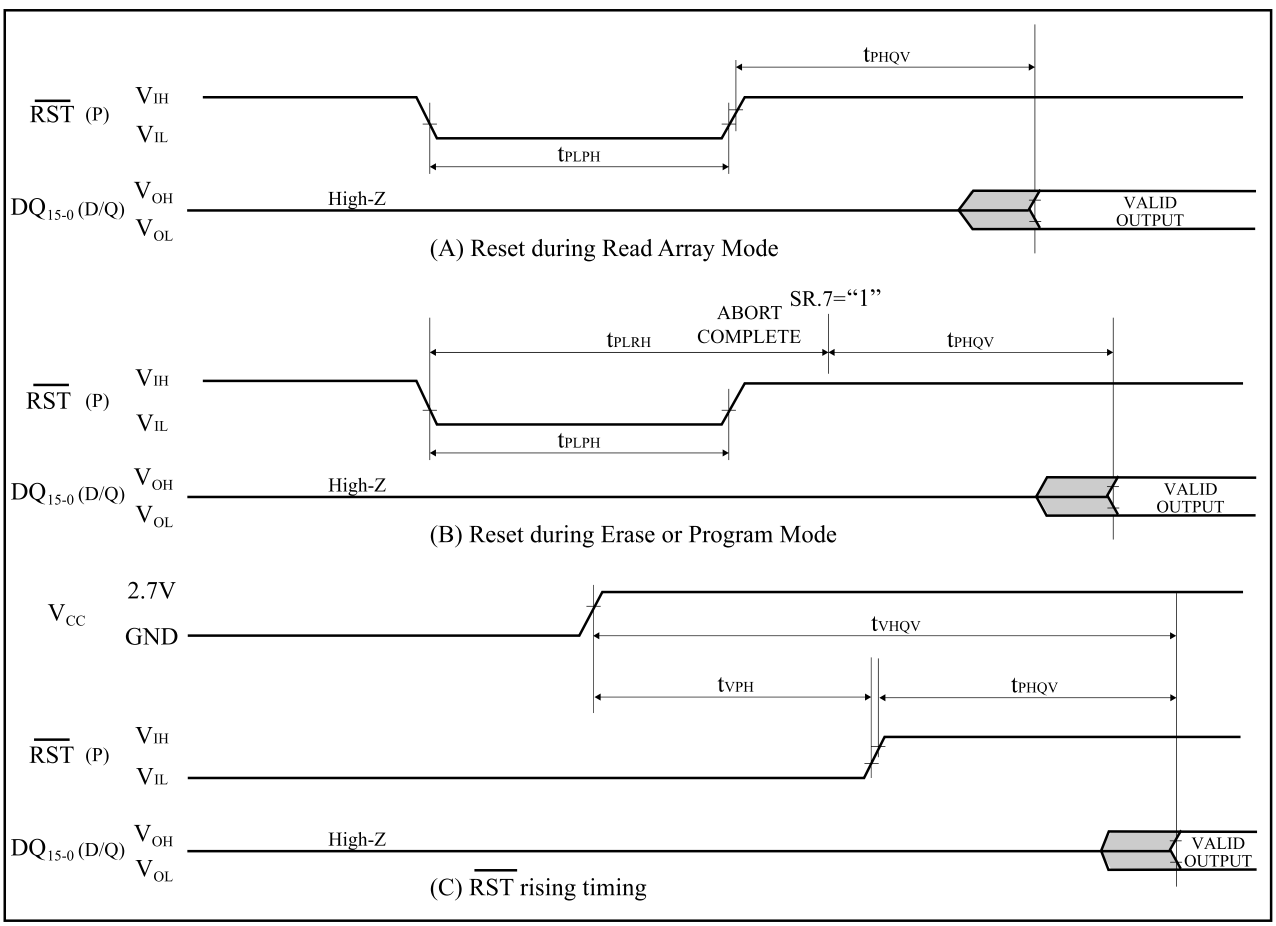
(T_A = -25°C to +85°C, V_{CC} = 2.7V to 3.1V)

Symbol	Parameter	Notes	Min.	Max.	Unit
t_{PLPH}	$\overline{RST}$ Low to Reset during Read ($\overline{RST}$ should be low during power-up.)	1, 2, 3	100		ns
t_{PLRH}	$\overline{RST}$ Low to Reset during Erase or Program	1, 3, 4		22	µs
t_{VPH}	V_{CC} = 2.7V to $\overline{RST}$ High	1, 3, 5	100		ns
t_{VHQV}	V_{CC} = 2.7V to Output Delay	3		1	ms

Notes:

1. A reset time, t_{PHQV}, is required from the later of SR.7 (RY/$\overline{BY}$) going “1” (High-Z) or $\overline{RST}$ going high until outputs are valid. See the AC Characteristics - read cycle for t_{PHQV}.
2. t_{PLPH} is <100ns the device may still reset but this is not guaranteed.
3. Sampled, not 100% tested.
4. If $\overline{RST}$ asserted while a block erase, full chip erase or (page buffer) program operation is not executing, the reset will complete within 100ns.
5. When the device power-up, holding $\overline{RST}$ low minimum 100ns is required after V_{CC} has been in predefined range and also has been in stable there.

AC Waveform for Reset Operation



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8. Smartcombo RAM

8.1 Truth Table

8.1.1 Bus Operation [1]

<table>
<tr><th>Smartcombo RAM</th><th>Notes</th><th>SC-$\overline{CE}_1$</th><th>CE_2</th><th>S-$\overline{OE}$</th><th>S-$\overline{WE}$</th><th>$\overline{LB}$</th><th>$\overline{UB}$</th><th>DQ_0 to Q_{15}</th></tr>
<tr><td>Read</td><td></td><td rowspan="3">L</td><td rowspan="4">H</td><td>L</td><td>H</td><td colspan="2">(3)</td><td>(3)</td></tr>
<tr><td>Output Disable</td><td></td><td>H</td><td>H</td><td>X</td><td>X</td><td>High - Z</td></tr>
<tr><td>Write</td><td></td><td>H</td><td>L</td><td colspan="2">(3)</td><td>(3)</td></tr>
<tr><td rowspan="2">Standby</td><td rowspan="2"></td><td>H</td><td rowspan="3">X</td><td rowspan="3">X</td><td>X</td><td>X</td><td rowspan="3">High - Z</td></tr>
<tr><td>X</td><td>H</td><td>H</td></tr>
<tr><td>Sleep</td><td>2</td><td>X</td><td>L</td><td>X</td><td>X</td></tr>
</table>

Notes:

1. L = V_{IL}, H = V_{IH}, X = H or L, High-Z = High impedance. Refer to the DC Characteristics.
2. CE_2 pin must be fixed to high level except sleep mode.
3. $\overline{LB}$, $\overline{UB}$ Control Mode

$\overline{LB}$	$\overline{UB}$	DQ_0 to DQ_7	DQ_8 to DQ_{15}
L	L	D_{OUT}/D_{IN}	D_{OUT}/D_{IN}
L	H	D_{OUT}/D_{IN}	High - Z
H	L	High - Z	D_{OUT}/D_{IN}

8.2 DC Electrical Characteristics for Smartcombo RAM

DC Electrical Characteristics

(T_A = -25°C to +85°C, V_{CC} = 2.7V to 3.1V)

Symbol	Parameter	Notes	Min.	Typ.	Max.	Unit	Test Conditions
C_{IN}	Input Capacitance	1			8	pF	V_{IN} = 0V
C_{IO}	I/O Capacitance	1			10	pF	$V_{I/O}$ = 0V
I_{LI}	Input Leakage Current				±1	μA	$V_{IN} = V_{CC}$ or GND
I_{LO}	Output Leakage Current				±1	μA	$V_{OUT} = V_{CC}$ or GND
I_{SB}	V_{CC} Standby Current	2			200	μA	SC-$\overline{CE}_1 \geq V_{CC}$ - 0.2V, $CE_2 \geq V_{CC}$ - 0.2V
I_{SLP}	V_{CC} Sleep Mode Current	3			100	μA	SC-$\overline{CE}_1 \geq V_{CC}$ - 0.2V, $CE_2 \leq$ 0.2V
I_{CC1}	V_{CC} Operation Current				50	mA	t_{CYCLE} = Min., $I_{I/O}$ = 0mA, SC-$\overline{CE}_1 = V_{IL}$
V_{IL}	Input Low Voltage	1	-0.2		0.4	V	
V_{IH}	Input High Voltage	1	Vcc -0.4		Vcc +0.2	V	
V_{OL}	Output Low Voltage	1			0.2Vcc	V	I_{OL} = 0.5mA
V_{OH}	Output High Voltage	1	0.8Vcc			V	I_{OH} = -0.5mA

Notes:
1. Sampled, not 100% tested.
2. Memory cell data is held. (CE_2 = "VIH")
3. Memory cell data is not held. (CE_2 = "VIL")

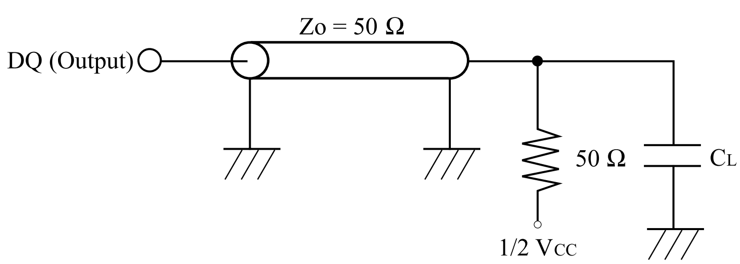
8.3 AC Electrical Characteristic for Smartcombo RAM

8.3.1 AC Test Conditions

Input Pulse Level	0.2VCC to 0.8VCC
Input Rise and Fall Time	5 ns
Input and Output Timing Ref. Level	1/2 V_{CC}
Output Load	1TTL +C_L (50pF) (1, 2)

Notes:

1. Including scope and socket capacitance.
2. AC characteristics directed with the note should be measured with the output load shown in below.



8.3.2 Read Cycle

(T_A = -25°C to +85°C, V_{CC} = 2.7V to 3.1V)

Symbol	Parameter	Notes	Min.	Max.	Unit
t_{RC}	Read Cycle Time		65		ns
t_{AA}	Address Access Time			65	ns
t_{ACE}	Chip Enable Access Time			65	ns
t_{OE}	Output Enable to Output Valid			45	ns
t_{BE}	Byte Enable Access Time			65	ns
t_{PAA}	Page Access Time			20	ns
t_{OH}	Output Hold from Address Change		5		ns
t_{PRC}	Page Read Cycle Time		20		ns
t_{CLZ}	SC-$\overline{CE}_1$ Low to Output Active		10		ns
t_{OLZ}	S-$\overline{OE}$ Low to Output Active		5		ns
t_{BLZ}	$\overline{UB}$ or $\overline{LB}$ Low to Output Active		5		ns
t_{CHZ}	SC-$\overline{CE}_1$ High to Output in High-Z			25	ns
t_{OHZ}	S-$\overline{OE}$ High to Output in High-Z			25	ns
t_{BHZ}	$\overline{UB}$ or $\overline{LB}$ High to Output in High-Z			25	ns
t_{ASO}	Address Setup to S-$\overline{OE}$ Low		0		ns
t_{OHAH}	S-$\overline{OE}$ High Level to Address Hold		-5		ns
t_{CHAH}	SC-$\overline{CE}_1$ High Level to Address Hold		0		ns
t_{BHAH}	$\overline{LB}$, $\overline{UB}$ High Level to Address Hold	2	0		ns
t_{CLOL}	SC-$\overline{CE}_1$ Low Level to S-$\overline{OE}$ Low Level	1	0	10,000	ns
t_{OLCH}	S-$\overline{OE}$ Low Level to SC-$\overline{CE}_1$ High Level		45		ns
t_{CP}	SC-$\overline{CE}_1$ High Level Pulse Width		10		ns
t_{BP}	$\overline{LB}$, $\overline{UB}$ High Level Pulse Width		10		ns
t_{OP}	S-$\overline{OE}$ High Level Pulse Width	1	2	10,000	ns

Notes:

1. t_{CLOL} and t_{OP} (Max.) are applied while SC-$\overline{CE}_1$ is being hold at low level.
2. t_{BHAH} is specified after both $\overline{LB}$ and $\overline{UB}$ are High.

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8.3.3 Write Cycle

(T_A = -25°C to +85°C, V_{CC} = 2.7V to 3.1V)

Symbol	Parameter	Notes	Min.	Max.	Unit
t_{WC}	Write Cycle Time		65		ns
t_{CW}	Chip Enable to End of Write		55		ns
t_{AW}	Address Valid to End of Write		55		ns
t_{BW}	Byte Select Time		55		ns
t_{WP}	Write Pulse Width		50		ns
t_{WR}	Write Recovery Time		0		ns
t_{CP}	SC-$\overline{CE}_1$ High Level Pulse Width		10		ns
t_{BP}	$\overline{LB}$, $\overline{UB}$ High Level Pulse Width		10		ns
t_{WHP}	S-$\overline{WE}$ High Pulse Width		10		ns
t_{WHZ}	S-$\overline{WE}$ Low to Output in High-Z			25	ns
t_{OW}	S-$\overline{WE}$ High to Output Active		15		ns
t_{AS}	Address Setup Time		0		ns
t_{DW}	Input Data Setup Time		30		ns
t_{DH}	Input Data Hold Time		0		ns
t_{OHAH}	S-$\overline{OE}$ High Level to Address Hold		-5		ns
t_{CHAH}	SC-$\overline{CE}_1$ High Level to Address Hold		0		ns
t_{BHAH}	$\overline{LB}$, $\overline{UB}$ High Level to Address Hold	2	0		ns
t_{OES}	S-$\overline{OE}$ High Level to S-$\overline{WE}$ Set	1	0	10,000	ns
t_{OEH}	S-$\overline{WE}$ High Level to S-$\overline{OE}$ Set	1	10	10,000	ns

Notes:

1. t_{OES} and t_{OEH} (Max.) are applied while SC-$\overline{CE}_1$ is being hold at low level.
2. t_{BHAH} is specified after both $\overline{LB}$ and $\overline{UB}$ are High.

8.3.4 Initialization

(T_A = -25°C to +85°C, V_{CC} = 2.7V to 3.1V)

Symbol	Parameter	Notes	Min.	Max.	Unit
t_{VHMH}	Power Application to CE_2 Low Level Hold		50		µs
t_{CHMH}	SC-$\overline{CE}_1$ High Level to CE_2 High Level		10		ns
t_{MHCL}	Following Power Application CE_2 High Level Hold to SC-$\overline{CE}_1$ Low Level	1	200		µs

Note:

1. When giving compatibility with the other type of Smartcombo RAM, 200µs must be changed to 300µs.

8.3.5 Sleep Mode Entry / Exit

(T_A = -25°C to +85°C, V_{CC} = 2.7V to 3.1V)

Symbol	Parameter	Notes	Min.	Max.	Unit
t_{CHML}	Sleep Mode Entry SC-$\overline{CE}_1$ High Level to CE_2 Low Level		0		ns
t_{MHCL}	Sleep Mode Exit to Normal Operation CE_2 High Level to SC-$\overline{CE}_1$ Low Level	1	200		µs

Note:

1. When giving compatibility with the other type of Smartcombo RAM, 200µs must be changed to 300µs.

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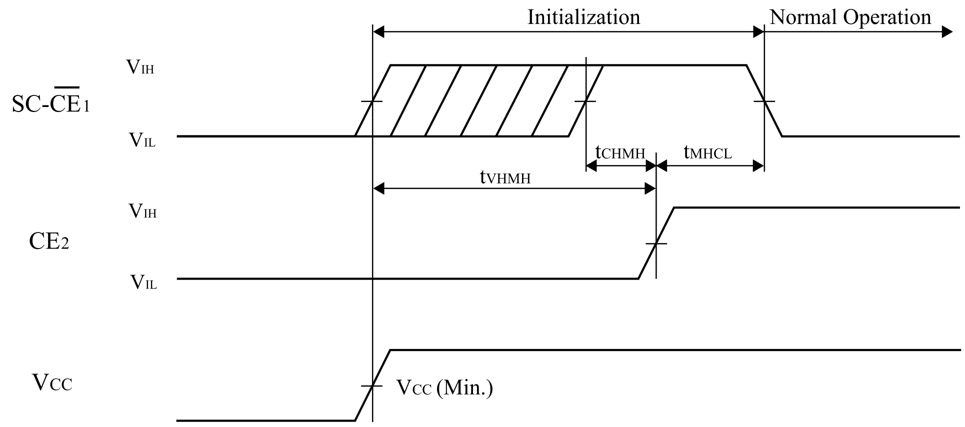
8.4 Initialization

Initialize the power application using the following sequence to stabilize internal circuits.

(1) Following power application, make CE_2 high level after fixing CE_2 to low level for the period of t_{VHMH}. Make SC-$\overline{CE}_1$ high level before making CE_2 high level.

(2) SC-$\overline{CE}_1$ and CE_2 are fixed to high level for the period of t_{MHCL}.

Normal operation is possible after the completion of initialization.



Notes:
1. Make CE_2 low level when starting the power supply.
2. t_{VHMH} is specified from when the power supply voltage reaches the prescribed minimum value (V_{CC} Min.).

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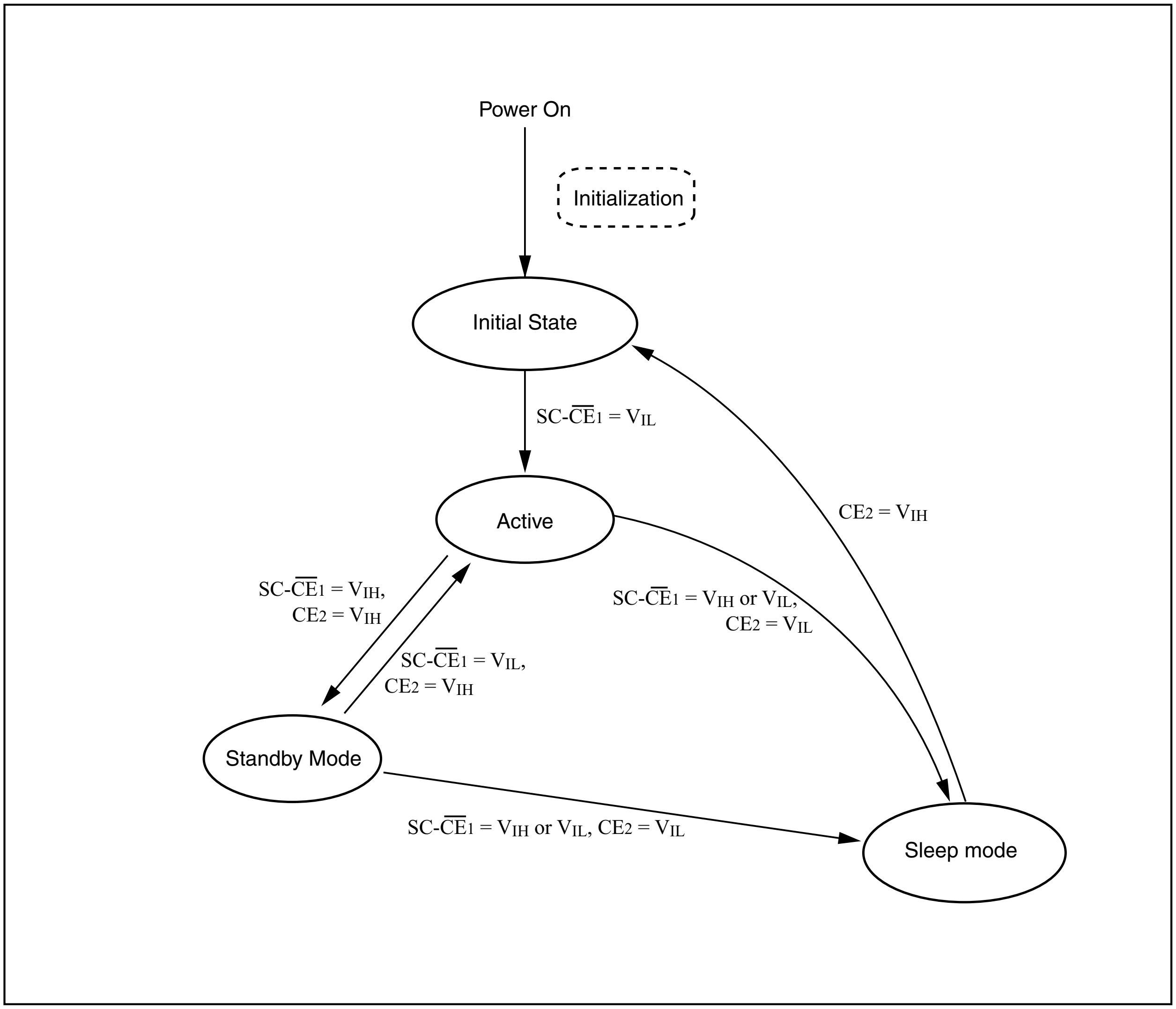
Standby Mode State Machine



8.5 Page Read Operation

8.5.1 Features of Page Read Operation [2]

Features	Notes	8 Words Mode
Page Length		8 words
Page Read-corresponding Addresses		A_2, A_1, A_0
Page Read Start Address		Don't care
Page Direction		Don't care
Interrupt during page read operation	1	Enabled

Notes:

1. An interrupt is output when SC-$\overline{CE}_1$ = High or in case A_3 or a higher address changes.
2. Page Length:
   8 words is supported as the page lengths.

   Page-Corresponding Addresses:
   The page read-enabled addresses are A_2, A_1, and A_0. Fix addresses other than A_2, A_1, and A_0 during page read operation.

   Page Start Address:
   Since random page read is supported, any address (A_2, A_1, A_0) can be used as the page read start address.

   Page Direction:
   Since random page read is possible, there is not restriction on the page direction.

   Interrupt during Page Read Operation:
   When generating an interrupt during page read, either make SC-$\overline{CE}_1$ high level or change A_3 and higher addresses.

   When page read is not used:
   Since random page read is supported, even when not using page read, random access is possible as usual.

8.6 Mode Register Settings

The sleep mode can be set using the mode register. Since the initial value of the mode register at power application is undefined, be sure to set the mode register after initialization at power application. However, since sleep mode is not entered unless CE_2 = Low when sleep mode is not used, it is not necessary to set the mode register. Moreover, when using page read without using sleep mode, it is not necessary to set the mode register.

8.6.1 Mode Register Setting Method

The mode register setting mode can be entered by successively writing two specific data after two continuous reads of the highest address (3FFFFFH). The mode register setting is a continuous four-cycle operation (two read cycles and two write cycles).

Commands are written to the command register. The command register is used to latch the addresses and data required for executing commands, and it does not have an exclusive memory area.

For the timing chart and flow chart, refer to Mode Register Setting Timing Chart (P.71), Mode Register Setting Flow Chart (P.72).

Following table shows the commands and command sequences.

Command Sequence

Command Sequence	1st Bus Cycle (Read Cycle)		2nd Bus Cycle (Read Cycle)		3rd Bus Cycle (Write Cycle)		4th Bus Cycle (Write Cycle)	
	Address	Data	Address	Data	Address	Data	Address	Data
Sleep Mode	3FFFFFH	-	3FFFFFH	-	3FFFFFH	00H	3FFFFFH	07H

4th Bus Cycle (Write cycle)

DQ	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Mode Register Setting	0	0	0	0	0	0	0	0	0	0	0	0	0	PL	1	1

Page Length	1	8 words

8.6.2 Cautions for Setting Mode Register

Since, for the mode register setting, the internal counter status is judged by toggling SC-$\overline{CE}_1$ and S-$\overline{OE}$, toggle SC-$\overline{CE}_1$ at every cycle during entry (read cycle twice, write cycle twice), and toggle S-$\overline{OE}$ like SC-$\overline{CE}_1$ at the first and second read cycles.

If incorrect addresses or data are written, or if addresses or data are written in the incorrect order, the setting of the mode register are not performed correctly.

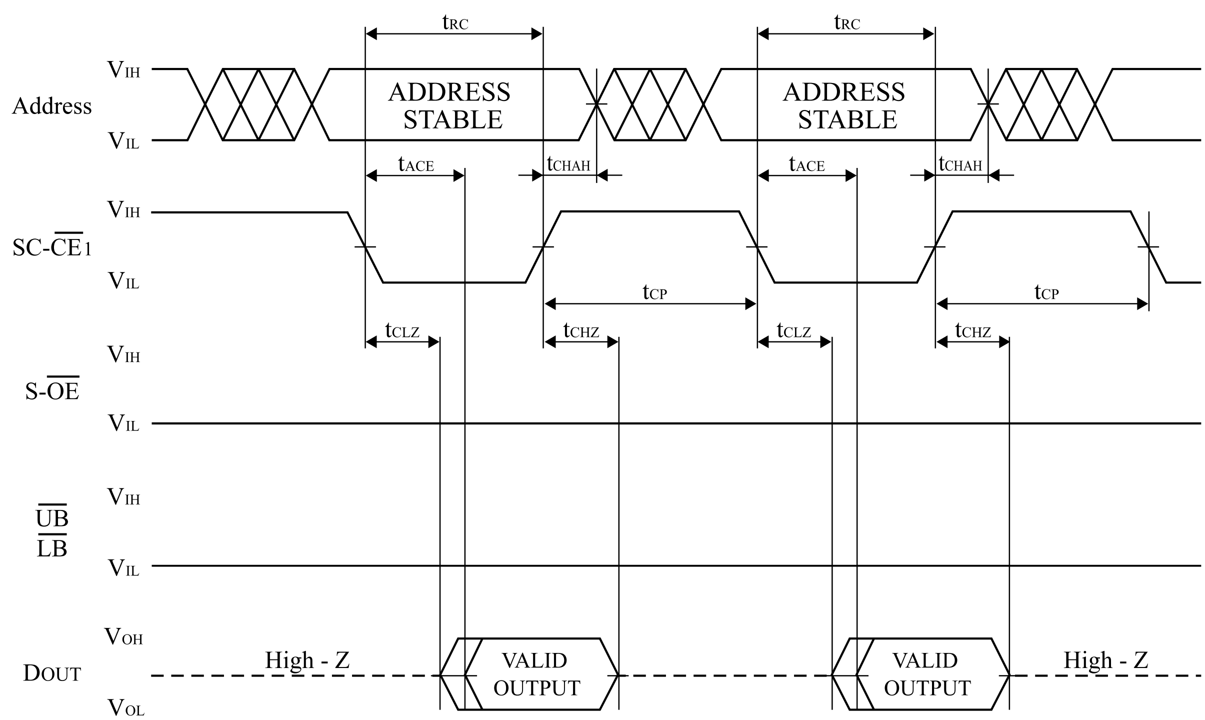
When the highest address (3FFFFFH) is read consecutively three or more times, the mode register setting entries are cancelled.

Once the sleep mode has been set in the mode register, these settings are retained until they are set again, while applying the power supply. However, the mode register setting will become undefined if the power is turned off, so set the mode register again after power application.

For the timing chart and flow chart, refer to Mode Register Setting Timing Chart (P.71), Mode Register Setting Flow Chart (P.72).

8.7 Smartcombo RAM AC Characteristics Timing Chart

Read Cycle Timing Chart 1 (SC-$\overline{CE}_1$ Controlled)



Note:
1. In read cycle, CE_2 and S-$\overline{WE}$ should be fixed to high level.

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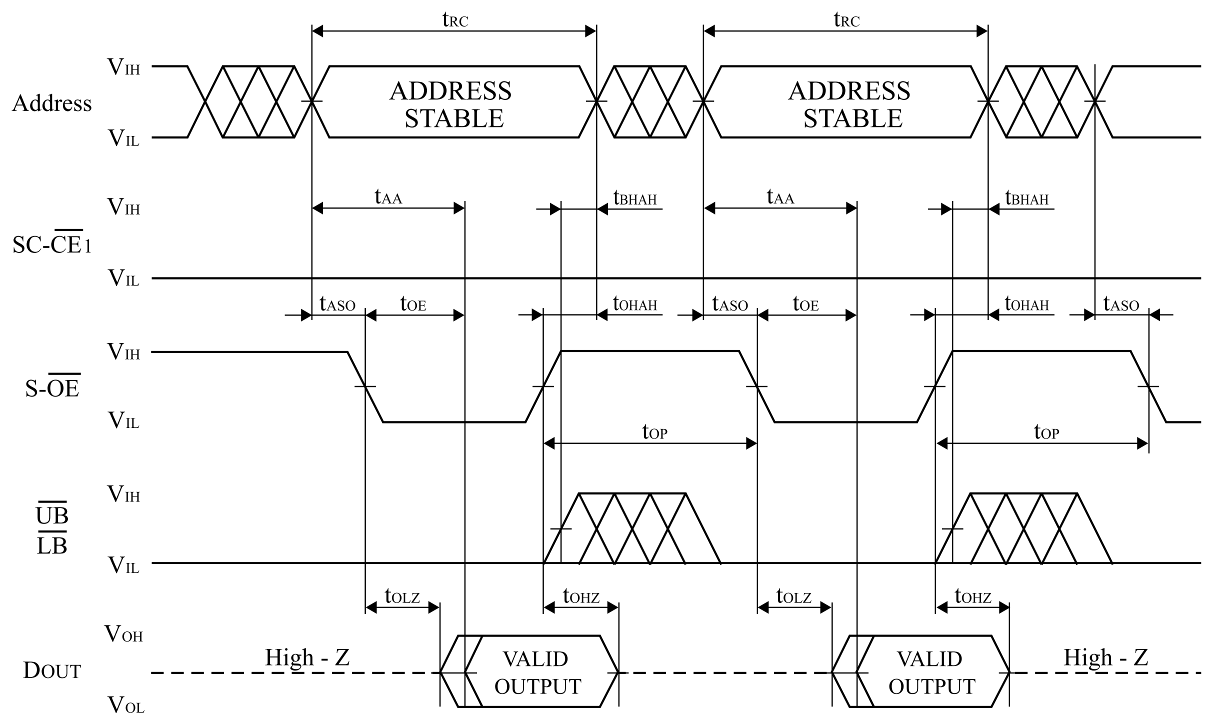
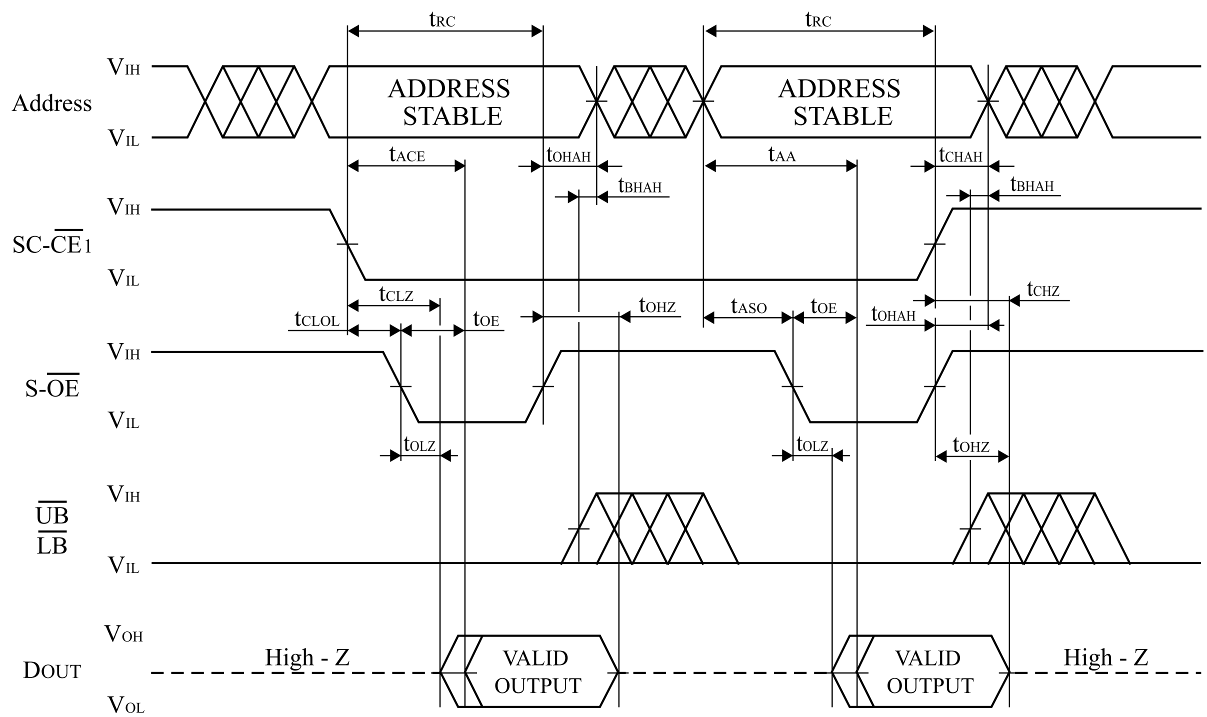
Read Cycle Timing Chart 2 (S-$\overline{OE}$ Controlled)



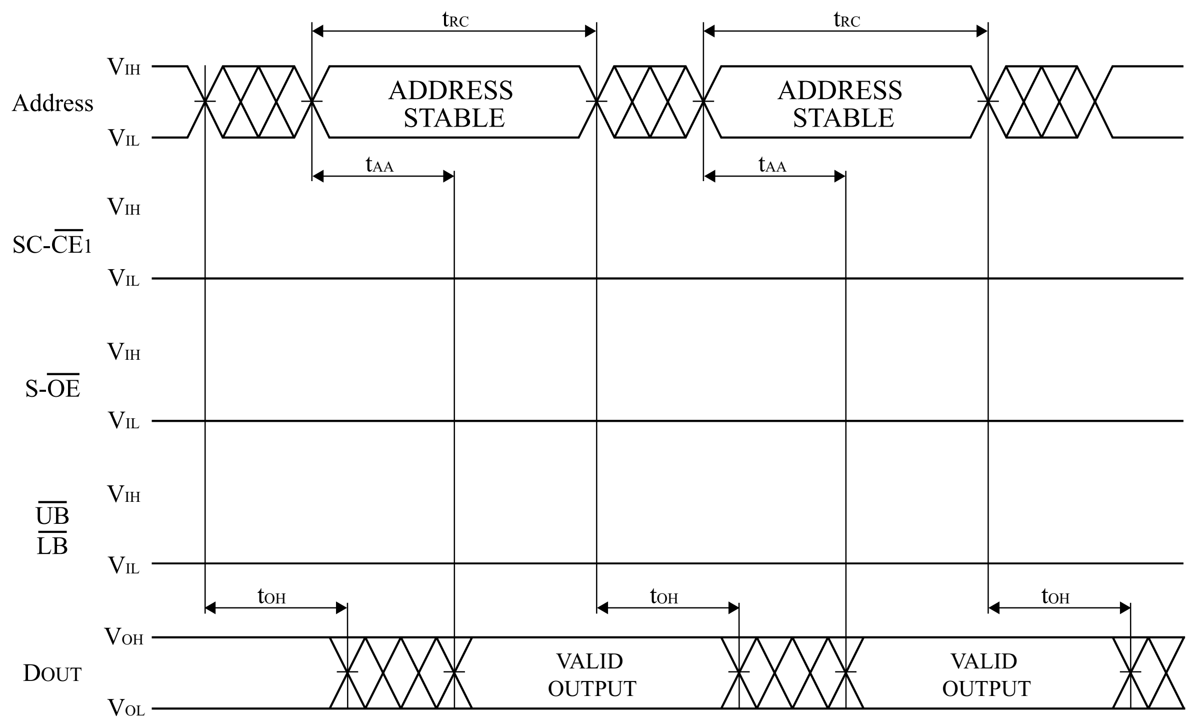
Note:
1. In read cycle, CE_2 and S-$\overline{WE}$ should be fixed to high level.

Read Cycle Timing Chart 3 (SC-$\overline{CE}_1$ / S-$\overline{OE}$ Controlled)



Note:
1. In read cycle, CE_2 and S-$\overline{WE}$ should be fixed to high level.

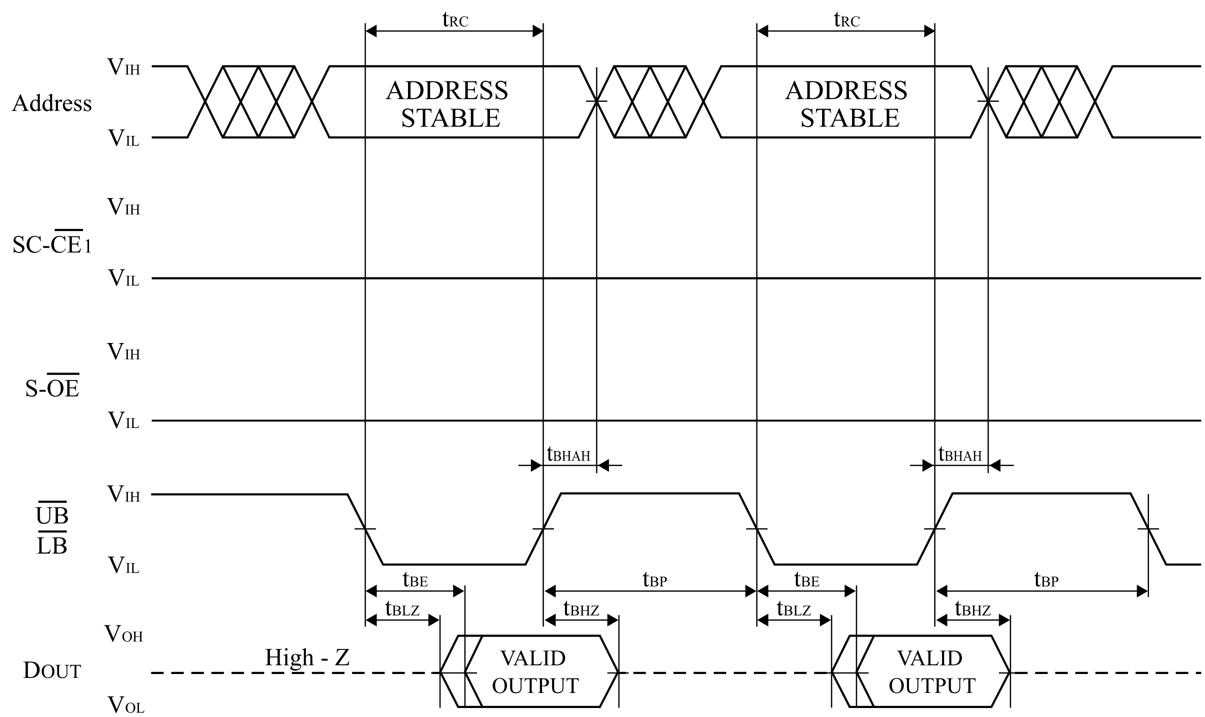
Read Cycle Timing Chart 4 (Address Controlled)



Notes:

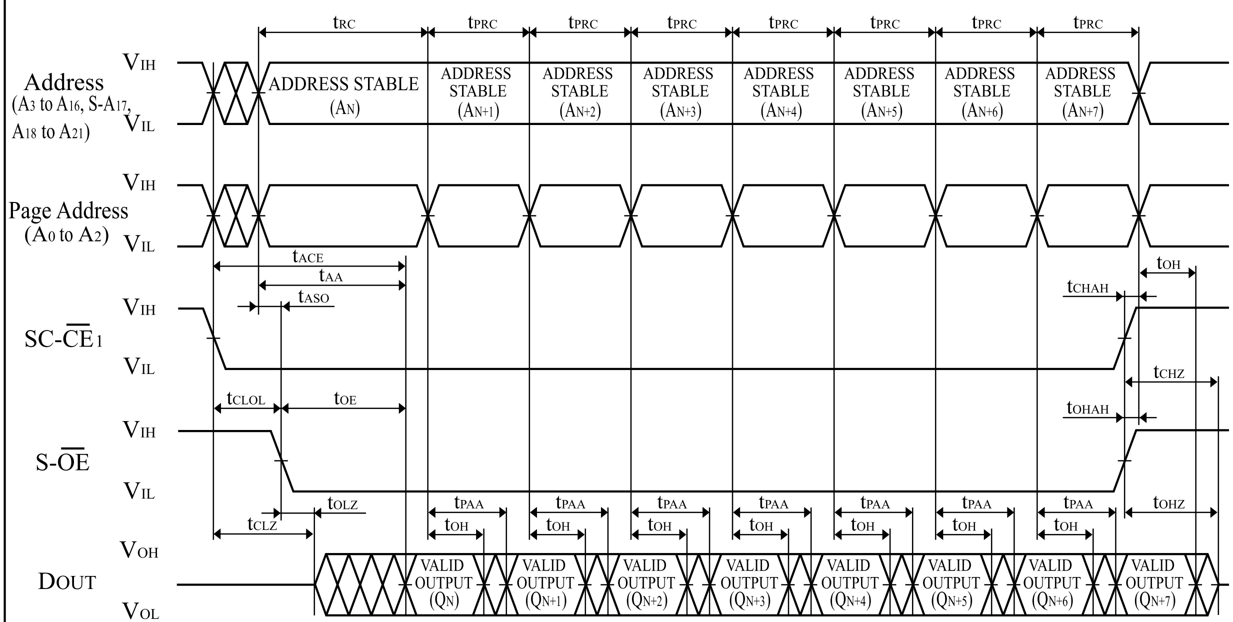
1. In read cycle, CE2 and S-$\overline{WE}$ should be fixed to high level.
2. When read cycle time is less than t_{RC} (Min.), the address access time (t_{AA}) is not guaranteed.

Read Cycle Timing Chart 5 ($\overline{LB}$ / $\overline{UB}$ Controlled)



Note:
1. In read cycle, CE2 and S-$\overline{WE}$ should be fixed to high level.

8 Word Page Read Cycle Timing Chart



Notes:
1. In read cycle, CE 2 and S-$\overline{WE}$ should be fixed to high level.
2. $\overline{LB}$ and $\overline{UB}$ are Low level.

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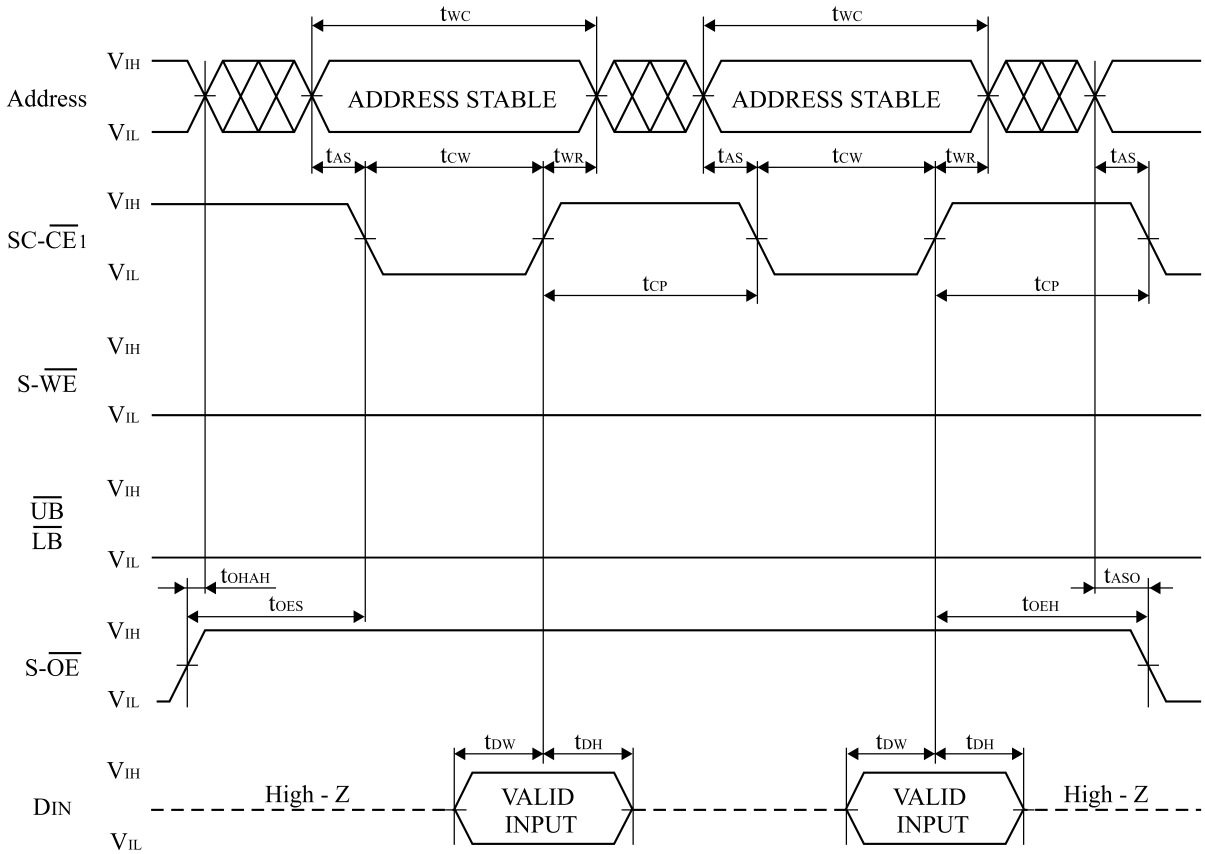
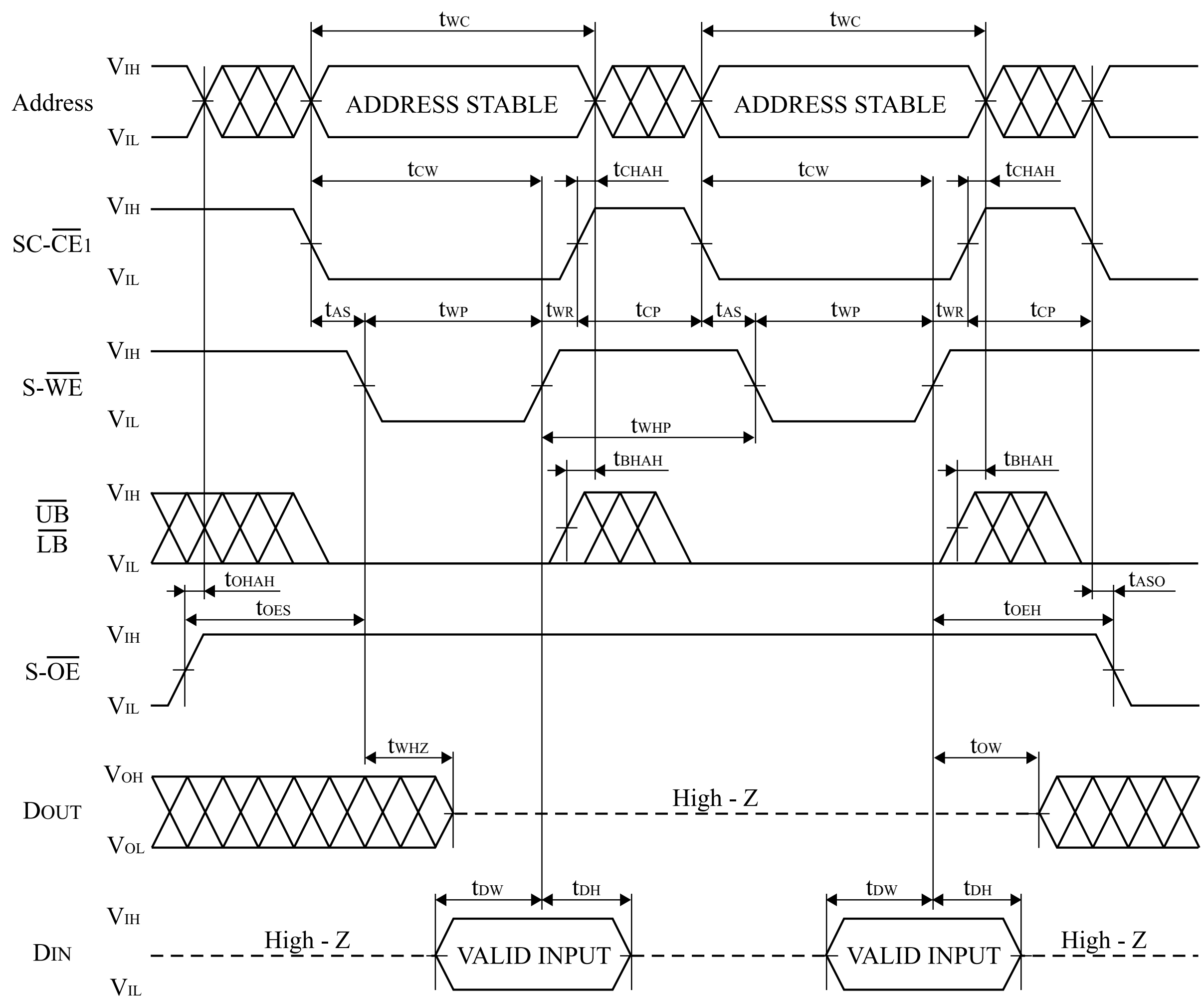
Write Cycle Timing Chart 1 (SC-$\overline{CE}_1$ Controlled))



Notes:

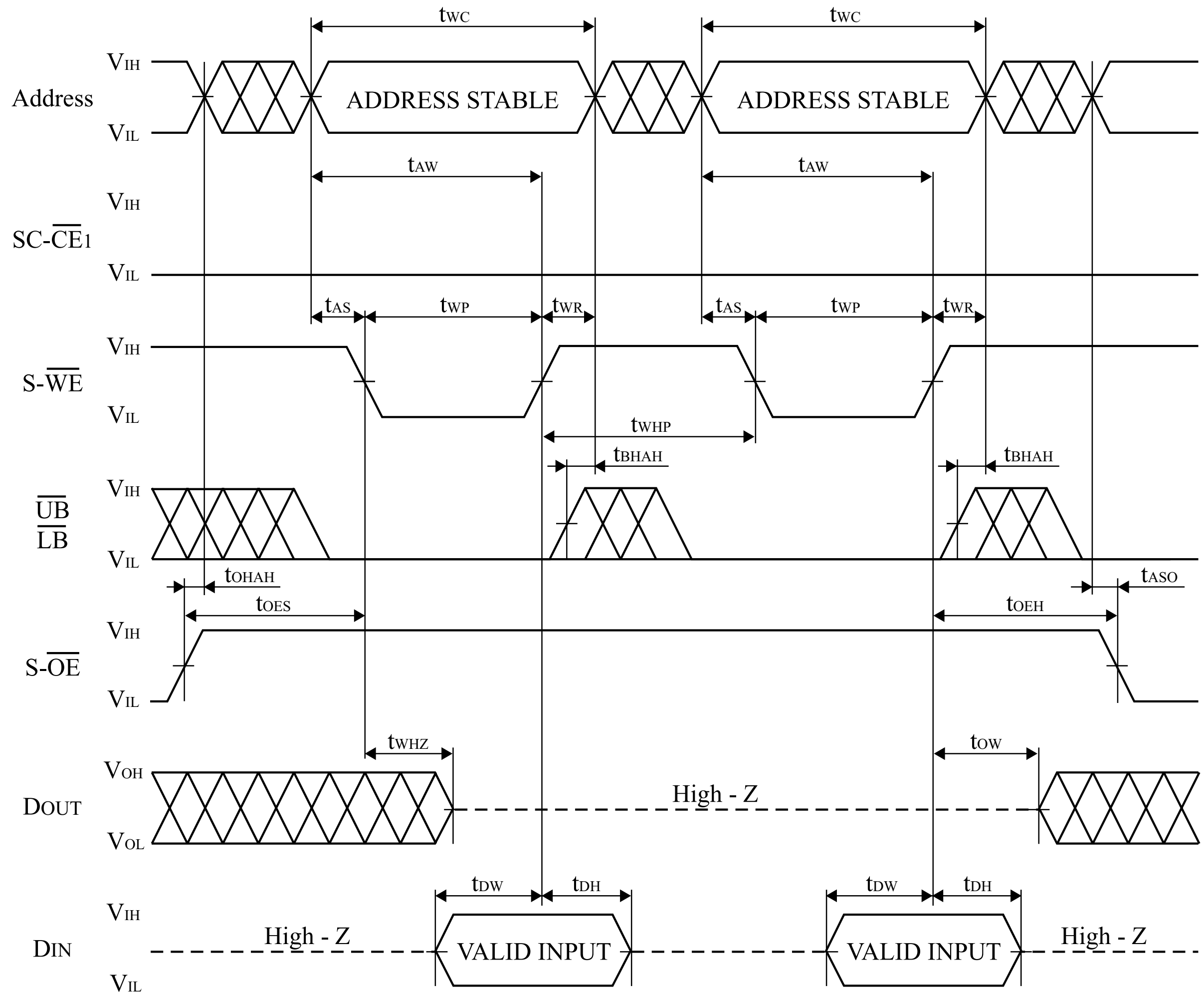
1. During address transition, at least one of S-$\overline{CE}_1$, S-$\overline{WE}$ or $\overline{LB}$, $\overline{UB}$ pins should be inactivated.
2. Do not input data to the DQ pins while they are in the output state.
3. In write cycle, CE 2 and S-$\overline{OE}$ should be fixed to high level.
4. Write operation is done during the overlap time of a low level SC-$\overline{CE}_1$, S-$\overline{WE}$, $\overline{LB}$ and/or $\overline{UB}$.

Write Cycle Timing Chart 2 (S-$\overline{WE}$ Controlled))



Notes:
1. During address transition, at least one of SC-$\overline{CE}_1$, S-$\overline{WE}$ or $\overline{LB}$, $\overline{UB}$ pins should be inactivated.
2. Do not input data to the DQ pins while they are in the output state.
3. In write cycle, CE_2 and S-$\overline{OE}$ should be fixed to high level.
4. Write operation is done during the overlap time of a low level SC-$\overline{CE}_1$, S-$\overline{WE}$, $\overline{LB}$ and/or $\overline{UB}$.

Write Cycle Timing Chart 3 (S-$\overline{WE}$ Controlled))



Notes:
1. During address transition, at least one of SC-$\overline{CE}$1, S-$\overline{WE}$ or $\overline{LB}$, $\overline{UB}$ pins should be inactivated.
2. Do not input data to the DQ pins while they are in the output state.
3. In write cycle, CE2 and S-$\overline{OE}$ should be fixed to high level.
4. Write operation is done during the overlap time of a low level SC-$\overline{CE}$1, S-$\overline{WE}$, $\overline{LB}$ and/or $\overline{UB}$.

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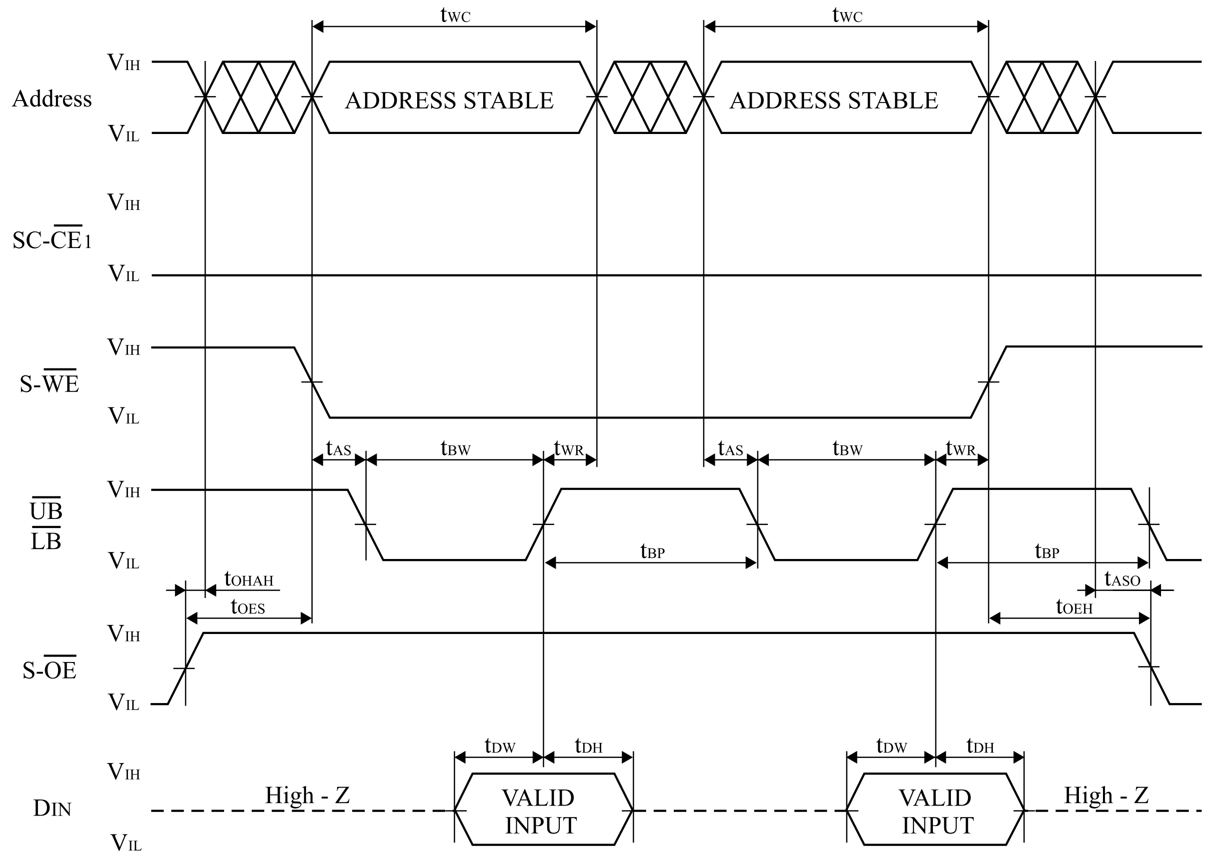
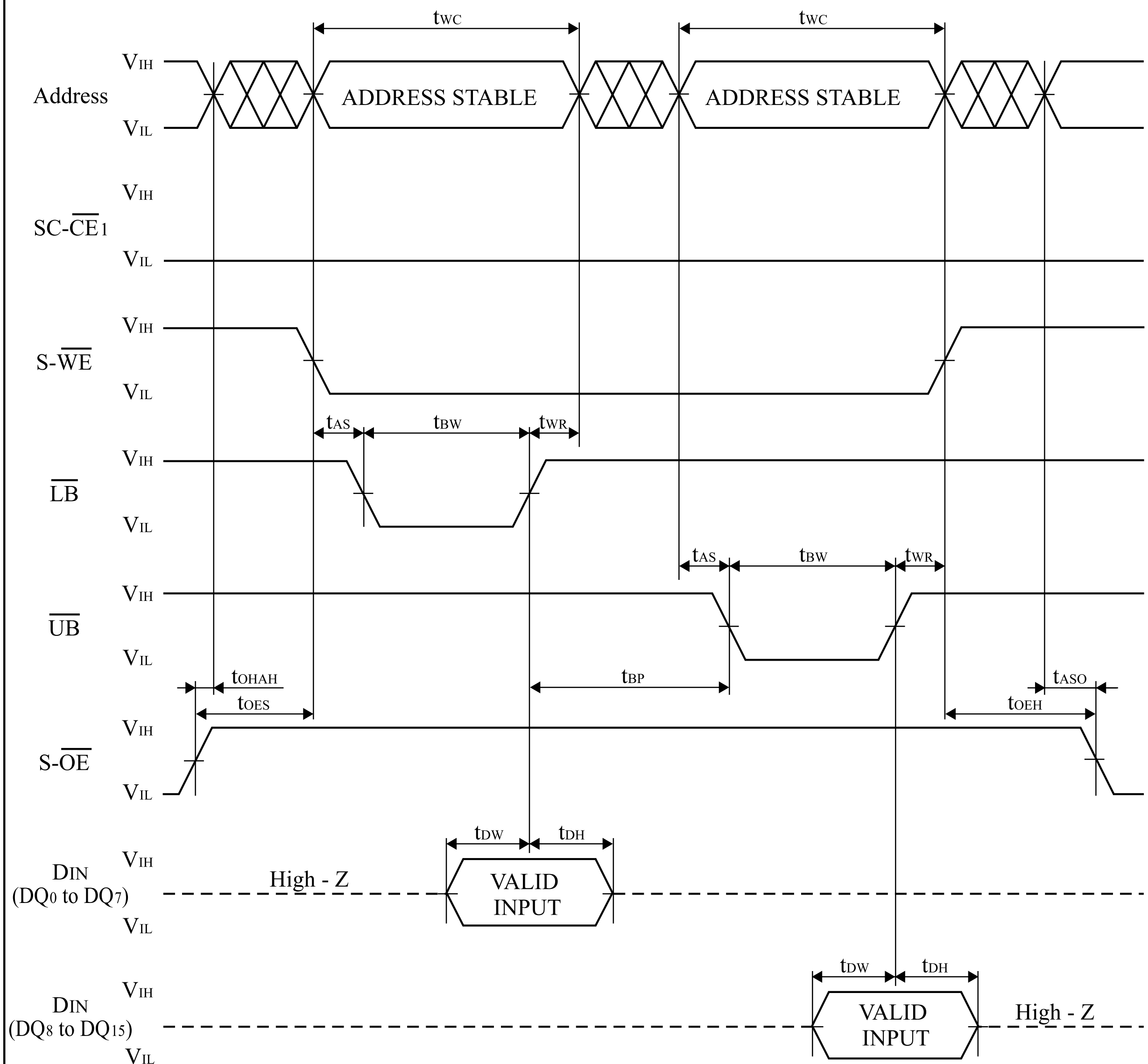
Write Cycle Timing Chart 4 ($\overline{LB}$ / $\overline{UB}$ Controlled))



Notes:

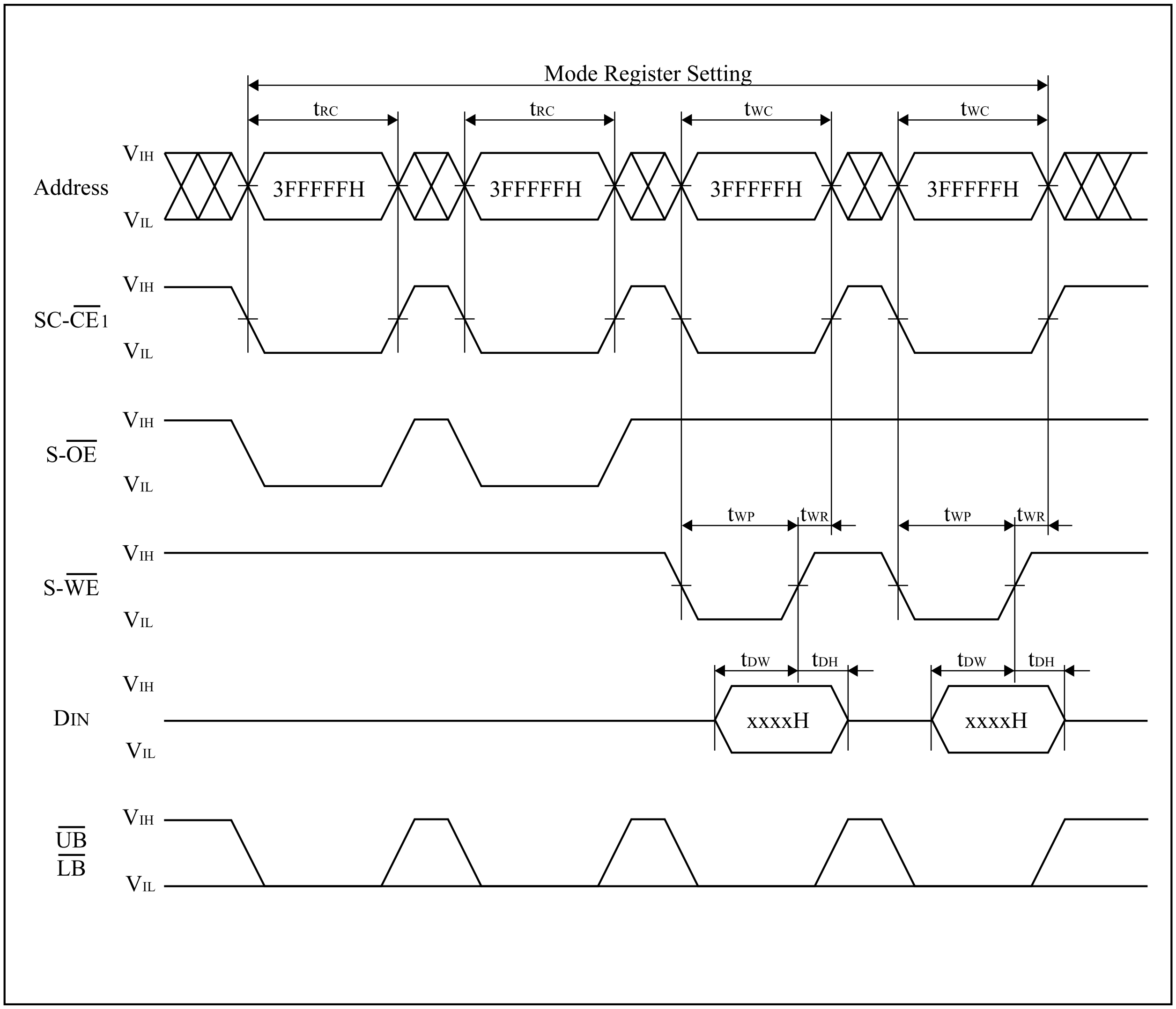
1. During address transition, at least one of SC-$\overline{CE}_1$, S-$\overline{WE}$ or $\overline{LB}$, $\overline{UB}$ pins should be inactivated.
2. Do not input data to the DQ pins while they are in the output state.
3. In write cycle, CE_2 and S-$\overline{OE}$ should be fixed to high level.
4. Write operation is done during the overlap time of a low level SC-$\overline{CE}_1$, S-$\overline{WE}$, $\overline{LB}$ and/or $\overline{UB}$.

Write Cycle Timing Chart 5 ($\overline{LB}$ / $\overline{UB}$ Independent Controlled))



Notes:
1. During address transition, at least one of SC-$\overline{CE}_1$, S-$\overline{WE}$ or $\overline{LB}$, $\overline{UB}$ pins should be inactivated.
2. Do not input data to the DQ pins while they are in the output state.
3. In write cycle, CE2 and S-$\overline{OE}$ should be fixed to high level.
4. Write operation is done during the overlap time of a low level SC-$\overline{CE}_1$, S-$\overline{WE}$, $\overline{LB}$ and/or $\overline{UB}$.

Mode Register Setting Timing Chart



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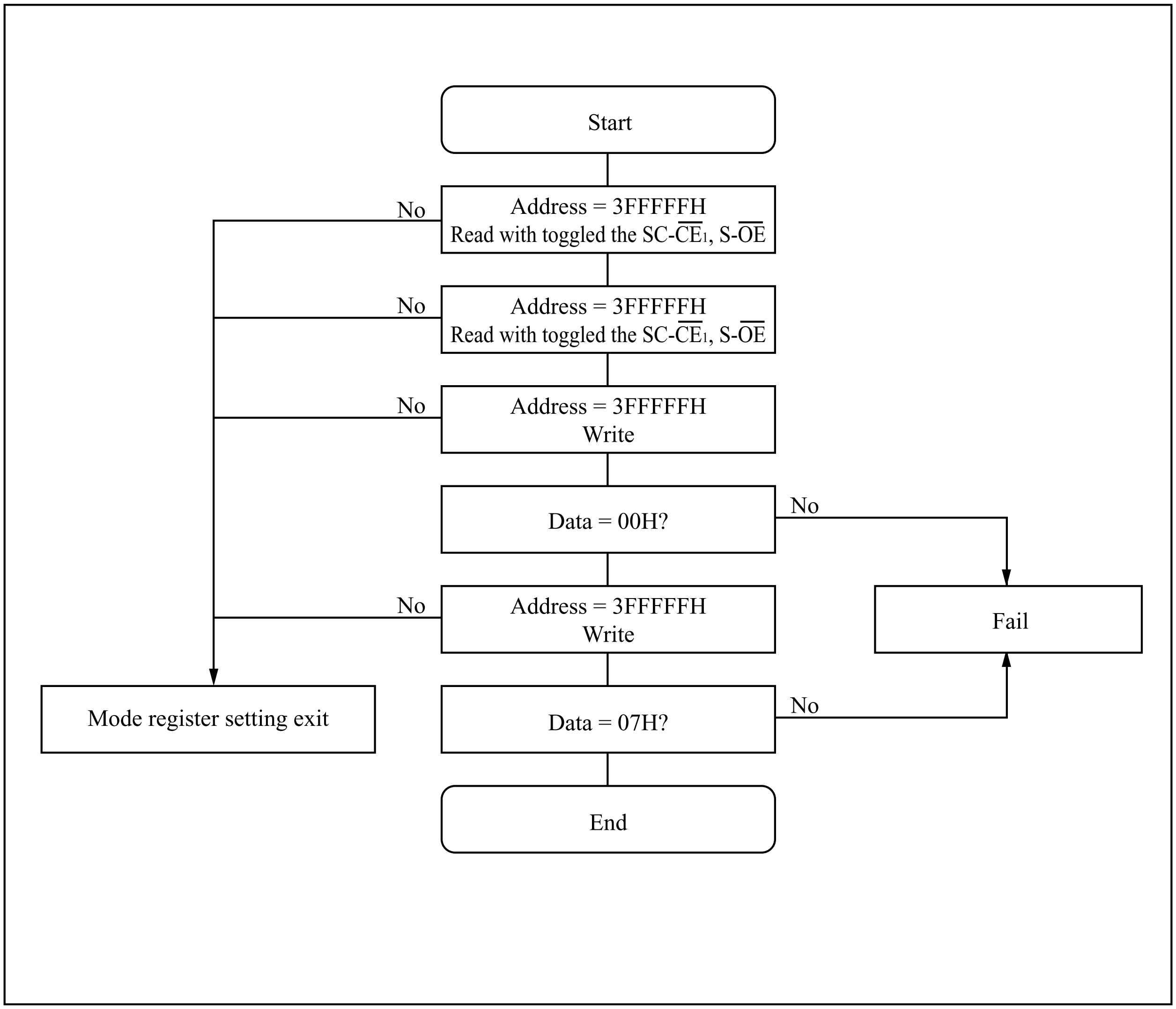
Mode Register Setting Flow Chart



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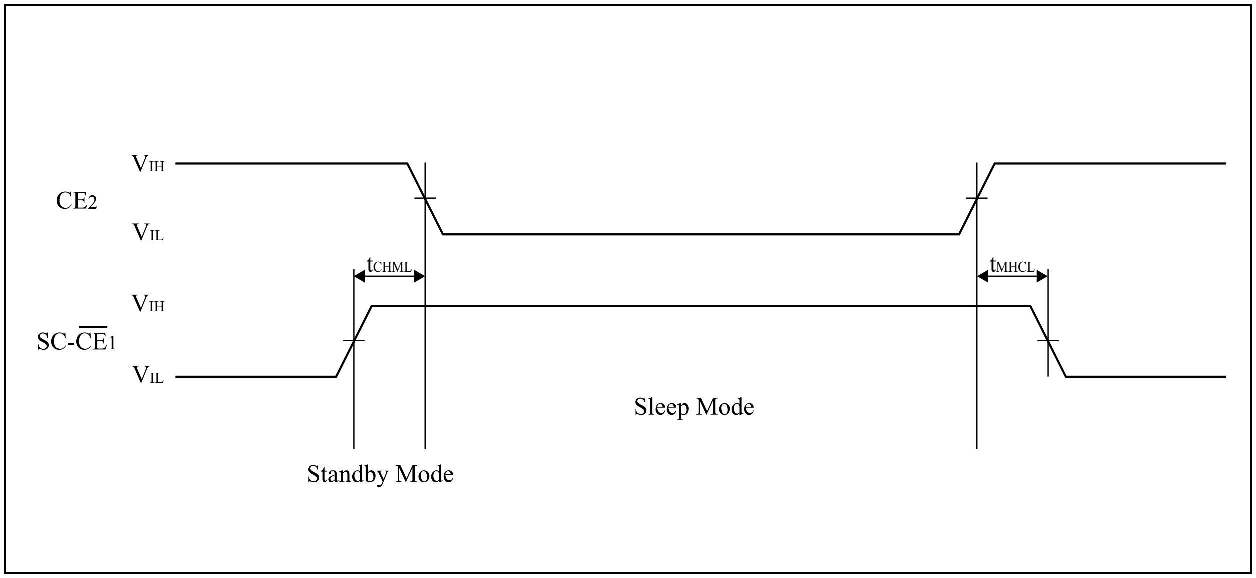
Sleep Mode Entry / Exit Timing Chart



9. SRAM

9.1 Truth Table

9.1.1 Bus Operation [1]

SRAM	Notes	S-$\overline{CE}_1$	CE_2	S-$\overline{OE}$	S-$\overline{WE}$	$\overline{LB}$	$\overline{UB}$	DQ_0 to DQ_{15}
Read		L	H	L	H	(2)		(2)
Output Disable				H	H	X	X	High - Z
				X	X	H	H	
Write				X	L	(2)		(2)
Standby		H	X	X	X	X	X	High - Z
		X	L			X	X	
		X	X			H	H	

Notes:

1. L = V_{IL}, H = V_{IH}, X = H or L, High-Z = High impedance. Refer to the DC Characteristics.
2. $\overline{LB}$, $\overline{UB}$ Control Mode

$\overline{LB}$	$\overline{UB}$	DQ_0 to DQ_7	DQ_8 to DQ_{15}
L	L	D_{OUT}/D_{IN}	D_{OUT}/D_{IN}
L	H	D_{OUT}/D_{IN}	High - Z
H	L	High - Z	D_{OUT}/D_{IN}

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9.2 DC Electrical Characteristics for SRAM

DC Electrical Characteristics

(T_A = -25°C to +85°C, V_{CC} = 2.7V to 3.1V)

Symbol	Parameter	Notes	Min.	Typ.	Max.	Unit	Test Conditions	
C_{IN}	Input Capacitance	1			8	pF	V_{IN} = 0V, f = 1MHz, T_A=25°C	
C_{IO}	I/O Capacitance	1			10	pF	$V_{I/O}$ = 0V, f = 1MHz, T_A=25°C	
I_{LI}	Input Leakage Current				±1	µA	$V_{IN} = V_{CC}$ or GND	
I_{LO}	Output Leakage Current				±1	µA	$V_{OUT} = V_{CC}$ or GND	
I_{SB}	V_{CC} Standby Current				15	µA	S-$\overline{CE}_1$, $CE_2 \geq V_{CC}$ - 0.2V or $CE_2 \leq$ 0.2V	
I_{CC1}	V_{CC} Operation Current				45	mA	S-$\overline{CE}_1 = V_{IL}$, $CE_2 = V_{IH}$, $V_{IN} = V_{IL}$ or V_{IH}	t_{CYCLE} = Min. $I_{I/O}$ = 0mA
I_{CC2}	V_{CC} Operation Current				8	mA	S-$\overline{CE}_1 \leq$ 0.2V, $CE_2 \geq V_{CC}$ -0.2V, $V_{IN} \geq V_{CC}$ -0.2V or $\leq$ 0.2V	t_{CYCLE} = 1µs $I_{I/O}$ = 0mA
V_{IL}	Input Low Voltage	1	-0.2		0.4	V		
V_{IH}	Input High Voltage	1	VCC -0.4		VCC +0.2	V		
V_{OL}	Output Low Voltage	1			0.2VCC	V	I_{OL} = 0.5mA	
V_{OH}	Output High Voltage	1	0.8V CC			V	I_{OH} = -0.5mA	

Notes:

1. Sampled, not 100% tested.

9.3 AC Electrical Characteristics for SRAM

9.3.1 AC Test Conditions

Input Pulse Level	0.4 to 2.4 V
Input Rise and Fall Time	5 ns
Input and Output Timing Ref. Level	1.5 V
Output Load	1TTL + C_L(30pF)(1)

Note:

1. Including scope and socket capacitance.

9.3.2 Read Cycle

(T_A = -25°C to +85°C, V_{CC} = 2.7V to 3.1V)

Symbol	Parameter	Notes	Min.	Max.	Unit
t_{RC}	Read Cycle Time		65		ns
t_{AA}	Address Access Time			65	ns
t_{ACE1}	Chip Enable Access Time (S-$\overline{CE}_1$)			65	ns
t_{ACE2}	Chip Enable Access Time (CE_2)			65	ns
t_{BE}	Byte Enable Access Time			65	ns
t_{OE}	Output Enable to Output Valid			40	ns
t_{OH}	Output Hold from Address Change		10		ns
t_{LZ1}	S-$\overline{CE}_1$ Low to Output Active	1	10		ns
t_{LZ2}	CE_2 High to Output Active	1	10		ns
t_{OLZ}	S-$\overline{OE}$ Low to Output Active	1	5		ns
t_{BLZ}	$\overline{UB}$ or $\overline{LB}$ Low to Output Active	1	10		ns
t_{HZ1}	S-$\overline{CE}_1$ High to Output in High-Z	1, 2	0	25	ns
t_{HZ2}	CE_2 Low to Output in High-Z	1, 2	0	25	ns
t_{OHZ}	S-$\overline{OE}$ High to Output in High-Z	1, 2	0	25	ns
t_{BHZ}	$\overline{UB}$ or $\overline{LB}$ High to Output in High-Z	1, 2	0	25	ns

Notes:

1. Active output to High-Z and High-Z to output active tests specified for a ±200mV transition from steady state levels into the test load.
2. The period from S-$\overline{CE}_1$ Rise, $\overline{UB}$ Rise, $\overline{LB}$ Rise S-$\overline{OE}$ Rise (CE_2: Falling) to output buffer off is logically 10ns.

9.3.3 Write Cycle

(T_A = -25°C to +85°C, V_{CC} = 2.7V to 3.1V)

Symbol	Parameter	Notes	Min.	Max.	Unit
t_{WC}	Write Cycle Time		65		ns
t_{CW}	Chip Enable to End of Write		60		ns
t_{AW}	Address Valid to End of Write		60		ns
t_{BW}	Byte Select Time		60		ns
t_{AS}	Address Setup Time		0		ns
t_{WP}	Write Pulse Width		50		ns
t_{WR}	Write Recovery Time		0		ns
t_{DW}	Input Data Setup Time		30		ns
t_{DH}	Input Data Hold Time		0		ns
t_{OW}	S-$\overline{WE}$ High to Output Active	1	5		ns
t_{WZ}	S-$\overline{WE}$ Low to Output in High-Z	1	0	25	ns

Note:

1. Active output to High-Z and High-Z to output active tests specified for a ±200mV transition from steady state levels into the test load.

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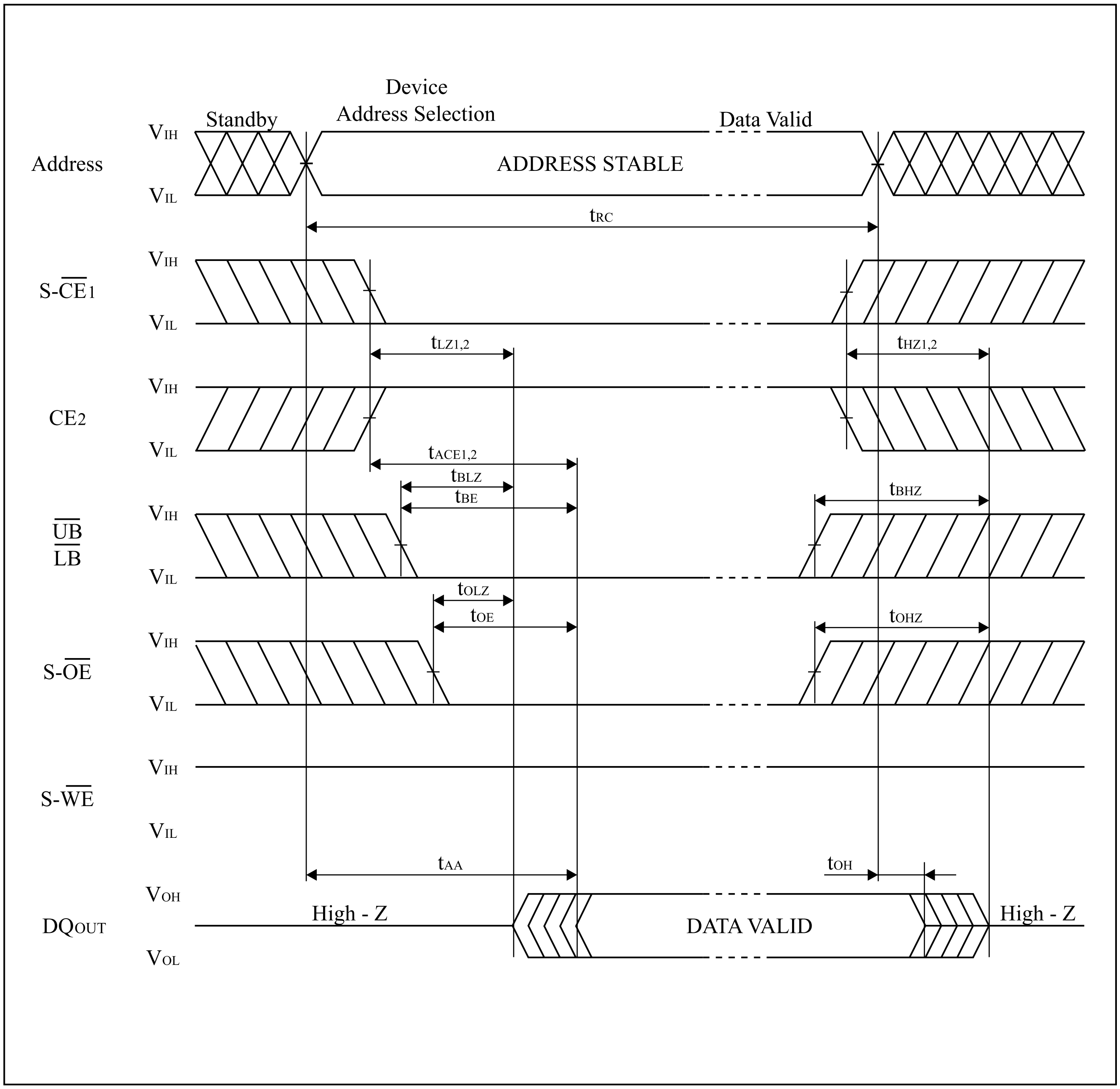
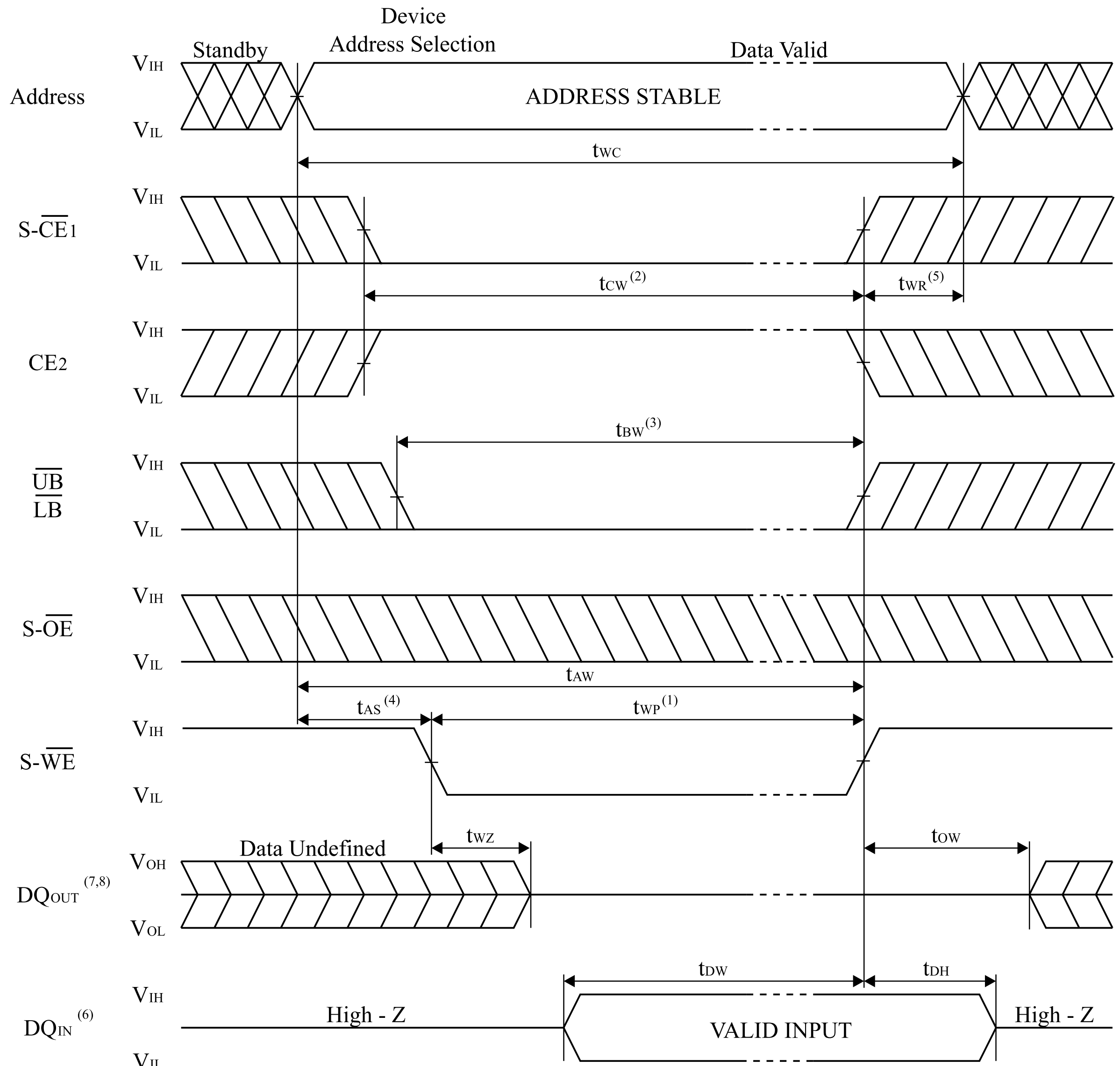
9.4 SRAM AC Characteristics Timing Chart

Read Cycle Timing Chart



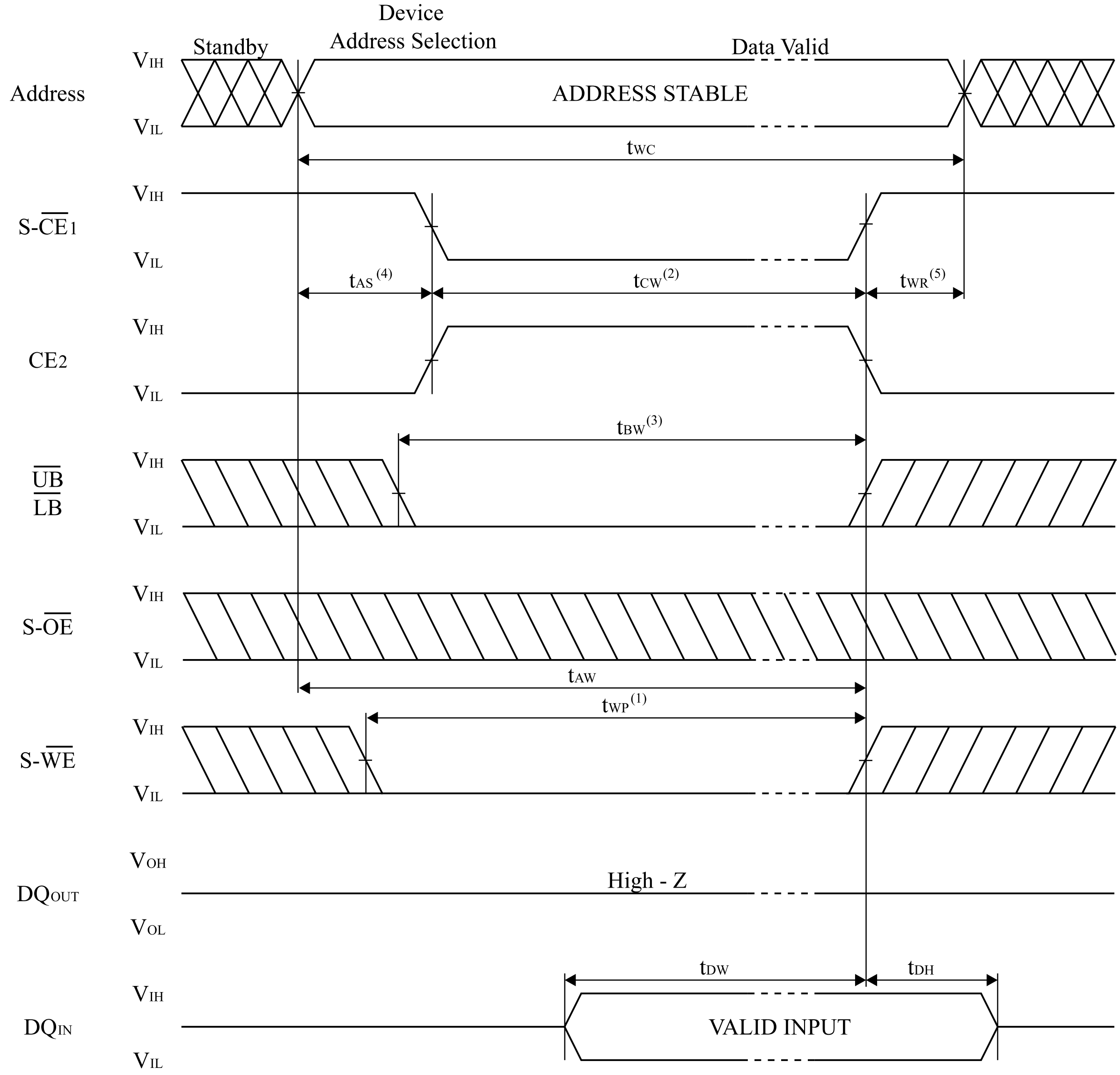
Write Cycle Timing Chart (S-$\overline{WE}$ Controlled)



Notes:

1. A write occurs during the overlap of a low S-$\overline{CE}_1$, a high CE_2 and a low S-$\overline{WE}$.
   A write begins at the latest transition among S-$\overline{CE}_1$ going low, CE_2 going high and S-$\overline{WE}$ going low.
   A write ends at the earliest transition among S-$\overline{CE}_1$ going high, CE_2 going low and S-$\overline{WE}$ going high.
   t_{WP} is measured from the beginning of write to the end of write.
2. t_{CW} is measured from the later of S-$\overline{CE}_1$ going low or CE_2 going high to the end of write.
3. t_{BW} is measured from the time of going low $\overline{UB}$ or low $\overline{LB}$ to the end of write.
4. t_{AS} is measured from the address valid to beginning of write.
5. t_{WR} is measured from the end of write to the address change. t_{WR} applies in case a write ends at S-$\overline{CE}_1$ going high, CE_2 going low or S-$\overline{WE}$ going high.
6. During this period DQ pins are in the output state, therefore the input signals of opposite phase to the outputs must not be applied.
7. If S-$\overline{CE}_1$ goes low or CE_2 goes high simultaneously with S-$\overline{WE}$ going low or after S-$\overline{WE}$ going low, the outputs remain in high impedance state.
8. If S-$\overline{CE}_1$ goes high or CE_2 goes low simultaneously with S-$\overline{WE}$ going high or before S-$\overline{WE}$ going high, the outputs remain in high impedance state.

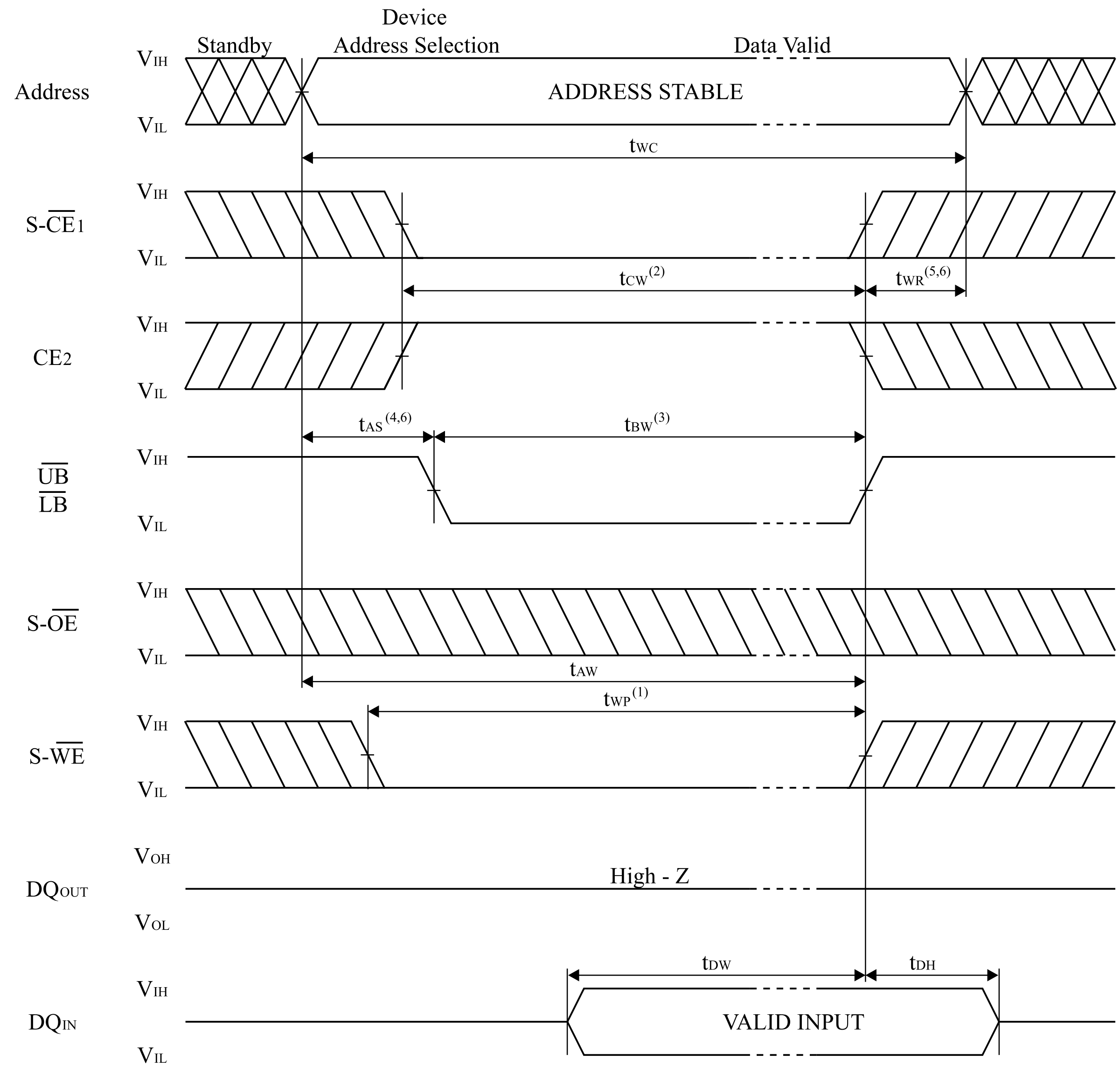
Write Cycle Timing Chart (S-$\overline{CE}_1$ Controlled)



Notes:

1. A write occurs during the overlap of a low S-$\overline{CE}_1$, a high CE_2 and a low S-$\overline{WE}$.
   A write begins at the latest transition among S-$\overline{CE}_1$ going low, CE_2 going high and S-$\overline{WE}$ going low.
   A write ends at the earliest transition among S-$\overline{CE}_1$ going high, CE_2 going low and S-$\overline{WE}$ going high.
   t_{WP} is measured from the beginning of write to the end of write.
2. t_{CW} is measured from the later of S-$\overline{CE}_1$ going low or CE_2 going high to the end of write.
3. t_{BW} is measured from the time of going low $\overline{UB}$ or low $\overline{LB}$ to the end of write.
4. t_{AS} is measured from the address valid to beginning of write.
5. t_{WR} is measured from the end of write to the address change. t_{WR} applies in case a write ends at S-$\overline{CE}_1$ going high, CE_2 going low or S-$\overline{WE}$ going high.

Write Cycle Timing Chart ($\overline{UB}$ / $\overline{LB}$ Controlled)



Notes:

1. A write occurs during the overlap of a low S-$\overline{CE}_1$, a high CE_2 and a low S-$\overline{WE}$.
   A write begins at the latest transition among S-$\overline{CE}_1$ going low, CE_2 going high and S-$\overline{WE}$ going low.
   A write ends at the earliest transition among S-$\overline{CE}_1$ going high, CE_2 going low and S-$\overline{WE}$ going high.
   t_{WP} is measured from the beginning of write to the end of write.
2. t_{CW} is measured from the later of S-$\overline{CE}_1$ going low or CE_2 going high to the end of write.
3. t_{BW} is measured from the time of going low $\overline{UB}$ or low $\overline{LB}$ to the end of write.
4. t_{AS} is measured from the address valid to beginning of write.
5. t_{WR} is measured from the end of write to the address change. t_{WR} applies in case a write ends at S-$\overline{CE}_1$ going high, CE_2 going low or S-$\overline{WE}$ going high.
6. $\overline{UB}$ and $\overline{LB}$ need to make the time of start of a cycle, and an end "high" level for reservation of t_{AS} and t_{WR}.

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9.5 Data Retention Characteristics for SRAM

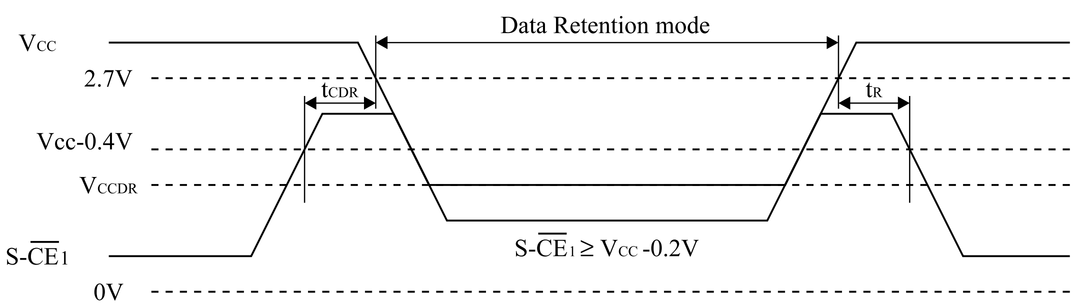
(T_A = -25°C to +85°C)

Symbol	Parameter	Note	Min.	Typ.(1)	Max.	Unit	Conditions
V_{CCDR}	Data Retention Supply voltage	2	1.5		3.1	V	$CE_2 \leq 0.2V$ or $S\text{-}\overline{CE}_1 \geq V_{CC}$ - 0.2V
I_{CCDR}	Data Retention Supply current	2		2	15	μA	V_{CC} = 3.0V, $CE_2 \leq 0.2V$ or $S\text{-}\overline{CE}_1 \geq V_{CC}$ - 0.2V
t_{CDR}	Chip enable setup time		0			ns	
t_R	Chip enable hold time		t_{RC}			ns	

Notes:

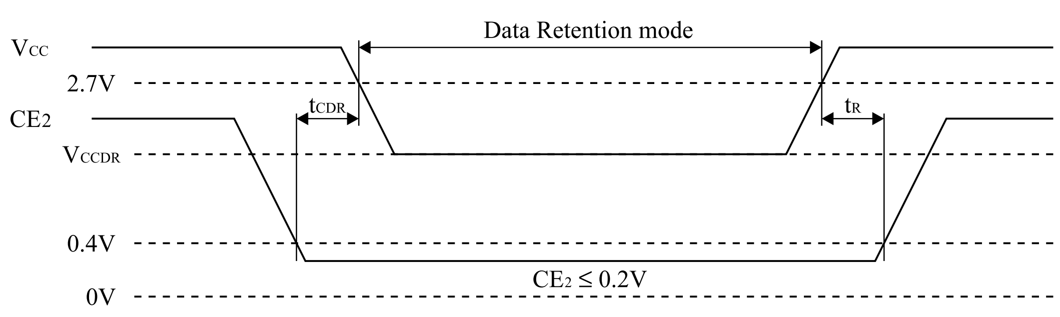
1. Reference value at T_A = 25°C, V_{CC} = 3.0V.
2. $S\text{-}\overline{CE}_1$ Š V_{CC} - 0.2V, CE_2 Š V_{CC} - 0.2V ($S\text{-}\overline{CE}_1$ controlled) or CE_2 £ 0.2V (CE_2 controlled).

Data Retention Timing Chart ($S\text{-}\overline{CE}_1$ Controlled) (1)



Note:
1. To control the data retention mode at $S\text{-}\overline{CE}_1$, fix the input level of CE_2 between "V_{CCDR} and V_{CCDR}-0.2V" or "0V and 0.2V" during the data retention mode.

Data Retention Timing Chart (CE_2 Controlled)



10. Notes

This product is a stacked CSP package that a 64M (x16) bit Flash Memory, a 64M (x16) bit Flash Memory, a 64M (x16) bit Smartcombo RAM and a 8M (x16) bit SRAM are assembled into.

-Supply Power

Maximum difference (between F/SC-V_{CC} and S-V_{CC}) of the voltage is less than 0.3V.

-Power Supply and Chip Enable of Flash Memory, Smartcombo RAM and SRAM

Two or more chips among Flash memory (F_1, F_2), Smartcombo RAM and SRAM should not be active simultaneously. If the two memories are active together, possibly they may not operate normally by interference noises or data collision on DQ bus.

Both F/SC-V_{CC} and S-V_{CC} are needed to be applied by the recommended supply voltage at the same time except Smartcombo RAM sleep mode and/or SRAM data retention mode.

-Power Up Sequence

When turning on Flash memory power supply, keep $\overline{RST}$ low. After F/SC-V_{CC} reaches over 2.7V, keep $\overline{RST}$ low for more than 100 nsec.

-Device Decoupling

This is a 4 chips stacked CSP package. When one of the chips is active, others are in standby mode. Therefor, these power supplies should be designed very carefully.

Exclusive power supply pins for each Memory and GND pin need careful decoupling of devices. Especially, note Flash Memory, Smartcombo RAM and SRAM peak current caused by transition of control signals.

When one of the Flash Memory is in busy mode, (page buffer) program, block erase and full chip erase command should not be inputted to the other (F_1-CE, F_2-CE, SC-CE_1, S-CE_1, CE_2).

11. Flash Memory Data Protection

Noises having a level exceeding the limit specified in the specification may be generated under specific operating conditions on some systems. Such noises, when induced onto F-$\overline{WE}$ signal or power supply, may be interpreted as false commands and causes undesired memory updating. To protect the data stored in the flash memory against unwanted writing, systems operating with the flash memory should have the following write protect designs, as appropriate:

■ The below describes data protection method.

1. Protection of data in each block
   - Any locked block by setting its block lock bit is protected against the data alternation. When $\overline{WP}$ is low, any locked-down block by setting its block lock-down bit is protected from lock status changes.
     By using this function, areas can be defined, for example, program area (locked blocks), and data area (unlocked blocks).
   - For detailed block locking scheme, see Section 6.2, 7.2 Command Definitions for Flash Memory.

2. Protection of data with V_{PP} control
   - When the level of V_{PP} is lower than V_{PPLK} (V_{PP} lockout voltage), write functions to all blocks are disabled. All blocks are locked and the data in the blocks are completely protected.

3. Protection of data with $\overline{RST}$
   - Especially during power transitions such as power-up and power-down, the flash memory enters reset mode by bringing $\overline{RST}$ to low, which inhibits write operation to all blocks.
   - For detailed description on $\overline{RST}$ control, see Section 6.6.6, 7.6.6 AC Electrical Characteristics for Flash Memory, Reset Operations.

■ Protection against noises on F-$\overline{WE}$ signal

To prevent the recognition of false commands as write commands, system designer should consider the method for reducing noises on F-$\overline{WE}$ signal.

12. Design Considerations

1. Power Supply Decoupling

To avoid a bad effect to the system by flash memory, Smartcombo RAM and SRAM power switching characteristics, each device should have a 0.1µF ceramic capacitor connected between F/SC-V_{CC} and GND, between V_{PP} and GND and between S-V_{CC} and GND.
Low inductance capacitors should be placed as close as possible to package leads.

2. V_{PP} Trace on Printed Circuit Boards

Updating the memory contents of flash memories that reside in the target system requires that the printed circuit board designer pay attention to the V_{PP} Power Supply trace. Use similar trace widths and layout considerations given to the F/SC-V_{CC} power bus.

3. The Inhibition of Overwrite Operation

Please do not execute reprograming “0” for the bit which has already been programed “0”. Overwrite operation may generate unerasable bit.

In case of reprograming “0” to the data which has been programed “1”.
•Program “0” for the bit in which you want to change data from “1” to “0”.
•Program “1” for the bit which has already been programed “0”.

For example, changing data from “1011110110111101” to “1010110110111100”
requires “1110111111111110” programing.

4. Power Supply

Block erase, full chip erase, (page buffer) program with an invalid V_{PP} (See Chapter 6.5, 7.5 DC Electrical Characteristics for Flash Memory) produce spurious results and should not be attempted.
Device operations at invalid F/SC-V_{CC} voltage (See Chapter 6.5, 7.5 DC Electrical Characteristics for Flash Memory) produce spurious results and should not be attempted.

13. Related Document Information[1]

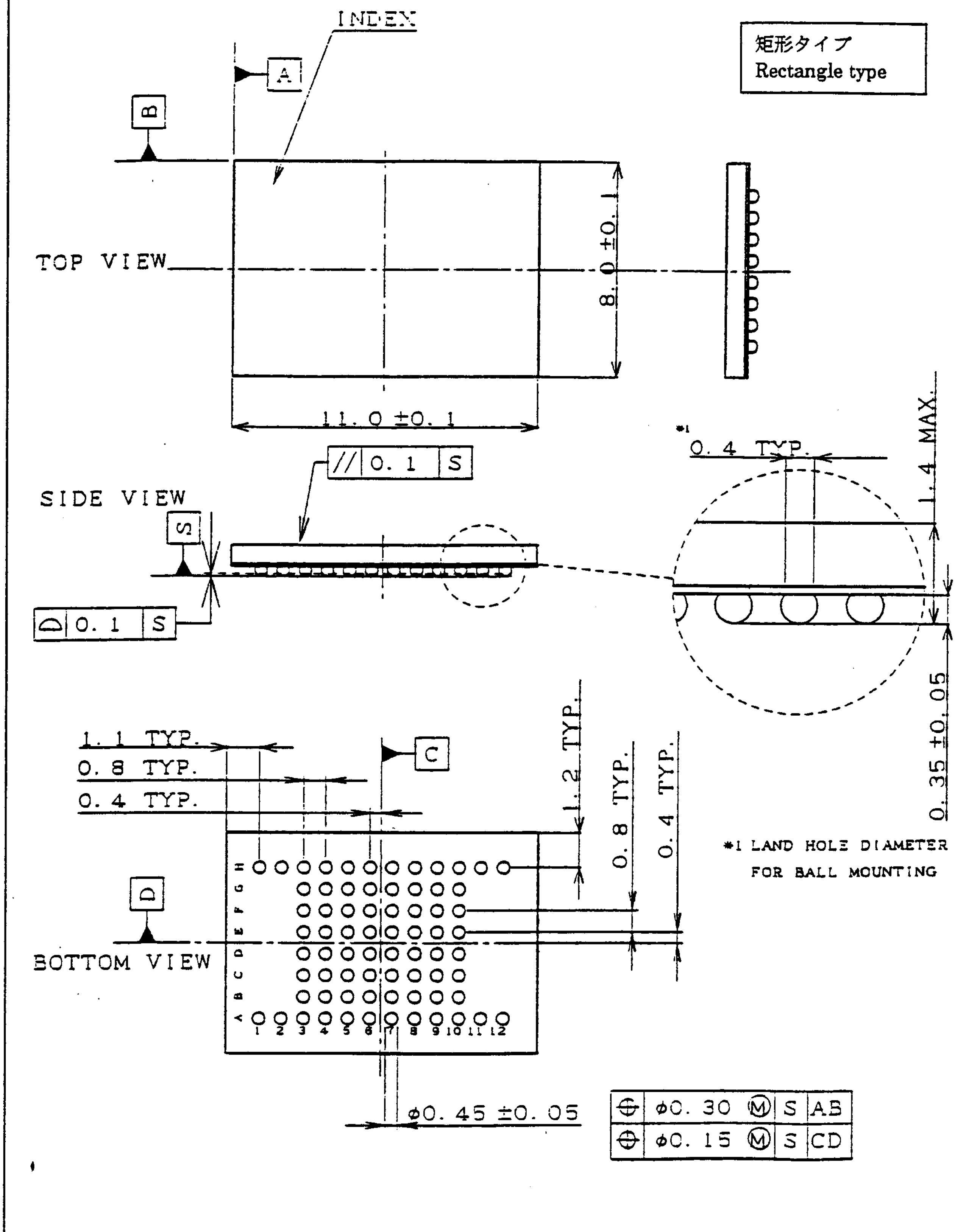
Document No.	Document Name
FUM00701	LH28F320BF, LH28F640BF, LH28F128BF Series Appendix

Note:
1. International customers should contact their local SHARP or distribution sales offices.

SHARP

REFERENCE

PRELIMINARY



名称 NAME	FBGA072/064-P-0811(LCSP072/064-P-0811)			備考 NOTE
DRAWING NO.	AA2149	単位 UNIT	mm	

20010910

SHARP

LRS1B07 Flash MEMORY ERRATA

1. AC Characteristics

PROBLEM

The table below summarizes the AC characteristics.

AC Characteristics - Write Operations

V_{CC}=2.7V-3.1V

Page	Symbol	Parameter		Min.	Max.	Unit
22, 43	t_{AVAV}	Write Cycle Time		75		ns
22, 43	t_{WLWH} (t_{ELEH})	F-$\overline{WE}$ (F-$\overline{CE}$) Pulse Width	t_{AVAV}=75ns	50		ns
22, 43	t_{AVWH} (t_{AVEH})	Address Setup to F-$\overline{WE}$ (F-$\overline{CE}$) Going High		50		ns
22, 43	t_{WHWL} (t_{EHEL})	F-$\overline{WE}$ (F-$\overline{CE}$) Pulse Width High		25		ns

WORKAROUND

System designers should consider these specifications.

STATUS

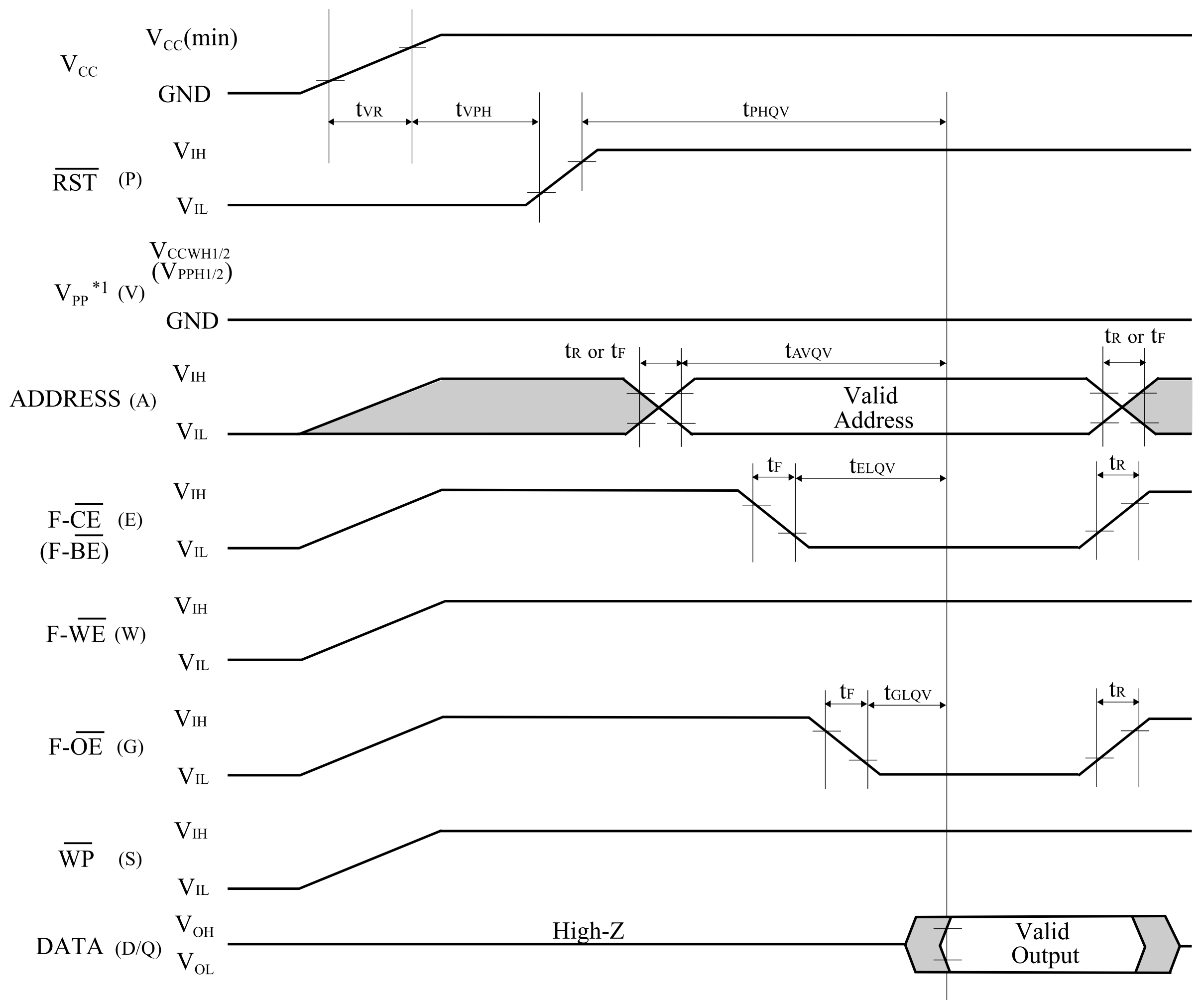
This is intended to be fixed in future devices.

SHARP

A-1 RECOMMENDED OPERATING CONDITIONS

A-1.1 At Device Power-Up

AC timing illustrated in Figure A-1 is recommended for the supply voltages and the control signals at device power-up. If the timing in the figure is ignored, the device may not operate correctly.



*1 To prevent the unwanted writes, system designers should consider the design, which applies V_{PP} to 0V during read operations and $V_{CCWH1/2}$ ($V_{PPH1/2}$) during write or erase operations. See the application note AP-007-SW-E for details.

Figure A-1. AC Timing at Device Power-Up

For the AC specifications t_{VR}, t_R, t_F in the figure, refer to the next page. See the "AC Electrical Characteristics for Flash Memory" described in specifications for the supply voltage range, the operating temperature and the AC specifications not shown in the next page.

SHARP

A-1.1.1 Rise and Fall Time

Symbol	Parameter	Notes	Min.	Max.	Unit
t_{VR}	V_{CC} Rise Time	1	0.5	30000	µs/V
t_R	Input Signal Rise Time	1, 2		1	µs/V
t_F	Input Signal Fall Time	1, 2		1	µs/V

NOTES:
1. Sampled, not 100% tested.
2. This specification is applied for not only the device power-up but also the normal operations.

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A-1.2 Glitch Noises

Do not input the glitch noises which are below V_{IH} (Min.) or above V_{IL} (Max.) on address, data, reset, and control signals, as shown in Figure A-2 (b). The acceptable glitch noises are illustrated in Figure A-2 (a).

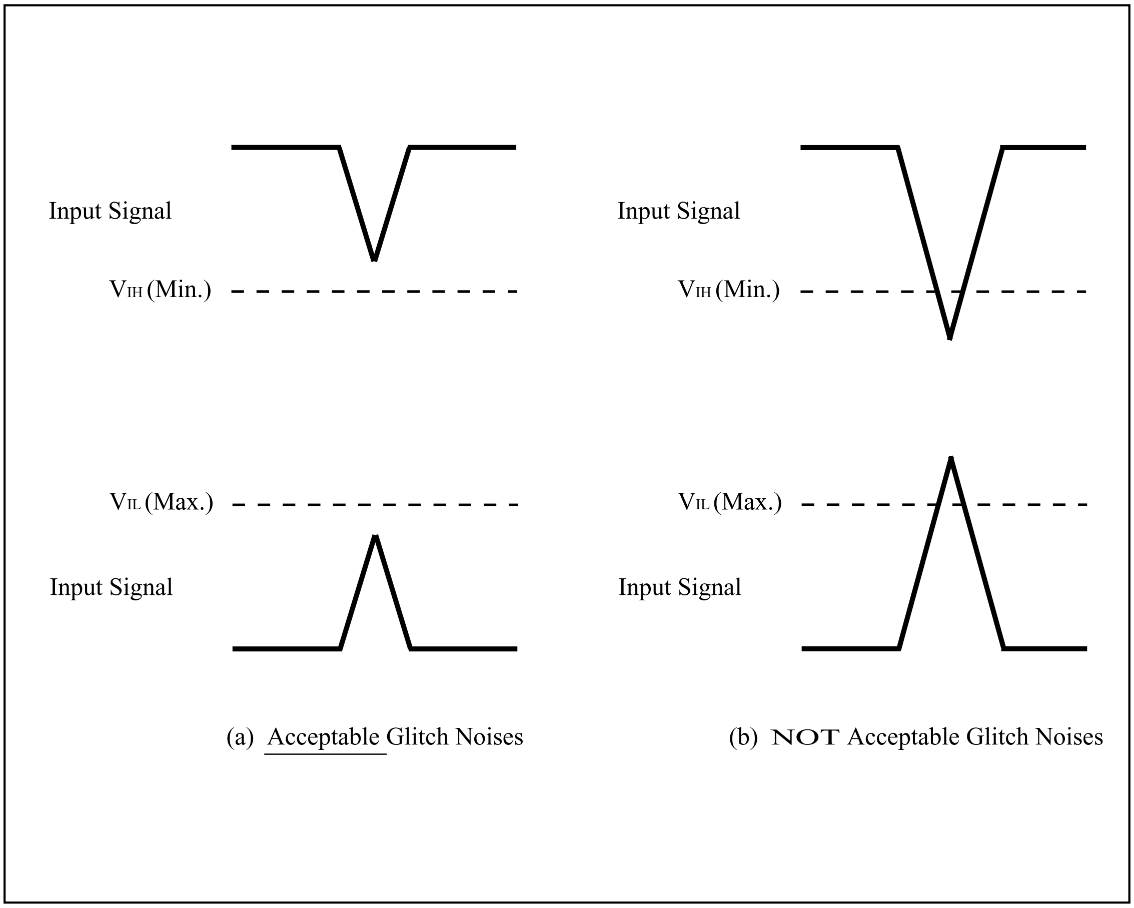


Figure A-2. Waveform for Glitch Noises

See the "DC Electrical Characteristics" described in specifications for V_{IH} (Min.) and V_{IL} (Max.).

SHARP

A-2 RELATED DOCUMENT INFORMATION[1]

Document No.	Document Name
AP-001-SD-E	Flash Memory Family Software Drivers
AP-006-PT-E	Data Protection Method of SHARP Flash Memory
AP-007-SW-E	RP#, V_{PP} Electric Potential Switching Circuit

NOTE:
1. International customers should contact their local SHARP or distribution sales office.

SHARP

B-1 POWER UP SEQUENCE OF Smartcombo RAM

When turning on Smartcombo RAM power supply, the following sequence is needed.

B-1.1 Sequence of Smartcombo RAM Power Supply

(1) Supply power.

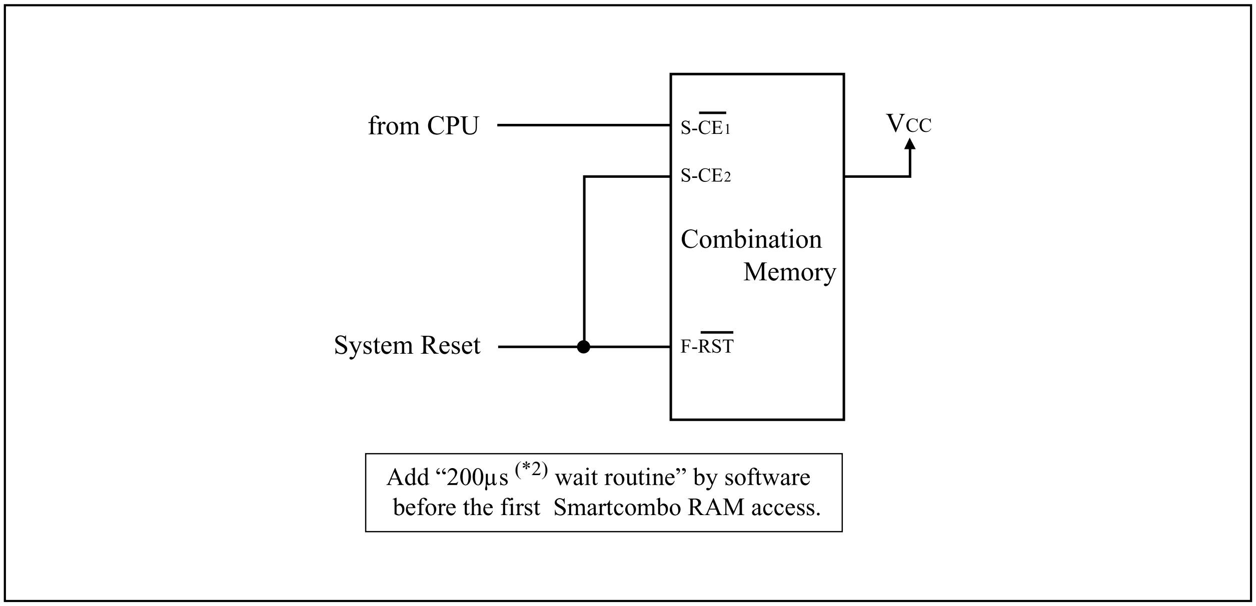
(2) Keep S-CE_2 low longer than or equal to 50µs. (See NOTES *1)

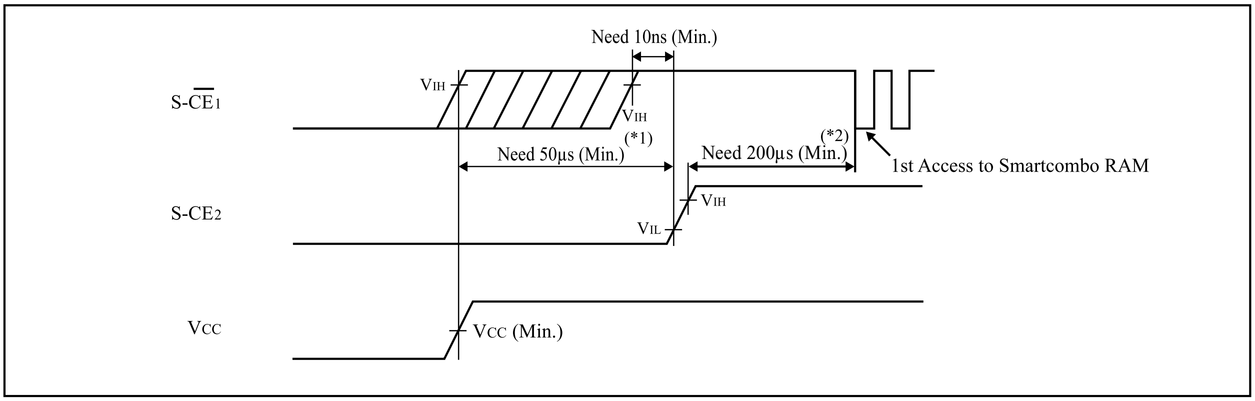
(3) Keep S-$\overline{CE}_1$ and S-CE_2 high longer than or equal to 200µs. (See NOTES *2)

(4) End of Initialization.

By executing above (1) to (4), the initialization of chip inside and the power occurred inside become stable.

<Example of the actual connection>





NOTES:

*1) Connect System Reset signal to S-CE_2 and hold S-CE_2 low longer than or equal to 50µs.

*2) By adding "200µs Wait Routine" (S-$\overline{CE}_1$ and S-CE_2 high) in the software, delay the first access to Smartcombo RAM longer than or equal to 200µs.

When giving compatibility with the other type of Smartcombo RAM, 200µs must be changed to 300µs.

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