1.2A Synchronous Step-down Converter with Integrated Inductor

Features

- Integrated inductor, Power MOSFETs and controller
- 2.5V to 5.5V Input Voltage Range
- 1200mA Load Current
- Efficiency: Up to 92% (VIN=5V, VOUT=3.3V, Iout=400mA)
- 1.5MHz Constant Switching Frequency
- 100% Duty Cycle in Dropout Operation
- Current Mode Control
- Thermal Shutdown
- Current Limit Protection
- Short Protection
- Support UVLO, Soft Start
- Small QFN-12 Package
- EU RoHS Compliant, Pb Free

Product Description

The LPM3810 is a 1.2A synchronous step-down DC/DC converter which integrates an inductor and a control IC adopting current mode control in one tiny package. External Schottky diodes are not required.

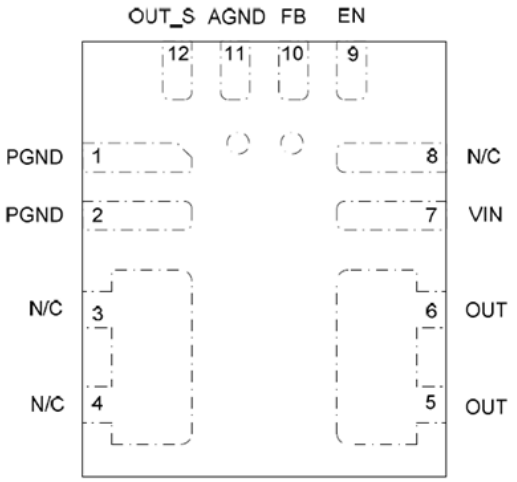
LPM3810 can supply 1.2A of load current from 2.5V to 5.5V supply voltage. The Output voltage is externally set by feedback resistor. The switching frequency is set at 1.5MHz, allowing the use of small surface mount capacitors. It can run 100% duty cycle for low dropout application.

The LPM3810 comes in a small surface mount QFN-12 (2.5mmx3.0mmx1.0mm) package.

Applications

- Cellular and Smart Phones
- Microprocessors and DSP Core Supplies
- Set Top Box
- USB Dongle
- Digital Still and Video Cameras
- Portable Navigation Device

Pin Configuration



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Typical Application Circuit

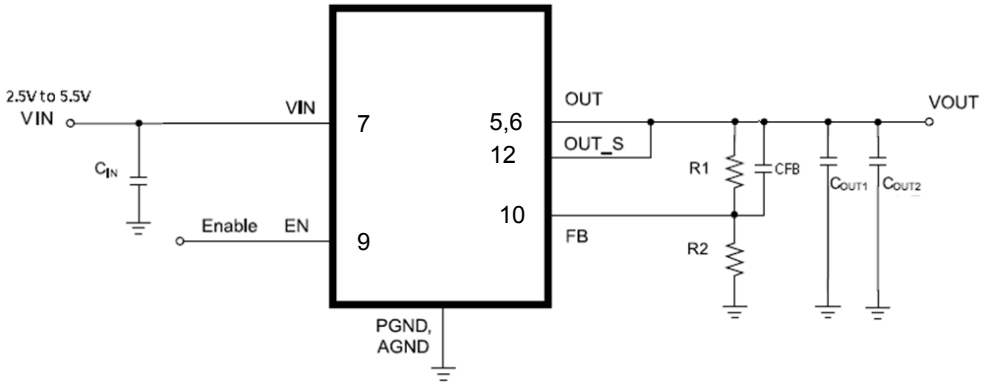

Figure 1 Typical Application Circuit

Vout	R1	R2	C_{FB}	C_{IN}	C_{OUT1}, C_{OUT2}
3.3V	300K	68K	Option	10uF	10uF
1.8V	100K	50K	Option	10uF	10uF
1.2V	50K	50K	Option	10uF	10uF

Table 1 Recommended Component Selection

Pin Function Description:

Pin NO.	Pin Name	Pin Description
1,2	PGND	Power Ground.
3,4	N/C	Internal SW Pad. Connected with copper pad for thermal sink.
5,6	OUT	Output Voltage Power Rail. Connect load to OUT. Output capacitor is needed.
7	VIN	Power Supply Input. Drive 2.5V to 5.5V voltage to this pin to power on this chip. Connecting a 10uF ceramic bypass capacitor between VIN and GND to eliminate noise.
8	N/C	
9	EN	On/Off Control Input. Pull EN above 1.5V to turn the device on.
10	FB	Feedback Input. Connect FB to the center point of the external resistor divider. The feedback threshold voltage is 0.6V.
11	AGND	Analogy Ground for Internal Control Circuit.
12	OUT_S	Output Voltage Sense.

Product Classification

Ordering Information
LPM3810-①:

DESIGNATOR	ITEM	SYMBOL	DESCRICPTION
①	Packages	V12	QFN-12 QFN-12 (2.5mmx3.0mmx1.0mm) (3,000pcs/Reel)

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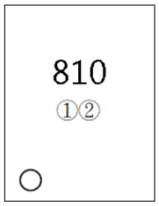
Marking Rule:



MARK	PRODUCT SERIESIES
810 **	LPM3810**

①②represents production lot number: 0 to 9, A to Z repeated.

Absolute Maximum Ratings: **(Note 1, 2)**

(V_{IN}=V_{EN}=5V, L = 2.2uH, T_A = 25°C, unless otherwise noted.)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
V_{IN}	Supply Voltage	-		6		V
	All Other Pins	-	-0.3	-	+6	V
T_J	Junction Temperature	-	-	150	-	°C
T_L	Lead Temperature		-	260	-	°C
T_S	Storage Temperature	-	-65	-	150	°C
	ESD Classification (HBM)	-	-	Class 2	-	V

Recommended Operating Conditions: **(Note 2)**

(V_{IN}=V_{EN}=5V, L = 2.2uH, T_A = 25°C, unless otherwise noted.)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
V_{IN}	Input Supply Voltage	-	2.5	-	5.5	V
V_{OUT}	Output Voltage	-	0.6	-	5.5	V
T_A	Ambient Temperature	-	-40	-	85	°C

Note 1: Stresses exceed those ratings may damage the device.
Note 2: If out of its operation conditions, the device is not guaranteed to function.

Electrical Characteristic: **(Note 2)**

(V_{IN}=V_{EN}=5V, L = 2.2uH, T_A = 25°C, unless otherwise noted.)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Input Voltage Range	V_{IN}	-	2.5	-	5.5	V
Quiescent Current	I_Q	Switching Without I_{Load} 5V→3.3V	-	3.2	-	Ma
Shutdown Current	I_S	V_{EN}=0V, V_{IN} =5.5V	-	0.1	1	uA
IN Under Voltage Lockout Threshold	UVLO	Vin Falling Edge	2.0	2.2	2.5	V
Reference Voltage	V_{REF}	-	0.582	0.6	0.618	V
Output Voltage Accuracy	$\Delta V_{out}/V_{out}$	I_{OUT} = 0~1.2A	-3		3	%
FB Input Current	I_{FB}	V_{FB} = 0.65V	-50		50	nA
PFET On Resistance (*)	$R_{(ON)\_P}$	I_{SW} = 200mA		0.28		Ω
NFET On Resistance (*)	$R_{(ON)\_N}$	I_{SW} = -200mA		0.25		Ω

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SW Leakage Current			-1		1	uA
PFET Current Limit		Duty Cycle = 100%, Current Pulse Width < 1ms	1.2	2.2		A
Oscillator Frequency	F_{SW}	V_{IN} = 3.6V, I_{OUT} = 200mA	1.2	1.5	1.8	MHz

Electrical Characteristic: (Cont.)

(VIN = 3.6V, VOUT=1.8V, TA = 25℃, unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Maximum Duty Cycle	V_{IN}	-	-	100	-	%
Minimum On-Time (*)		T_{ON}	-	80	-	nS
Thermal Shutdown Trip Threshold (*)			-	145	-	°C
EN High-Level Input Voltage		–40°C ≤ T_A ≤ +85°C	1.5			V
EN Low-Level Input Voltage					0.4	V
EN Input Current		V_{EN} = 0V to 5.5V	-1	-	1	uA
Inductance		Test Frequency =1MHz	-	1.0	-	uH

*: Guaranteed by design

Functional Block Diagram:

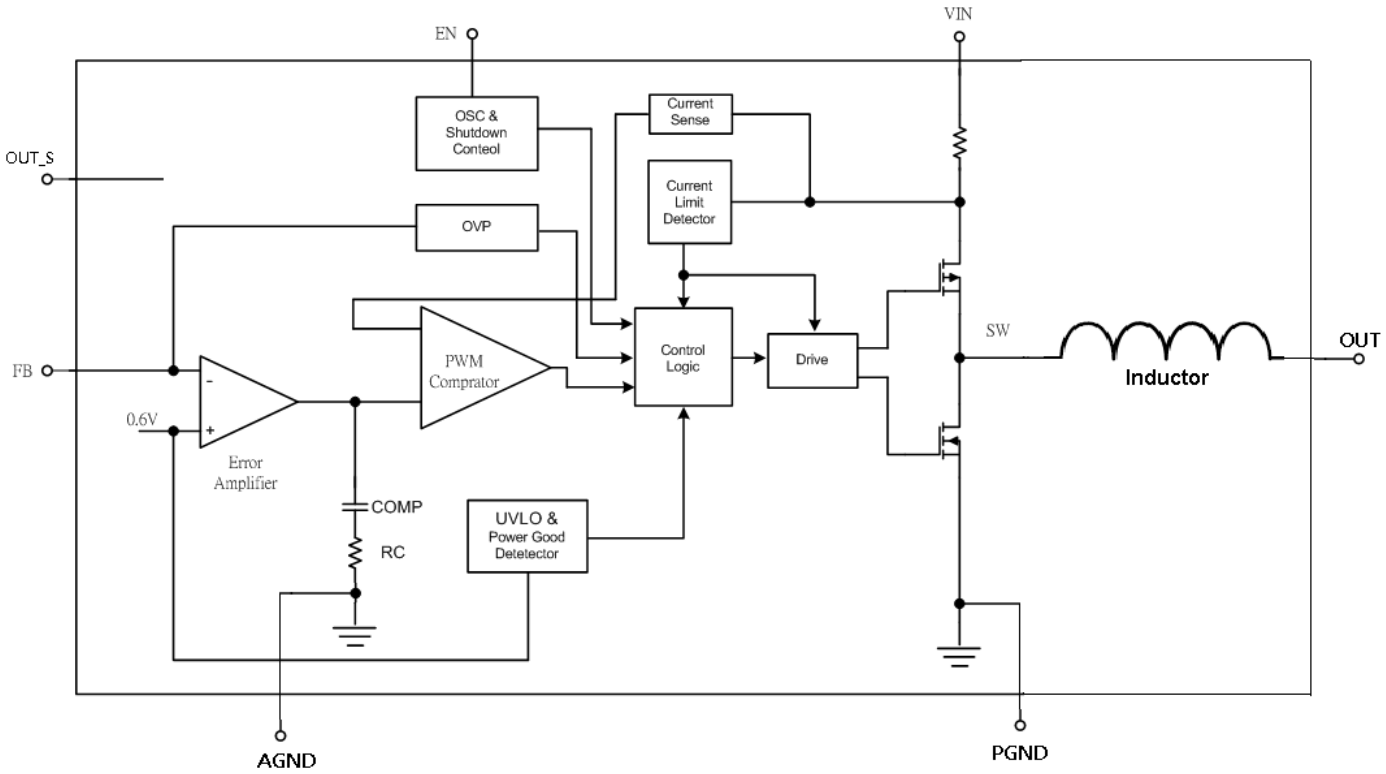

Figure 2 Functional Block Diagram

Note:

Diodes inside the circuit are an ESD protection diode and a parasitic diode.

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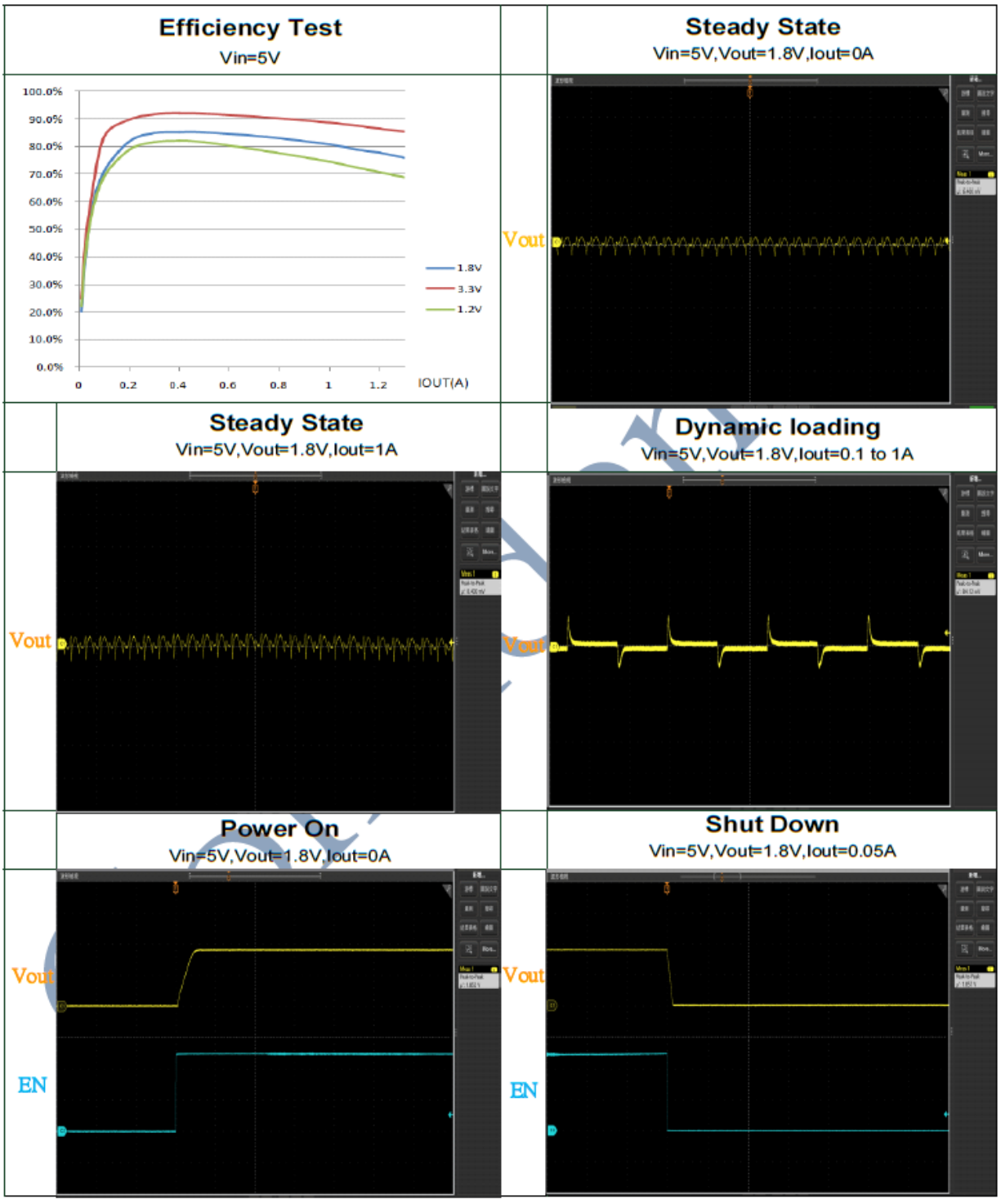
Typical Performance Characteristics

Tested under TA=25°C, unless otherwise specified



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Applications Information:

- Setting the Output Voltage

The external resistor divider sets the output voltage. The feedback resistor R1 also sets the feedback loop bandwidth with the internal compensation capacitor. Table 1 shows a list of resistor selection for common output voltages

$$VOUT = 0.6V * (1 + \frac{\mathrm{R1}}{\mathrm{R2}})$$

- Selecting the Input Capacitor

The input capacitor reduces the surge current drawn from the input and switching noise from the device. The input capacitor impedance at the switching frequency shall be less than input source impedance to prevent high frequency switching current passing to the input. Ceramic capacitors with X5R or X7R dielectrics are highly recommended because of their low ESR and small temperature coefficients. For most applications, a 10uF capacitor is sufficient.

- Selecting the Output Capacitor

The output capacitor keeps output voltage ripple small and ensures regulation loop stable. The output capacitor impedance shall be low at the switching frequency. Ceramic capacitors with X5R or X7R dielectrics are recommended.

The output ripple ΔV_{OUT} is approximately:

$$\triangle\ V_{OUT} \leq \frac{V_{OUT} \times (V_{IN} - V_{OUT})}{V_{IN} \times F_{SW} \times L} \times \left[ESR + \frac{1}{8 \times F_{SW} \times C2}\right]$$

- PCB Layout Recommendation

Especially noted in the pattern layout are as follows:

1) Wire the large current line using thick, short connecting traces. This makes it possible to reduce the wire impedance, which is expected to reduce noise and improve heat dissipation. If the wire impedance of the large current line is large, it may cause noise or the IC to not operate normally.
2) Place the input capacitance CIN, output capacitance CL, and IC which the large current flows on the same surface. If they are placed on both sides, a large current will flow through Via, which has high impedance, it may cause noise and the IC may not operate normally.

$$I_{SAT,MIN} > I_{OUT,MAX} + \frac{\mathrm{V}_{OUT}(1 - \frac{V_{OUT}}{V_{IN,MAX}})}{2 * F_{SW} * L}$$

3) Please mount each external component as close to the IC as possible. Especially place the input capacitance CIN near the IC and connect it with as low impedance as possible. If the input capacity CIN and IC are too far apart, it may cause noise or the IC may not operate normally.

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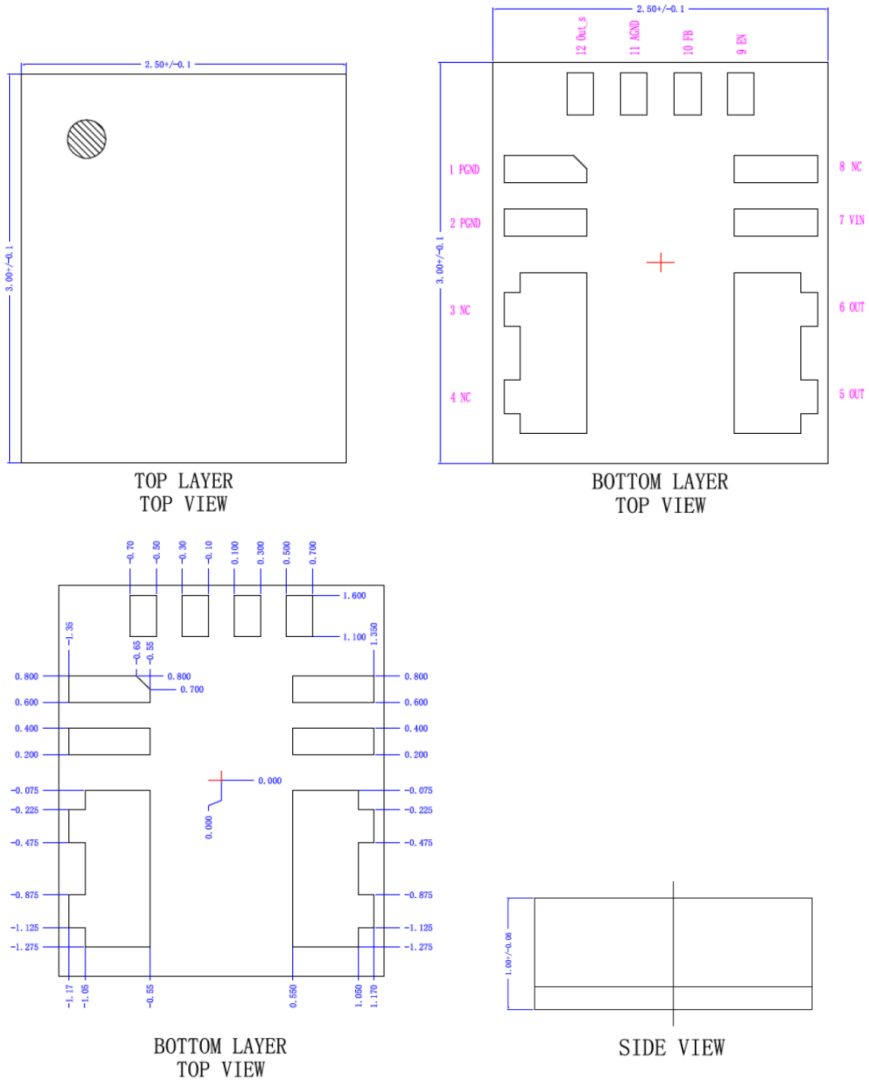
Package Dimension:

QFN-12 (2.5mmx3.0mmx1.0mm)



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