Ver.03

Date : Feb 05, 2018

Specification

[Product Name : LPM013M091A]

Japan Display Inc.

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1. BASIC SPECIFICATIONS

This product is the reflective display which can perform 2 types, super low power 8 colors of MIP (Memory In Pixel) mode and normal 262k colors by the command changes. Therefore, the specification is defined in reflective mode only unless otherwise specified in the specification sheet.

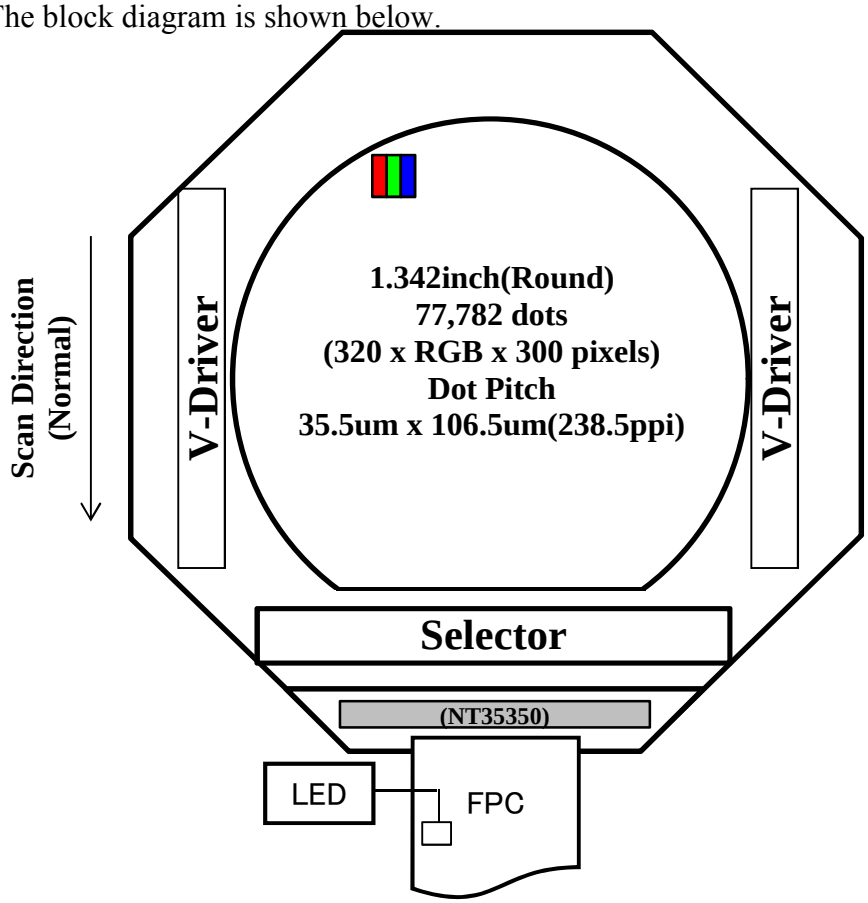
1.1 STRUCTURES

No.	FACTOR	SPECIFICATIONS	UNIT
1	LCD structure	LTPS AC-VCOM Analog(Normal) driving mode or Memory in Pixel mode	-
2	Outward (W x H x D)	37.28×38.18×1.55(*1-1)	mm
3	Weight	2.8(Typ.)	g
4	Screen size	34.08 (1.34 inch) *round type	mm
5	Number of dots	77,782(320xRGBx300)	dot
6	Dot pitch (Horizontal x Vertica	0.0355×0.1065	mm
7	Dot layout	RGB Stripe	-
8	Interface	SPI / 1-lane MIPI DSI	-
9	Number of colors	8 colors at MIP mode or 262k colors at normal mode	–
10	LCD optical mode	ECB normally black (Reflective type)	-
11	Polarizer	Hard Coat type (*Pencil Hardness : 2H)	-
12	Light source type	Backlight with white LED (1chip)	-

(*1-1) Excluding FPC and part of protruding. See attached drawing for details.

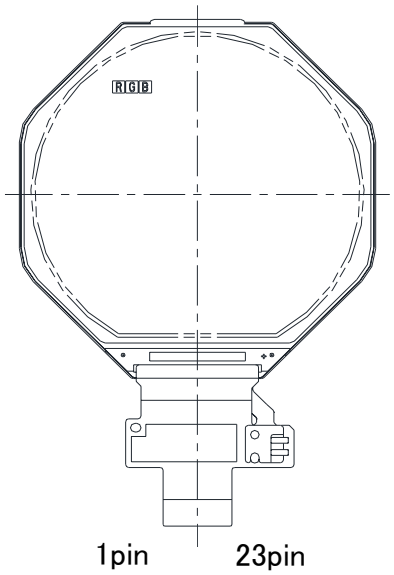
1.2 BLOCK DIAGRAM

The block diagram is shown below.



1.3 I/O PINS

Pin No.	LCD_TEST(GND)	I/O	Power/Signal	Description
1	N.C.	-	-	LCD TEST Pin (Please open)
2	VCI	I	Power	Power Supply for Analog Circuit
3	VDDI	I	Power	Power Supply for I/O
4	GND	-	-	GND
5	HSSI_D0_N	I/O	Signal	MIPI negative data signal
6	HSSI_D0_P	I/O	Signal	MIPI positive data signal
7	GND	-	-	GND
8	HSSI_CLK_N	I	Signal	MIPI negative clock signal
9	HSSI_CLK_P	I	Signal	MIPI positive clock signal
10	GND	-	-	GND
11	SDI	I/O	Signal	Serial data input/output
12	SCL	I	Signal	Synchronous clock signal
13	DCX	I	Signal	Connect to VDDI for 3 wires mode, or data command select signal for 4 wires mode in SPI.
14	CSX	I	Signal	Chip select signal
15	GND	-	-	GND
16	RESX	I	Signal	Reset pin (Active Low)
17	IM0	I	Signal	GND for 3 wires mode,or connect to VDDI for 4 wires mode in SPI.
18	LCD_TEST(GND)	-	-	LCD TEST Pin(Please connect to GND)
19	LEDPWM	O	Signal	PWM feedback Signal for LED Driver
20	TE	O	Signal	Frame Head Signal
21	N.C.	-	-	LCD TEST Pin (Please open)
22	LED_A	I	Power	Power supply for LED backlight anode
23	LED_K	I	Power	Power supply for LED backlight cathode



2. ABSOLUTE MAXIMUM RATING

Item	Symbol	Rated value	Unit	Description
Power Supply for I/O	VDDI	-0.3 ~ +4.0	V	
Power Supply for Analog Circuit	VCI	-0.3 ~ +5.5	V	
Digital input terminal voltage	VIN	-0.3 ~ VDDI+0.3	V	
	VO	-0.3 ~ VDDI+0.3	V	
Differential input voltage	HSSI_CLK_P/N HSSI_D0_P/N	-0.3~+1.45	V	
Operating temperature range (LCD panel surface)	Topr	-20 ~ +70	℃	(*2-1)
Storage temperature range	Tstg	-30 ~ +80	℃	(*2-1)
LED Forward current	Iled	+35	mA	

Note)

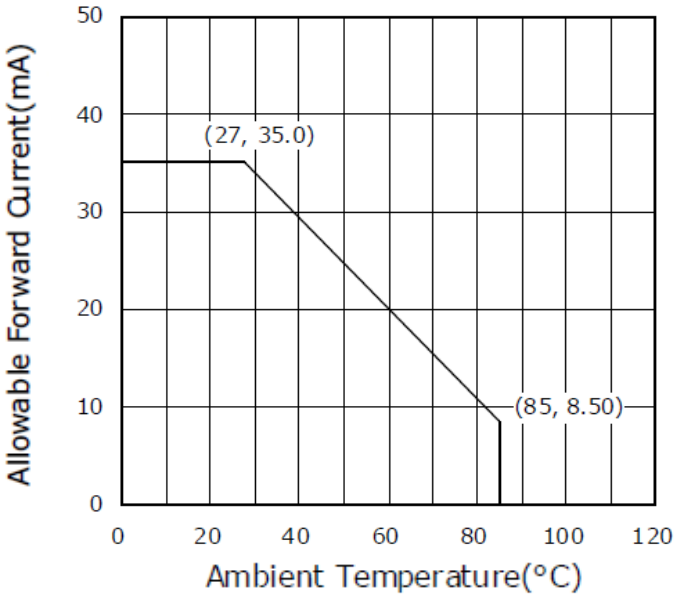
(*2-1): Maximum humidity is defined as follows:

Ta≦40°C : 85%RH Max.

Ta> 40°C : Absolute humidity needs to be equal or less than the numeric value at the condition of Ta=40°C, 85%RH.

Don't condense dew.

(*2-2): Ambient Temperature vs Allowable Forward Current is due to the following graph.



3. ELECTRICAL SPECIFICATIONS

3.1. Operating Conditions

3.1.1 Input and output power supply voltage conditions

(GND=0V)

Item	Symbol	Min.	Typ.	Max.	Unit
Power Supply for I/O	VDDI	1.7	1.8	1.9	V
Power Supply for Analog Circuit	VCI	3.0	3.1	3.2	V

3.1.2 Input signal voltage conditions (DC conditions)

Item	Symbol	Min.	Typ.	Max.	Unit	Application Terminal
High level threshold voltage	VIH	0.8xVDDI	-	VDDI	V	All Input terminal
Low level threshold voltage	VIL	VSS	-	0.2xVDDI	V	
High level current leakage	ILIH	-	-	10	uA	
Low level current leakage	ILIL	-10	-	-	uA	

3.1.3 DC characteristic power consumption characteristics, input threshold

VDDI=1.8V , VCI=3.1V

Item	Symbol	Measurement condition	Min.	Typ.	Max.	Unit	Application Terminal
Normal Mode consumption current	Ivvdi	Ta=25℃,White raster display	-	1.11	1.40	mA	VDDI
	Ivci		-	1.75	2.70		VCI
MIP Mode consumption current	Ivvdi	Ta=25℃,White raster display	-	0.23	0.34		VDDI
	Ivci		-	0.13	0.22		VCI
Sleep Mode consumption current	Ivvdi	Ta=25℃	-	-	0.200		VDDI
	Ivci		-	-	0.005		VCI

3.1.4 Backlight Operating Conditions

(Iled=20mA)

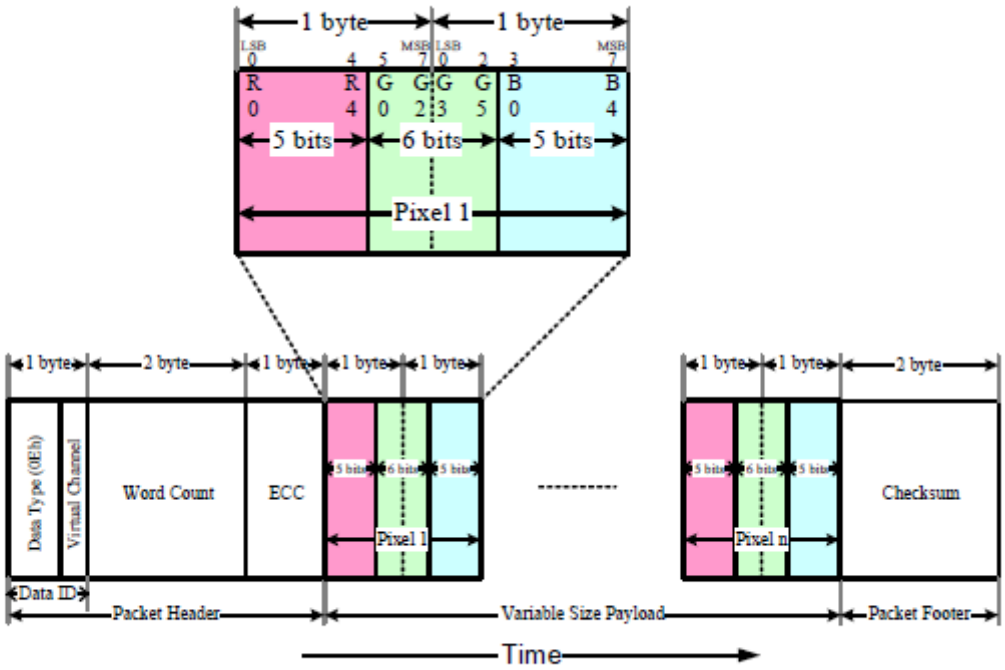
Item	Symbol	Min.	Typ.	Max.	Unit
Backlight forward voltage	Vfbl	-	2.9	3.2	V

4. INTERFACE

4.1 MIPI INTERFACE

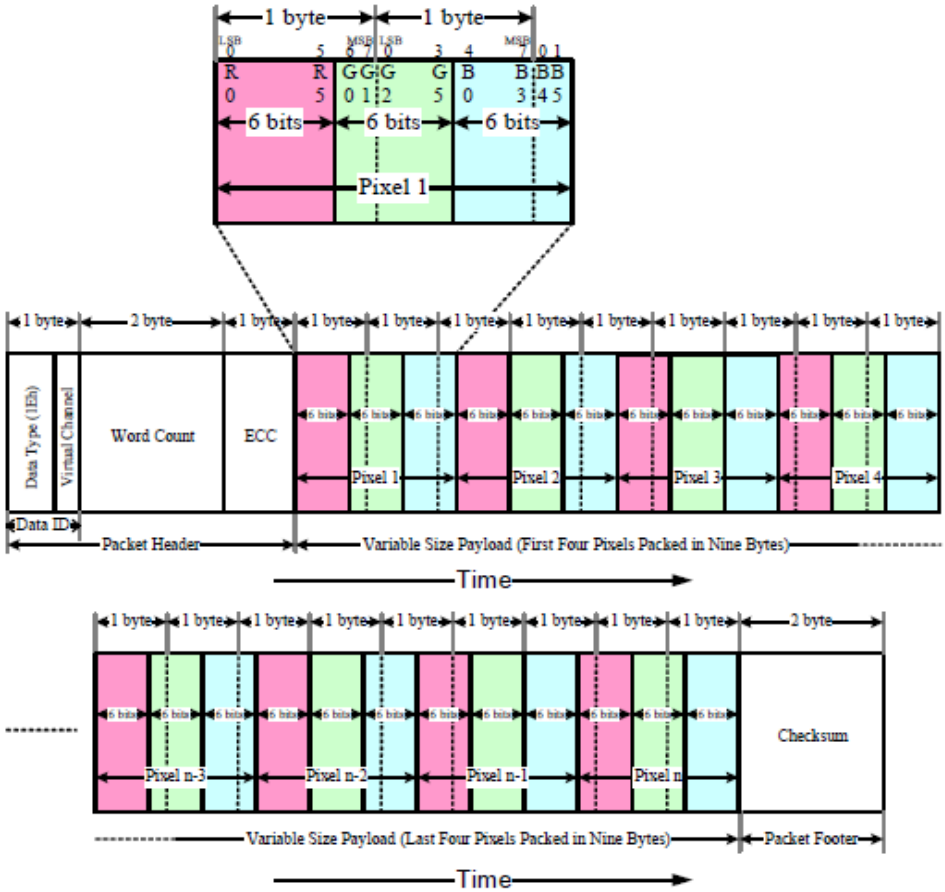
Follow the MIPI Standerd.
D-PHY: V1.0
DSI:1.01.00
DCS:1.01.00
MIPI I/F Supported 1 data lane (MIPI CLK speed up to 300Mbps).
MIPI I/F Supported only command mode.

Packed Pixel Stream, 16-bits Format, Long packet, Data Type 1228 pe 00 1110 (0Eh)



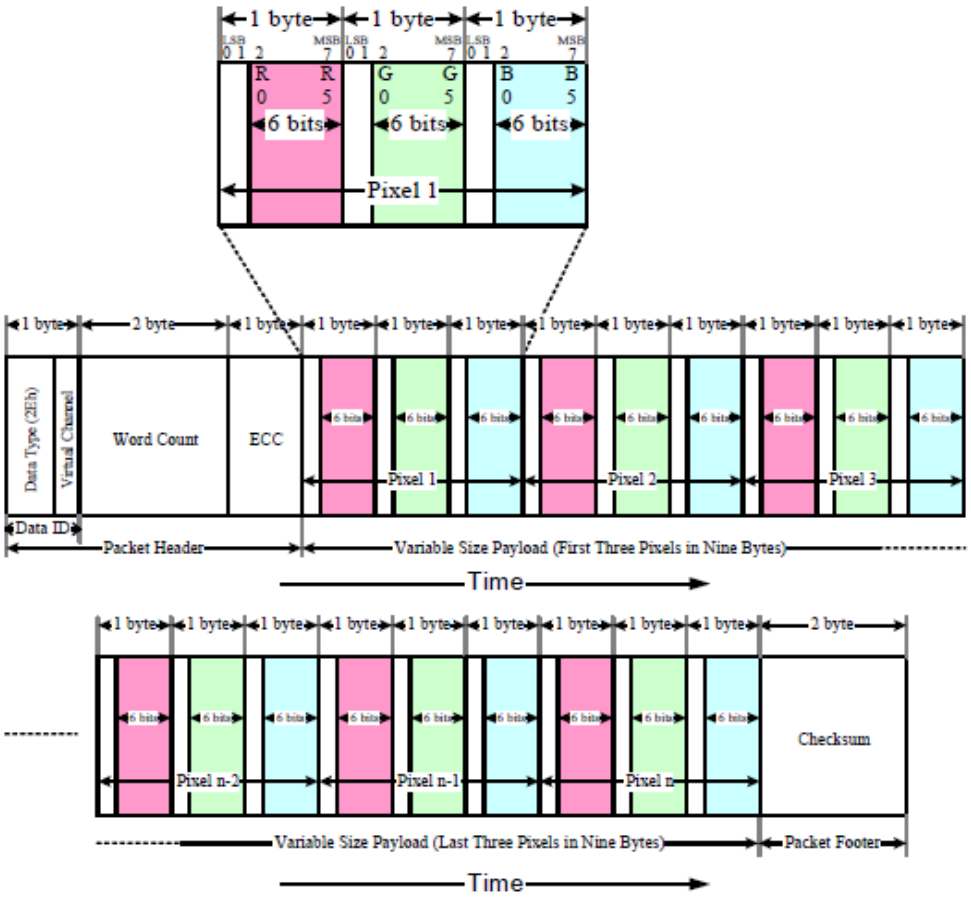
16-bit per Pixel – RGB Color Format, Long packet

Packed Pixel Stream, 18-bits Format, Long packet, Data type = 01 1110 (1Eh)



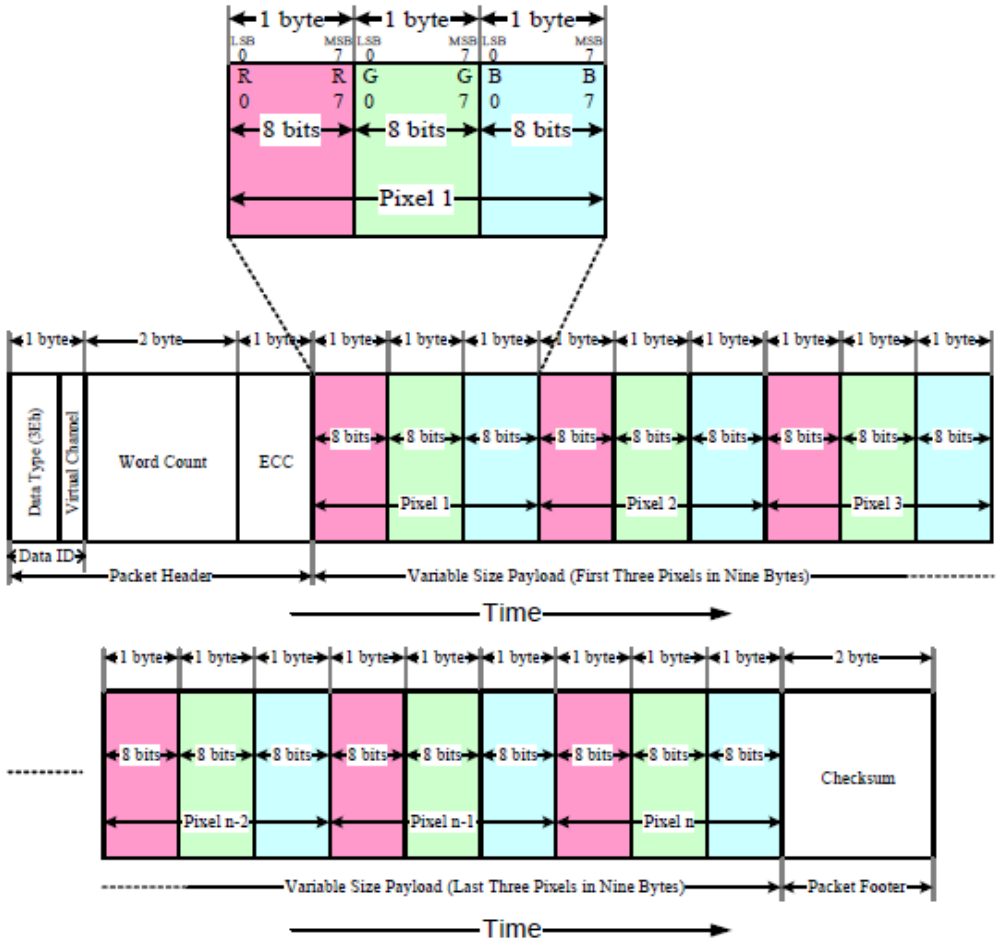
18-bit per Pixel (Packed)– RGB Color Format, Long packet

Pixel Stream, 18-bits Format in Three Bytes, Long packet, Data Type = 101110 (2Eh)



18-bit per Pixel (Loosely Packed)– RGB Color Format, Long packet

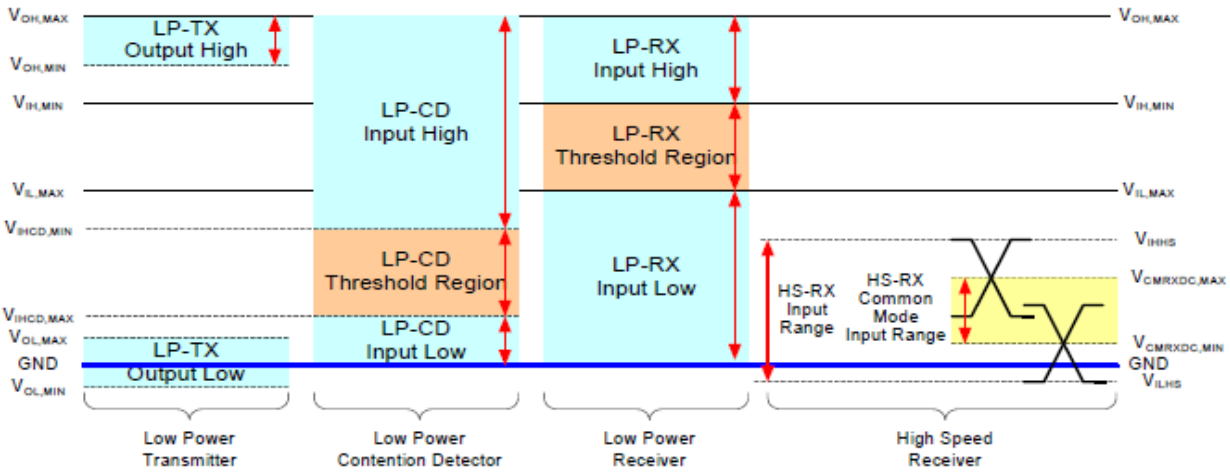
Packed Pixel Stream, 24-bits Format, Long packet, Data Type = 11 1110 (3Eh)



24-bit per Pixel – RGB Color Format, Long packet

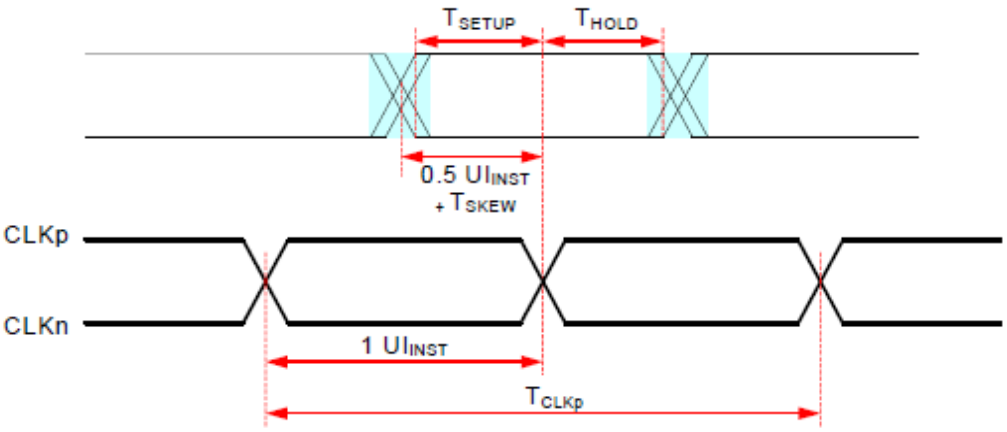
4.2 MIPI DC CHARACTERISTICS

Symbol	Parameter	Min	Typ	Max	Unit
MIPI Characteristics for High Speed Receiver					
VILHS	Single-ended input low voltage	-40	-	-	mV
VIHHS	Single-ended input high voltage	-	-	460	mV
VCMRXDC	Common-mode voltage	70	-	330	mV
ZID	Differential input impedance	80	100	125	ohm
V_{IDTH}	Different input high threshold	-	-	70	mV
V_{IDTL}	Different input low threshold	-70	-	-	mV
$V_{TERM-EN}$	Single-ended threshold for HS termination enable	-	-	450	mV
MIPI Characteristics for Low Power Mode					
VI	Pad signal voltage range	-50	-	1350	mV
VGNDSH	Ground shift	-50	-	50	mV
VIL	Logic 0 input threshold	0.0	-	550	mV
VIH	Logic 1 input threshold	880	-	VDD	mV
VHYST	Input hysteresis	25	-	-	mV
VOL	Output low level	-50	-	50	mV
VOH	Output high level	1.1	1.2	1.3	V
VIHCD,MAX	Logic 0 contention threshold	0.0	-	200	mV
VILCD,MIN	Logic 1 contention threshold	450	-	VDD	mV



4.3 MIPI AC CHARACTERISTICS

High Speed Data Transmission: Data-Clock Timing



Parameter	Symbol	Min	Typ	Max	Units	Notes
UI instantaneous	UI_{INST}	3.33	-	12.5	ns	
Data to Clock Skew [measured at transmitter]	T_{SKEW}[TX]	-0.15	-	0.15	UI_{INST}	
Data to Clock Setup Time [measured at receiver]	T_{SETUP}[RX]	0.15	-	-	UI_{INST}	
Data to Clock Hold Time [measured at receiver]	T_{HOLD}[RX]	0.15	-	-	UI_{INST}	
20% - 80% rise time and fall time	t_R / t_F	150	-	-	ps	
		-	-	0.3	UI_{INST}	

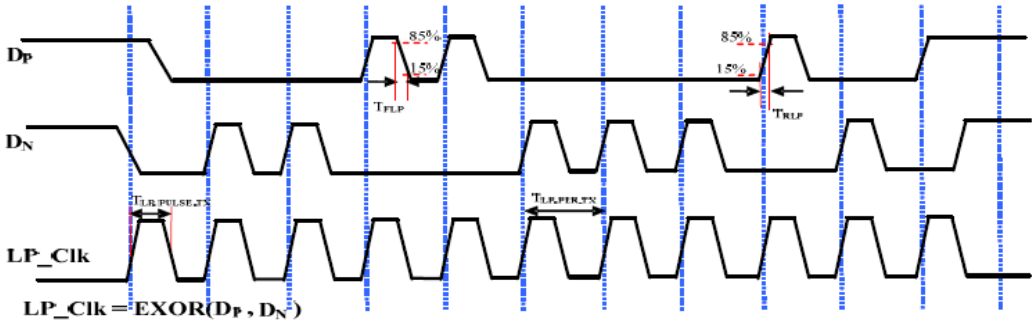
Note:

1. This value corresponds to a minimum 80 MHz data rate.

2. The minimum UI shall not be violated for any single bit period, i.e.,any DDR half cycle within a data burst.

3. For MIPI speed limitations: 300Mbps.

LP Transmission AC Specification



Parameter		Symbol	Min	Typ	Max	Units	Notes
15%-85% rise time and fall time		T_{RLP} / T_{FLP}	-	-	25	ns	1
30%-85% rise time and fall time		T_{REOT}	-	-	35	ns	1,5,6
Pulse width of the LP exclusive-OR clock	First LP exclusive-OR clock pulse after STOP state or last pulse before stop state	$T_{LP-PULSE-TX}$	40	-	-	ns	4
	All other pulses		20	-	-	ns	4
Period of the LP exclusive-OR clock		$T_{LP-PER-TX}$	90	-	-	ns	
Slew Rate@ C_{LOAD} = 0pF		$\delta V/\delta t_{SR}$	30	-	500	mV/ns	1,2,3,7
Slew Rate@ C_{LOAD} = 5pF			30	-	200	mV/ns	1,2,3,7
Slew Rate@ C_{LOAD} = 20pF			30	-	150	mV/ns	1,2,3,7
Slew Rate@ C_{LOAD} = 70pF			30	-	100	mV/ns	1,2,3,7
Load Capacitance		C_{LOAD}	-	-	70	pF	1

Note:

1. CLOAD includes the low-frequency equivalent transmission line capacitance. The capacitance of TX and RX are assumed to always be <10pF. The distributed line capacitance can be up to 50pF for a transmission line with 2ns delay.

2. When the output voltage is between 15% and below 85% of the fully settled LP signal levels.

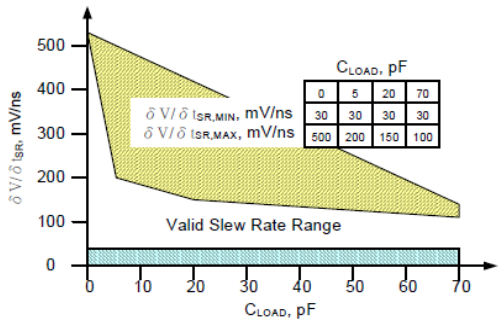
3. Measured as average across any 50 mV segment of the output signal transition.

4. This parameter value can be lower then TLPX due to differences in rise vs. fall signal slopes and trip levels and mismatches between Dp and Dn LP transmitters. Any LP exclusive-OR pulse observed during HS EoT (transition from HS level to LP-11) is glitch behavior.

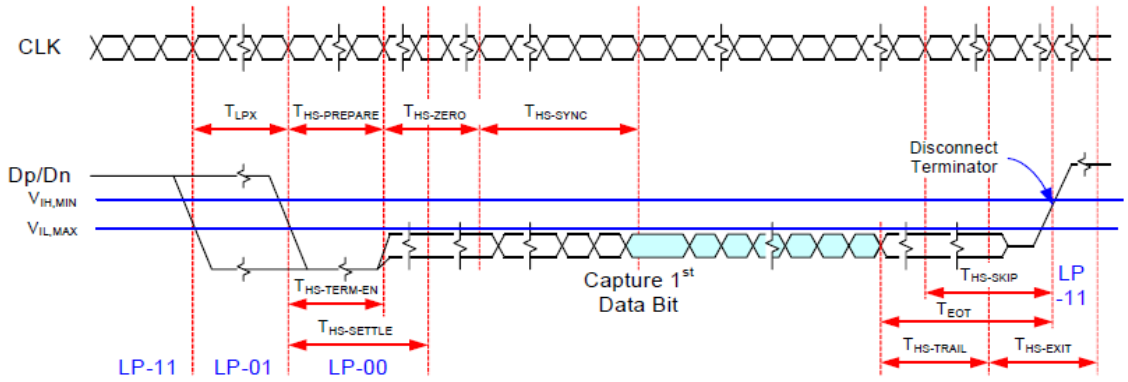
5. The rise-time of TREOT starts from the HS common-level at the moment the differential amplitude drops below 70mV, due to stopping the differential drive.

6. With an additional load capacitance CCM between 0-60pF on the termination center tap at RX side of the Lane.

7. This value represents a corner point in a piecewise linear curve as bellowed.



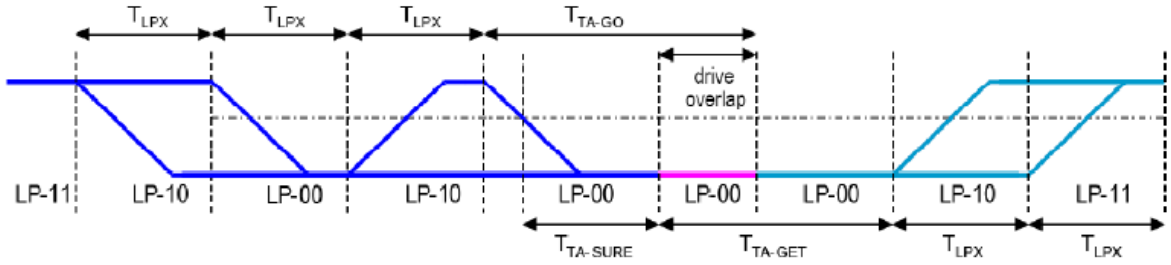
High-Speed Data Transmission in Bursts



Parameter	Symbol	Min	Typ	Max	Units
Time to drive LP-00 to prepare for HS transmission	$T_{HS-PREPARE}$	40+4UI		85+6UI	ns
Time from start of tHS-TRAIL or tCLK-TRAIL period to start of LP-11 state	T_{EOT}			105+12UI	ns
Time to enable Data Lane receiver line termination measured from when Dn cross VIL,MAX	$T_{HS-TERM-EN}$			35+4UI	ns
Time to drive flipped differential state after last payload data bit of a HS transmission burst	$T_{HS-TRAIL}$	60+4UI			ns
Time-out at RX to ignore transition period of EoT	$T_{HS-SKIP}$	40		55+4UI	ns
Time to drive LP-11 after HS burst	$T_{HS-EXIT}$	100			ns
Length of any Low-Power state period	T_{LPX}	50			ns
Sync sequence period	$T_{HS-SYNC}$		8UI		ns
Minimum lead HS-0 drive period before the Sync sequence	$T_{HS-ZERO}$	105+6UI			ns

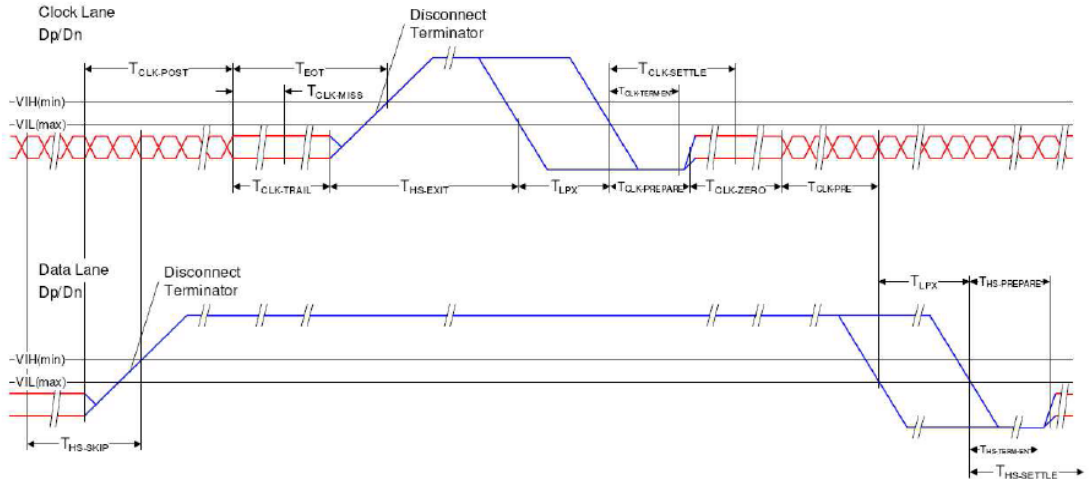
Note:
1: The minimum value depends on the bit rate. Implementations should ensure proper operation for all the supported bit rates.
2: UI means Unit Interval, equal to one half HS the clock period on the Clock Lane.
3: TLPX is an internal state machine timing reference. Externally measured values may differ slightly from the specified values due to asymmetrical rise and fall times.

Turnaround Procedure



Parameter	Symbol	Min	Typ	Max	Units
Length of any Low-Power state period : Master side	T_{LPX}	50		75	ns
Length of any Low-Power state period : Slave side	T_{LPX}	50		75	ns
Ratio of TLPX(MASTER)/TLPX(SLAVE) between Master and Slave side	Ratio T_{LPX}	2/3		3/2	
Time-out before new TX side start driving	$T_{TA-SURE}$	T_{LPX}		$2T_{LPX}$	ns
Time to drive LP-00 by new TX	T_{TA-GET}		$5T_{LPX}$		ns
Time to drive LP-00 after Turnaround Request	T_{TA-GO}		$4T_{LPX}$		ns

Switching the Clock Lane between Clock Transmission and Low-Power Mode

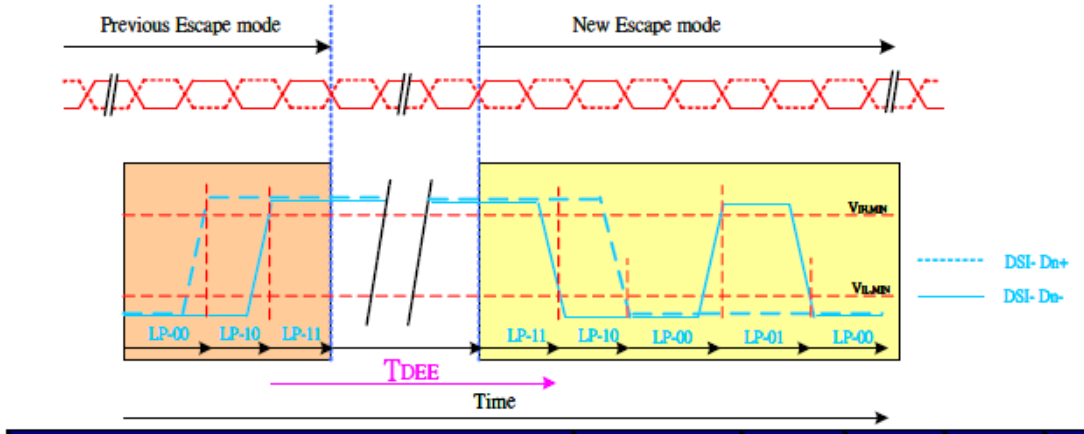


Parameter	Symbol	Min	Typ	Max	Units
Time that the transmitter shall continue sending HS clock after the last associated Data Lane has transitioned to LP mode.	$T_{CLK-POST}$	60+52UI	-	-	ns
Detection time that the clock has stopped toggling	$T_{CLK-MISS}$	-	-	60	ns
Time to drive LP-00 to prepare for HS clock transmission	$T_{CLK-PREPARE}$	38	-	95	ns
Minimum lead HS-0 drive period before starting Clock	$T_{CLK-PREPARE}$ +$T_{CLK-ZERO}$	300	-	-	ns
Time to enable Clock Lane receiver line termination measured from when Dn cross VIL,MAX	$T_{HS-TERM-EN}$	-	-	38	ns
Minimum time that the HS clock must be set prior to any associated date lane beginning the transmission from LP to HS mode	$T_{CLK-PRE}$	8	-	-	UI
Time to drive HS differential state after last payload clock bit of a HS transmission burst	$T_{CLK-TRAIL}$	60	-	-	ns

LP11 timing request between data transformation

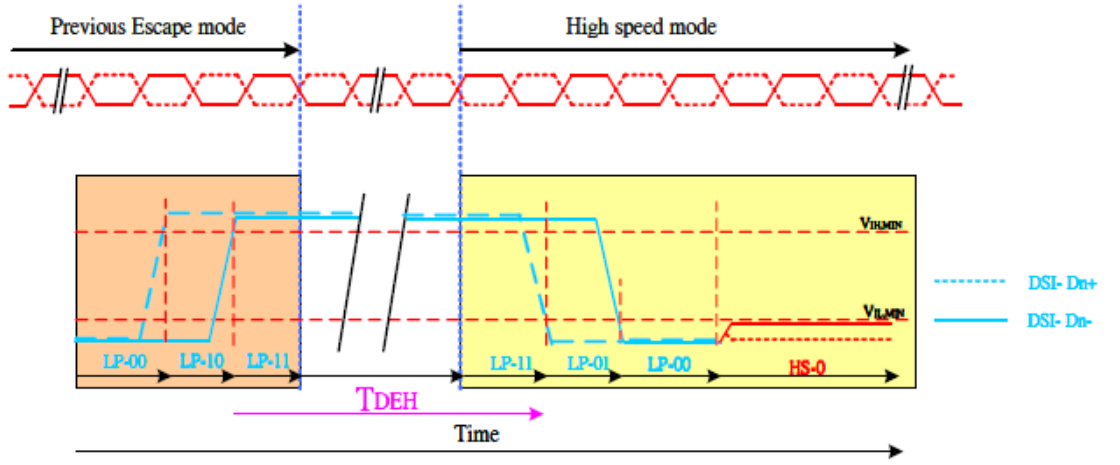
When Clock lane of DSI TX chip always keeps High speed mode, then Clock lane never go back to Low power mode. If Date lane of TX chip needs to transmit the next new data transmission or sequence, after the end of Low power mode or High speed mode or BTA. Then TX chip needs to keep LP-11 stop state before the next new data transmission, no matter in Low power mode or High speed mode or BTA. The LP-11 minimum timing is required for RX chip in the following 9 conditions, include of LP – LP, LP – HS, HS – LP, HS – HS, BTA – BTA, LP – BTA, BTA – LP, HS – BTA, and BTA – HS. This rule is suitable for short or long packet between TX and RX data transmission.

(1) Timing between LP – LP command



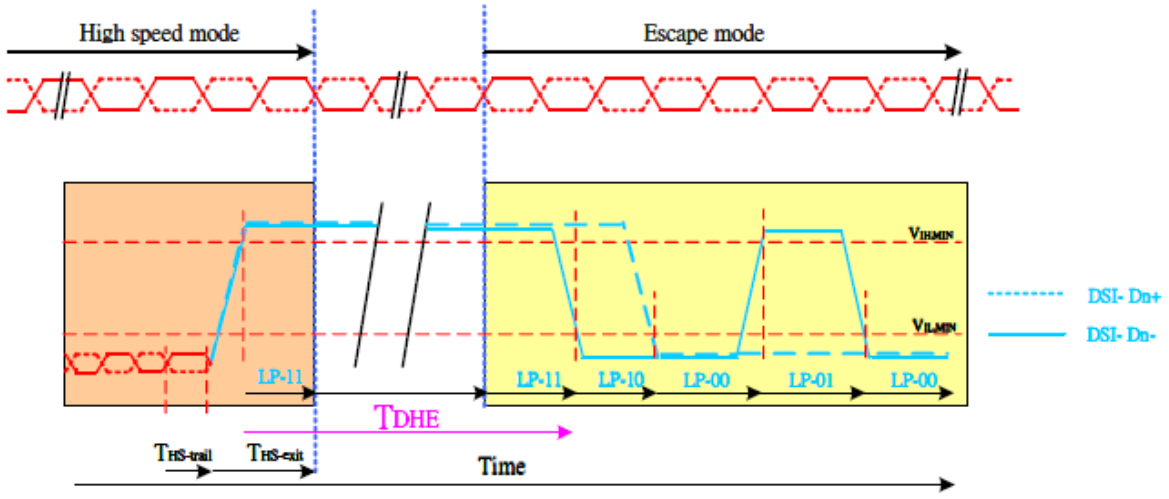
Parameter	Symbol	Min	Typ	Max	Units
LP-11 delay to a start of the new Escape Mode Entry	T_{DEE}	100			ns

(2)Timing between LP – HS command



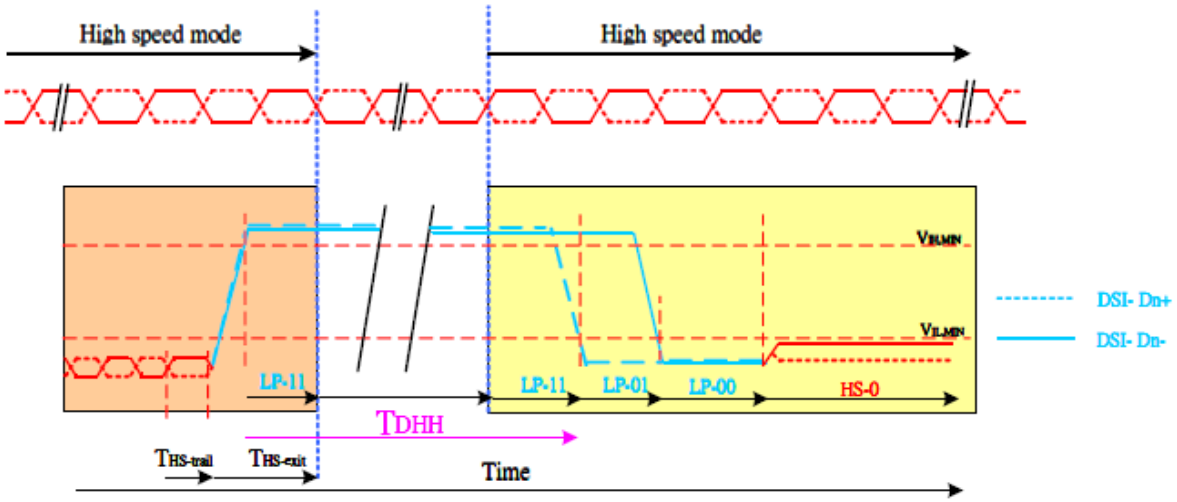
Parameter	Symbol	Min	Typ	Max	Units
LP-11 delay to a start of the Entering High Speed Mode	T_{DEH}	Max(100,32UI)			ns

(3)Timing between HS – LP command



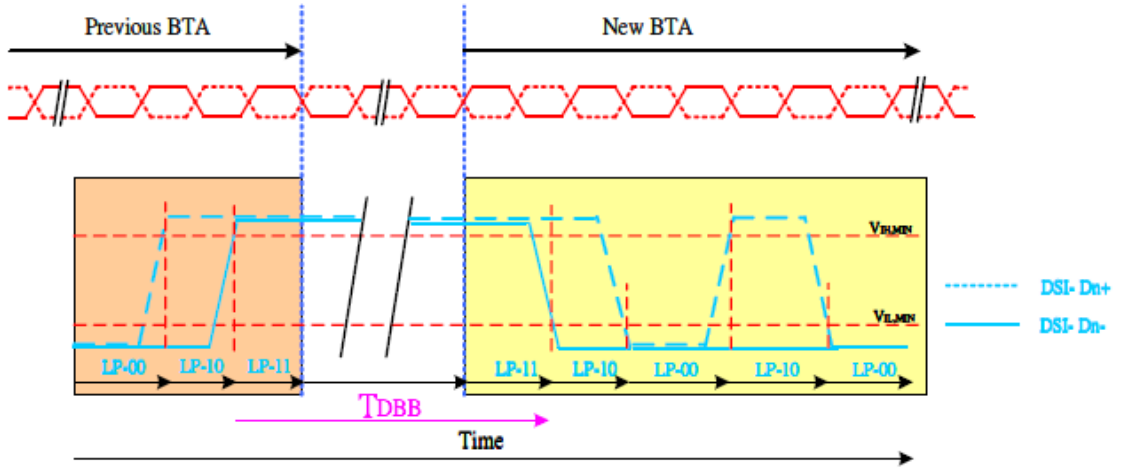
Parameter	Symbol	Min	Typ	Max	Units
LP-11 delay to a start of the Escape Mode Entry	T_{DHE}	Max(100,32UI)			ns

(4)Timing between HS –HS command



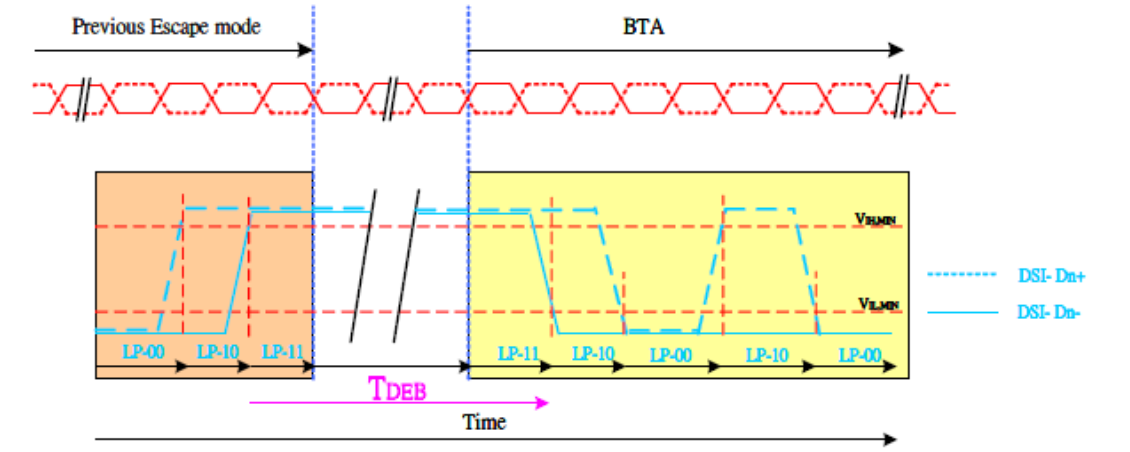
Parameter	Symbol	Min	Typ	Max	Units
LP-11vdelay to a start of the Entering High Speed Mode	T_{DHH}	Max(100,32UI)			ns

(5)Timing between BTA – BTA command



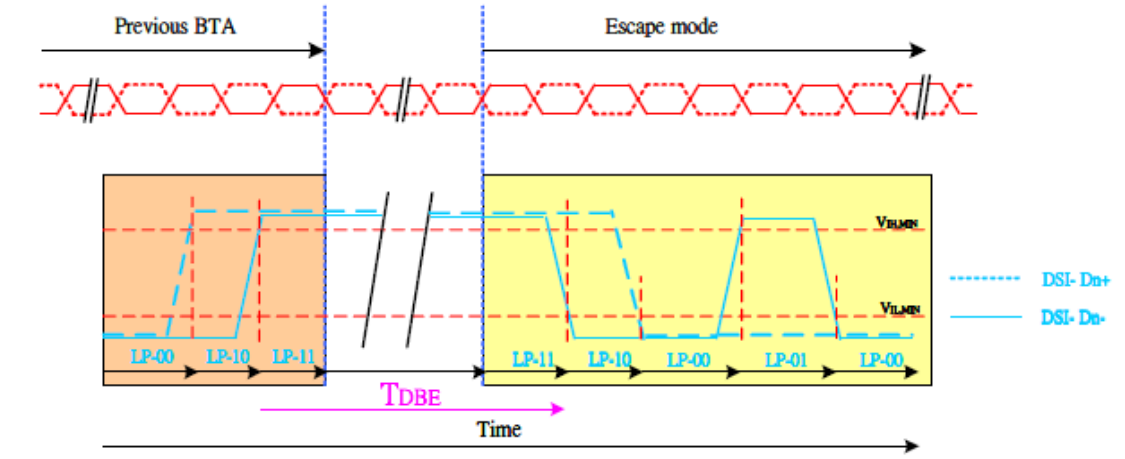
Parameter	Symbol	Min	Typ	Max	Units
LP-11vdelay to a start of the new BTA	T_{DBB}	100			ns

(6)Timing between LP– BTA command



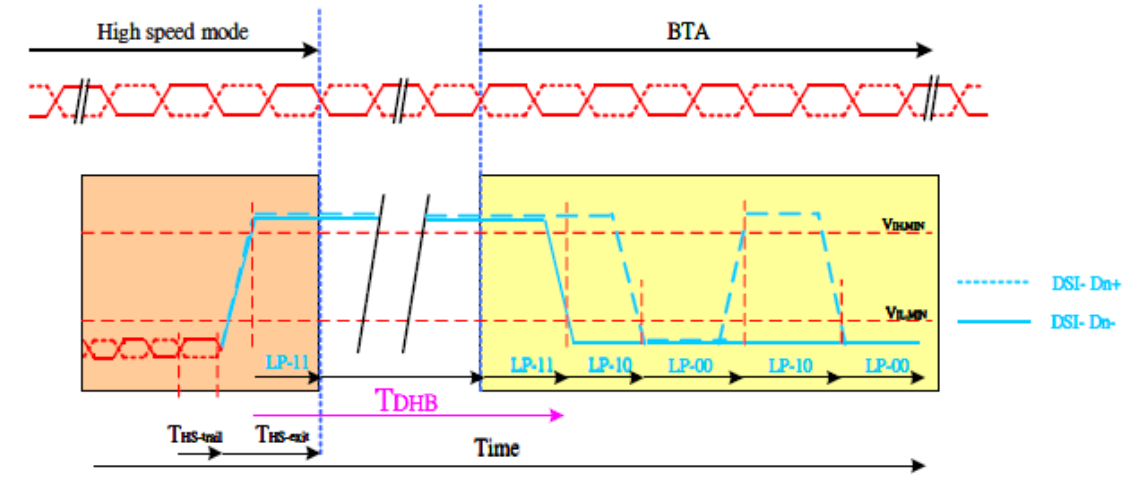
Parameter	Symbol	Min	Typ	Max	Units
LP-11vdelay to a start of the BTA	T_{DEB}	100			ns

(7)Timing between BTA – LP command



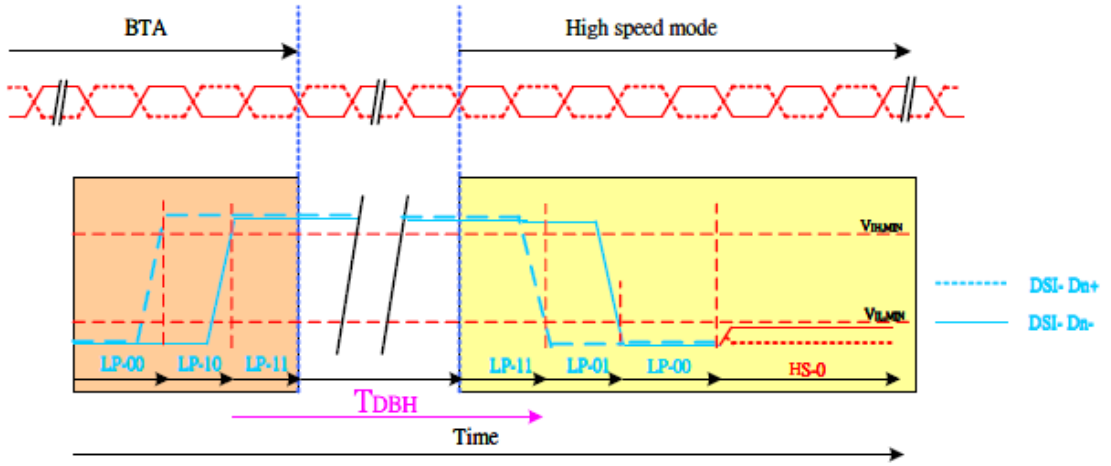
Parameter	Symbol	Min	Typ	Max	Units
LP-11vdelay to a start of the Escape Mode Entry	T_{DBE}	100			ns

(8)Timing between HS – BTA command



Parameter	Symbol	Min	Typ	Max	Units
LP-11vdelay to a start of the BTA	T_{DHB}	Max(100,32UI)			ns

(9)Timing between BTA – HS command

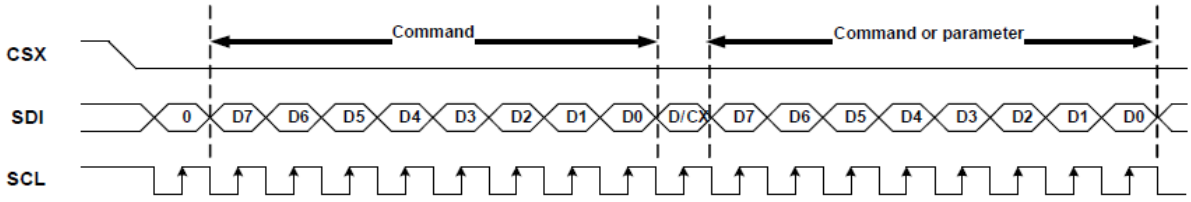


Parameter	Symbol	Min	Typ	Max	Units
LP-11vdelay to a start of the Entering High Speed Mode	T_{DBH}	Max(100,32UI)			ns

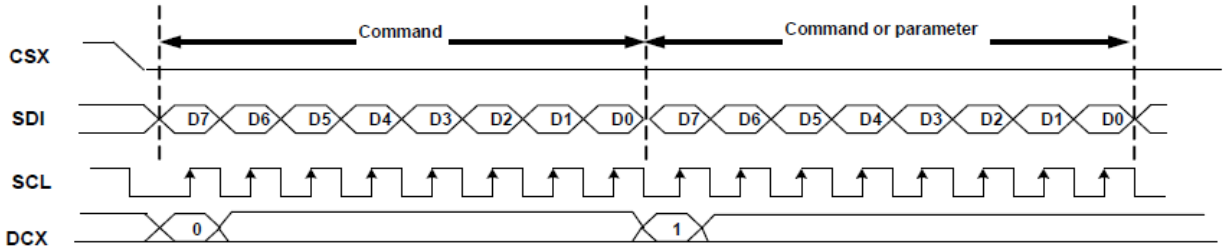
4.4 SPI

Command Write for LoSSI

The host CPU drives the CSX pin low and starts by setting the D/CX-bit on SDI or by DCX pin. The bit is read by the display on the first rising
edge of SCL. For 4-Wires Mode, first bit is data bit (D7) is set on SDI by the CPU. Then on the next falling edge of SCL the MSB data bit (D6) is
set on SDI by the CPU and so on. For 3-Wires Mode, the next falling edge of SCL the MSB data bit (D7) is set on SDI by the CPU. On the next
falling edge of SCL the next bit (D6) is set on SDI and so on. This continues until all 8 Data bits have been transmitted as shown in below figures:
Command Write.



Command/GRAM Write for 3-Wires Mode 9-bit Type SPI



Command/GRAM Write for 4-Wires Mode 8-bit Type SPI

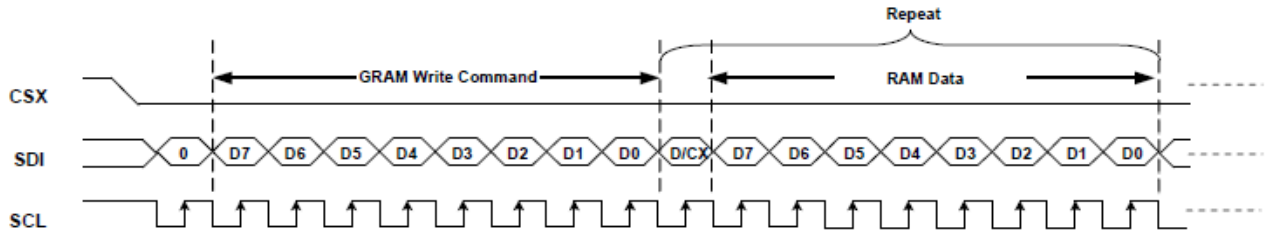
Note:
(*4-1)The GRAM write command should be 2Ch/3Ch.

(*4-2)When using SPI,differential input voltage for MIPI,such as HSSI_D0_N,HSSI_D0_P,HSSI_CLK_N, HSSI_CLK_P,should be fixed 1.2V,which is the high level of the differential input voltage. The power on sequence for these pins should follow LP11(See Page.27) even if not using MIPI.

Serial Interface SPI for RAM Data Write/Read

Different display data formats are available for two colors depth supported by the NT35350 listed below.

- 8 colors, RGB 1-1-1-bits pixel data input. (Only support GRAM Write by 0x2C command, not support GRAM Read)
- 65k colors, RGB 5-6-5-bits pixel data input.
- 262k colors, RGB 6- 6-6-bits pixel data input.



TYPE1:

RGB 1-1-1-bits	DCX	D[7]	D[6]	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]	Note
CMDWR	0	0	0	1	0	1	1	0	0	0x2C for GRAM Write
1st RAM Data Write	1	R1[0]	G1[0]	B1[0]	R2[0]	G2[0]	B2[0]	R3[0]	G3[0]	1, 2, 3 Pixel Data write
2nd RAM Data Write	1	B3[5]	R4[0]	G4[0]	B4[0]	R5[0]	G5[0]	B5[0]	R6[0]	3, 4, 5, 6 Pixel Data write
3rd RAM Data Write	1	G6[0]	B6[0]	R7[0]	G7[0]	B7[0]	R8[0]	G8[0]	B8[0]	6, 7, 8 Pixel Data write
So on…										

Note: Transfer data including DCX bit

Table 1. RGB 1-1-1-bits GRAM Write for 3-Wires Mode 9-bit Type SPI

TYPE2:

RGB 1-1-1-bits	DCX	D[7]	D[6]	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]	Note
CMDWR	0	0	0	1	0	1	1	0	0	0x2C for GRAM Write
1st RAM Data Write	1	X	X	R1[0]	G1[0]	B1[0]	R2[0]	G2[0]	B2[0]	1, 2 Pixel Data write
2nd RAM Data Write	1	X	X	R3[0]	G3[0]	B3[5]	R4[0]	G4[0]	B4[0]	3, 4 Pixel Data write
3rd RAM Data Write	1	X	X	R5[0]	G5[0]	B5[0]	R6[0]	G6[0]	B6[0]	5, 6 Pixel Data write
So on…										

Note: Transfer data including DCX bit

Table 2. RGB 1-1-1-bits GRAM Write for 3-Wires Mode 9-bit Type SPI

RGB 5-6-5-bits	DCX	D[7]	D[6]	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]	Note
CMDWR	0	0	0	1	0	1	1	0	0	0x2C for GRAM Write
1st RAM Data Write	1	R1[4]	R1[3]	R1[2]	R1[1]	R1[0]	G1[5]	G1[4]	G1[3]	1st Pixel Data Write (R1, G1, B1)
2nd RAM Data Write	1	G1[2]	G1[1]	G1[0]	B1[4]	B1[3]	B1[2]	B1[1]	B1[0]	
3rd RAM Data Write	1	R2[4]	R2[3]	R2[2]	R2[1]	R2[0]	G2[5]	G2[4]	G2[3]	2nd Pixel Data Write (R2, G2, B2)
4th RAM Data Write	1	G2[2]	G2[1]	G2[0]	B2[4]	B2[3]	B2[2]	B2[1]	B2[0]	
5th RAM Data Write	1	R3[4]	R3[3]	R3[2]	R3[1]	R3[0]	G3[5]	G3[4]	G3[3]	3rd Pixel Data Write (R3, G3, B3)
6th RAM Data Write	1	G3[2]	G3[1]	G3[0]	B3[4]	B3[3]	B3[2]	B3[1]	B3[0]	
So on…										

Note: Transfer data including DCX bit

Table 3. RGB 5-6-5-bits GRAM Write for 3-Wires Mode 9-bit Type SPI

RGB 6-6-6-bits	DCX	D[7]	D[6]	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]	Note
CMDWR	0	0	0	1	0	1	1	0	0	0x2C for GRAM Write
1st RAM Data Write	1	R1[5]	R1[4]	R1[3]	R1[2]	R1[1]	R1[0]	X	X	1st Pixel Data Write (R1, G1, B1)
2nd RAM Data Write	1	G1[5]	G1[4]	G1[3]	G1[2]	G1[1]	G1[0]	X	X	
3rd RAM Data Write	1	B1[5]	B1[4]	B1[3]	B1[2]	B1[1]	B1[0]	X	X	
4th RAM Data Write	1	R2[5]	R2[4]	R2[3]	R2[2]	R2[1]	R2[0]	X	X	2nd Pixel Data Write (R2, G2, B2)
5th RAM Data Write	1	G2[5]	G2[4]	G2[3]	G2[2]	G2[1]	G2[0]	X	X	
6th RAM Data Write	1	B2[5]	B2[4]	B2[3]	B2[2]	B2[1]	B2[0]	X	X	
So on…										

Note: Transfer data including DCX bit

Note: x means don't case

Table 4. RGB 6-6-6-bits GRAM Write for 3-Wires Mode 9-bit Type SPI

2

SPI SPEC

Serial Interface Timing Characteristics

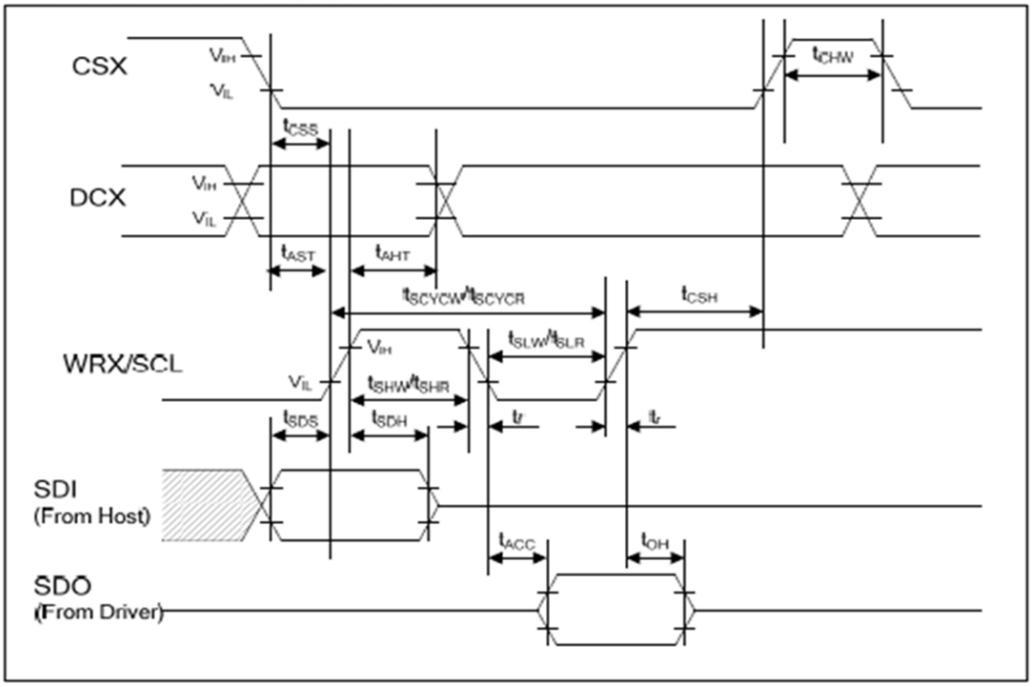


Figure1. Serial Interface Operation for 3-Wires/4-Wires 9/8-bit Type SPI

Register access(excluding 2C/3C command) SPI SPEC

Item	Symbol	Min.	Typ.	Max.	Unit
SCL clock cycle time Write (received)	t SCYCW	80	–	20,000	ns
SCL clock cycle time Read (transmitted)	t SCYCR	280	–	20,000	ns
SCL “High” pulse width Write (received)	t SHW	40	–	–	ns
SCL “High” pulse width Read (transmitted)	t SHR	140	–	–	ns
SCL “Low” pulse width Write (received)	t SLW	40	–	–	ns
SCL “Low” pulse width Read (transmitted)	t SLR	140	–	–	ns
SCL clock rise/fall time	t r , t f	–	–	10	ns
Chip select setup time	t CSS	20	–	–	ns
Chip select hold time	t CSH	50	–	–	ns
Input data setup time	t SDS	20	–	–	ns
Input data hold time	t SDH	20	–	–	ns
DCX to SCL Write setup time	tAST	20	–	–	ns
DCX to SCL Write hold time	tAHT	2	–	–	ns
Output data access time	t ACC	–	–	120	ns
Output data hold time	t OH	5	–	–	ns
Chip deselect “High” pulse width	t CHW	40	–	–	ns

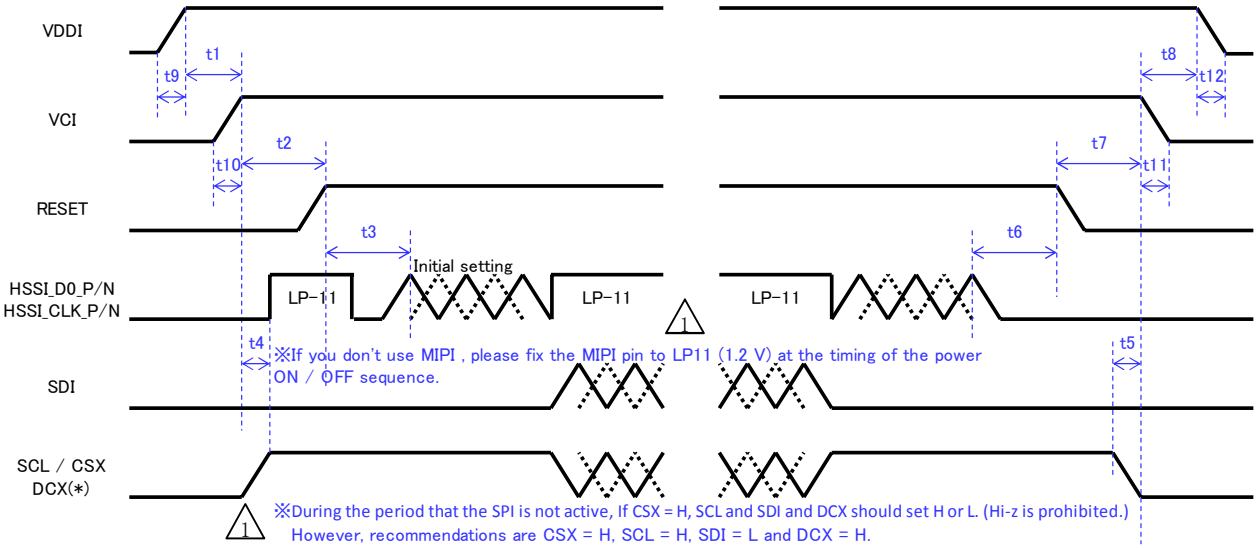
△2

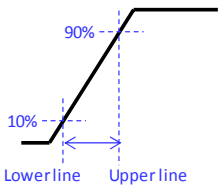
2C/3C command(GRAM access) SPI SPEC

Item	Symbol	Min.	Typ.	Max.	Unit
SCL clock cycle time Write (received)	t SCYCW	16	–	20,000	ns
SCL clock cycle time Read (transmitted)	t SCYCR	280	–	20,000	ns
SCL "High" pulse width Write (received)	t SHW	8	–	–	ns
SCL "High" pulse width Read (transmitted)	t SHR	140	–	–	ns
SCL "Low" pulse width Write (received)	t SLW	8	–	–	ns
SCL "Low" pulse width Read (transmitted)	t SLR	140	–	–	ns
SCL clock rise/fall time	t r , t f	–	–	10	ns
Chip select setup time	t CSS	4	–	–	ns
Chip select hold time	t CSH	12	–	–	ns
Input data setup time	t SDS	5	–	–	ns
Input data hold time	t SDH	5	–	–	ns
DCX to SCL Write setup time	tAST	20	–	–	ns
DCX to SCL Write hold time	tAHT	2	–	–	ns
Output data access time	t ACC	–	–	120	ns
Output data hold time	t OH	5	–	–	ns
Chip deselect "High" pulse width **From GRAM Write(2C/3C) to GRAM Write(2C/3C)**	t CHW	8	–	–	ns
Chip deselect "High" pulse width **From GRAM Write(2C/3C) to command (not 2C/3C)**	t CHW	1000	–	–	ns

5. POWER SEQUENCE

5.1 Power ON/OFF sequence





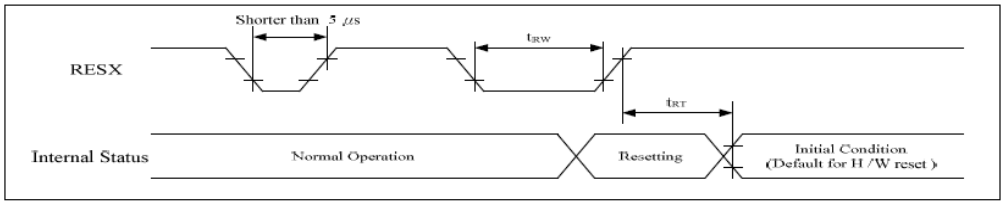
	Min	Typ	Max	unit
t1	0	–	–	ms
t2	10	–	–	ms
t3	10	50	–	ms
t4	0	5	–	ms
t9	–	–	2*	ms
t10	1	–	10	ms

	Min	Typ	Max	unit
t5	0	–	–	ms
t6	10	80	–	ms
t7	0	–	–	ms
t8	0	–	–	ms
t11	1	–	10	ms
t12	–	–	10	ms

Command (HEX)	Address (HEX)
Wait more than 10ms	
FF	E0
28	40
28	0
Wait more than 10ms	
FF	10

*If t9 over than 2ms, please add right command in front of "Initinal setting"

5.2 Reset Timing Characteristics



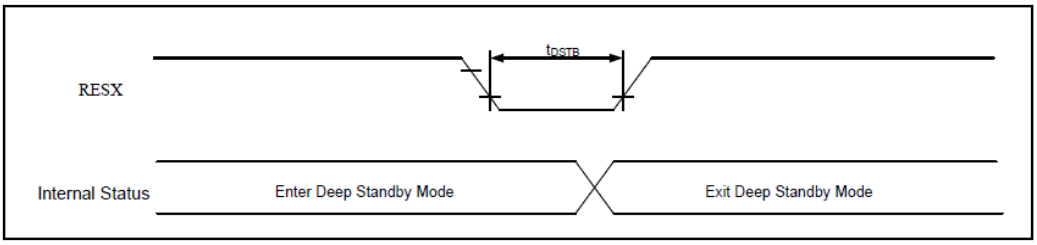


Figure 2. Reset Operation

Signal	Symbol	Parameter	Min.	Max.	Unit
RESX	t_{RW}	Reset pulse duration	10	-	us
	t_{RT}	Reset cancel	-	10 (Note 5)	ms
			-	120 (Note 6)	ms
	tDSTB	Reset pulse duration	3	-	ms

Note :

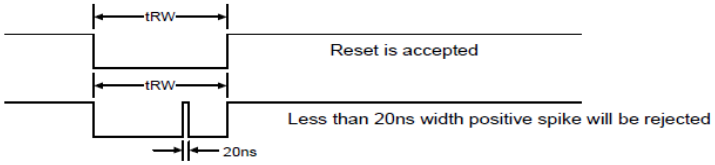
-1. The reset cancel also includes required time for loading ID bytes, VCOM setting and other settings from EEPROM (or similar device) to registers. This loading is done every time when there is HW reset cancel time (tRT) within 10ms after a rising edge of RESX.

-2. Spike due to an electrostatic discharge on RESX line does not cause irregular system reset according to the table below :

RESX	Pulse Action
Shorter than 5us	Reset Rejected
Longer than 9us	Reset
Between 5us and 9us	Reset Starts

-3. During the Resetting period, the display will be blanked(The display is entering blanking sequence, which maximum time is 120 ms, when Reset Starts at Sleep-Out status. The display remains the blank state in Sleep-In mode). Then return to Default condition for Hardware Reset.

-4. Spike Rejection also applies during a valid reset pulse as shown below :

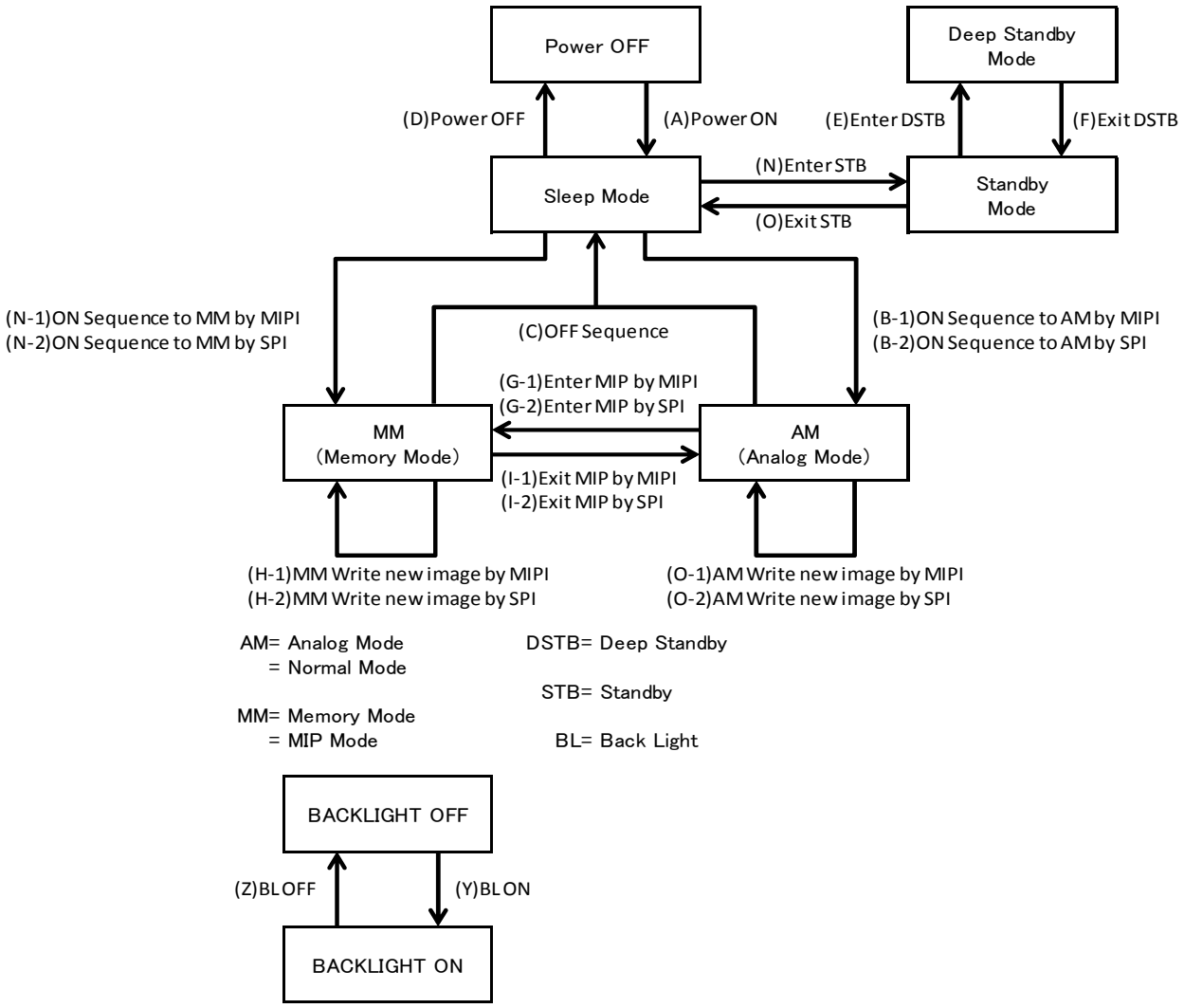


-5. When Reset applied during Sleep-In Mode.

-6. When Reset applied during Sleep-Out Mode.

6. CHANGE STATUS

6.1 Status flow



6.1.1 Sequence 1 (A,B-1,B-2,N-1,N-2)

(A)Power ON

Write/ Read	DCS/ Generic	Data Type (HEX)	Para. Num. (DEC)	Command address (HEX)	Parameter value (HEX)	Description
Pwer OFF						
Power supply on VDDI						DSI input should be at GND level while VDDI/VCI off.
Wait more than 0ms						
Power supply on VCI						DSI input should be at GND level while VDDI/VCI off.
Wait more than 5ms						
Set MIPI-DSI to LP-11, SPI to halt state						Refer to "Power ON_OFF sequence"
Wait more than 10ms						
Hard Reset L=>H						
Wait more than 50ms						
Sleep Mode						

(B-1)ON Sequence to AM by MIPI

Write/ Read	DCS/ Generic	Data Type (HEX)	Para. Num. (DEC)	Command address (HEX)	Parameter value (HEX)	Description
Sleep Mode						
Write	DCS	05	-	01	-	Soft reset
Wait more than 10ms						
Write	DCS	15	1	FB	01	RELOAD cancel
Write	DCS	15	1	3A	06	Set the color format (18bit:06h 16bit:05h)
Write	DCS	05	-	11	-	Sleep out
Wait more than 10ms						
Write	DCS	39	-	2C/3C	-	Transfer image data ※note1,note5
Wait more than 120ms						
Write	DCS	05	-	29	-	Display On ※note2
Analog Mode						

(B-2)ON Sequence to AM by SPI

Write/ Read	DCS/ Generic	Data Type (HEX)	Para. Num. (DEC)	Command address (HEX)	Parameter value (HEX)	Description
Sleep Mode						
Write	-	-	-	01	-	Soft reset
Wait more than 10ms						
Write	-	-	-	FB	01	RELOAD cancel
Write	-	-	-	F3	02	SPI GRAM access enable
Write	-	-	-	3A	06	Set the color format (18bit:06h 16bit:05h)
Write	-	-	-	11	-	Sleep out
Wait more than 10ms						
Write	-	-	-	2C/3C	-	Transfer image data ※note1,note6
Wait more than 120ms						
Write	-	-	-	29	-	Display On ※note2
Write	-	-	-	BB	00	
Analog Mode						

(N-1)ON Sequence to MM by MIPI

Write/ Read	DCS/ Generic	Data Type (HEX)	Para. Num. (DEC)	Command address (HEX)	Parameter value (HEX)	Description
Sleep Mode						
Write	DCS	05	-	01	-	Soft reset
Wait more than 10ms						
Write	GenericSP	23	1	FF	20	
Write	DCS	15	1	FB	01	
Write	GenericSP	23	1	6D	74	
Write	DCS	15	1	FF	10	
Write	DCS	15	1	FB	01	
Write	DCS	15	1	B3	15	
Write	DCS	15	1	BB	10	
Write	DCS	15	1	3A	06	Set the color format (18bit:06h 16bit:05h)
Write	DCS	05	-	11	-	Sleep out
Wait more than 10ms						
Write	DCS	39	-	2C/3C	-	Transfer image data ※note1,note5
Wait more than 120ms						
Write	DCS	05	-	29	-	Display On ※note2
Write	DCS	15	1	BB	00	
Write	DCS	15	1	B3	35	
Write	GenericSP	23	1	FF	20	
Write	GenericSP	23	1	0B	00	
Memory Mode						

(N-2)ON Sequence to MM by SPI

Write/ Read	DCS/ Generic	Data Type (HEX)	Para. Num. (DEC)	Command address (HEX)	Parameter value (HEX)	Description
Sleep Mode						
Write	-	-	-	01	-	Soft reset
Wait more than 10ms						
Write	-	-	-	FF	20	
Write	-	-	-	FB	01	
Write	-	-	-	6D	74	
Write	-	-	-	FF	10	
Write	-	-	-	FB	01	
Write	-	-	-	B3	15	
Write	-	-	-	BB	10	
Write	-	-	-	F3	02	
Write	-	-	-	3A	06	Set the color format (18bit:06h 16bit:05h 3bit_Type1:01h 3bit_Type2:09h , Refer to datasheet.)
Write	-	-	-	11	-	Sleep out
Wait more than 10ms						
Write	-	-	-	2C/3C	-	Transfer image data ※note1,note6
Wait more than 120ms						
Write	-	-	-	29	-	Display On ※note2
Write	-	-	-	BB	00	
Write	-	-	-	B3	35	
Write	-	-	-	FF	20	
Write	-	-	-	0B	00	
Memory Mode						

6.1.2 Sequence 2 (C,D,E,F,L,M,N,O,Y,Z)

(C)OFF Sequence

Write/ Read	DCS/ Generic	Data Type (HEX)	Para. Num. (DEC)	Command address (HEX)	Parameter value (HEX)	Description
Analog Mode						
Write	-	-	-	FF	10	Select CMD1 (If already setted CMD1, skip this command)
Write	DCS	05	-	28	-	Display Off
Wait more than 20ms						
Write	DCS	05	-	10	-	Sleep In
Wait more than 100ms						
Sleep Mode						

(D)Power OFF

Write/ Read	DCS/ Generic	Data Type (HEX)	Para. Num. (DEC)	Command address (HEX)	Parameter value (HEX)	Description
Sleep Mode						
Hard Reset H=>L						
Power supply off VCI						
Power supply off VDDI						DSI input should be at GND level while VDDI off.
Pwer OFF						

(E)Enter DSTB

Write/ Read	DCS/ Generic	Data Type (HEX)	Para. Num. (DEC)	Command address (HEX)	Parameter value (HEX)	Description
Sleep Mode						
Write	DCS	15	1	4F	01	Enter DSTB
Set MIPI-DSI to ULPM, SPI to halt state						
Deep Standby Mode						

(F)Exit DSTB

Write/ Read	DCS/ Generic	Data Type (HEX)	Para. Num. (DEC)	Command address (HEX)	Parameter value (HEX)	Description
Deep Standby Mode						
Wait more than 10ms						
Hard Reset H=>L						
Wait more than 3ms						
Hard Reset L=>H						
Wait more than 50ms						
Set MIPI-DSI to LP-11, SPI to halt state						
Sleep Mode						

(N)Enter STB

Write/ Read	DCS/ Generic	Data Type (HEX)	Para. Num. (DEC)	Command address (HEX)	Parameter value (HEX)	Description
Sleep Mode						
Power supply off VCI						
Standby Mode						

(O)Exit STB

Write/ Read	DCS/ Generic	Data Type (HEX)	Para. Num. (DEC)	Command address (HEX)	Parameter value (HEX)	Description
Standby Mode						
Power supply on VCI						
Sleep Mode						

(Y)BL ON

Write/ Read	DCS/ Generic	Data Type (HEX)	Para. Num. (DEC)	Command address (HEX)	Parameter value (HEX)	Description
Analog Mode						
Write	DCS	15	1	FF	10	Select CMD1 (If already setted CMD1, skip this command)
Write	DCS	15	1	53	24	BACKLIGHT ON
Write	DCS	15	1	51	xx	LEDPWMduty setting(00h:0% ~ FFh:100%)

(Z)BL OFF

Write/ Read	DCS/ Generic	Data Type (HEX)	Para. Num. (DEC)	Command address (HEX)	Parameter value (HEX)	Description
Analog Mode						
Write	DCS	15	1	FF	10	Select CMD1 (If already setted CMD1, skip this command)
Write	DCS	15	1	53	00	BACKLIGHT OFF

6.1.3 Sequence 3 (G-1,G-2,O-1,O-2)

(G-1)Enter MIP by MIPI

Write/ Read	DCS/ Generic	Data Type (HEX)	Para. Num. (DEC)	Command address (HEX)	Parameter value (HEX)	Description
Analog Mode						
Write	DCS	15	1	FF	10	Select CMD1 (If already setted CMD1, skip this command)
Write	DCS	15	1	BB	10	
Write	DCS	15	1	F3	00	MIPI GRAM access enable
Write	DCS	15	1	3A	06	Set the color format (18bit:06h 16bit:05h)
Write	DCS	39	1	2A	00	Set X-direction display address
			2		00	
			3		01	
			4		3F	
Write	DCS	39	1	2B	00	Set Y-direction display address
			2		00	
			3		01	
			4		2B	
Write	GenericSP	23	1	FF	20	
Write	GenericSP	23	1	6D	74	
Write	DCS	15	1	FF	10	
Write	DCS	15	1	B3	15	
Wait more than 50ms						
Write	DCS	39	-	2C/3C	-	Transfer image data ※note1,note5
Write	DCS	15	1	BB	00	
Write	DCS	15	1	B3	35	
Write	GenericSP	23	1	FF	20	
Write	GenericSP	23	1	0B	00	
Memory Mode						

It can set the range of partial update area.

(G-2)Enter MIP by SPI

Write/ Read	DCS/ Generic	Data Type (HEX)	Para. Num. (DEC)	Command address (HEX)	Parameter value (HEX)	Description
Analog Mode						
Write	-	-	-	FF	10	Select CMD1 (If already setted CMD1, skip this command)
Write	-	-	-	BB	10	
Write	-	-	-	F3	02	SPI GRAM access enable
Write	-	-	-	3A	09	Set the color format (18bit:06h 16bit:05h 3bit_Type1:01h 3bit_Type2:09h , Refer to datasheet.)
Write	-	-	1	2A	00	Set X-direction display address
			2		00	
			3		01	
			4		3F	
Write	-	-	1	2B	00	Set Y-direction display address
			2		00	
			3		01	
			4		2B	
Write	-	-	-	FF	20	
Write	-	-	-	6D	74	
Write	-	-	-	FF	10	
Write	-	-	-	B3	15	
Wait more than 50ms						
Write	-	-	-	2C/3C	-	Transfer image data ※note1,note6
Wait more than 1us						
Write	-	-	-	BB	00	
Write	-	-	-	B3	35	
Write	-	-	-	FF	20	
Write	-	-	-	0B	00	
Memory Mode						

It can set the range of partial update area.

(O-1)AM Write new image by MIPI

Write/ Read	DCS/ Generic	Data Type (HEX)	Para. Num. (DEC)	Command address (HEX)	Parameter value (HEX)	Description
Analog Mode						
Write	DCS	15	1	FF	10	Select CMD1 (If already setted CMD1, skip this command)
Write	DCS	15	1	3A	06	Set the color format (18bit:06h 16bit:05h)
Write	DCS	39	1	2A	00	Set X-direction display address
			2		00	
			3		01	
			4		3F	
Write	DCS	39	1	2B	00	Set Y-direction display address
			2		00	
			3		01	
			4		2B	
Write	DCS	39	-	2C/3C	-	Transfer image data ※note1,note5
Analog Mode						

It can set the range of partial update area.

(O-2)AM Write new image by SPI

Write/ Read	DCS/ Generic	Data Type (HEX)	Para. Num. (DEC)	Command address (HEX)	Parameter value (HEX)	Description
Analog Mode						
Write	-	-	-	FF	10	Select CMD1 (If already setted CMD1, skip this command)
Write	-	-	-	BB	10	
Write	-	-	-	F3	02	SPI GRAM access enable
Write	-	-	-	3A	06	Set the color format (18bit:06h 16bit:05h)
Write	-	-	-	2A	00	Set X-direction display address
					00	
					01	
					3F	
Write	-	-	-	2B	00	Set Y-direction display address
					00	
					01	
					2B	
Write	-	-	-	2C/3C	-	Transfer image data ※note1,note6
Wait more than 1us						
Write	-	-	-	BB	00	
Analog Mode						

It can set the range of partial update area.

6.1.4 Sequence 4 (H-1,H-2,I-1,I-2) 2

(H-1)MM Write new image by MIPI(※note3)

Write/ Read	DCS/ Generic	Data Type (HEX)	Para. Num. (DEC)	Command address (HEX)	Parameter value (HEX)	Description
Memory Mode						
Write	DCS	15	1	FF	10	Select CMD1 (If already setted CMD1, skip this command)
Write	DCS	15	1	BB	10	
Write	DCS	15	1	3A	06	Set the color format (18bit:06h 16bit:05h)
Write	DCS	39	1	2A	00	Set X-direction display address
			2		00	
			3		01	
			4		3F	
Write	DCS	39	1	2B	00	Set Y-direction display address
			2		00	
			3		01	
			4		2B	
Write	DCS	39	-	2C/3C	-	Transfer image data ※note1,note5 2
Write	DCS	15	1	BB	00	
Write	DCS	15	1	B3	35	
Memory Mode						

It can set the range of partial update area.

(H-2)MM Write new image by SPI(※note3)

Write/ Read	DCS/ Generic	Data Type (HEX)	Para. Num. (DEC)	Command address (HEX)	Parameter value (HEX)	Description
Memory Mode						
Write	-	-	-	FF	10	Select CMD1 (If already setted CMD1, skip this command)
Write	-	-	-	BB	10	
Write	-	-	-	F3	02	SPI GRAM access enable 2
Write	-	-	-	3A	09	Set the color format (18bit:06h 16bit:05h 3bit_Type1:01h 3bit_Type2:09h , Refer to datasheet.)
Write	-	-	-	2A	00	Set X-direction display address
					00	
					01	
					3F	
Write	-	-	-	2B	00	Set Y-direction display address
					00	
					01	
					2B	
Write	-	-	-	2C/3C	-	Transfer image data ※note1,note6 2
Wait more than 1us 2						
Write	-	-	-	BB	00	
Write	-	-	-	B3	35	
Memory Mode						

It can set the range of partial update area.

(I-1)Exit MIP by MIPI

Write/ Read	DCS/ Generic	Data Type (HEX)	Para. Num. (DEC)	Command address (HEX)	Parameter value (HEX)	Description
Memory Mode						
Write	DCS	15	1	FF	10	Select CMD1 (If already setted CMD1, skip this command)
Write	DCS	15	1	BB	10	
Write	DCS	15	1	F3	00	MIPI GRAM access enable
Write	DCS	15	1	3A	06	Set the color format (18bit:06h 16bit:05h)
Write	DCS	39	1	2A	00	Set X-direction display address
			2		00	
			3		01	
			4		3F	
Write	DCS	39	1	2B	00	Set Y-direction display address
			2		00	
			3		01	
			4		2B	
Write	DCS	39	-	2C/3C	-	Transfer image data ※note1,note4,note5 2
2 Write	GenericSP	23	1	FF	20	
Write	GenericSP	23	1	0B	88	
Write	DCS	15	1	FF	10	
Write	DCS	15	1	B3	02	
Analog Mode						

(I-2)Exit MIP by SPI

Write/ Read	DCS/ Generic	Data Type (HEX)	Para. Num. (DEC)	Command address (HEX)	Parameter value (HEX)	Description
Memory Mode						
Write	-	-	-	FF	10	Select CMD1 (If already setted CMD1, skip this command)
Write	-	-	-	F3	02	SPI GRAM access enable
Write	-	-	-	BB	10	
Write	-	-	-	3A	06	Set the color format (18bit:06h 16bit:05h)
Write	-	-	-	2A	00	Set X-direction display address
					00	
					01	
					3F	
Write	-	-	-	2B	00	Set Y-direction display address
					00	
					01	
					2B	
Write	-	-	-	2C/3C	-	Transfer image data ※note1,note4,note6 2
Wait more than 1us 2						
Write	-	-	-	BB	00	
2 Write	-	-	-	FF	20	
Write	-	-	-	0B	88	
Write	-	-	-	FF	10	
Write	-	-	-	B3	02	
Analog Mode						

note1 : If the communication is interrupted during transmission of the 2Ch/3Ch command, please re-send 2Ch/3Ch command from the beginning of the frame

【example】

・18bit/16bit mode

2Ch(ADD), xxh(data),…,xxh(data) ⇒ Data is transmitted for 320 pixels. (1st line)

3Ch(ADD), xxh(data),…,xxh(data) ⇒ Data is transmitted for 320 pixels. (2nd line)

(repeat 3Ch command)

3Ch(ADD), xxh(data),…,xxh(data) ⇒ Data is transmitted for 320 pixels. (300th line)

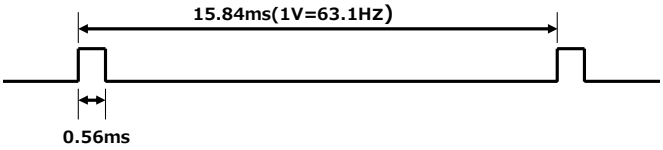
・RGB1-1-1 mode (RGB 1-1-1-bits is only supported on 3-Wire mode 9-bit SPI interface.)

2Ch(ADD), xxh(data),…,xxh(data) ⇒ Data is transmitted for 320 x 300 pixels. (1frame data)

△2

note2 : After Display on, TE signal is output. Timing is as belows.

TE : Frequency 15.84ms(1V=63.1Hz)、H width 0.56ms

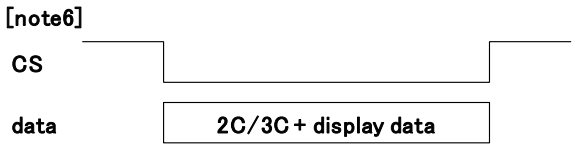


note3 MM Write new image updating cycle ≧ 1sec

△2 note4 When switching from (AM to MM) or (MM to AM), please update the display image data with RGB format suitable for each mode.
The display image to be updated at AM is sent with RGB 666 or RGB 656 format. Be careful if you are using RGB 111 at MM.

△2 note5 When using MIPI I/F, For the 2C / 3C command, it must be used the High speed mode,
and for the other commands, it must be used the Low Power mode.

△2 note6 When using SPI I/F, about CS=H period, specifications of 2C / 3C command and other commands are different.
Please refer to 25,26page.
The register access can be sent by separating CS by address and data, but when sending 2C / 3C command,
it must be sent all of {2C + data} or {3C + data} with CS = L state.



6.2 ID read address

(CMD1_DAh) : Read ID1

DAh	D7	D6	D5	D4	D3	D2	D1	D0
1st parameter	0	0	Prototype Level		Prototype No.			

◆Prototype Level (2bit)

Prototype Level	Bit
WS	00
ES	01
CS	10
MP	11

◆Prototype Number (2bit)

Prototype No.	Bit
1	0000
2	0001
3	0010
・・・	・・・
14	1101
15	1110
16	1111

7. OPTICAL SPECIFICATION

7.1 OPTICAL CHARACTERISTICS

7.1.1 Reflective mode

*Vcom frequency :60Hz±10%
*VCI=3.1V / VDDI=1.8V
*Analog(Normal) driving mode

Item	Symbol	Temp. (℃)	Rating			Unit	Definition (Measurement setup)	Remark
			Min.	Typ.	Max.			
Contrast	CR	25	10	20	-	-	1	
Response	tr	25	-	3	6	ms	2	Black → White
	td		-	6	10			White → Black
Color Coordinates	Rx	25	-	0.505	-	-	3	
	Ry		-	0.315	-			
	Gx		-	0.300	-			
	Gy		-	0.445	-			
	Bx		-	0.170	-			
	By		-	0.175	-			
	Wx		-	0.315	-			
	Wy		-	0.335	-			
NTSC ratio	-	25	-	23	-	%	4	
Reflectance	-	25	-	21	-	%	-	
Viewing Angle (CR>2)	θL	25	45	60	-	deg.	5	Horizontal
	θR		50	65	-			
	θT		50	65	-			Vertical
	θB		45	60	-			

7.1.2 Transmissive mode

*Vcom frequency :60Hz±10%
*VCI=3.1V / VDDI=1.8V / I_{LED}=20mA
*Analog(Normal) driving mode, White raster

Item	Symbol	Temp. (℃)	Rating			Unit	Definition (Measurement setup)	Remark
			Min.	Typ.	Max.			
Brightness	B	25	-	10	-	cd/㎡		

7.2 DEFINITION AND CONDITION OF OPTICAL CHARACTERISTICS

Definition 1

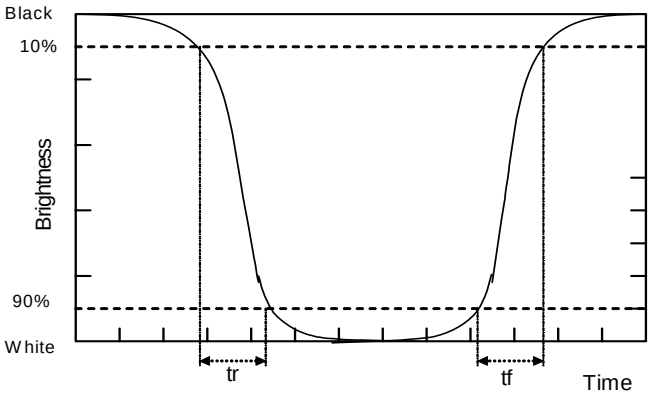
This is a ratio between the screen surface reflectance of the white raster and the black raster

$$\text{Contrast ratio (CR)} = \frac{\text{Reflection intensity on all pixels White}}{\text{Reflection intensity on all pixels Black}}$$

Definition 2

The response time is defined as the following figure and shall be measured by matching the input signal for "Black" and "White".

・Normally Black mode



tr : Response time from Black to White

tf : Response time from White to Black

Definition 3

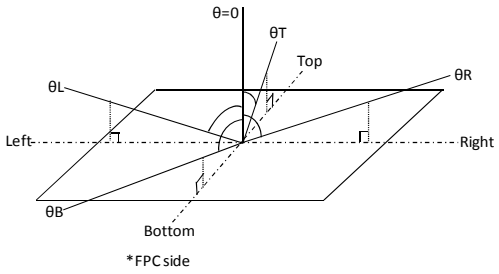
This is the x-y coordinate of Red, Green, Blue and White colors specified on the CIE1931 chromaticity Diagram. (* It is not a guaranteed value)

Definition 4

This is an area of a triangle shaped by R, G, B coordinates on the CIE1931 chromaticity diagram.

Definition 5

This is a maximum angle θ from the normal direction that keeps having the contrast more than 2.



- Measurement method of optical characteristics -

< Basic measurement conditions >

a) Driving voltage

VCI = 3.1V
VDDI= 1.8V

b) Measurement temperature

25° C unless otherwise specified

c) Measurement point

Center of the Active area (one point) unless otherwise specified

< Measurement system-I for reflective mode>

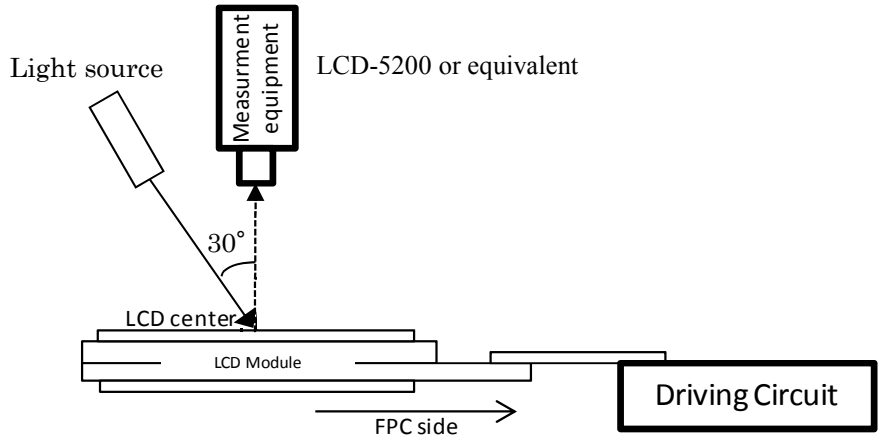
Light source:

Parallel light source

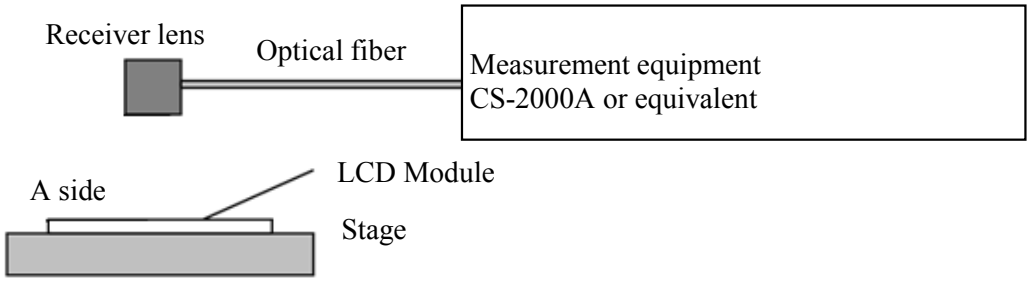
・D65 / 2 degree viewing angle

・Light source input direction : from opposite side of FPC (30°)

・Light source receive direction : at LCD center (0°)



< Measurement system-II for transparent mode>



8. INSPECTION

Please refer to the shipment inspection standard for LPM013M091A ver.02.

9. RELIABILITY TEST

9.1 CONDITIONS OF RELIABILITY AND MECHANICAL TEST

No.	TEST ITEM	CONDITION		REMARK
1	High Temperature Storage	Ta=80℃	240h	
2	Low Temperature Storage	Ta=-30℃	240h	
3	High Temperature & High Humidity Storage	Ta=60℃/90%RH (No condensation)	240h	
4	High Temperature & High Humidity Operation	Ta=40℃/90%RH (No condensation)	240h	
5	High Temperature Operation	Ta=70℃	240h	
6	Low Temperature Operation	Ta=-20℃	240h	
7	Thermal shock (non-operating)	Ta=-30℃ to 80℃ (30min each)	50cycles	
8	ESD	HBM IEC 61340-3-1, ESD STM5.1 V=±1.0kV(contact) R=1.5kΩ,C=100pF	1 time each terminal	
9	Shock	100G,6ms ±X,±Y,±Z	3 times Each direction	
10	Packing Vibration	Random Vibration	101min Direction:Z	
11	Packing Drop	Height 60cm,1 corner 3 edges,6 surfaces	1 time Each direction	

Note)
If a nonconformance is found, both parties will have a discussion to solve it.

9.2 CRITERIA FOR JUDGEMENT

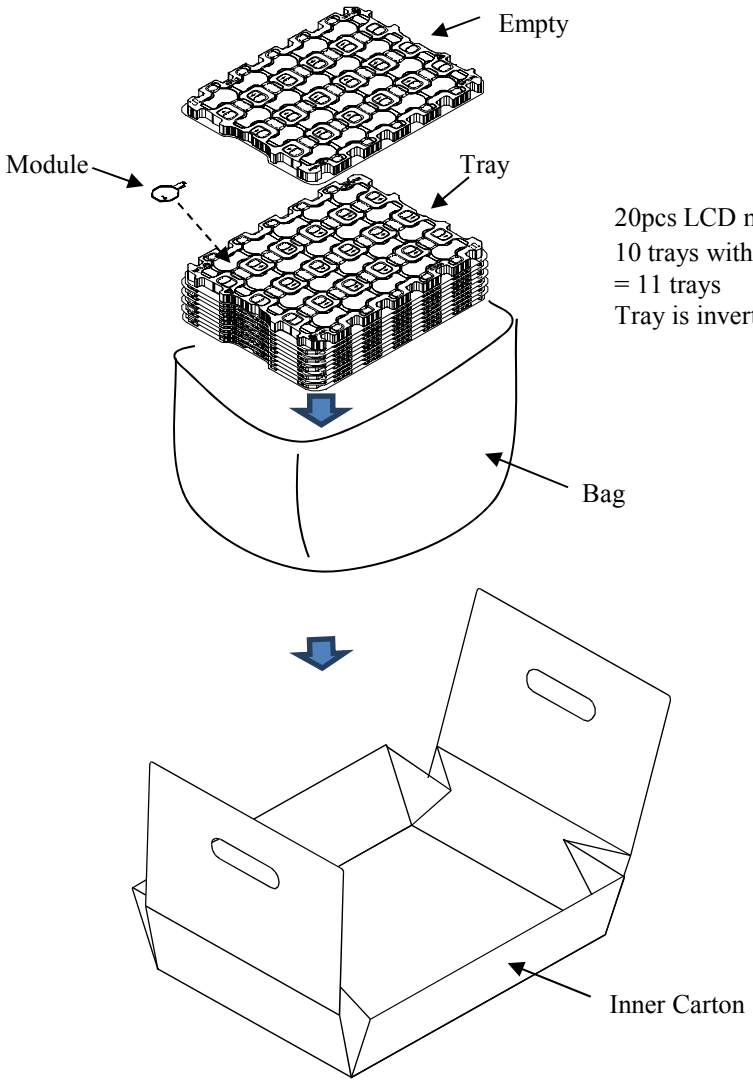
After the above tests, return samples to the normal temperature and moisture environment in the thermostat chamber room over 30 minutes not to condense. Inspect samples kept for more than 1 hour after pulling them out of the thermostat chamber room.

(1) There shall be no abnormality in the functions (Ex. No display, abnormal display, line defects).

(2) There shall be no serious degradation (Ex. Brightness uniformity, reversible changes, optical changes. The degradation due to backlight or polarizer is ignored).

10. PACKING SPECIFICATIONS

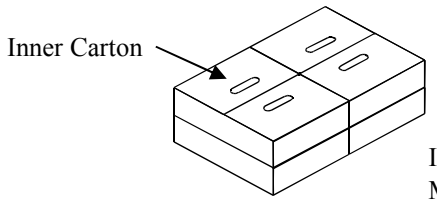
10.1 INNER CARTON



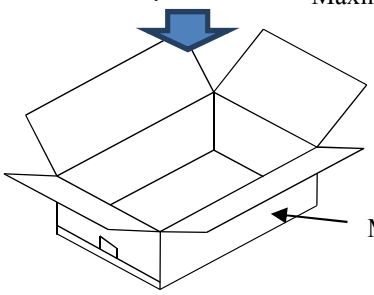
20pcs LCD modules per tray
10 trays with products + empty tray as cover
= 11 trays
Tray is inverted 180 degrees and piled up.

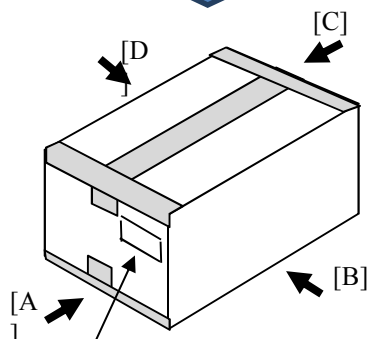
Note)
Tray orientation must be alternately arranged.
If you do not stack trays alternately, it will lead to panel damaged.

10.2 MASTER CARTON



Insert four (4) inner cartons within a master carton.
Maximum quantity per a master carton : 20 × 10 × 4 = 800pcs

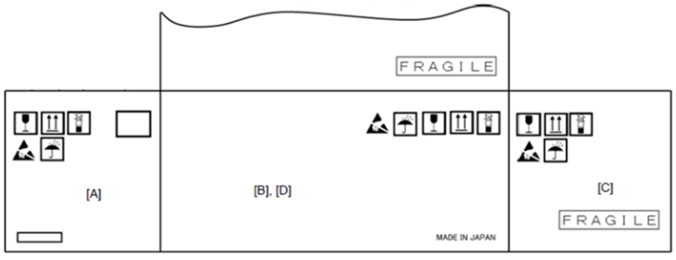




(Notes)
Master carton size : W395 × L596 ×H223 (mm).
Gap is filled if necessary.
Tape is applied if necessary.
Tied if necessary.

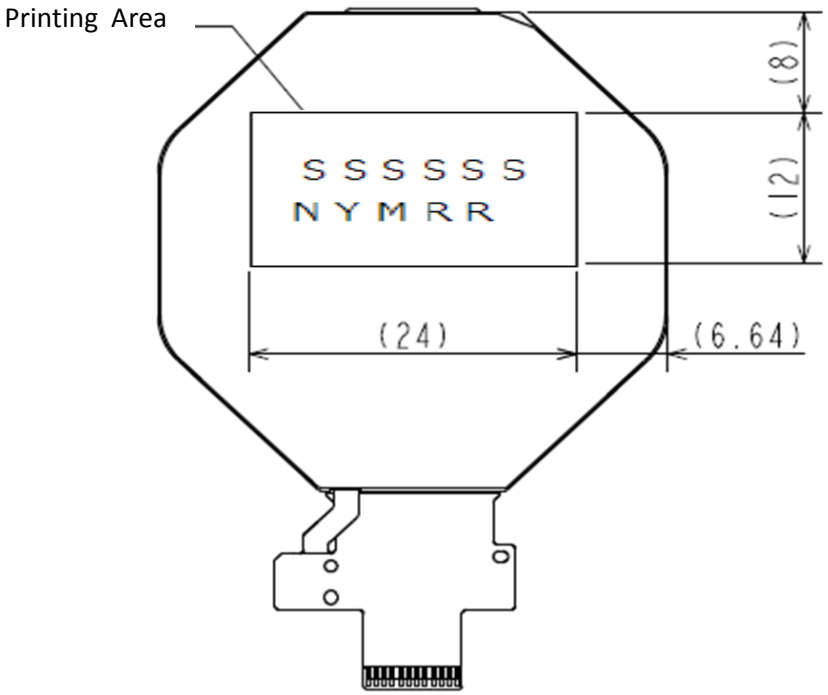
≪Outer label≫

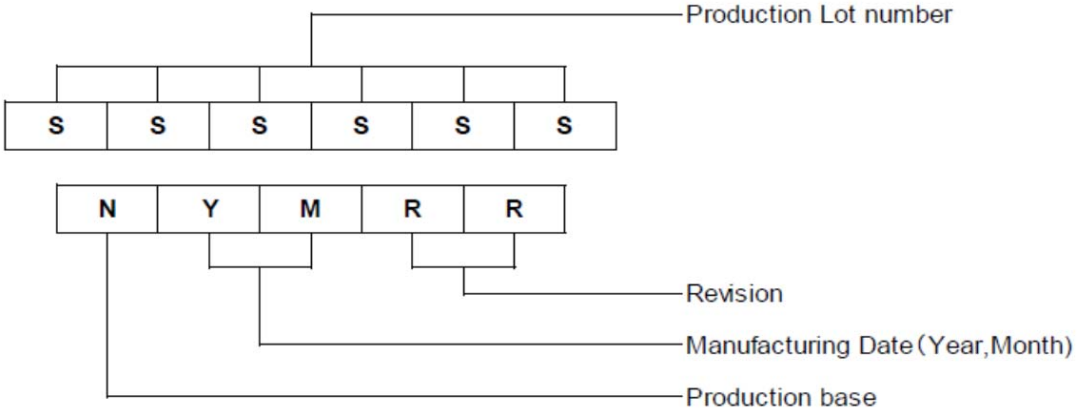
Indication onto [A] [B] [C] [D] on master carton are shown as below.



11. DESIGNATION OF LOT MARK

Lot mark is printed on the rear of the LCD module.





Year	Figure in lot mark
2017	7
2018	8
2019	9
2020	0
2021	1

Month	Figure in lot mark	Month	Figure in lot mark
Jan.	A	Jul.	G
Feb.	B	Aug.	H
Mar.	C	Sep.	I
Apr.	D	Oct.	J
May	E	Nov.	K
Jun.	F	Dec.	L

12. LCD MODULE USAGE AND PRECAUTIONS

12.1 HANDLING

(1) The display panel is made of glass. Do not subject it to mechanical shock such as dropping it from a high position, etc.
(2) If the display panel is damaged and internal liquid crystal substance leaks out, be sure not to inhale or consume it. If the internal liquid crystal substance comes into contact with skin or clothing, promptly wash it off using soap and running water.
(3) Do not apply excessive force on the surface, perimeter or adjoining areas of LCD module since this may cause display panel color tone to vary.
(4) The polarizer covering the display panel surface of the LCD module is soft and can be easily scratched. Handle the LCD module carefully.
(5) If the surface polarizer becomes contaminated, use the following recommended or equivalent adhesive tape for contaminants removal.
• Scotch-brand mending tape (No. 810)
(6) Do not breathe on the display surface or use solvents such as Ethyl Alcohol to remove contaminants. Those may cause polarizer discoloration. Additionally, the following liquids can damage the polarizer.
• Water
• Ketones
• Aromatic solvents
(7) When mounting the LCD Module, be sure that it is free from twisting, warping, or distortion. Any stress can bring great influence on the display quality. Be sure to secure sufficient stiffness on the outer case and the frame for a robust design.
(8) Do not apply pressure at or around the FPC bonding area and the surrounding area.
(9) Do not attempt to disassemble or rework the LCD module.
(10) To prevent destruction of the elements by static electricity, be careful to maintain an optimum working environment.
• Be sure to ground your body before handling the LCD module.
• Make sure that solder guns and all other tools required for assembly have been grounded.
• To reduce occurrence of static electricity, avoid using this product in dry environments.
• A protective film has been attached to the surface of the LCD panel. When peeling off the protective film, be careful to prevent electrostatic discharges.
(11) To minimize performance degradation of the LCD module caused by destructive forces such as static electricity, etc., avoid direct contact to the following sections when handling the LCD module.
• Terminal electrodes of connector
• Wiring pattern on FPC
(12) The protective film attached on the LCD panel must be removed before final product installation. After removal of protective film, some adhesive residues may be left on the LCD panel, especially after a long storage period. Please refer to section (5) listed above for proper contaminant removal procedure.
(13) Take precaution to minimize corrosion of electrodes. Corrosion of electrodes is accelerated by moisture, condensation or a current flow in a high-humidity environment.
(14) Do not apply excessive pressure to the FPC part. Force type such as twist, warp, etc., may cause FPC patterning damage and/or peeling FPC.
(15) Keep the LCD module away from rigid objects such as a tool. Don't put any heavy object on the display surface. Don't stack or pile up the LCD modules. As the polarizer material tends to be easily scratched, the LCD module must be handled with due care to avoid being touched, pressed or rubbed with any rigid object.

(16) Do not touch or handle the LCD module directly with bare hands. Residue of dirt, oil or water may have the possibility to cause corrosion. Be sure to wear finger sacks or gloves when handling LCD modules. When holding an LCD panel module, carefully hold the panel by the edges of the glass plate.
(17) Avoid using LCD module under condensation or high humidity environment because polarizer etc. maybe damaged in these conditions.
(18) Trays are used to package LCD modules for shipment. If LCD modules scratch the tray during shipment, material of the scratched tray may be left on LCD modules. In such case, clean up LCD modules after removal from trays.
(19) When installing LCD module, don't apply excess stress of bending or stretching to the input cable (FPC).
(20) Keep NC terminals open electrically unless otherwise specified.
(21) After storage under high humidity or condensation environment, keep LCD module under room temperature more than 30 minutes before operation.
(22) Take precautions to handle LCD module because the glass plate has very keen edges.

12.2 DESIGN OF APPLICATION

(1) The absolute maximum ratings represent the rated values which LCD module cannot exceed. When LCD modules are used beyond these rated values, the operating characteristics may be adversely affected.
(2) To prevent the occurrence of erroneous operation caused by noise, special attention on satisfying VIL, VIH specified values is required. This includes taking the precautionary measures of using short cables for signal transferring.
(3) An inherent characteristic of liquid crystal display is its temperature dependency. Be sure to use the LCD modules within the specified operating temperature range. Recognition of the display becomes difficult when the LCD module is used outside its range. Also, keep in mind that the voltage levels necessary for clear display images will vary according to temperature.
(4) It is recommended that power supply lines (V_SYS, V_INTERFACE, LED+) include current surge protection. (Fuse etc. recommend value: 0.5A)
(5) Note the peripheral devices can cause mutual noise interference with LCD modules. Especially, input devices such as Touch Panel, etc., may output operational level by radiation noise even when these devices are not in operation. Actual performance confirmation and verification under actual usage environment by actual final product are highly recommended.
(6) To avoid EMI, preventive measures should be implemented for the final product.
(7) Display abnormality may occur with sudden removal of the battery pack. Electric design should be well studied so that sudden electric power interruption will not occur. LCD module quality cannot be guaranteed under the condition that unexpected power shutdown can possibly occur.
(8) Ensure sufficient light shading measures during design phase and then mount the LCD module.
(9) Ensure sufficient light shading measures in the inspection process.
(10) As well as general electronic components, ESD may cause the LCD IC to malfunction. Provide ESD prevention measures entirely around the LCD module.
(11) While display data may be kept, the data can be easily changed by external noise. Noise can be minimized at device or system level.
(12) Unexpected external noise may cause abnormal display and/or IC malfunction. Periodic refresh operation such as resending commands and display data is highly recommended as a part of the software routine.
(13) When logic circuit power is off, do not apply any signals to the input terminals.
(14) As the pressure bonding of the FPC tends to be easily peeled by mechanical stress, never hold the LCD module by the FPC when handling. Additionally, when mounting the LCD Module and/or fixing the FPC, keep them free from twisting or bending. Those may cause wiring pattern breaks and/or bonding separation. Remember not to bend/pull them toward the direction in which the bonding goes separate because there is a high possibility of wiring pattern breaks.

12.3 DISPLAY CHARACTERISTECS

(1) Because the optimum LCD driving voltage depends on the ambient temperature, display may slightly flicker at the environment of high temperature.
(2) One of the special characteristics of liquid crystal is that it freezes when stored at the temperature below the storage temperature range. Such freezing may cause orientation defects or bubbles (black or white) to appear in the LCD panel. Bubbles may also occur if the panel receives an impact in a low-temperature environment.
(3) If the LCD module is left operating for a long time with the same display showing, the displayed pattern may leave traces on the screen or the contrast may become inconsistent. These issues will usually recover in time, but the phenomenon may persist in significant cases.
It is unavoidable with the current technology. The final product must be designed with this property in mind and need to avoid displaying a fixed pattern for a long period. Any afterimage issue is excluded from the LCD Module appearance specifications that we warrant.

12.4 KEEPING

(1) When keeping LCD modules, avoid the following condition or environment.
• Exposure to direct sunlight or fluorescent lamp lighting.
• High-temperature/high-humidity or very low-temperature (below 0° C) environments.
• Exposure to water droplets, condensation, etc.
Furthermore, keep LCD modules in anti-static bags to prevent static electricity charge ups. Whenever possible, LCD modules should be stored in the same conditions in which they were shipped from Japan Display Inc.
(2) Take precaution to minimize corrosion of electrodes. Corrosion of electrodes is accelerated by moisture, condensation or a current flow in a high-humidity environment.
(3) Recommended keeping conditions.
• Keeping environment : +15° C to 35° C, less than 65%RH
• Duration: up to 2 months after shipping date
(4) Excessive load can damage or destroy the carton boxes. Please follow the printed instruction on the carton for maximum number of stacks of cartons for both storage and transportation.

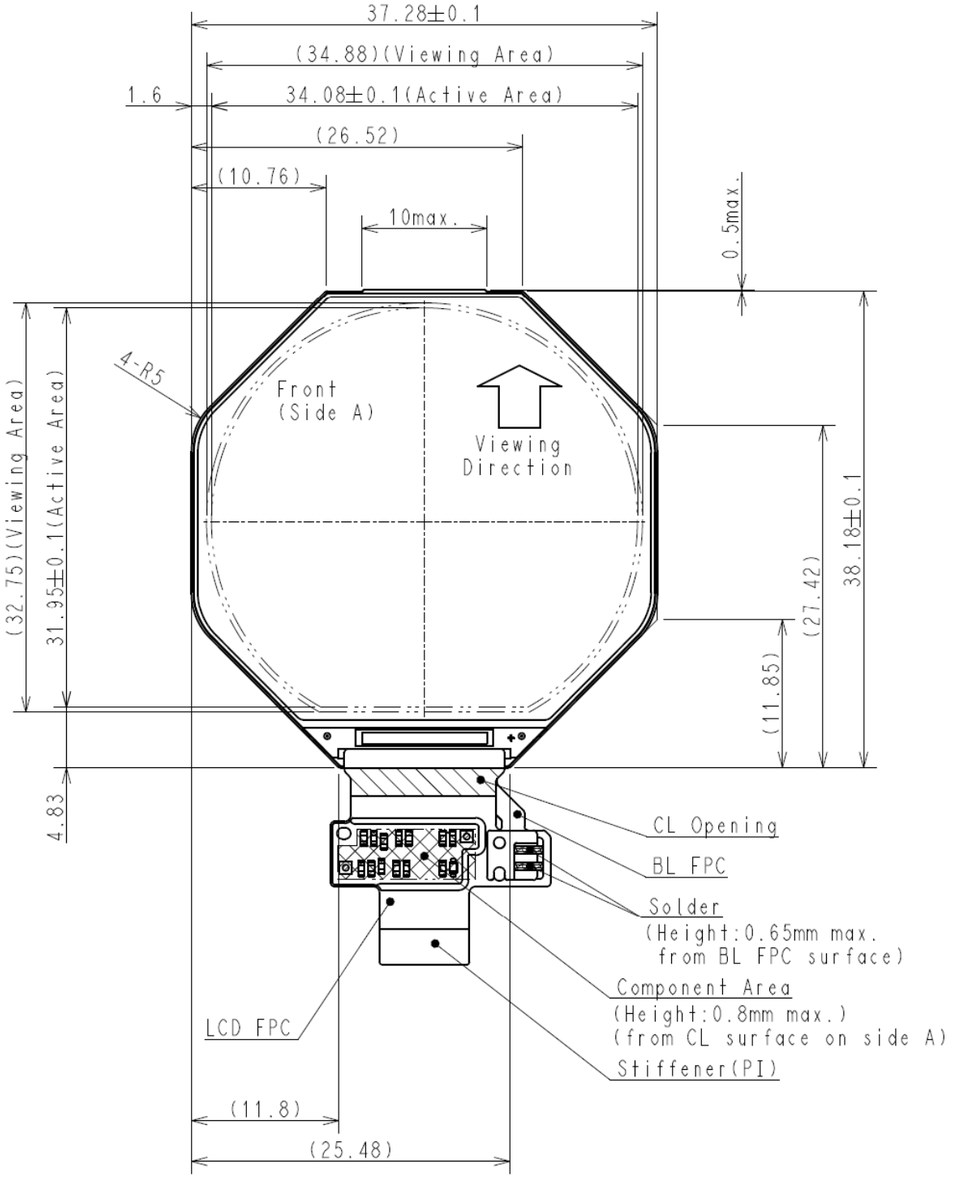
12.5 DISPOSAL

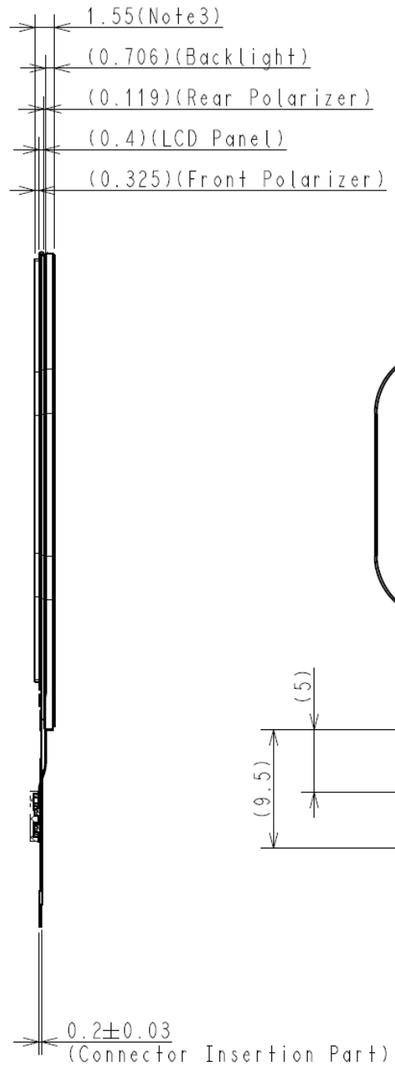
(1) Abide by national laws, legislation and local regulations when disposing of this LCD module.
(2) Consult a company specialized in industrial waste treatment which is permitted by the government or local authority. When incineration is the method of LCD module disposal, law of environmental hygienic must be obeyed.

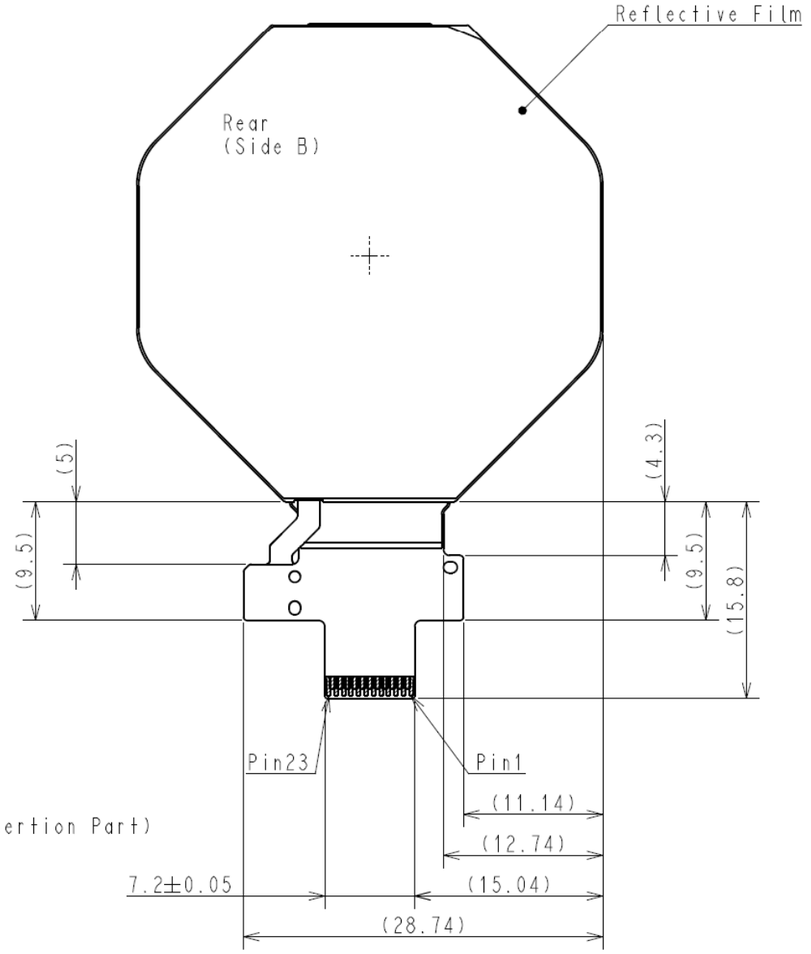
12.6 OTHERS

(1) This product is designed to be used in ordinary electronic devices. Do not use this product in other applications, especially in devices that may directly affect end users (such as weapons, military purposes, aerospace equipment, life-support system equipment, or safety equipment).
(2) Japan Display Inc. shall not be responsible for defects that occur in this product if the product is used in an environment that exceeds the ranges specified in this document, or in an environment not described in this document.

13. OUTLINE DRAWING







No.	I/F Terminal
1	N.C.
2	VCI
3	VDDI
4	GND
5	HSSI_D0_N
6	HSSI_D0_P
7	GND
8	HSSI_CLK_N
9	HSSI_CLK_P
10	GND
11	SDI
12	SCL
13	DCX
14	CSX
15	GND
16	RESX
17	IM0
18	LCD_TEST(GND)
19	LEDPWM
20	TE
21	N.C.
22	LED_A
23	LED_K

Note:
(*13-1)Unit:mm
(*13-2)No specified size tolerance:±0.2
(*13-3)Example of suitable FPC connector : FH35C-23S-0.3SHW(50) 23pin / Hirose
(*13-4)Do not bend FPC around area where mounted components and solder are located, in addtion to around FPC crimping area,
so that these areas on the FPC do not have any stress.
(*13-5)Viewing Direction is the direction to get the best reflective performance.