1.5MHz, 3A Step-down Converter With Soft-Start

General Description

The LP6343 contains a independent 1.5MHz constant frequency, current mode, PWM step-down converters. The converter integrates a main switch and a synchronous rectifier for high efficiency without an external Schottky diode. The LP6343 is ideal for powering portable equipment that runs from a single cell Lithium-Ion (Li+) battery. The converter can supply 3000mA of load current from a 2.5V to 5.5V input voltage. The output voltage can be regulated as low as 0.6V. The LP6343 can also run at 100% duty cycle for low dropout applications.

The LP6343 is available in a 10-lead 3mm*3mm TDFN-10 and EMSOP-10 package and is rated over the -40°C to 85°C temperature range.

Order Information

LP6343□ □ □ □

- F: Pb-Free
- Package Type
  - QV: TDFN-10
  - MS: MSOP-10(E)
- Output type
  - A: Adjustable

Features

- Input Voltage Range: 2.5V to 5.5V
- Output Voltage Range: 0.6V to VIN
- 3000mA Load Current on Channel
- Up to 95% Efficiency
- 100% Duty Cycle in Dropout
- < 1 u A Quiescent Current
- 1.5MHz Switching Frequency
- Soft star Function
- Short Circuit Protection
- Current Mode Operation
- Thermal Fault Protection
- 3 m m × 3 m m TDFN-10 or MSOP-10 Package
- RoHS Compliant and 100% Lead (Pb)-Free

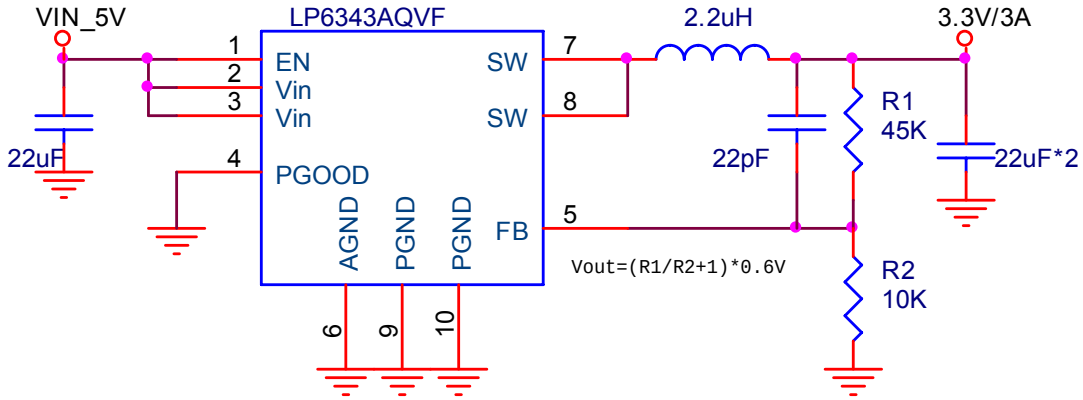
Applications

- Portable Media Players
- Cellular and Smart mobile phone
- PDA/DSC
- GPS Applications

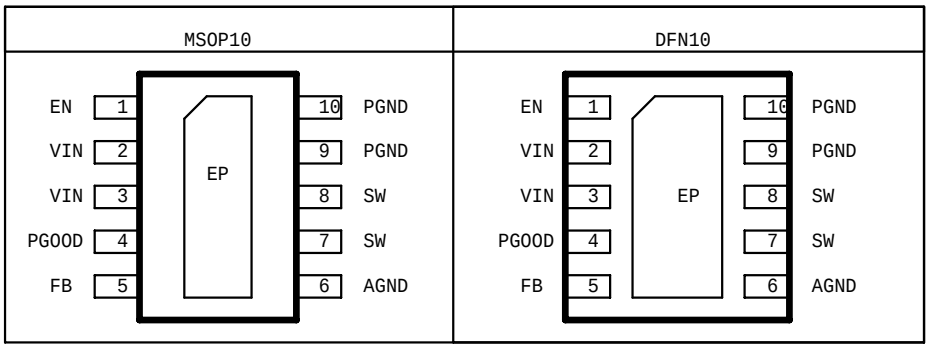
Marking Information

Please see website. www.lowpowersemi.com

Typical Application Circuit



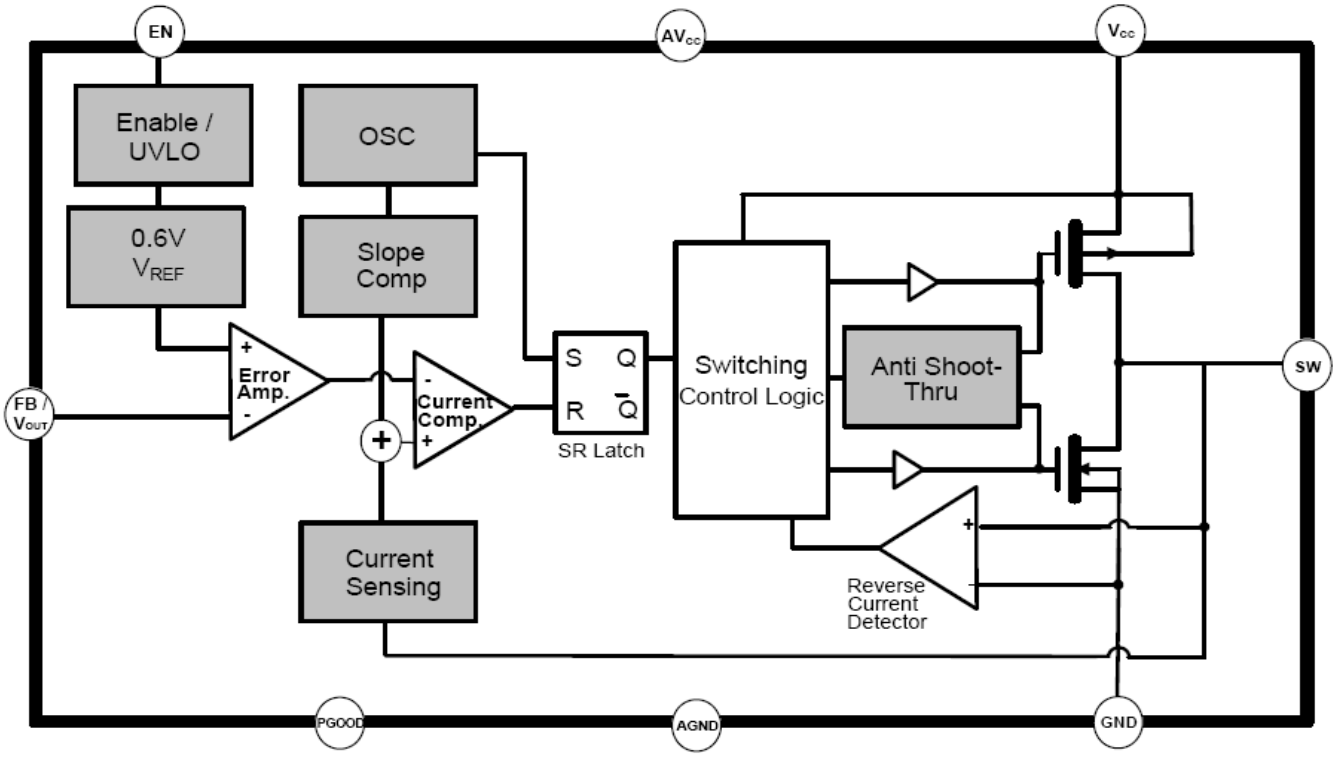
Functional Pin Description



Pin Description

Pin NO	PIN	DESCRIPTION
1	EN	Enable Control Input. Drive EN1 above 1.5V to turn on the Channel. Drive EN below 0.4V to turn it off (shutdown current < 0.1μA).
2, 3	Vin	Supply Input.
4	PGOOD	Power Good Open Drain Output. Connects a 100kΩ pull up resistor between VIN and this pin to obtain a PGOOD voltage. Connect this pin to AGND if not used.
5	FB	Feedback Input. Connect FB to the center point of the external resistor divider. Normal voltage for this pin is 0.6V.
7, 8	SW	Switch Mode Connection to Inductor. This pin connects to the drains of the internal main and synchronous power MOSFET switches.
6,9,10	AGND/PGND	Ground.
11	EP	Exposed PAD - must connect to Ground

Function Block Diagram



Absolute Maximum Ratings

- ✧ Input Voltage to GND ---------- 6V
- ✧ SW to GND (V_{SW}) ---------- 0.3V to V_{IN} +0.3V
- ✧ FB to GND (V_{FB}) ---------- 0.3V to V_{IN} +0.3V
- ✧ EN EN_BAT to GND (V_{EN}) ----------0.3V to 6V
- ✧ Operating Junction Temperature Range (T_J) ----------40℃ to 150℃
- ✧ Maximum Soldering Temperature (at leads, 1 0sec) ----------260℃

Electrical Characteristics

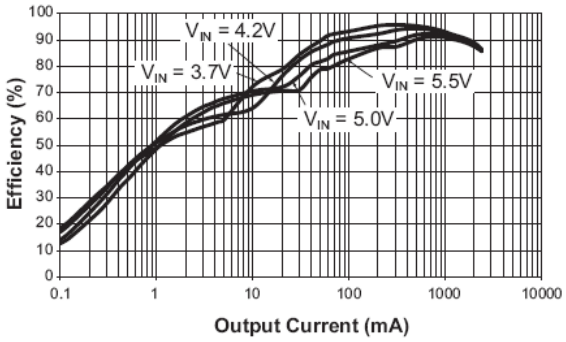
(V_{IN} =V_{EN},Typical values are T_A=25℃)

Symbol	Parameter	Conditions		LP6343		Unit
			Min.	Typ.	Max.	
V_{IN}	Input Voltage		2.5		5.5	V
V_{FB}	Feedback Threshold Voltage Accuracy	V_{FB}, TA=25°C	0.588	0.6	0.612	V
		V_{FB}, TA= -40°C ~+85°C	0.582	0.6	0.618	
△V_{OUT}	Output Voltage Line Regulation	I_{LOAD} = 0 V_{INB} = 2.5V to 5.5V		0.04	0.4	%/V
△V_{FB}	Reference Voltage Line Regulation	V_{INB} = 2.5V to 5.5V		0.04	0.4	%/V
V_{OUT}	Output Voltage Range		0.6		V_{INB}	V
I_Q	Quiescent Current	Active, V_{FB} =0.5V,V_{IN}= V_{EN}		170		µA
		PSM,V_{FB} =0.7V,V_{IN}= V_{EN}		80		µA
I_{SHDN}	Shutdown Current	V_{EN} =0V		1		µA
I_{LIM}	P-Channel Current Limit			3.8		A
I_{PK}	Peak Inductor Current	V_{FB} =0.5V		3.5		A
$R_{DS(ON)H}$	High-Side Switch On Resistance			135		m Ω
$R_{DS(ON)L}$	Low-Side Switch On Resistance			130		m Ω
I_{LXLEAK}	LX Leakage Current	V_{EN}=0V, V_{SW}=0 or 5V, V_{IN}=5V			1	µA
$\Delta V_{Line-reg}/\Delta V_{IN}$	Line Regulation	V_{IN} = 2.8V to 5.5V		0.2	0.4	%/V
I_{FB}	FB Leakage Current	V_{OUT} = 1 .0V		30		nA
FOSC	Oscillator Frequency	V_{FB} =0V	1.2	1.5	1.8	MHz
T_S	Startup Time	From Enable to Output Regulation		120		µs
T_{SD}	Over-Temperature Shutdown Threshold			150		℃
T_{HYS}	Over-Temperature Shutdown Hysteresis			20		℃
$V_{EN(L)}$	Enable Threshold Low				0.4	V
$V_{EN(H)}$	Enable Threshold High		0.3	1.0	1.5	V
I_{EN}	Input Low Current	V_{IN} = V_{EN} = 5.5V	-1		1	µA

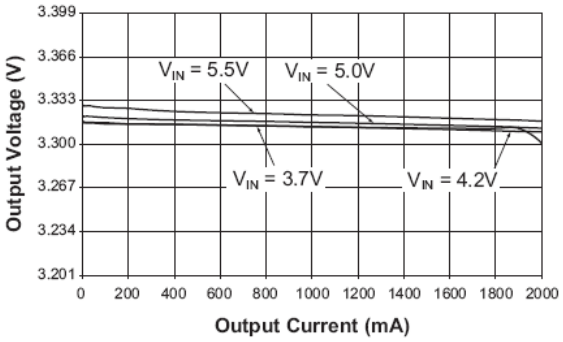
Note: Output Voltage: Vout = 0.6 X (1+R2/R1) Volts;

Typical Operating Characteristics

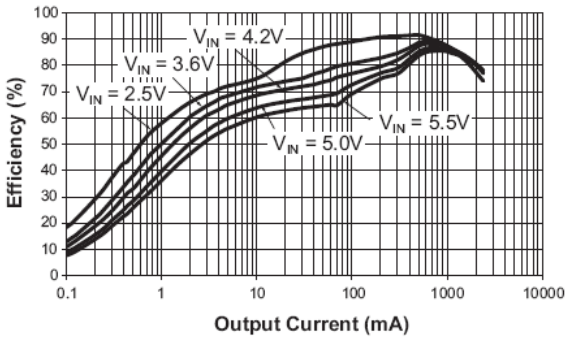
Efficiency vs. Output Current
(V_{OUT} = 3.3V, T_A = 25°C, L = 2.2μH, C_{IN} = C_{OUT} = 22μF)



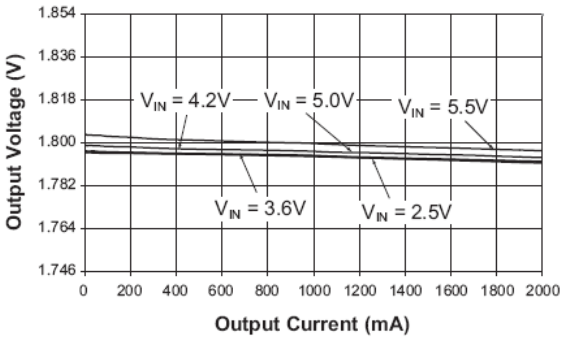
DC Regulation
(V_{OUT} = 3.3V, T_A = 25°C, L = 2.2μH, C_{IN} = C_{OUT} = 22μF)



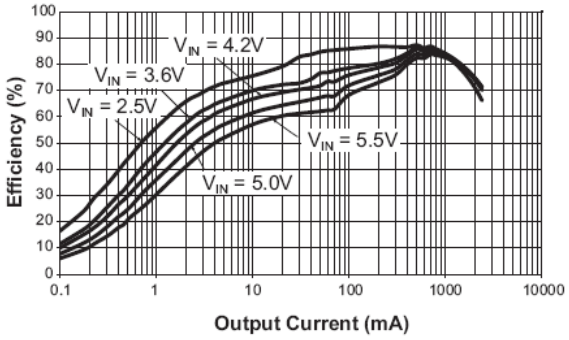
Efficiency vs. Output Current
(V_{OUT} = 1.8V, T_A = 25°C, L = 2.2μH, C_{IN} = C_{OUT} = 22μF)



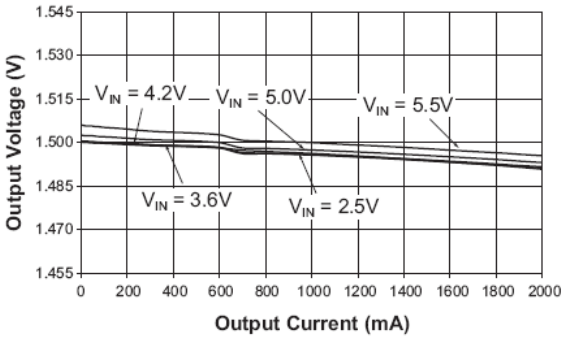
DC Regulation
(V_{OUT} = 1.8V, T_A = 25°C, L = 2.2μH, C_{IN} = C_{OUT} = 22μF)



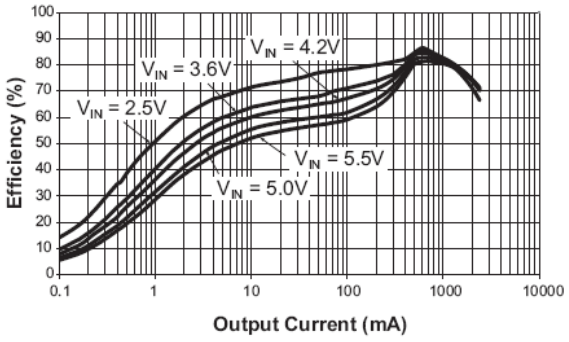
Efficiency vs. Output Current
(V_{OUT} = 1.5V, T_A = 25°C, L = 2.2μH, C_{IN} = C_{OUT} = 22μF)



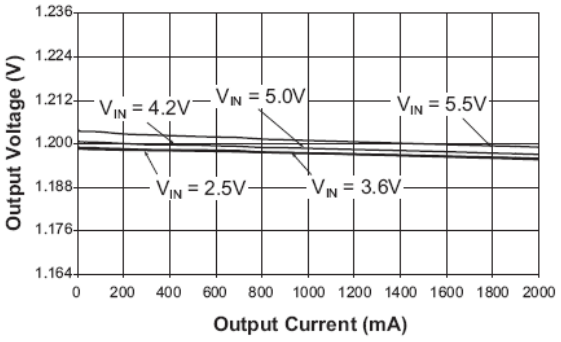
DC Regulation
(V_{OUT} = 1.5V, T_A = 25°C, L = 2.2μH, C_{IN} = C_{OUT} = 22μF)



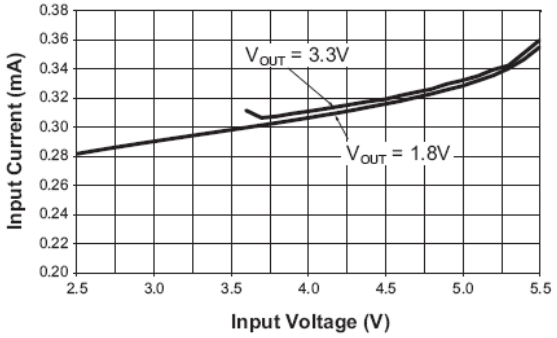
Efficiency vs. Output Current
(V_{OUT} = 1.2V, T_A = 25°C, L = 2.2μH, C_{IN} = C_{OUT} = 22μF)



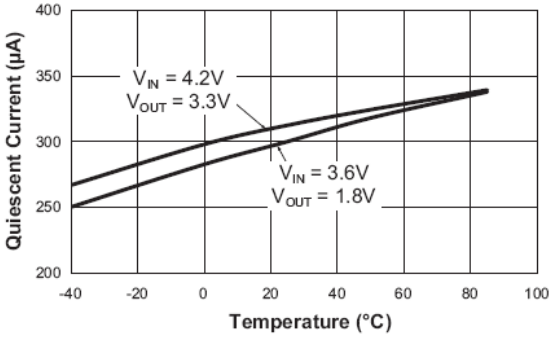
DC Regulation
(V_{OUT} = 1.2V, T_A = 25°C, L = 2.2μH, C_{IN} = C_{OUT} = 22μF)



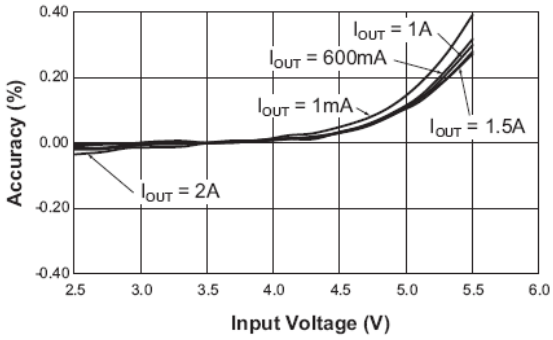
Quiescent Current vs. Input Voltage
(T_A = 25°C, L = 2.2μH, C_{IN} = C_{OUT} = 22μF)



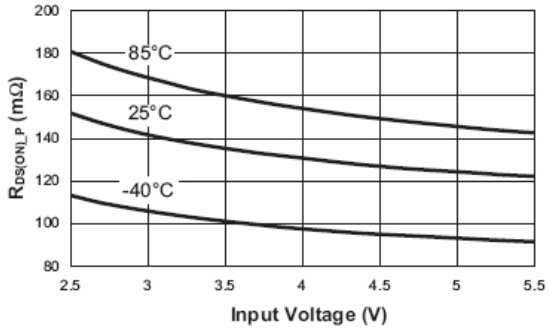
Quiescent Current vs. Temperature
(L = 2.2μH, C_{IN} = C_{OUT} = 22μF)



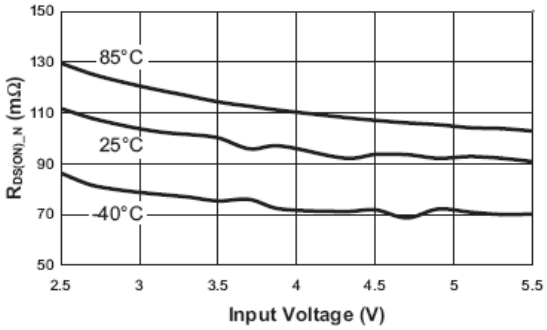
Line Regulation
(V_{OUT} = 1.8V, L = 2.2μH, C_{IN} = C_{OUT} = 22μF)



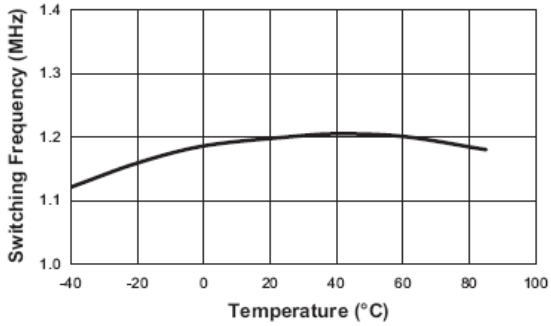
P-Channel $R_{DS(ON)}$ vs. Input Voltage



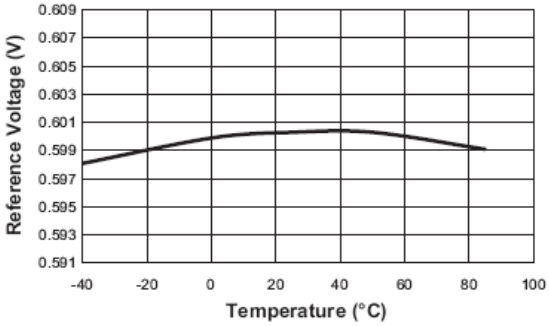
N-Channel $R_{DS(ON)}$ vs. Input Voltage



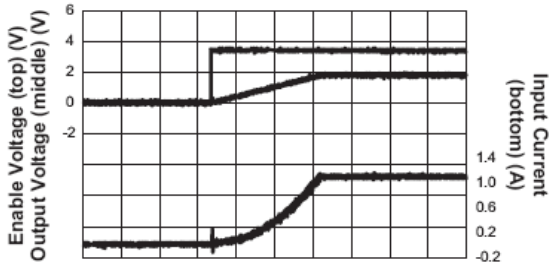
Switching Frequency vs. Temperature
(V_{IN} = 3.6V; V_{OUT} = 1.8V)



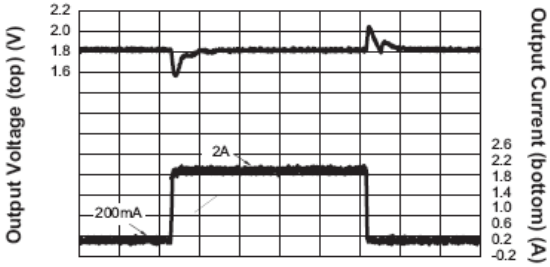
Reference Voltage vs. Temperature
(V_{IN} = 3.6V)

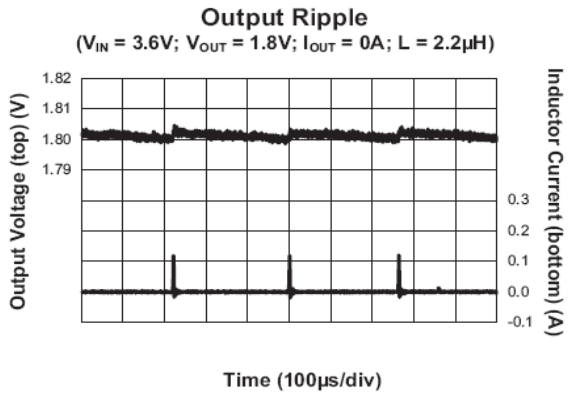


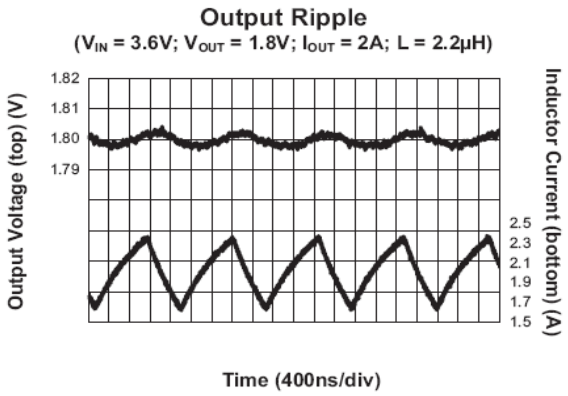
Soft Start
(V_{IN} = 3.6V; V_{OUT} = 1.8V; I_{OUT} = 2A; C_{FF} = 22pF)



Load Transient Response
(V_{IN} = 3.6V; V_{OUT} = 1.8V; L = 2.2μH; C_{IN} = C_{OUT} = 22μF)







Application Information

The LP6343 is a high output current monolithic switch-mode step-down DC-DC converter. The device operates at a fixed 1.2MHz switching frequency, and uses a slope compensated current mode architecture. This step-down DC-DC converter can supply up to 2A output current at VIN = 3V and has an input voltage range from 2.5V to 5.5V. It minimizes external component size and opti-mizes efficiency at the heavy load range. The slope com-pensation allows the device to remain stable over a wider range of inductor values so that smaller values (1µH to 4.7µH) with lower DCR can be used to achieve higher efficiency. Apart from the small bypass input capacitor, only a small L-C filter is required at the output. The device can be programmed with external feedback to any voltage, ranging from 0.6V to near the input volt-age. It uses internal MOSFETs to achieve high efficiency and can generate very low output voltages by using an internal reference of 0.6V. At dropout, the converter duty cycle increases to 100% and the output voltage tracks the input voltage minus the low RDS(ON) drop of the P-channel high-side MOSFET and the inductor DCR. The internal error amplifier and compensation provides excellent transient response, load and line regulation. Internal soft start eliminates any output voltage over-shoot when the enable or the input voltage is applied.

Current Mode PWM Control

Slope compensated current mode PWM control provides stable switching and cycle-by-cycle current limit for excellent load and line response with protection of the internal main switch (P-channel MOSFET) and synchronous rectifier (N-channel MOSFET). During normal operation, the internal P-channel MOSFET is turned on for a specified time to ramp the inductor current at each rising edge of the internal oscillator, and switched off when the peak inductor current is above the error volt-age. The current comparator, ICOMP, limits the peak inductor current. When the main switch is off, the synchronous rectifier turns on immediately and stays on until either the inductor current starts to reverse, as indicated by the current reversal comparator, IZERO, or the beginning of the next clock cycle.

Control Loop

The LP6343 is a peak current mode step-down converter. The current through the P-channel MOSFET (high side) is sensed for current loop control, as well as short circuit and overload protection. A slope compensation signal is added to the sensed current to maintain stability for duty cycles greater than 50%. The peak current mode loop appears as a voltage-programmed current source in parallel with the output capacitor. The output of the voltage error amplifier programs the current mode loop for the necessary peak switch current to force a constant output voltage for all load and line conditions. Internal loop compensation terminates the transconductance voltage error amplifier output. The error amplifier reference is fixed at 0.6V.

Soft Start / Enable

Soft start limits the current surge seen at the input and eliminates output voltage overshoot. The enable pin is active high. When pulled low, the enable input (EN) forces the LP6343 into a low-power, non-switching state. The total input current during shutdown is less than 1µA.

Setting the Output Voltage

Figure 1 shows the basic application circuit for the LP6343. The LP6343 can be externally programmed. Resistors R1 and R2 in Figure 1 program the output to regulate at a voltage higher than 0.6V. To limit the bias current required for the external feedback resistor string while maintaining good noise immunity, the minimum suggested value for R2 is 59kΩ. Although a larger value will further reduce quiescent current, it will also increase the impedance of the feedback node, making it more sensitive to external noise and interference. Table 1 summarizes the resistor values for various output volt-ages with R2 set to either 59kΩ for good noise immunity or 316kΩ for reduced no load input current. The LP6343, combined with an external feed forward capacitor (C3 in Figure 1), delivers enhanced transient response for extreme pulsed load applications. The addition of the feed forward capacitor typically requires a larger output capacitor C2 for stability. The external resistor sets the output voltage according to the following equation:

Vout=0.6 V x (1+R1/R2)

Table 1 shows the resistor selection for different output voltage settings.

Vout(V)	R2=59KΩ R1(KΩ)	R1=316KΩ R2(KΩ)
0.8	19.6	105
0.9	29.4	158
1.0	39.2	210
1.1	49.9	261
1.2	59	316
1.3	68.1	365
1.4	78.7	422
1.5	88.7	475
1.8	118	634
1.85	124	655
2.0	137	732
2.5	187	1000
3.3	267	1430

Table 1: Resistor Selections for Different Output Voltage Settings (Standard 1% Resistors Substituted For Calculated Values).

Inductor Selection

For most designs, the LP6343 operates with inductor values of 1μH to 4.7μH. Low inductance values are physically smaller but require faster switching, which results in some efficiency loss. The inductor value can be derived from the following equation:

$$L = \frac{V_{OUT} \cdot (V_{IN} - V_{OUT})}{V_{IN} \cdot \Delta I_L \cdot f_{OSC}}$$

Where ΔIL is inductor ripple current. Large value inductors lower ripple current and small value inductors result in high ripple currents. Choose inductor ripple current approximately 30% of the maximum load current 2A, or

ΔI_L=600mA

For output voltages above 2.0V, when light-load efficiency is important, the minimum recommended inductor is 2.2μH. Manufacturer's specifications list both the inductor DC current rating, which is a thermal limitation, and the peak current rating, which is determined by the saturation characteristics. The inductor should not show any appreciable saturation under normal load conditions. Some inductors may meet the peak and average current ratings yet result in excessive losses due to a high DCR.

Always consider the losses associated with the DCR and its effect on the total converter efficiency when selecting an inductor. For optimum voltage-positioning load transients, choose an inductor with DC series resistance in the 20mΩ to 100mΩ range. For higher efficiency at heavy loads (above 200mA), or minimal load regulation (but some transient overshoot), the resistance should be kept below 100mΩ. The DC current rating of the inductor should be at least equal to the maximum load current plus half the ripple current to prevent core saturation (2A + 600mA). Table 2 lists some typical surface mount inductors that meet target applications for the LP6343. For example, the 2.2μH CDRH5D16-2R2 inductor selected from Sumida has a 28.7mΩ DCR and a 3.0ADC cur-rent rating. At full load, the inductor DC loss is 57mW which gives a 1.6% loss in efficiency for a 1200mA, 1.8V output.

Slope Compensation

The LP6343 step-down converter uses peak current mode control with slope compensation for stability when duty cycles are greater than 50%. The slope compensation is set to maintain stability with lower value inductors which provide better overall efficiency. The output inductor value must be selected so the inductor current down slope meets the internal slope compensation requirements. As an example, the value of the slope compensation is set to 1A/μs which is large enough to guarantee stability when using a 2.2μH inductor for all output volt-age levels from 0.6V to 3.3V. The worst case external current slope (m) using the 2.2μH inductor is when VOUT = 3.3V and is:

$$m = \frac{V_{OUT}}{L} = \frac{3.3}{2.2} = 1.5A/\mu s$$

To keep the power supply stable when the duty cycle is above 50%, the internal slope compensation (mA) should be:

$$m_a \geq \frac{1}{2} \cdot m = 0.75A/\mu s$$

Therefore, to guarantee current loop stability, the slope of the compensation ramp must be greater than one-half of the down slope of the current waveform. So the internal slope compensated value of 1A/μs will guarantee stability using a 2.2μH inductor value for all output volt-ages from 0.6V to 3.3V.

Input Capacitor Selection

The input capacitor reduces the surge current drawn from the input and switching noise from the device. The input capacitor impedance at the switching frequency should be less than the input source impedance to pre-vent high frequency switching current passing to the input. The calculated value varies with input voltage and is a maximum when VIN is double the output voltage.

$$C_{IN} = \frac{\frac{V_O}{V_{IN}} \cdot \left(1 - \frac{V_O}{V_{IN}}\right)}{\left(\frac{V_{PP}}{I_O} - ESR\right) \cdot f_S}$$

$$C_{IN(MIN)} = \frac{1}{\left(\frac{V_{PP}}{I_O} - ESR\right) \cdot 4 \cdot f_S}$$

A low ESR input capacitor sized for maximum RMS cur-rent must be used. Ceramic capacitors with X5R or X7R dielectrics are highly recommended because of their low ESR and small temperature coefficients. A 22μF ceramic capacitor for most applications is sufficient. A large value may be used for improved input voltage filtering.The maximum input capacitor RMS current is:

$$I_{RMS} = I_O \cdot \sqrt{\frac{V_O}{V_{IN}} \cdot \left(1 - \frac{V_O}{V_{IN}}\right)}$$

The input capacitor RMS ripple current varies with the input and output voltage and will always be less than or equal to half of the total DC load current.

$$I_{RMS(MAX)} = \frac{1}{2} \cdot I_O$$

To minimize stray inductance, the capacitor should be placed as closely as possible to the IC. This keeps the high frequency content of the input current localized, minimizing EMI and input voltage ripple. The proper placement of the input capacitor (C1) can be seen in the evaluation board layout in Figures 2 and 3.

A laboratory test set-up typically consists of two long wires running from the bench power supply to the evaluation board input voltage pins. The inductance of these wires, along with the low-ESR ceramic input capacitor, can create a high Q network that may affect converter performance. This problem often becomes apparent in the form of excessive ringing in the output voltage during load transients. Errors in the loop phase and gain measurements can also result. Since the inductance of a short PCB trace feeding the input voltage is significantly lower than the power leads from the bench power supply, most applications do not exhibit this problem. In applications where the input power source lead inductance cannot be reduced to a level that does not affect the converter performance, a high ESR tantalum or aluminum electrolytic should be placed in parallel with the low ESR, ESL bypass ceramic. This dampens the high Q network and stabilizes the system.

Output Capacitor Selection

The function of output capacitance is to store energy to attempt to maintain a constant voltage. The energy is stored in the capacitor's electric field due to the voltage applied. The value of output capacitance is generally selected to limit output voltage ripple to the level required by the specification. Since the ripple current in the output inductor is usually determined by L, VOUT and VIN, the series impedance of the capacitor primarily determines the out-put voltage ripple. The three elements of the capacitor that contribute to its impedance (and output voltage ripple) are equivalent series resistance (ESR), equivalent series inductance (ESL), and capacitance (C). The output voltage droop due to a load transient is dominated by the capacitance of the ceramic output capacitor. During a step increase in load current, the ceramic output capacitor alone supplies the load current until the loop responds. Within three switching cycles, the loop responds and the inductor current increases to match the load current demand. The relationship of the output voltage droop during the three switching cycles to the output capacitance can be estimated by:

$$C_{OUT} = \frac{3 \cdot \Delta I_{LOAD}}{V_{DROOP} \cdot f_S}$$

In many practical designs, to get the required ESR, a capacitor with much more capacitance than is needed must be selected. For both continuous or discontinuous inductor current mode operation, the ESR of the COUT needed to limit the ripple to ΔVO, V peak-to-peak is:

$$ESR \le \frac{\Delta V_O}{\Delta I_L}$$

Ripple current flowing through a capacitor's ESR causes power dissipation in the capacitor. This power dissipation causes a temperature increase internal to the capacitor. Excessive temperature can seriously shorten the expected life of a capacitor. Capacitors have ripple current ratings that are dependent on ambient temperature and should not be exceeded. The output capacitor ripple cur-rent is the inductor current, IL, minus the output current, IO. The RMS value of the ripple current flowing in the output capacitance (continuous inductor current mode operation) is given by:

$$I_{RMS} = \Delta I_L \cdot \frac{\sqrt{3}}{6} = \Delta I_L \cdot 0.289$$

ESL can be a problem by causing ringing in the low megahertz region but can be controlled by choosing low ESL capacitors, limiting lead length (PCB and capacitor), and replacing one large device with several smaller ones connected in parallel. In conclusion, in order to meet the requirement of out-put voltage ripple small and regulation loop stability, ceramic capacitors with X5R or X7R dielectrics are recommended due to their low ESR and high ripple current ratings. The output ripple VOUT is determined by:

$$\Delta V_{OUT} \le \frac{V_{OUT} \cdot (V_{IN} - V_{OUT})}{V_{IN} \cdot f_{OSC} \cdot L} \cdot \left(ESR + \frac{1}{8 \cdot f_{OSC} \cdot C_{OUT}}\right)$$

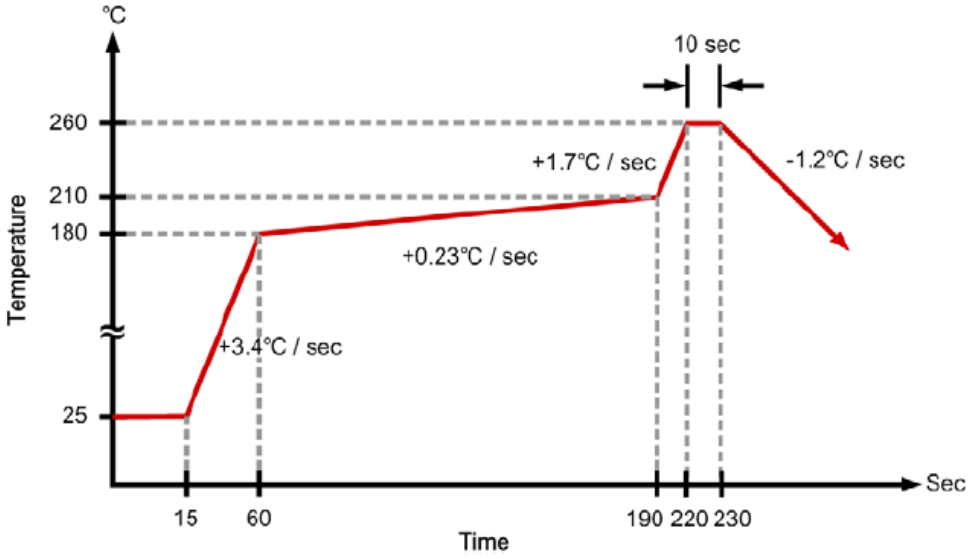
A 22μF ceramic capacitor can satisfy most applications.

Layout Guidance

When laying out the PC board, the following layout guideline should be followed to ensure proper operation of the LP6343:

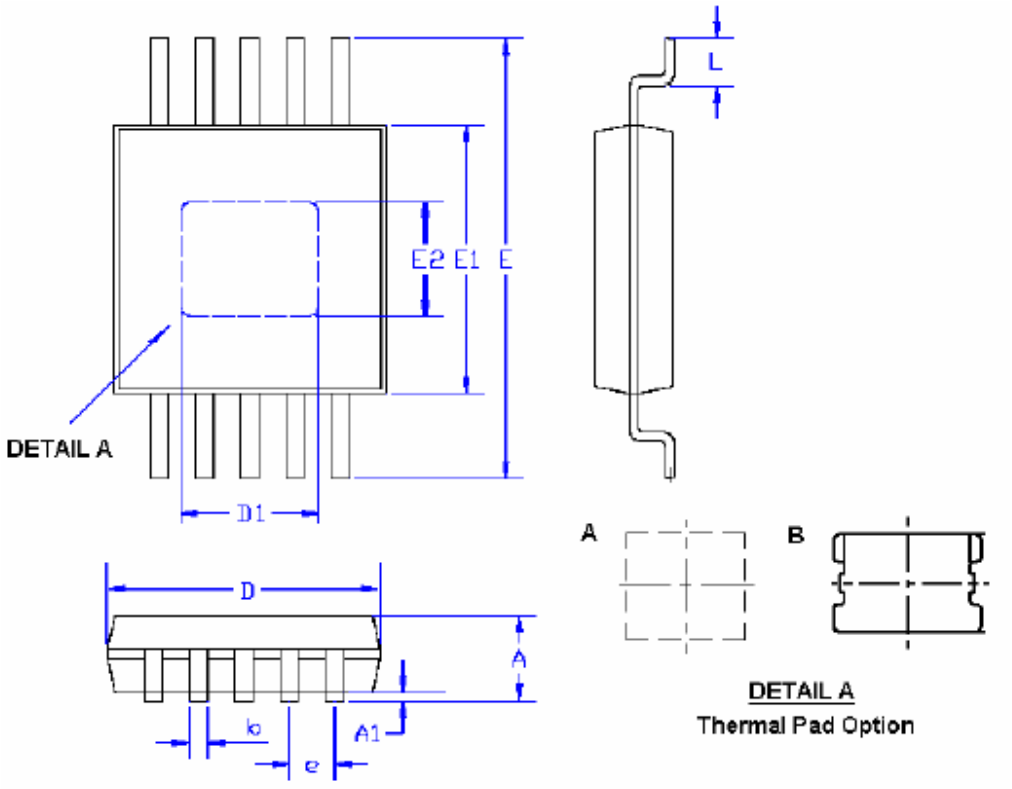
1. The exposed pad (EP) must be reliably soldered to the GND plane. A PGND pad below EP is strongly recommended.
2. The power traces, including the GND trace, the LX trace and the IN trace should be kept short, direct and wide to allow large current flow. The L1 connection to the LX pins should be as short as possible. Use several VIA pads when routing between layers.
3. The input capacitor (C1) should connect as closely as possible to IN (Pin 2) and AGND (Pins 4 and 6) to get good power filtering.
4. Keep the switching node, LX (Pins 7 and 8) away from the sensitive FB/OUT node.
5. The feedback trace or OUT pin (Pin 2) should be separate from any power trace and connect as closely as possible to the load point. Sensing along a high-current load trace will degrade DC load regulation. If external feedback resistors are used, they should be placed as closely as possible to the FB pin (Pin 5) to minimize the length of the high impedance feedback trace.
6. The output capacitor C2 and L1 should be connected as closely as possible. The connection of L1 to the LX pin should be as short as possible and there should not be any signal lines under the inductor.
7. The resistance of the trace from the load return to PGND should be kept to a minimum. This will help to minimize any error in DC regulation due to differences in the potential of the internal signal ground and the power ground.

IR Re-flow Soldering Curve



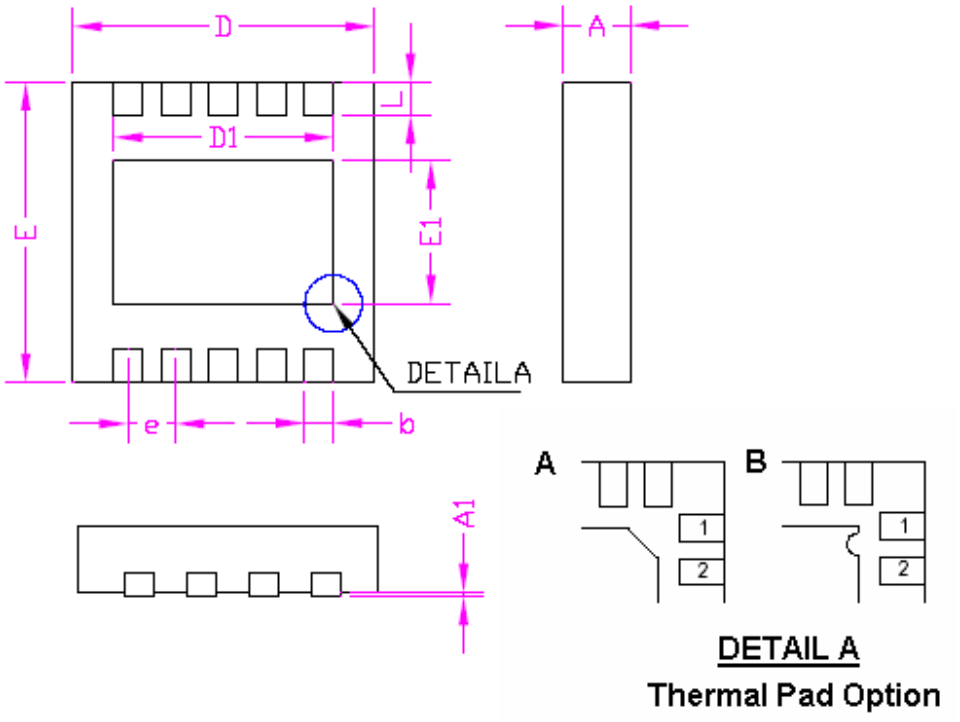
Packaging Information

MSOP-10



SYMBOLS	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
A	-	1.10	-	0.043
A1	0.00	0.15	0.000	0.006
D	3.00		0.118	
E1	3.00		0.118	
E	4.70	5.10	0.185	0.201
L	0.40	0.80	0.016	0.031
b	0.17	0.33	0.006	0.013
e	0.50		0.020	
D1	1.80		0.071	
E2	1.66		0.065	

TDFN-10



SYMBOLS	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
A	0.70	0.80	0.028	0.031
A1	0.00	0.05	0.000	0.002
D1	2.50		0.098	
D	2.90	3.10	0.114	0.122
E1	1.70		0.067	
E	2.90	3.10	0.114	0.122
L	0.30	0.50	0.012	0.020
b	0.18	0.30	0.007	0.012
e	0.50		0.020	
D1	2.40		0.094	