National Semiconductor

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LP38841-ADJ
0.8A Ultra Low Dropout Adjustable Linear Regulators
Stable with Ceramic Output Capacitors

General Description

The LP38841-ADJ is a high current, fast response regulator which can maintain output voltage regulation with minimum input to output voltage drop. Fabricated on a CMOS process, the device operates from two input voltages: Vbias provides voltage to drive the gate of the N-MOS power transistor, while Vin is the input voltage which supplies power to the load. The use of an external bias rail allows the part to operate from ultra low Vin voltages. Unlike bipolar regulators, the CMOS architecture consumes extremely low quiescent current at any output load current. The use of an N-MOS power transistor results in wide bandwidth, yet minimum external capacitance is required to maintain loop stability.

The fast transient response of these devices makes them suitable for use in powering DSP, Microcontroller Core voltages and Switch Mode Power Supply post regulators. The parts are available in the PSOP package.

Dropout Voltage: 75 mV (typ) @ 0.8A load current.

Quiescent Current: 30 mA (typ) at full load.

Shutdown Current: 30 nA (typ) when S/D pin is low.

Precision Reference Voltage: 1.5% room temperature accuracy.

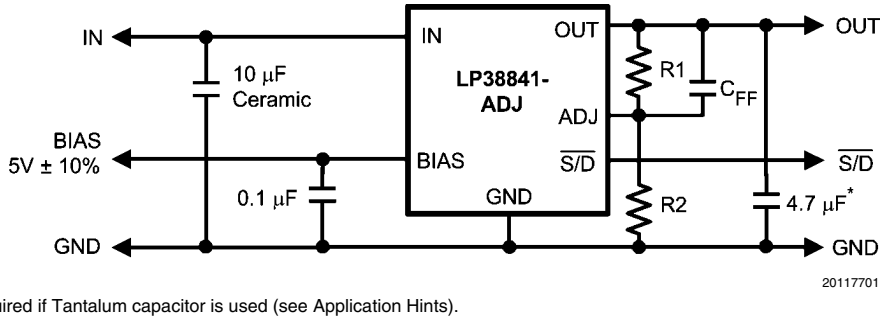
Features

- Ideal for conversion from 1.8V or 1.5V inputs
- Designed for use with low ESR ceramic capacitors
- Ultra low dropout voltage (75mV @ 0.8A typ)
- 0.56V to 1.5V adjustable output range
- Load regulation of 0.1%/A (typ)
- 30nA quiescent current in shutdown (typ)
- Low ground pin current at all loads
- Over temperature/over current protection
- Available in 8 lead PSOP package
- –40°C to +125°C junction temperature range
- UVLO disables output when V_{BIAS} < 3.8V

Applications

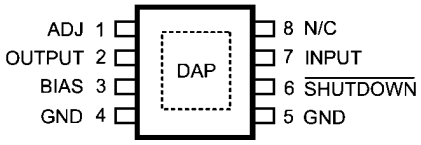
- ASIC Power Supplies In:
  - Desktops, Notebooks, and Graphics Cards, Servers
  - Gaming Set Top Boxes, Printers and Copiers
- Server Core and I/O Supplies
- DSP and FPGA Power Supplies
- SMPS Post-Regulators

Typical Application Circuit



* Minimum value required if Tantalum capacitor is used (see Application Hints).

Connection Diagram



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PSOP-8, Top View

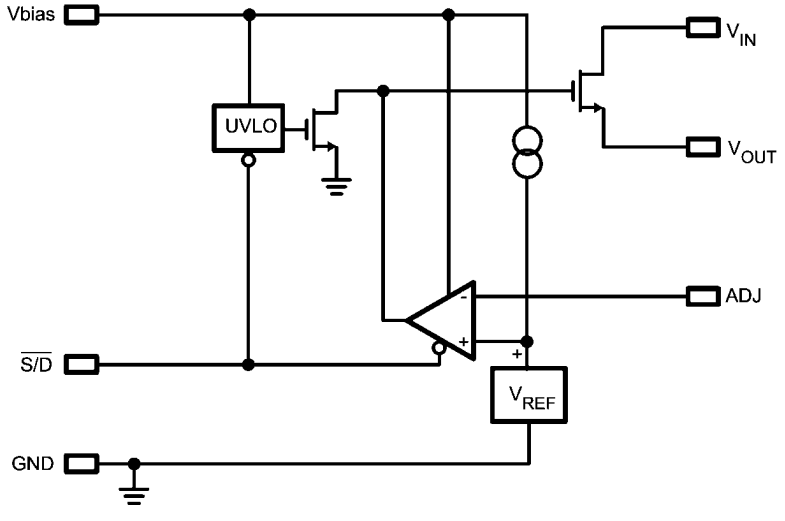
Pin Description

Pin Number	Pin Name	Pin Description
1	ADJ	The Adjust pin is used to set the regulated output voltage by connecting it to the external resistors R1 and R2 (see Typical Application Circuit).
2	OUTPUT	The regulated output voltage is connected to this pin.
3	BIAS	The Bias pin is used to provide the low current bias voltage to the chip which operates the internal circuitry and provides drive voltage for the N-FET.
4, 5	GND	These are the power and analog grounds for the IC. Connect both pins to ground.
6	$\overline{\text{SHUTDOWN}}$	This provides a low power shutdown function which turns the regulated output OFF. Tie to V_{BIAS} if this function is not used.
7	INPUT	The high current input voltage which is regulated down to the nominal output voltage must be connected to this pin. Because the bias voltage to operate the chip is provided separately, the input voltage can be as low as a few hundred millivolts above the output voltage.
8	N/C	This pin is floating, it has no internal connection.
DAP	DAP	The PSOP DAP is a thermal connection that is physically connected to the backside of the die, and is used as a thermal connection to the PC Board copper. The DAP is not a ground pin connection, but should be connected to ground potential.

Ordering Information

Order Number	Package Type	Package Drawing	Supplied As
LP38841MR-ADJ	PSOP-8	MRA08A	95 Units Tape and Reel
LP38841MRX-ADJ	PSOP-8	MRA08A	2500 Units Tape and Reel

Block Diagram



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Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Storage Temperature Range	−65°C to +150°C
Lead Temp. (Soldering, 5 seconds)	260°C
ESD Rating	
Human Body Model (Note 3)	2 kV
Machine Model (Note 9)	200V
Power Dissipation (Note 2)	Internally Limited
V_{IN} Supply Voltage (Survival)	−0.3V to +6V
V_{BIAS} Supply Voltage (Survival)	−0.3V to +7V
Shutdown Input Voltage (Survival)	−0.3V to +7V
V_{ADJ}	-0.3V to +6V
I_{OUT} (Survival)	Internally Limited
Output Voltage (Survival)	−0.3V to +6V
Junction Temperature	−40°C to +150°C

Operating Ratings

V_{IN} Supply Voltage	(V_{OUT} + V_{DO}) to 5.5V
Shutdown Input Voltage	0 to +5.5V
I_{OUT}	0.8A
Operating Junction Temperature Range	−40°C to +125°C
V_{BIAS} Supply Voltage	4.5V to 5.5V
V_{OUT}	0.56V to 1.5V

Electrical Characteristics

Limits in standard typeface are for T_J = 25°C, and limits in **boldface type** apply over the full operating temperature range. Unless otherwise specified: $V_{IN} = V_O(NOM) + 1V$, V_{BIAS} = 4.5V, I_L = 10 mA, C_{IN} = 10 µF CER, C_{OUT} = 22 µF CER, $V_{S/D} = V_{BIAS}$. Min/Max limits are guaranteed through testing, statistical correlation, or design.

Symbol	Parameter	Conditions	MIN	TYP (Note 4)	MAX	Units
V_{ADJ}	Adjust Pin Voltage	10 mA < I_L < 0.8A $V_O(NOM) + 1V \le V_{IN} \le 5.5V$ $4.5V \le V_{BIAS} \le 5.5V$	0.552 **0.543**	0.56	0.568 **0.577**	V
I_{ADJ}	Adjust Pin Bias Current	10 mA < I_L < 0.8A $V_O(NOM) + 1V \le V_{IN} \le 5.5V$ $4.5V \le V_{BIAS} \le 5.5V$		1		µA
$\Delta V_O/\Delta V_{IN}$	Output Voltage Line Regulation (Note 6)	$V_O(NOM) + 1V \le V_{IN} \le 5.5V$		0.01		%/V
$\Delta V_O/\Delta I_L$	Output Voltage Load Regulation (Note 7)	10 mA < I_L < 0.8A		0.1	0.4 **1.3**	%/A
V_{DO}	Dropout Voltage (Note 8)	I_L = 0.8A		75	120 **205**	mV
$I_Q(V_{IN})$	Quiescent Current Drawn from V_{IN} Supply	10 mA < I_L < 0.8A		30	35 **40**	mA
		$V_{\overline{S/D}} \le 0.3V$		0.06	1 **30**	µA
$I_Q(V_{BIAS})$	Quiescent Current Drawn from V_{BIAS} Supply	10 mA < I_L < 0.8A		2	4 **6**	mA
		$V_{\overline{S/D}} \le 0.3V$		0.03	1 **30**	µA
UVLO	V_{BIAS} Voltage Where Regulator Output Is Enabled			3.8		V
I_{SC}	Short-Circuit Current	V_{OUT} = 0V		2.6		A
Shutdown Input						
V_{SDT}	Output Turn-off Threshold	Output = ON		0.7	**1.3**	V
		Output = OFF	**0.3**	0.7		
Td (OFF)	Turn-OFF Delay	R_{LOAD} X C_{OUT} << Td (OFF)		20		µs
Td (ON)	Turn-ON Delay	R_{LOAD} X C_{OUT} << Td (ON)		15		
$I_{\overline{S/D}}$	$\overline{S/D}$ Input Current	$V_{\overline{S/D}}$ =1.3V		1		µA
		$V_{\overline{S/D}} \le 0.3V$		−1		
θ_{J-A}	Junction to Ambient Thermal Resistance	PSOP-8 Package (Note 10)		43		°C/W
AC Parameters						

Symbol	Parameter	Conditions	MIN	TYP (Note 4)	MAX	Units
PSRR (V_{IN})	Ripple Rejection for V_{IN} Input Voltage	$V_{IN} = V_{OUT}$ +1V, f = 120 Hz		80		dB
		$V_{IN} = V_{OUT}$ + 1V, f = 1 kHz		65		
PSRR (V_{BIAS})	Ripple Rejection for V_{BIAS} Voltage	$V_{BIAS} = V_{OUT}$ + 3V, f = 120 Hz		58		
		$V_{BIAS} = V_{OUT}$ + 3V, f = 1 kHz		58		
	Output Noise Density	f = 120 Hz		1		µV/root–Hz
e_n	Output Noise Voltage V_{OUT} = 1.5V	BW = 10 Hz – 100 kHz		150		µV (rms)
		BW = 300 Hz – 300 kHz		90		

Note 1: Absolute maximum ratings indicate limits beyond which damage to the component may occur. Operating ratings indicate conditions for which the device is intended to be functional, but do not guarantee specific performance limits. For guaranteed specifications, see Electrical Characteristics. Specifications do not apply when operating the device outside of its rated operating conditions.

Note 2: At elevated temperatures, device power dissipation must be derated based on package thermal resistance and heatsink thermal values. If power dissipation causes the junction temperature to exceed specified limits, the device will go into thermal shutdown.

Note 3: The human body model is a 100 pF capacitor discharged through a 1.5k resistor into each pin.

Note 4: Typical numbers represent the most likely parametric norm for 25°C operation.

Note 5: If used in a dual-supply system where the regulator load is returned to a negative supply, the output pin must be diode clamped to ground.

Note 6: Output voltage line regulation is defined as the change in output voltage from nominal value resulting from a change in input voltage.

Note 7: Output voltage load regulation is defined as the change in output voltage from nominal value as the load current increases from no load to full load.

Note 8: Dropout voltage is defined as the minimum input to output differential required to maintain the output with 2% of nominal value.

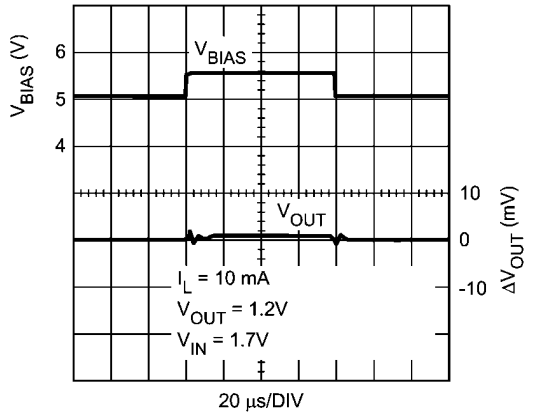
Note 9: The machine model is a 220 pF capacitor discharged directly into each pin.

Note 10: For optimum heat dissipation, the exposed DAP on the bottom of the PSOP package must be soldered to a copper plane or connected using thermal vias to an internal copper plane.

Typical Performance Characteristics

Unless otherwise specified: T_J = 25°C, C_{IN} = 10 µF CER, C_{OUT} = 22 µF CER, C_{BIAS} = 1 µF CER, $\overline{S/D}$ Pin is tied to V_{BIAS}, V_{OUT} = 1.2V, I_L = 10mA, V_{BIAS} = 5V, V_{IN} = V_{OUT} + 1V.

V_{BIAS} Transient Response



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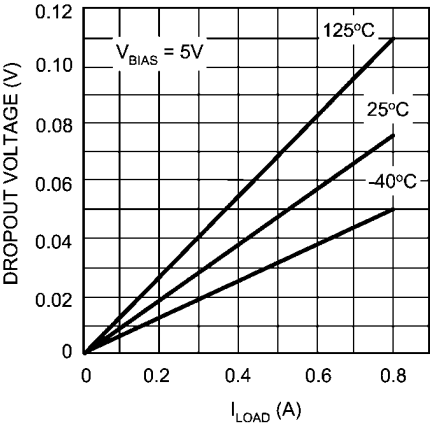
Dropout Voltage Over Temperature



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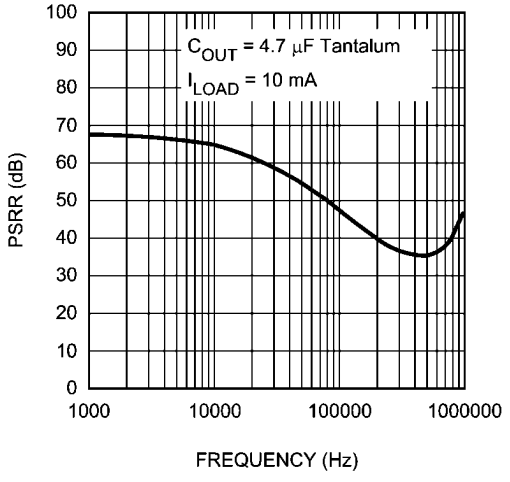
V_{BIAS} PSRR



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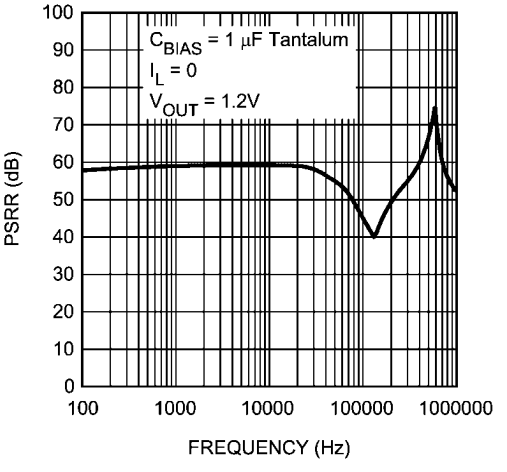
V_{BIAS} PSRR



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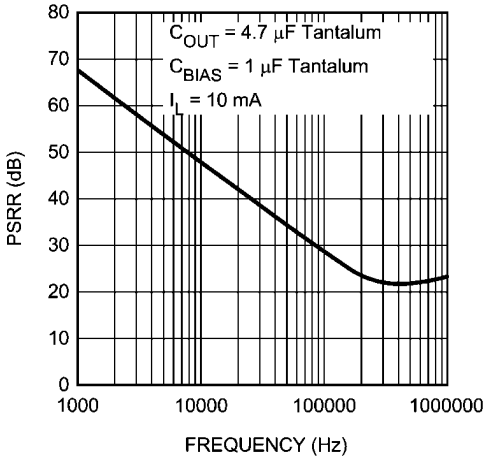
V_{IN} PSRR



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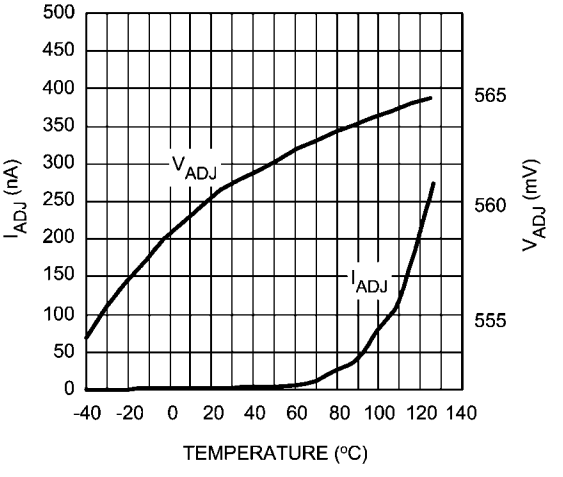
V_{ADJ} / I_{ADJ} vs Temperature



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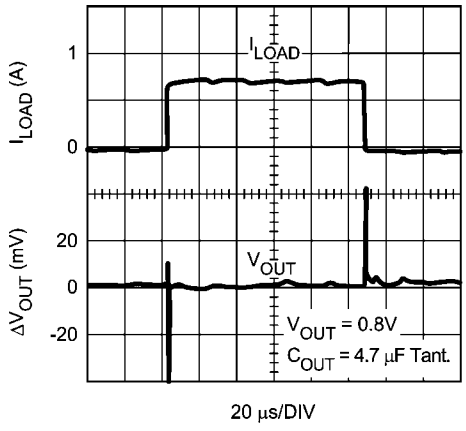
Load Transient Response



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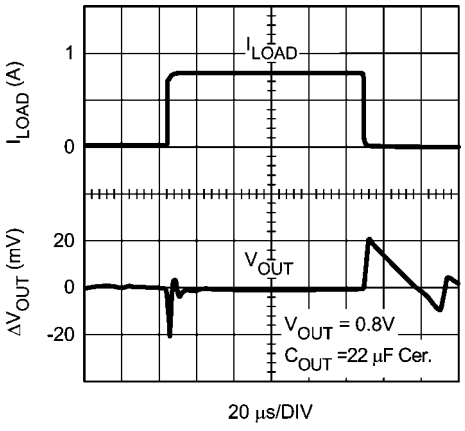
Load Transient Response



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Application Hints

SETTING THE OUTPUT VOLTAGE (Refer to Typical Application Circuit)

The output voltage is set using the resistive divider R1 and R2. The output voltage is given by the formula:

$$V_{OUT} = V_{ADJ} \times (1 + R1 / R2)$$

The value of R2 must be 10k or less for proper operation.

EXTERNAL CAPACITORS

To assure regulator stability, input and output capacitors are required as shown in the Typical Application Circuit.

OUTPUT CAPACITOR

An output capacitor is required on the LP3884X devices for loop stability. The minimum value of capacitance necessary depends on type of capacitor: if a solid Tantalum capacitor is used, the part is stable with capacitor values as low as 4.7µF. If a ceramic capacitor is used, a minimum of 22 µF of capacitance must be used (capacitance may be increased without limit). The reason a larger ceramic capacitor is required is that the output capacitor sets a pole which limits the loop bandwidth. The Tantalum capacitor has a higher ESR than the ceramic which provides more phase margin to the loop, thereby allowing the use of a smaller output capacitor because adequate phase margin can be maintained out to a higher crossover frequency. The tantalum capacitor will typically also provide faster settling time on the output after a fast changing load transient occurs, but the ceramic capacitor is superior for bypassing high frequency noise.

The output capacitor must be located less than one centimeter from the output pin and returned to a clean analog ground. Care must be taken in choosing the output capacitor to ensure that sufficient capacitance is provided over the full operating temperature range. If ceramics are selected, only X7R or X5R types may be used because Z5U and Y5F types suffer severe loss of capacitance with temperature and applied voltage and may only provide 20% of their rated capacitance in operation.

INPUT CAPACITOR

The input capacitor is also critical to loop stability because it provides a low source impedance for the regulator. The minimum required input capacitance is 10 µF ceramic (Tantalum not recommended). The value of C_{IN} may be increased without limit. As stated above, X5R or X7R must be used to ensure sufficient capacitance is provided. The input capacitor must be located less than one centimeter from the input pin and returned to a clean analog ground.

FEED FORWARD CAPACITOR (Refer to Typical Application Circuit)

A capacitor placed across R1 can provide some additional phase margin and improve transient response. The capacitor C_{FF} and R1 form a zero in the loop response given by the formula:

$$F_Z = 1 / (2 \times \pi \times C_{FF} \times R1)$$

For best effect, select C_{FF} so the zero frequency is approximately 70 kHz. The phase lead provided by C_{FF} drops as the output voltage gets closer to 0.56V (and R1 reduces in value). The reason is that C_{FF} also forms a pole whose frequency is given by:

$$F_P = 1 / (2 \times \pi \times C_{FF} \times R1 \,//\, R2)$$

As R1 reduces, the two equations come closer to being equal and the pole and zero begin to cancel each other out which removes the beneficial phase lead of the zero.

BIAS CAPACITOR

The 0.1µF capacitor on the bias line can be any good quality capacitor (ceramic is recommended).

BIAS VOLTAGE

The bias voltage is an external voltage rail required to get gate drive for the N-FET pass transistor. Bias voltage must be in the range of 4.5 - 5.5V to assure proper operation of the part.

UNDER VOLTAGE LOCKOUT

The bias voltage is monitored by a circuit which prevents the regulator output from turning on if the bias voltage is below approximately 3.8V.

SHUTDOWN OPERATION

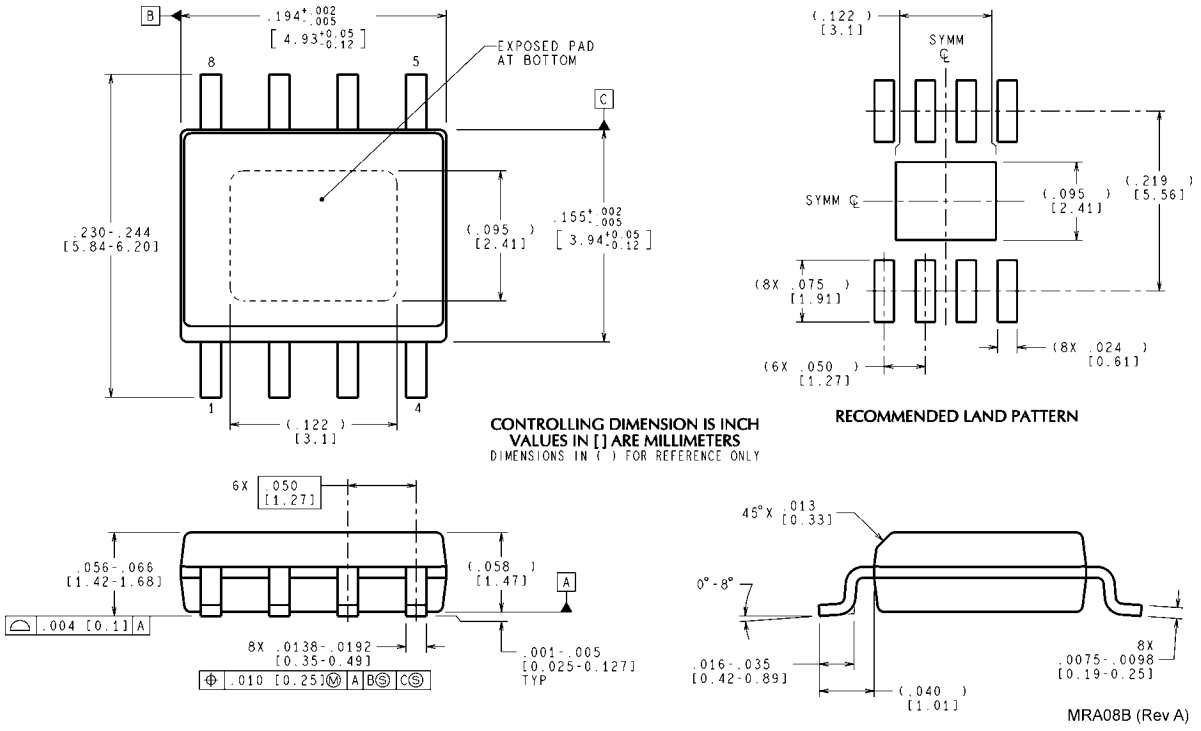
Pulling down the shutdown ($\overline{S/D}$) pin will turn-off the regulator. The $\overline{S/D}$ pin must be actively terminated through a pull-up resistor (10 kΩ to 100 kΩ) for a proper operation. If this pin is driven from a source that actively pulls high and low (such as a CMOS rail to rail comparator), the pull-up resistor is not required. This pin must be tied to Vin if not used.

POWER DISSIPATION/HEATSINKING

Heatsinking for the PSOP-8 package is accomplished by allowing heat to flow through the exposed DAP on the bottom

of the package into the copper on the PC board. The exposed DAP must be soldered down to a copper plane to get good heat transfer. It can also be connected through thermal vias to internal copper planes. Since the DAP is physically connected to the backside of the die, it must be held at ground potential. Under all possible conditions, the junction temperature must be within the range specified under operating conditions.

Physical Dimensions inches (millimeters) unless otherwise noted



PSOP-8 8-Lead Molded PSOP-2
NS Package Number MRA08B

Notes

Notes

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