300mA, Dual Channel Ultra-Fast CMOS LDO Regulato

General Description

The LP2202 is a dual channel, low noise, and low dropout regulator sourcing up to 300mA at each channel. The range of output voltage is from 1.2V to 3.6V by operating from 2.5V to 5.5V input.

LP2202 offers 2% accuracy, extremely low dropout voltage (220mV @ 300mA), and extremely low ground current, only 75μA per LDO. The shutdown current is near zero current which is suitable for battery-power devices. Other features include current limiting, over temperature, output short circuit protection.

LP2202 can operate stably with very small ceramic output capacitors, reducing required board space and component cost. LP2202 is available in fixed output voltages in the SOT-23-6 package.

Order Information

LP2201 □□ □□ □

- F: Pb-Free
- Package Type
  - B6: SOT23-6
- Out1/Out2 Voltage Type
  - 25/28: 2.5V/2.8V
  - 28/18: 2.8V/1.8V
  - 28/28: 2.8V/2.8V

Features

- Wide Operating Voltage Ranges : 2.5V to 5.5V
- Low-Noise for RF Applications
- High PSRR 75dB at 1kHz
- No Noise Bypass Capacitor Required
- Fast Response in Line/Load Transient
- TTL-Logic-Controlled Shutdown Input
- Dual LDO Outputs (220mV/300mA)
- High Output Accuracy 2%
- Ultra-low Quiescent Current 75uA
- Thermal Shutdown Protection
- Thermal Shutdown Protection
- RoHS Compliant and 100% Lead (Pb)-Free

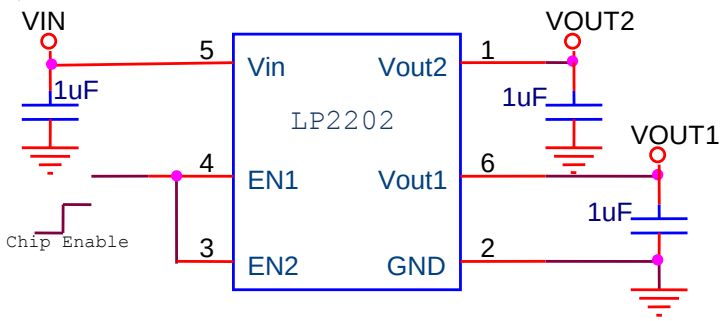
Applications

- CDMA/GSM Cellular Handsets
- Smart mobile phone
- Battery-Powered Equipment
- DSC Sensor
- Wireless Card

Marking Information

Device	Marking	Package	Shipping
LP2202	XXXX	SOT23-6	3K/REEL
Marking indication: X represents production batch.			

Typical Application Circuit



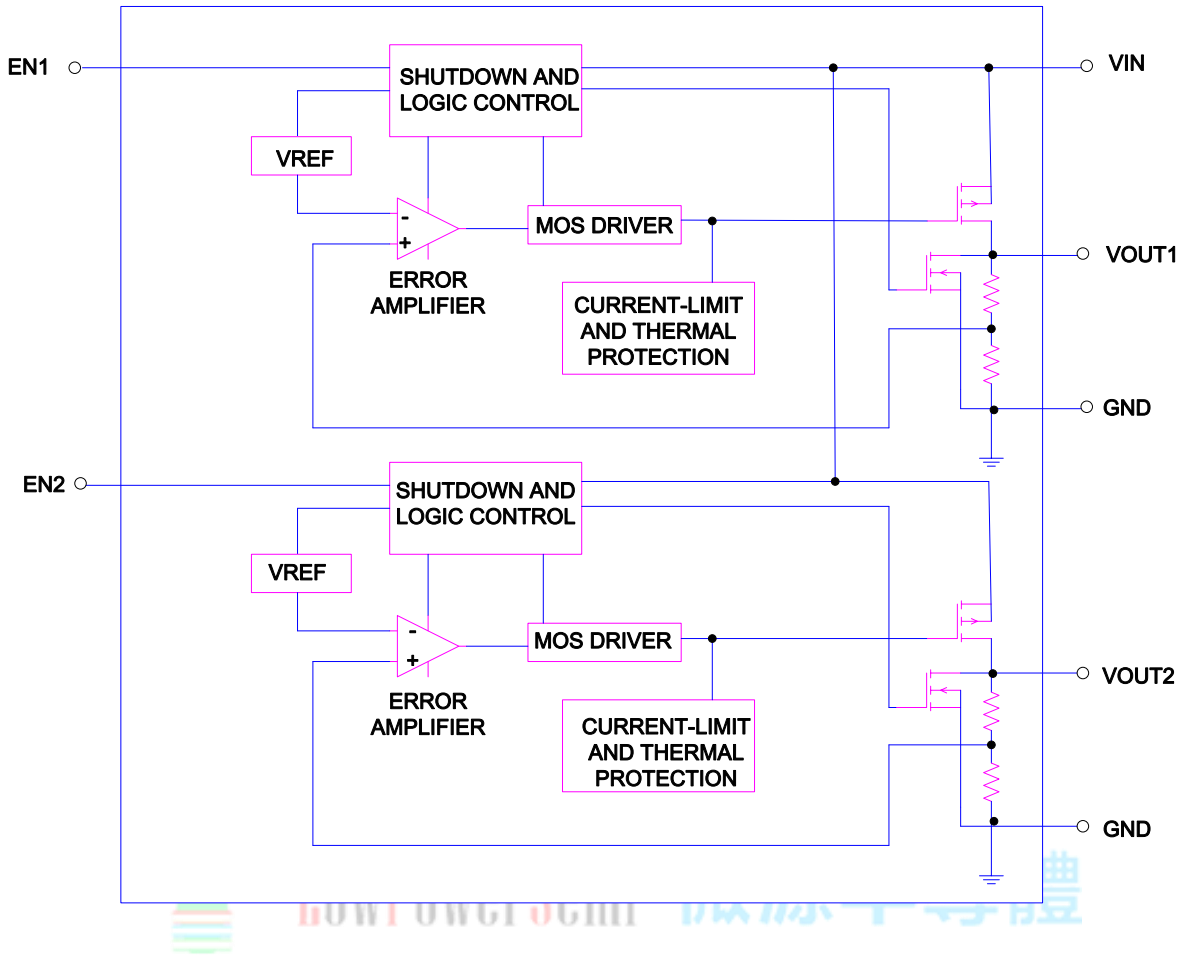
Functional Pin Description

Package Type	Pin Configurations
SOT23-6	TOP VIEW EN1 1 VIN 2 EN2 3 6 VOUT1 5 GND 4 VOUT2 SOT23-6

Pin Description

Pin	Name	Description
1	EN1	Chip Enable1 (Active High)
2	VIN	Supply Input
3	EN2	Chip Enable2 (Active High)
4	VOUT2	Channel 2 Output Voltage
5	GND	Common Ground
6	VOUT1	Channel 1 Output Voltage

Function Diagram



Absolute Maximum Ratings

✧ Supply Input Voltage ---------- 6V

Power Dissipation, PD @ TA = 25°C

✧ SOT23-6 ---------- 450mW

Package Thermal Resistance

✧ SOT23-6, θJA ---------- 250°C/W

✧ Lead Temperature (Soldering, 10 sec.) ---------- 260°C

✧ Storage Temperature Range ---------- −65°C to 165°C

ESD Susceptibility

✧ HBM (Human Body Mode) ---------- 2kV

✧ MM(Machine-Mode) ---------- 200V

Recommended Operating Conditions

✧ Operation Junction Temperature Range ---------- −40°C to 125°C

✧ Operation Ambient Temperature Range ---------- −40°C to 85°C

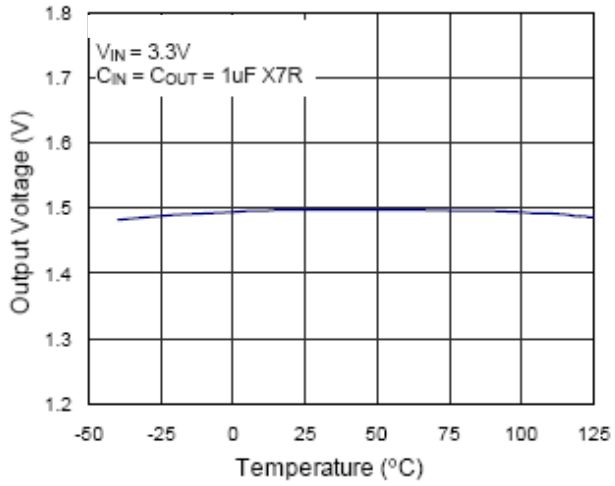
Electrical Characteristics

(V_{IN} = V_{OUT} + 1V, C_{IN} = C_{OUT} = 1μF, T_A = 25° C, unless otherwise specified)

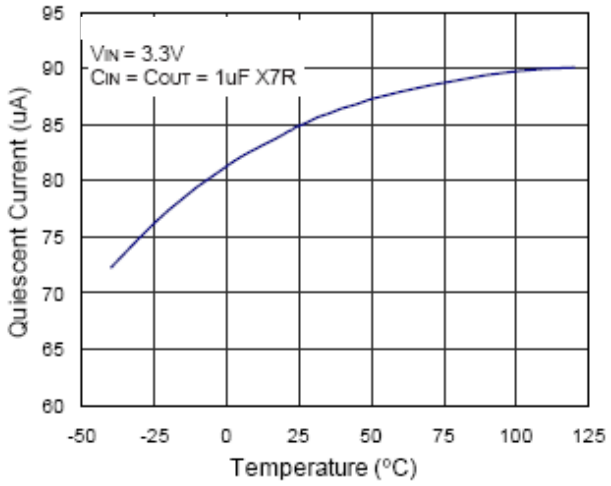
Parameter		Symbol	Test Conditions	Min	Typ	Max	Units
Output Voltage Accuracy		ΔV_{OUT}	$I_{OUT=}$1mA	−2	--	+2	%
Maximum output Current		I_{max}	Continuous	300			mA
Current Limit		I_{LIM}	R_{LOAD}=1Ω	360	400		mA
Quiescent Current		I_Q	V_{EN}≥1.2V, I_{OUT}=0mA		75		μA
Dropout Voltage		V_{DROP}	I_{OUT}=30mA, V_{OUT}>2.8V		30	45	mV
			I_{OUT}=150mA, V_{OUT}>2.8V		80	150	mV
Line Regulation		ΔV_{LINE}	V_{IN}=(V_{OUT}+1V) to 5.5V, I_{OUT}=1mA			0.3	%
Load Regulation		ΔV_{LOAD}	1mA<I_{OUT}<300mA			2	%
Standby Current		I_{STBY}	V_{EN}=GND, Shutdown		0.01	1	μA
EN Input Bias Current		I_{IBSD}	V_{EN}=GND or V_{IN}		1	5	uA
EN Threshold	Logic-Low Voltage	V_{IL}	V_{IN}=3V to 5.5V, Shutdown			0.4	V
	Logic-High Voltage	V_{IH}	V_{IN}=3V to 5.5V, Start-Up	1.4			V
Output Noise Voltage			10Hz to 100kHz, I_{OUT}=200mA C_{OUT}=1μF		100		uVRMS
Power Supply Rejection Rate	f=1kHz	PSRR	C_{OUT}=1μF, I_{OUT}=10mA		−75		dB
	f=10kHz				−65		dB
Thermal Shutdown Temperature		T_{SD}			150		°C

Typical Operating Characteristics

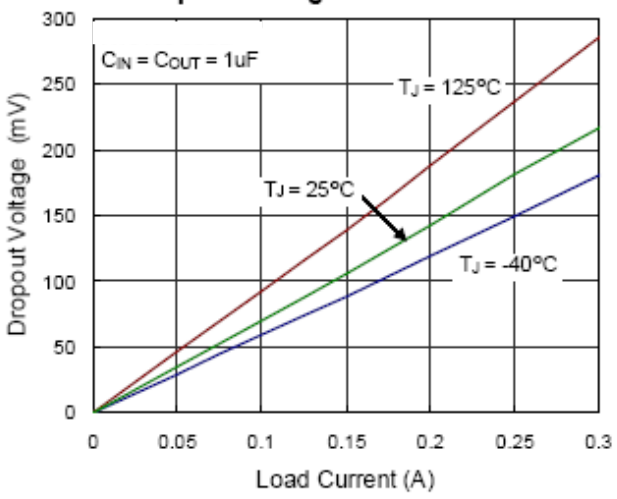
Output Voltage vs. Temperature



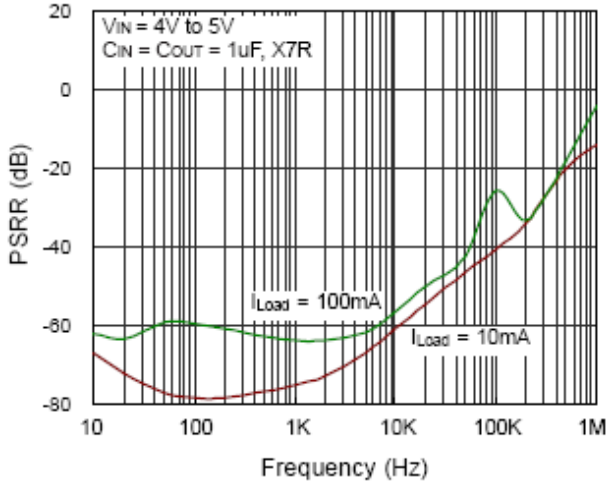
Quiescent Current vs. Temperature



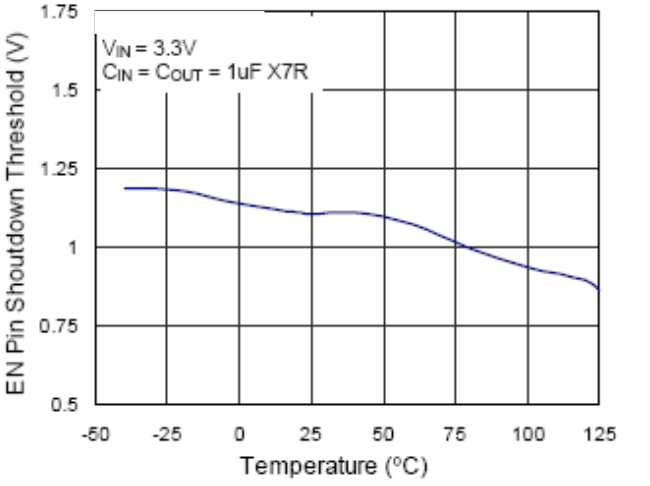
Dropout Voltage vs. Load Current



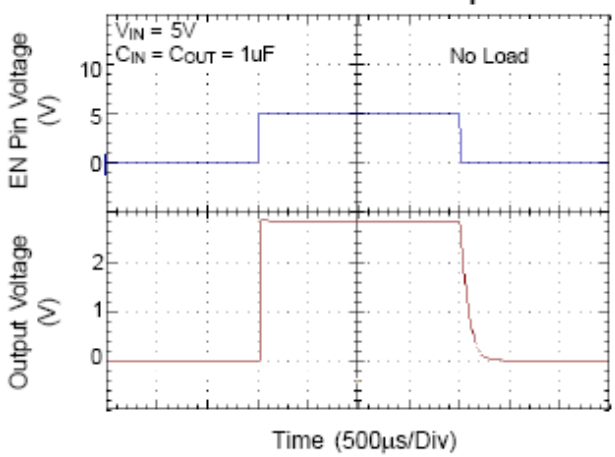
PSRR



EN Pin Shoutdown Threshold vs. Temperature



EN Pin Shutdown Response



Applications Information

Like any low-dropout regulator, the external capacitors used with the LP2202 must be carefully selected for regulator stability and performance. Using a capacitor whose value is > 1μF on the LP2202 input and the amount of capacitance can be increased without limit. The input capacitor must be located a distance of not more than 0.5 inch from the input pin of the IC and returned to a clean analog ground. Any good quality ceramic or tantalum can be used for this capacitor. The capacitor with larger value and lower ESR (equivalent series resistance) provides better PSRR and line-transient response. The output capacitor must meet both requirements for minimum amount of capacitance and ESR in all LDOs application. The LP2202 is designed specifically to work with low ESR ceramic output capacitor in space-saving and performance consideration. Using a ceramic capacitor whose value is at least 1μF with ESR is > 25mΩ on the LP2202 output ensures stability. The LP2202 still works well with output capacitor of other types due to the wide stable ESR range. Output capacitor of larger capacitance can reduce noise and improve load transient response. The output capacitor should be located no more than 0.5 inch from the V_{OUT} pin of the LP2202 and returned to a clean analog ground.

Start-up Function Enable Function

The LP2202 features an LDO regulator enable/disable function. To ensure the LDO regulator will switch on, the EN turn on control level must be greater than 1.4 volts. The LDO regulator will go into the shutdown mode when the voltage on the EN pin falls below 0.4 volts. To protect the system, the LP2202 have a quick-discharge function. If the enable function is not needed in a specific application, it may be tied to V_{IN} to keep the LDO regulator in a continuously on state mode.

Thermal Considerations

Thermal protection limits power dissipation in LP2202. When the operation junction temperature exceeds 150°C, the OTP circuit starts the thermal shutdown function turn the pass element off. The pass element turns on again after the junction temperature cools by 25°C. For continue operation, do not exceed absolute maximum operation junction temperature 150°C.

The power dissipation definition in device is:

$$P_D = (V_{IN}-V_{OUT}) \times I_{OUT} + V_{IN} \times I_Q$$

The maximum power dissipation depends on the thermal resistance of IC package, PCB layout, the rate of surroundings airflow and temperature difference between junction and ambient.

The maximum power dissipation can be calculated by following formula:

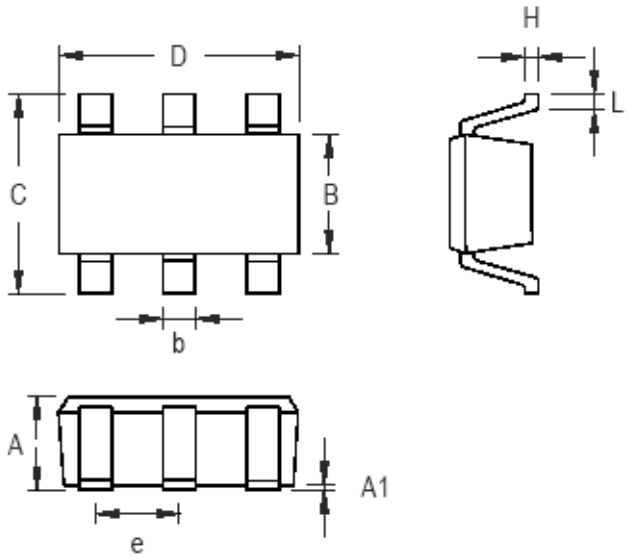
$$P_{D(MAX)} = (T_J - T_A) / \theta_{JA}$$

Where T_J is the maximum operation junction temperature 125°C, T_A is the ambient temperature and the θ_{JA} is the junction to ambient thermal resistance. For recommended operating conditions specification of LP2202, where $T_{J(MAX)}$ is the maximum junction temperature of the die (125°C) and T_A is the maximum ambient temperature. The junction to ambient thermal resistance (θ_{JA} is layout dependent) for SOT23-6 package is 250°C/W.

$$P_D = (125°C-25°C) / 250 = 400mW$$

The maximum power dissipation depends on operating ambient temperature for fixed $T_{J(MAX)}$ and thermal resistance θ_{JA}. Considering the thermal characteristic of PCB it may be larger than 400mW.

Package Information



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	0.889	1.295	0.031	0.051
A1	0.000	0.152	0.000	0.006
B	1.397	1.803	0.055	0.071
b	0.250	0.560	0.010	0.022
C	2.591	2.997	0.102	0.118
D	2.692	3.099	0.106	0.122
e	0.838	1.041	0.033	0.041
H	0.080	0.254	0.003	0.010
L	0.300	0.610	0.012	0.024

SOT-23-6 Surface Mount Package