SPECIFICATION
FOR
APPROVAL

( ) **Preliminary Specification**

(●) **Final Specification**

Title	17.3” FHD TFT LCD

BUYER	
MODEL	

SUPPLIER	LG Display Co., Ltd.
*MODEL	LP173WF3
Suffix	SLB3

*When you obtain standard approval,
please use the above model name without suffix

APPROVED BY	SIGNATURE
/	
/	
/	

Please return 1 copy for your confirmation with your signature and comments.

APPROVED BY	SIGNATURE
S. R. Kim / S.Manager	
REVIEWED BY	
M. J. Lee / S.Manager	
PREPARED BY **S. I. Joo / Engineer** **J. P. Lee / Engineer**	

Products Engineering Dept.
LG Display Co., Ltd

Contents

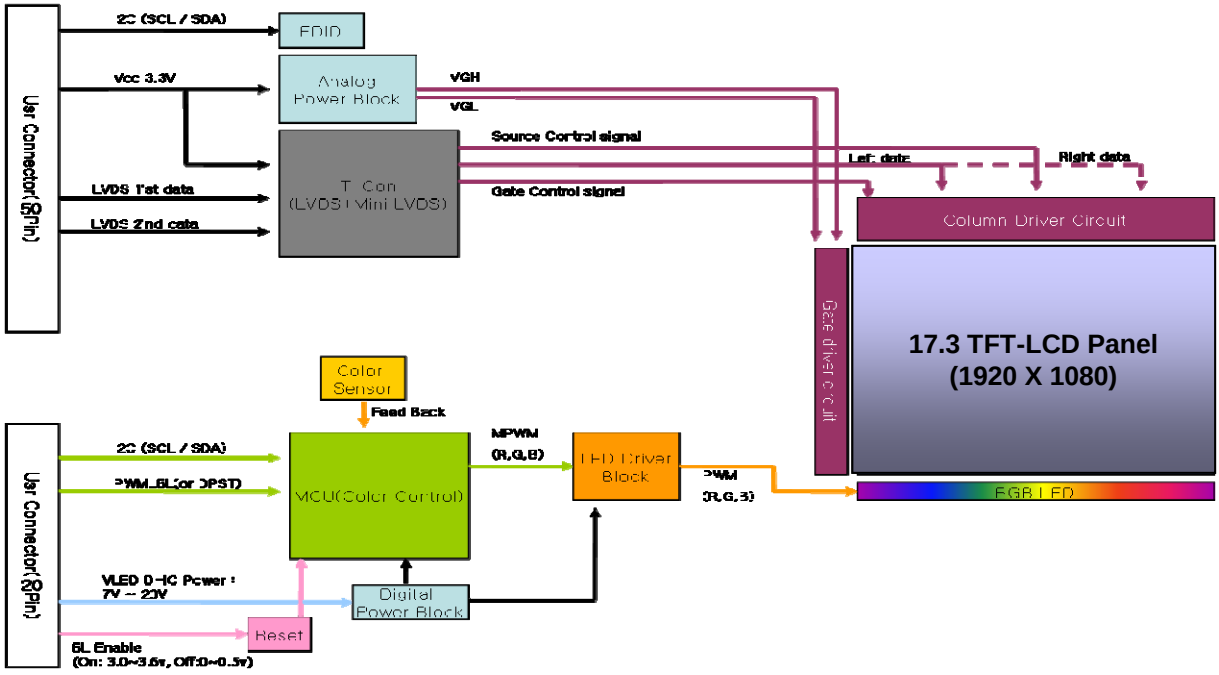
RECORD OF REVISIONS

Revision No	Revision Date	Page	Description	EDID ver
1.0	17. Aug. 2011	-	Final Specification	1.0
1.1	20. Oct. 2011	20	Update Rear View Drawing	1.0

1. General Description

The LP173WF3 is a Color Active Matrix Liquid Crystal Display with an integral RGB LED backlight system. The matrix employs a-Si Thin Film Transistor as the active element. It is a transmissive type display operating in the normally black mode. This TFT-LCD has 17.3 inches diagonally measured active display area with Full HD resolution(1920 horizontal by 1080 vertical pixel array). Each pixel is divided into Red, Green and Blue sub-pixels or dots which are arranged in vertical stripes. Gray scale or the brightness of the sub-pixel color is determined with a 10-bit gray scale signal for each dot, thus, presenting a palette of more than 1.073G(True) colors.

The LP173WF3 has been designed to apply the interface method that enables low power, high speed, low EMI. The LP173WF3 is intended to support applications where thin thickness, low power are critical factors and graphic displays are important. In combination with the vertical arrangement of the sub-pixels, the LP173WF3(SLB3) characteristics provide an excellent flat display for office automation products such as Notebook PC.



General Features

Active Screen Size	17.3 inches diagonal
Outline Dimension	398.1 (H, Typ) × 234.3 (V, Typ) × 7.2(D, Max) mm
Pixel Pitch	0.199mm × 0.199 mm
Pixel Format	1920 horiz. by 1080 vert. Pixels RGB strip arrangement
Color Depth	10-bit, 1.073G colors
Luminance, White	300 cd/m2(Typ.), 5 point
Power Consumption	18.2W (Typ.) [4.10W (Logic, Typ.) + 14.1W (B/L, Typ.)]
Weight (Max.)	830g
Display Operating Mode	Transmissive mode, Normally black
Surface Treatment	Hard coating(3H), Anti-Glare treatment of the front polarizer

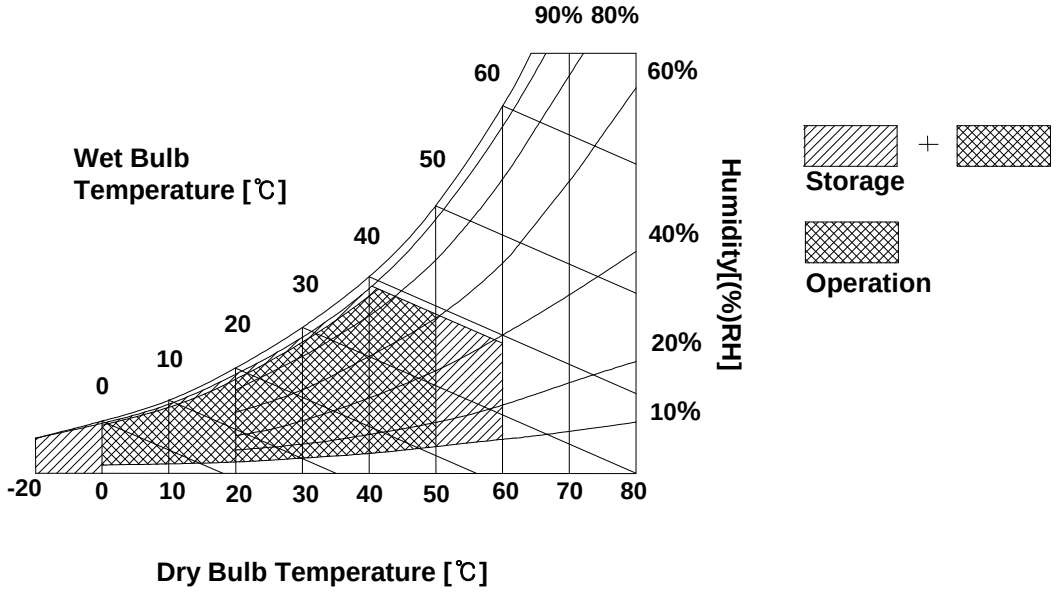
2. Absolute Maximum Ratings

The following are maximum values which, if exceeded, may cause faulty operation or damage to the unit.

Table 1. ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Values		Units	Notes
		Min	Max		
Power Input Voltage	VCC	-0.3	4.0	Vdc	at 25 ± 5°C
Operating Temperature	TOP	0	50	°C	1
Storage Temperature	HST	-20	60	°C	1
Operating Ambient Humidity	HOP	10	90	%RH	1
Storage Humidity	HST	10	90	%RH	1

Note : 1. Temperature and relative humidity range are shown in the figure below.
Wet bulb temperature should be 39°C Max, and no condensation of water.
Note : 2. Storage Condition is guaranteed under packing condition.



3. Electrical Specifications

3-1. Electrical Characteristics

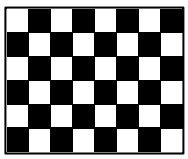
The LP173WF3(SLB3)requires two power inputs. One is employed to power the LCD electronics and to drive the TFT array and liquid crystal. The second input which powers the LED, is typically generated by an LED Driver. The LED Driver is an internal unit to the LCD.

Table 2. ELECTRICAL CHARACTERISTICS

Parameter		Symbol	Values			Unit	Notes
			Min	Typ	Max		
MODULE :							
Power Supply Input Voltage		VCC	3.0	3.3	3.6	V_{DC}	
Power Supply Input Current	Mosaic	I_{CC}	1.03	1.24	1.49	A	1
	White	I_{CC}	1.29	1.52	1.75		
Power Consumption (Mosaic)		Pc	-	4.1	4.92	Watt	1
Differential Impedance		Zm	90	100	110	Ohm	2
LED Backlight :							
Power Supply Input Voltage		V_{BL+}	7.5	14.4	21	V_{DC}	
Operating Voltage		$V_{LED\ (R,G,B)}$	-	-	45	V	3
Operating Current per string		$I_{LED\ (R,G,B)}$	-	-	50	mA	3
Power Consumption		P_{BL}		14.1	16.2	Watt	4
Life Time			15,000	-	-	Hrs	5

Note)

1. The specified current and power consumption are under the Vcc = 3.3V , 25℃, fv = 60Hz condition whereas Mosaic pattern (8x6) is displayed and fv is the frame frequency.



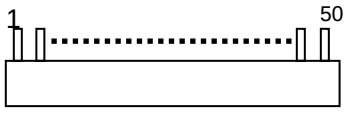
2. This impedance value is needed to proper display and measured form LVDS Tx to the mating connector.
3. RGB LED Operating Voltage and Operating Current per string should be within Max. SPEC.
4. The LED power consumption (Typ) shown above does include power of internal LED driver circuit for typical current condition. (Luminance = 300nit condition)
   The power consumption (Max) condition is R,G,B LED 100% Dimming.
5. The life time is determined as the time at which brightness of LED is 50% compare to that of initial value at the typical LED current.

3-2. Interface Connections

This LCD employs two interface connections, a 50 pin connector is used for the module electronics interface and the other connector is used for the integral backlight system.

Table 3. MODULE CONNECTOR PIN CONFIGURATION (CN1)

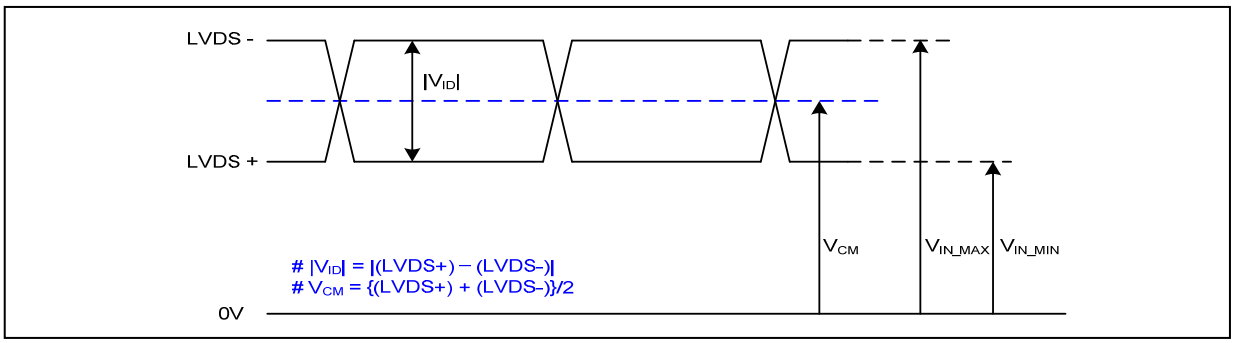
Pin	Symbol	Description	Notes
1	GND	Ground	
2	AVDD	Power Supply, 3.3V Typ.	
3	AVDD	Power Supply, 3.3V Typ.	
4	AVDD	Power Supply, 3.3V Typ.	
5	AVDD	Power Supply, 3.3V Typ.	
6	AVDD	Power Supply, 3.3V Typ.	
7	AVDD	Power Supply, 3.3V Typ.	
8	AVDD	Power Supply, 3.3V Typ.	
9	DVDD	Digital Power supply (3.3V Typ)	
10	DVDD	Digital Power supply (3.3V Typ)	
11	BIST	BIST	
12	Clk EEDID	Two wire serial interface clock	1, Interface chips
13	DATA EEDID	Two wire serial interface data	1.1 LCD : LGE (MAKO)
14	GND	Ground	including LVDS Receiver,
15	RXinO0-	- LVDS differential data input, Chan 0-Odd	VESA LVDS 10bit Format
16	RXinO0+	+ LVDS differential data input, Chan 0-Odd	1.2 System :
17	GND	Ground	* Pin to Pin compatible with LVDS
18	RXinO1	- LVDS differential data input, Chan 1-Odd	
19	RXinO1+	+ LVDS differential data input, Chan 1-Odd	
20	GND	Ground	2.Connector
21	RXinO2-	- LVDS differential data input, Chan 2-Odd	2.1 LCD : JAE FI-VHP50S-A-HF11
22	RXinO2+	+ LVDS differential data input, Chan 2-Odd	or equivalent
23	GND	Ground	2.2 Mating: JAE or equivalent
24	RXOC-	- LVDS Differential Clock input (Odd)	2.3 Connector pin arrangement
25	RXOC+	+ LVDS Differential Clock input (Odd)	LCD rear view
26	GND	Ground	
27	RXinO3-	- LVDS differential data input, Chan 3-Odd	
28	RXinO3+	+ LVDS differential data input, Chan 3-Odd	
29	GND	Ground	
30	RXinO4-	- LVDS differential data input, Chan 4-Odd	
31	RXinO4+	+ LVDS differential data input, Chan 4-Odd	
32	GND	Ground	
33	RXinE0-	- LVDS differential data input, Chan 0-Even	
34	RXinE0+	+ LVDS differential data input, Chan 0-Even	
35	GND	Ground	
36	RXinE1-	- LVDS differential data input, Chan 1-Even	
37	RXinE1+	+ LVDS differential data input, Chan 1-Even	
38	GND	Ground	
39	RXinE2-	- LVDS differential data input, Chan 2-Even	
40	RXinE2+	+ LVDS differential data input, Chan 2-Even	
41	GND	Ground	
42	RXEC-	- LVDS Differential Clock input (Even)	
43	RXEC+	+ LVDS Differential Clock input (Even)	
44	GND	Ground	
45	RXinE3-	- LVDS differential data input, Chan 3-Even	
46	RXinE3+	+ LVDS differential data input, Chan 3-Even	
47	GND	Ground	
48	RXinE4-	- LVDS differential data input, Chan 4-Even	
49	RXinE4+	+ LVDS differential data input, Chan 4-Even	
50	GND	Ground	



[LCD Module Rear View]

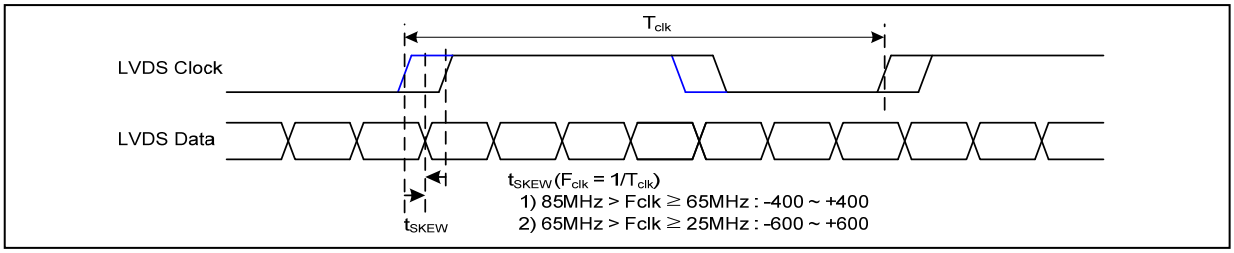
3-3. LVDS Signal Timing Specifications

3-3-1. DC Specification

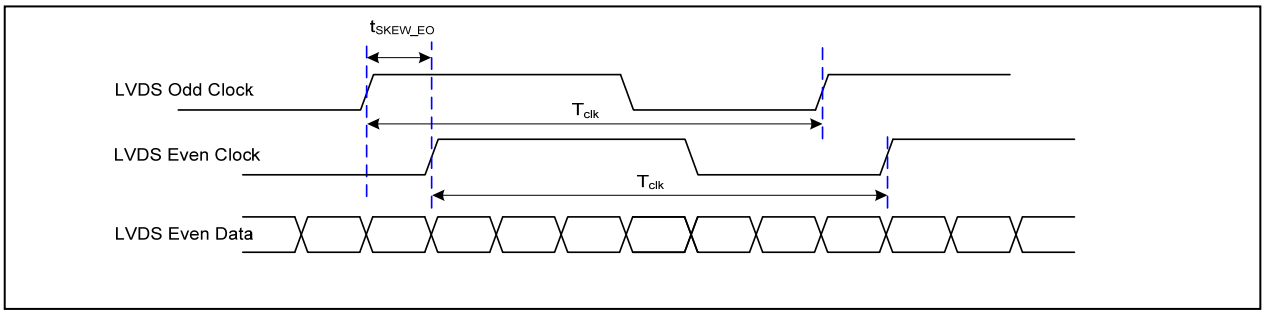


Description	Symbol	Min	Max	Unit	Notes
LVDS Differential Voltage	$\|V_{ID}\|$	100	600	mV	-
LVDS Common mode Voltage	V_{CM}	0.6	1.8	V	-
LVDS Input Voltage Range	V_{IN}	0.3	2.1	V	-

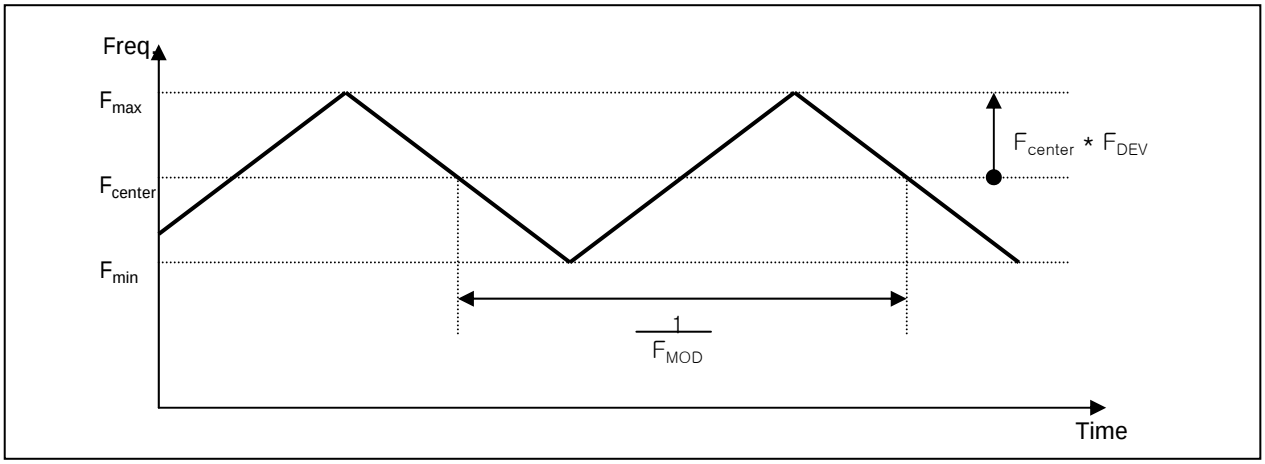
3-3-2. AC Specification



Description	Symbol	Min	Max	Unit	Notes
LVDS Clock to Data Skew Margin	t_{SKEW}	- 400	+ 400	ps	85MHz > Fclk ≥ 65MHz
	t_{SKEW}	- 600	+ 600	ps	65MHz > Fclk ≥ 25MHz
LVDS Clock to Clock Skew Margin (Even to Odd)	t_{SKEW_EO}	- 1/7	+ 1/7	T_{clk}	-
Maximum deviation of input clock frequency during SSC	F_{DEV}	-	± 3	%	-
Maximum modulation frequency of input clock during SSC	F_{MOD}	-	200	KHz	-



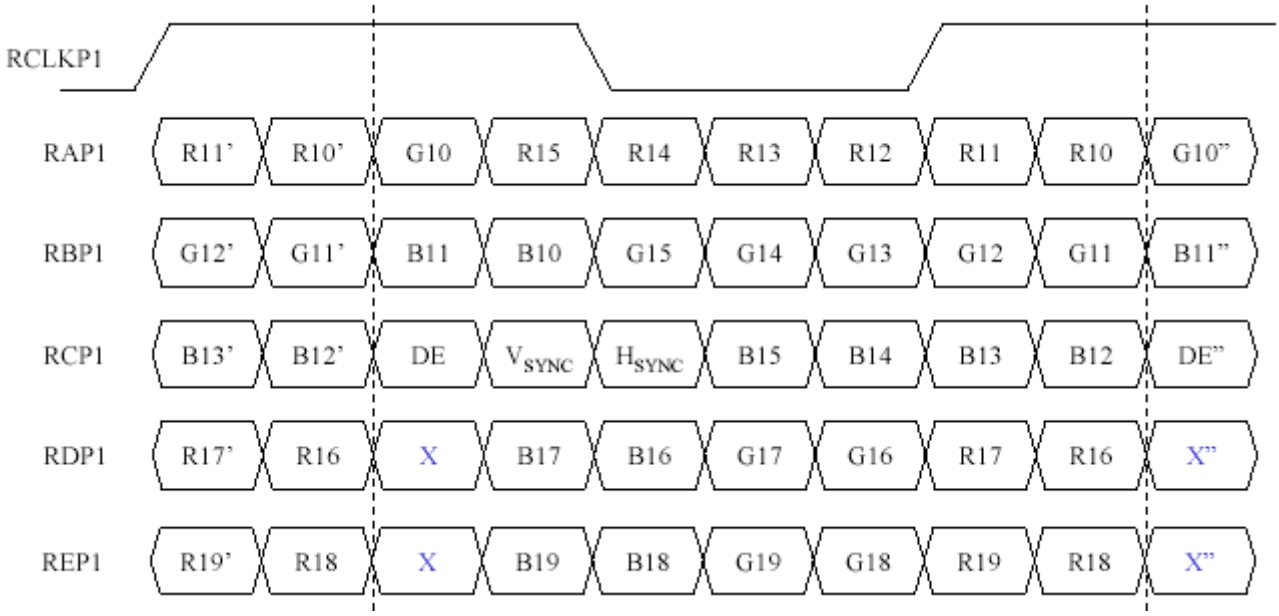
< Clock skew margin between channel >



< Spread Spectrum >

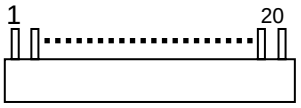
3-3-3. Data Format

1) LVDS Data Port



< LVDS Data Format >

Table 4. BACKLIGHT CONNECTOR PIN CONFIGURATION (CN2)

Pin	Symbol	Description	Notes
1	GND	Ground	1. Connector 1.1 LCD : Hirose DF19KR or equivalent 1.2 Mating : Hirose equivalent. 1.3 Connector pin arrangement  [LCD Module Rear View]
2	VBL+	7V - 20V LED Power	
3	VBL+	7V - 20V LED Power	
4	VBL+	7V - 20V LED Power	
5	VBL+	7V - 20V LED Power	
6	VBL+	7V - 20V LED Power	
7	VBL-	Ground	
8	VBL-	Ground	
9	VBL-	Ground	
10	VBL-	Ground	
11	VBL-	Ground	
12	NC	No Connection	
13	GND	Ground	
14	I2C_DATA	DATA for RGB control	
15	I2C_CLK	CLK for RGB control	
16	GND	Ground	
17	BL_Enable	BL On/Off Control (On: 3.0V ~ 3.6V, Off: 0V ~ 0.5V)	
18	BLIM	PWM for Luminance Control (200~1KHz, 3.3V, 5~100%) or DC(0~3.3v)	
19	Reserved	Reserved	
20	GND	Ground	

3-3. Signal Timing Specifications

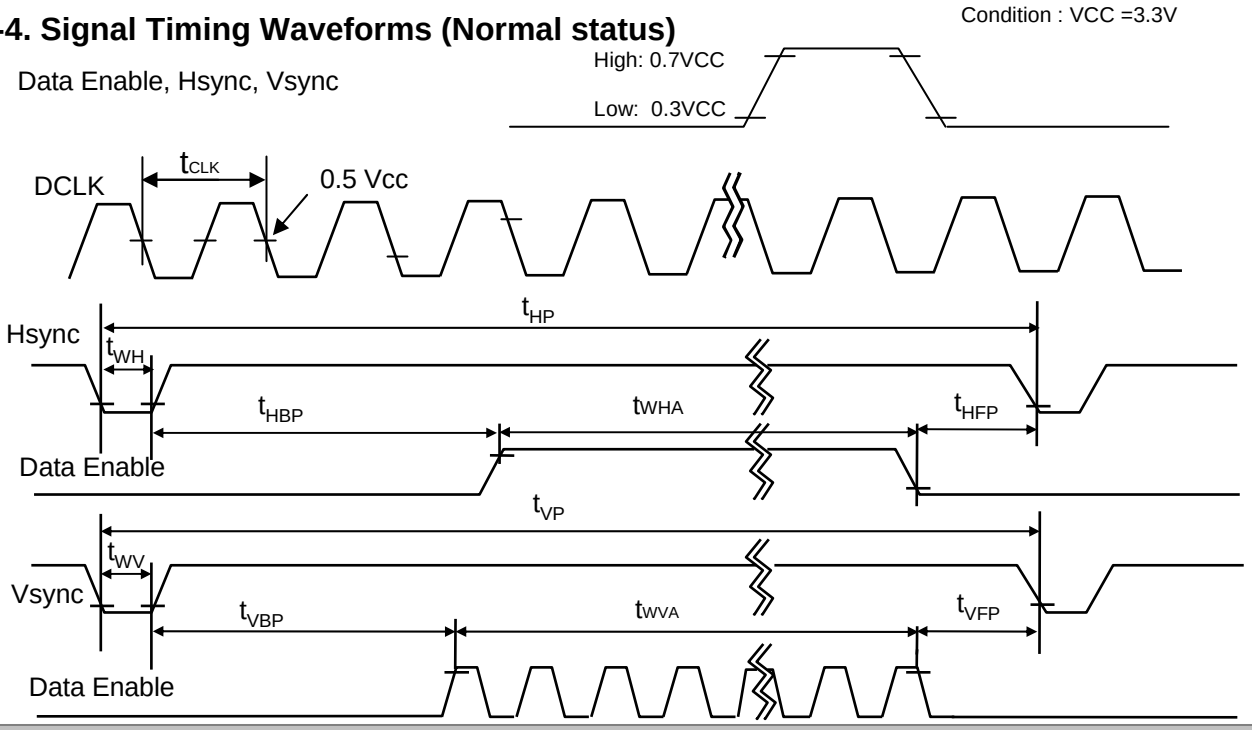
This is the signal timing required at the input of the User connector. All of the interface signal timing should be satisfied with the following specifications and specifications of LVDS Tx/Rx for its proper operation.

Table 5. TIMING TABLE

ITEM	Symbol		Min	Typ	Max	Unit	Note
DCLK	Frequency	f_{CLK}	67.17	69.35	72.65	MHz	LVDS 2 Port
Hsync	Period	t_{HP}	1020	1040	1078	tCLK	
	Width	t_{WH}	16	16	16		
	Width-Active	t_{WHA}	960	960	960		
Vsync	Period	t_{VP}	1096	1111	1122	tHP	
	Width	t_{WV}	5	5	5		
	Width-Active	t_{WVA}	1080	1080	1080		
Data Enable	Horizontal back porch	t_{HBP}	34	40	50	tCLK	
	Horizontal front porch	t_{HFP}	10	24	52		
	Vertical back porch	t_{VBP}	10	23	28	tHP	
	Vertical front porch	t_{VFP}	1	3	9		

Appendix) 1) All reliabilities are specified for timing specification based on refresh rate of 60 Hz. Even though actual performance in 50Hz and 48Hz for low power is displayed normally, remark and inform to user that display quality in 50 Hz and 48 Hz is out of guarantee range.
2) Timing is controlled by EEDID Timing at refresh rate of 60Hz. All display quality is guaranteed based on refresh rate of 60Hz controlled by EEDID timing.

3-4. Signal Timing Waveforms (Normal status)



3-5. Color Input Data Reference

The brightness of each primary color (red,green and blue) is based on the 10-bit gray scale data input for the color ; the higher the binary input, the brighter the color. The table below provides a reference for color versus data input.

Table 6. COLOR DATA REFERENCE

Color		Input Color Data																													
		RED										GREEN										BLUE									
		MSB									LSB	MSB									LSB	MSB									LSB
		R9	R8	R7	R6	R5	R4	R3	R2	R1	R0	G9	G8	G7	G6	G5	G4	G3	G2	G1	G0	B9	B8	B7	B6	B5	B4	B3	B2	B1	B0
Basic Color	Black	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red (1023)	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Green (1023)	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0
	Blue (1023)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1
	Cyan	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
	Magenta	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1
	Yellow	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0
	White	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
RED	RED (000)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	RED (001)	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	...					...										...										...					
	RED (1022)	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	RED (1023)	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
GREEN	GREEN (000)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	GREEN (001)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0
	...					...										...										...					
	GREEN (1022)	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0
	GREEN (1023)	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0
BLUE	BLUE (000)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	BLUE (001)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1
	...					...										...										...					
	BLUE (1022)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	0
	BLUE (1023)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1

3-6. Power Sequence

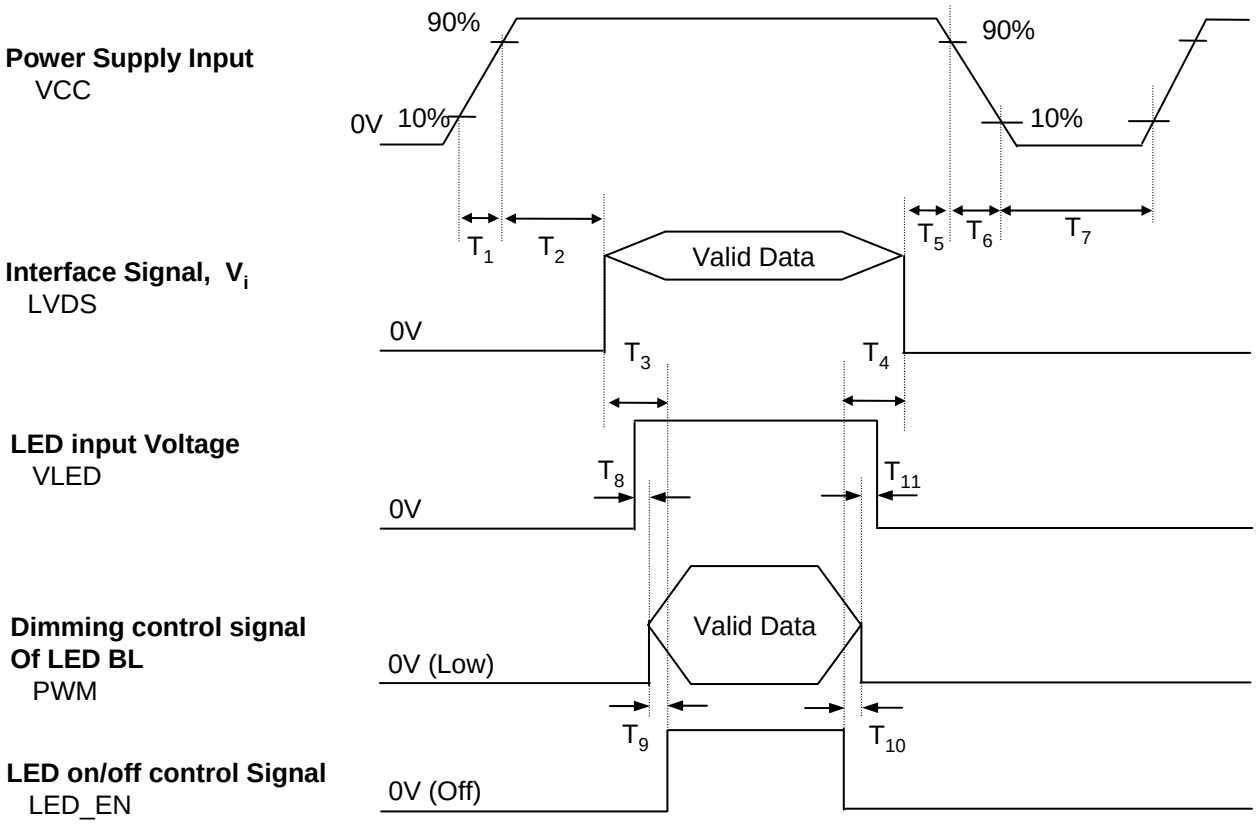


Table 6. POWER SEQUENCE TABLE

Parameter	Value			Units
	Min.	Typ.	Max.	
T_1	0.5	-	10	ms
T_2	0	-	50	ms
T_3	300	-	-	ms
T_4	300	-	-	ms
T_5	0	-	50	ms
T_6	3	-	10	ms
T_7	400	-	-	ms
T_8	10	-	-	ms
T_9	10	-	-	ms
T_{10}	10	-	-	ms
T_{11}	10	-	-	ms

Note)
1. Valid Data is Data to meet “3-3. LVDS Signal Timing Specifications”
2. Please avoid floating state of interface signal at invalid period.
3. When the interface signal is invalid, be sure to pull down the power supply for LCD VCC to 0V.
4. Lamp power must be turn on after power supply for LCD and interface signal are valid.

4. Optical Specification

Optical characteristics are determined after the unit has been 'ON' and stable for approximately 30 minutes in a dark environment at 25°C. The values specified are at an approximate distance 50cm from the LCD surface at a viewing angle of Φ and Θ equal to 0°.
FIG. 1 presents additional information concerning the measurement equipment and method.

FIG. 1 Optical Characteristic Measurement Equipment and Method

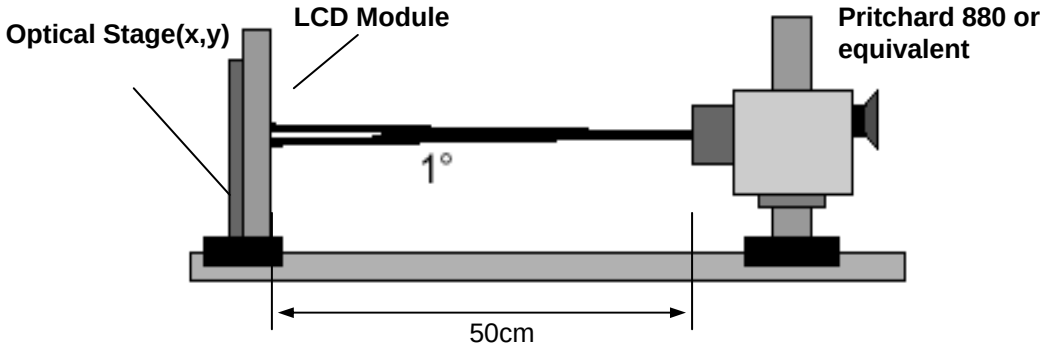


Table 8. OPTICAL CHARACTERISTICS

Ta=25°C, VCC=3.3V, fv=60Hz, f_{CLK}= 69.35MHz(LVDS 2Port), Finished Color Calibration

Parameter		Symbol	Values			Units	Notes
			Min	Typ	Max		
Contrast Ratio		CR	600	800	-		1
Surface Luminance, white		L_{WH}	250	300	-	cd/m²	2
Luminance Variation		δ_{WHITE}	-	1.4	1.6		3
Response Time							4
Rise Time+Decay Time (W to B)		$Tr_{R+}Tr_D$	-	35	50	ms	
Color Coordinates							
	RED	RX	0.652	0.682	0.712		
		RY	0.275	0.305	0.335		
	GREEN	GX	0.169	0.199	0.229		
		GY	0.691	0.721	0.751		
	BLUE	BX	0.121	0.151	0.181		
		BY	0.015	0.045	0.075		
	WHITE	WX	0.283	0.313	0.343		
		WY	0.299	0.329	0.359		
Viewing Angle							5
x axis, right(Φ=0°)		Θr	80	89	-	degree	
x axis, left (Φ=180°)		Θl	80	89	-	degree	
y axis, up (Φ=90°)		Θu	80	89	-	degree	
y axis, down (Φ=270°)		Θd	80	89	-	degree	

Note)

1. Contrast Ratio(CR) is defined mathematically as

$$\text{Contrast Ratio} = \frac{\text{Surface Luminance with all white pixels}}{\text{Surface Luminance with all black pixels}}$$

2. Surface luminance is the 5point (1~5)average across the LCD surface 50cm from the surface with all pixels displaying white Luminance (300nit). For more information see FIG 2.

3. Luminance % uniformity is measured for 13 point For more information see FIG 2.
   δ WHITE = Maximum(LN1,LN2, ….. LN13) ÷ Minimum(LN1,LN2, ….. LN13)

4. Response time is the time required for the display to transition from white to black (rise time, Tr_R) and from black to white(Decay Time, Tr_D). For additional information see FIG 3.

5. Viewing angle is the angle at which the contrast ratio is greater than 10. The angles are determined for the horizontal or x axis and the vertical or y axis with respect to the z axis which is normal to the LCD surface. For more information see FIG 4.

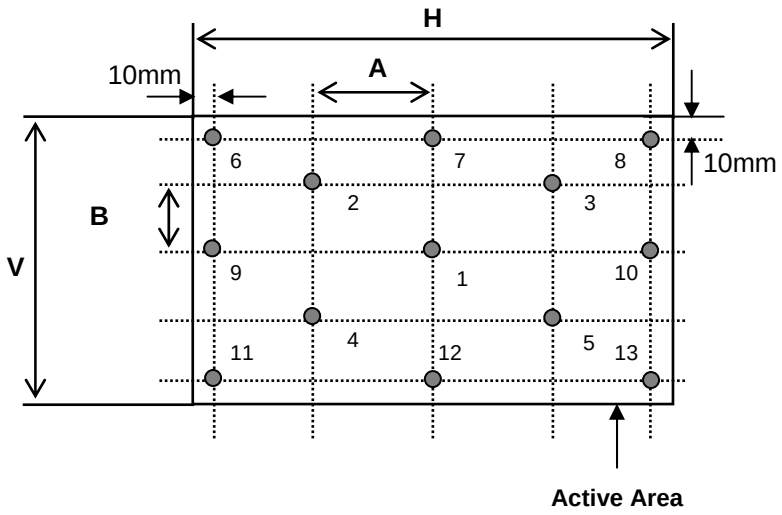
6. Gray scale specification * f_V=60Hz

Gray Level	Luminance [%] (Typ)
L0	0.10
L63	0.23
L127	0.79
L191	2.13
L255	4.49
L319	7.70
L383	11.7
L447	16.3
L511	21.4
L575	27.9
L639	35.2
L703	43.1
L767	51.8
L831	62.1
L895	74.4
L959	87.6
L1023	100

-. △L Reference Level : 16 steps from gray 0 to gray 1023

FIG. 2 Luminance

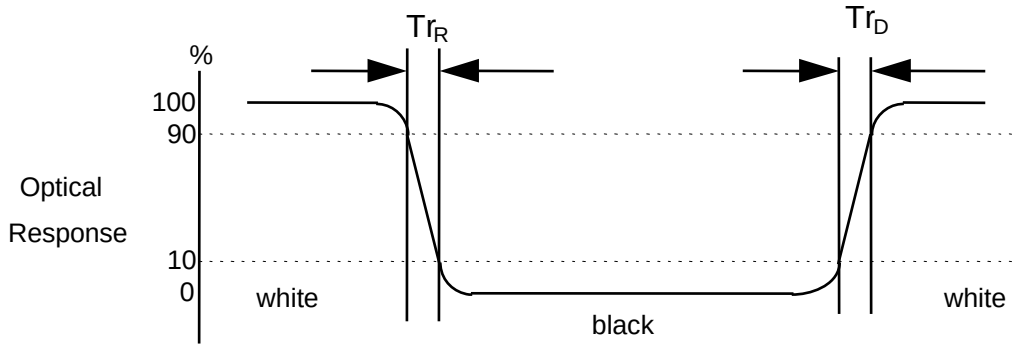
<measuring point for surface luminance & measuring point for luminance variation>



H,V : ACTIVE AREA
A : H/4 mm
B : V/4 mm
POINTS: 13 POINTS

FIG. 3 Response Time

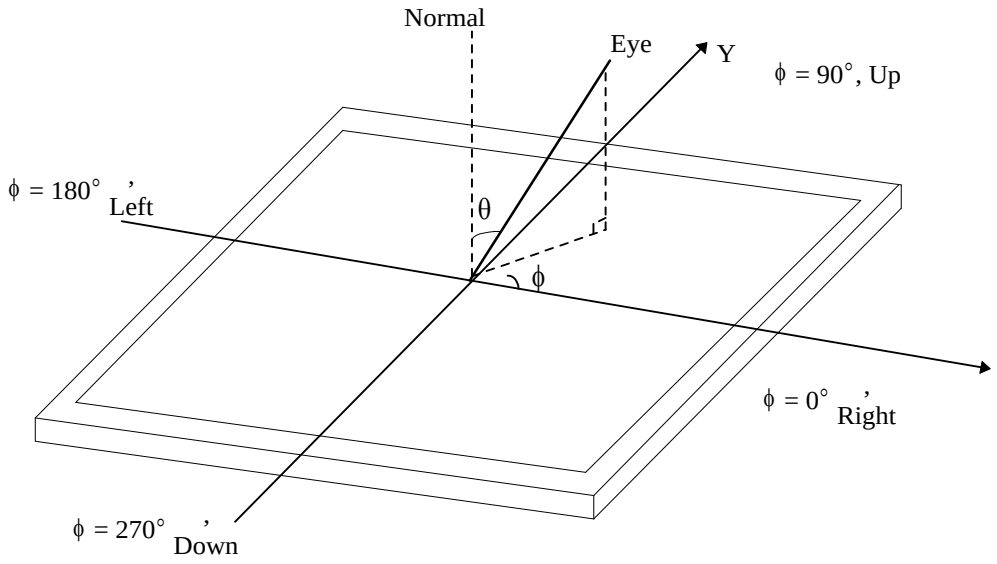
The response time is defined as the following figure and shall be measured by switching the input signal for “black” and “white” In condition of RGB LED Duty 100%



In other condition (For example, RGB LED Duty 80%), The response time defined as measurement data which is not lack

FIG. 4 Viewing angle

<Dimension of viewing angle range>



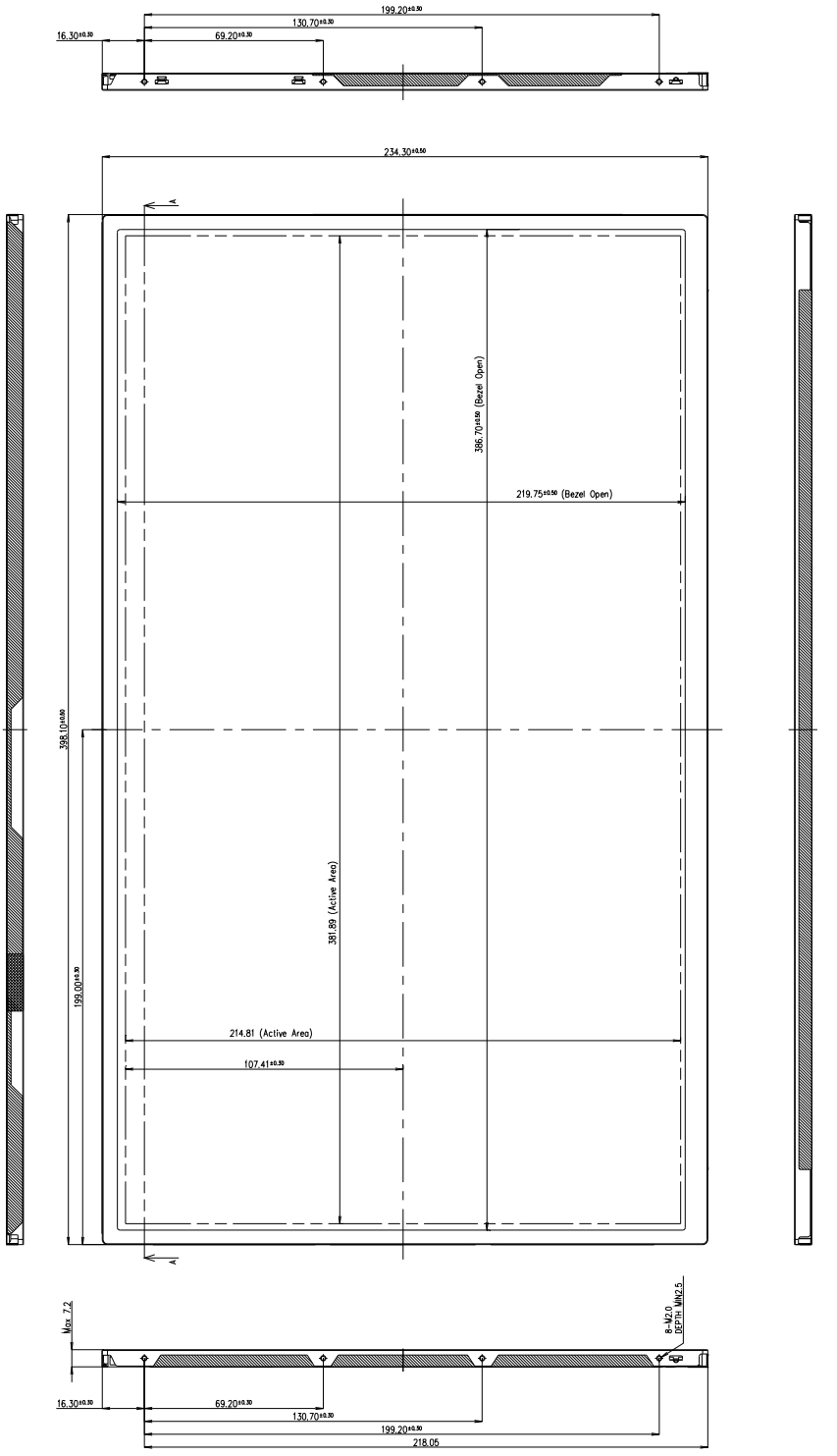
5. Mechanical Characteristics

The contents provide general mechanical characteristics for the model LP173WF3(SLB3). In addition the figures in the next page are detailed mechanical drawing of the LCD.

Outline Dimension	Horizontal	398.1 ± 0.5 mm
	Vertical	234.3 ± 0.5 mm
	Depth (Max)	7.2 mm
Bezel Area	Horizontal	386.70(H)
	Vertical	219.75(V)
Active Display Area	Horizontal	381.90 mm
	Vertical	214.80 mm
Weight	830 g (MAX)	
Surface Treatment	Hard coating(3H), Anti-Glare treatment of the front polarizer	

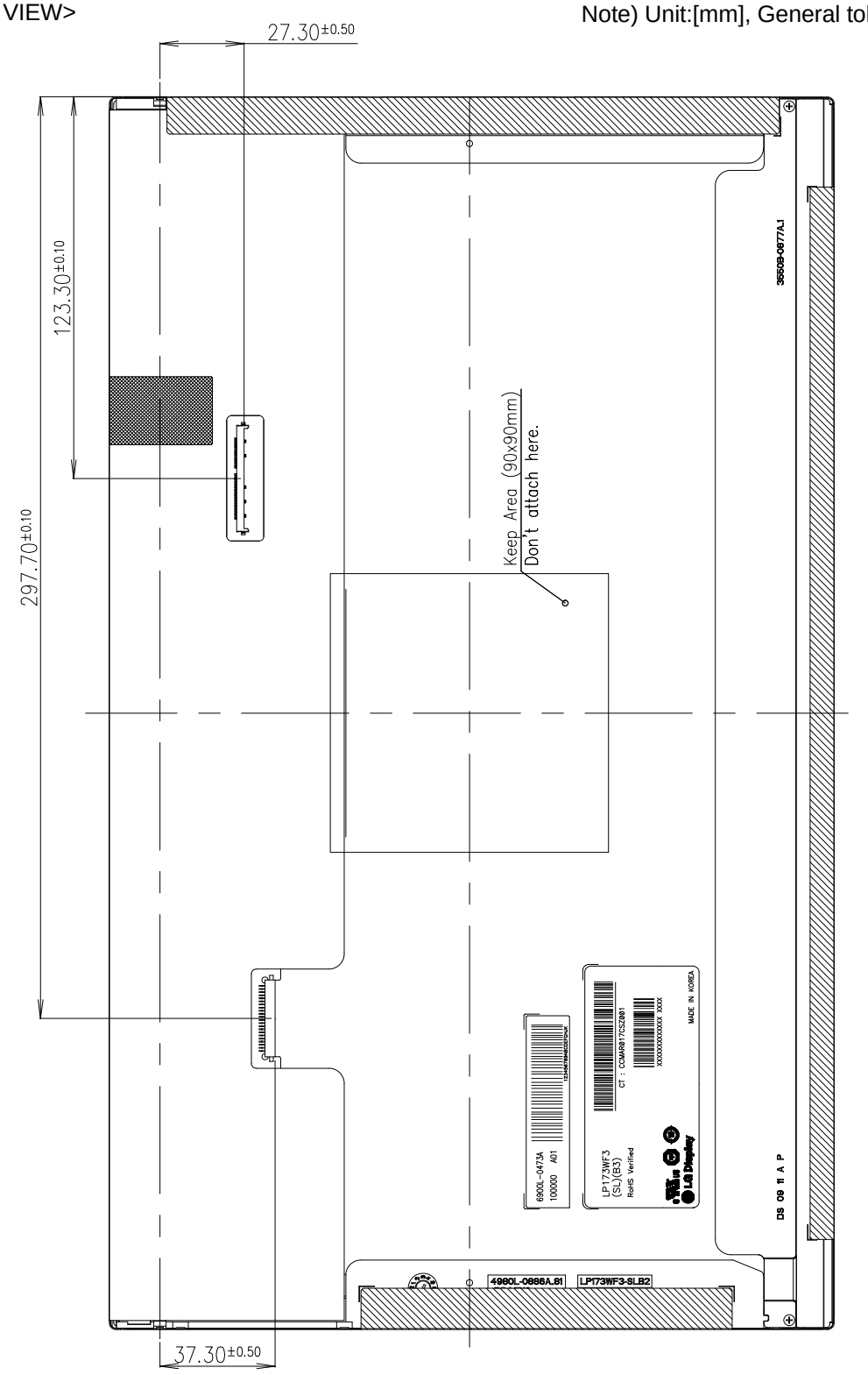
<FRONT VIEW>

Note) Unit:[mm], General tolerance: ± 0.5mm

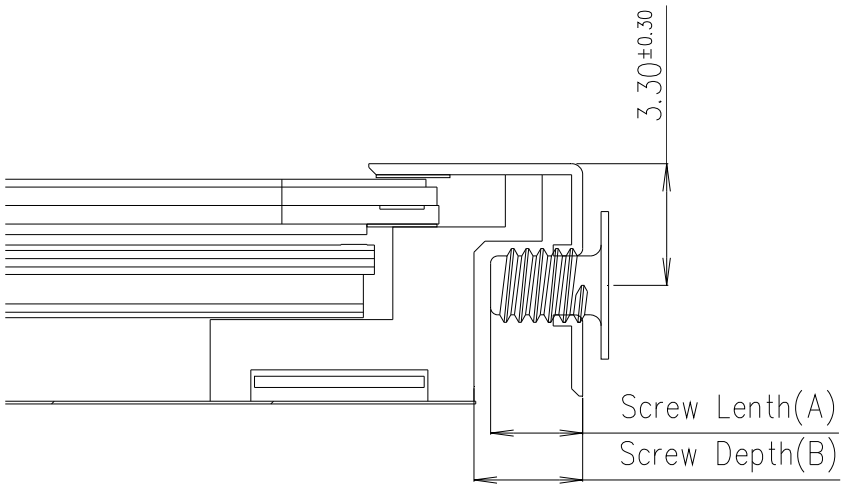


<REAR VIEW>

Note) Unit:[mm], General tolerance: ± 0.5mm



[DETAIL DESCRIPTION OF SIDE MOUNTING SCREW]



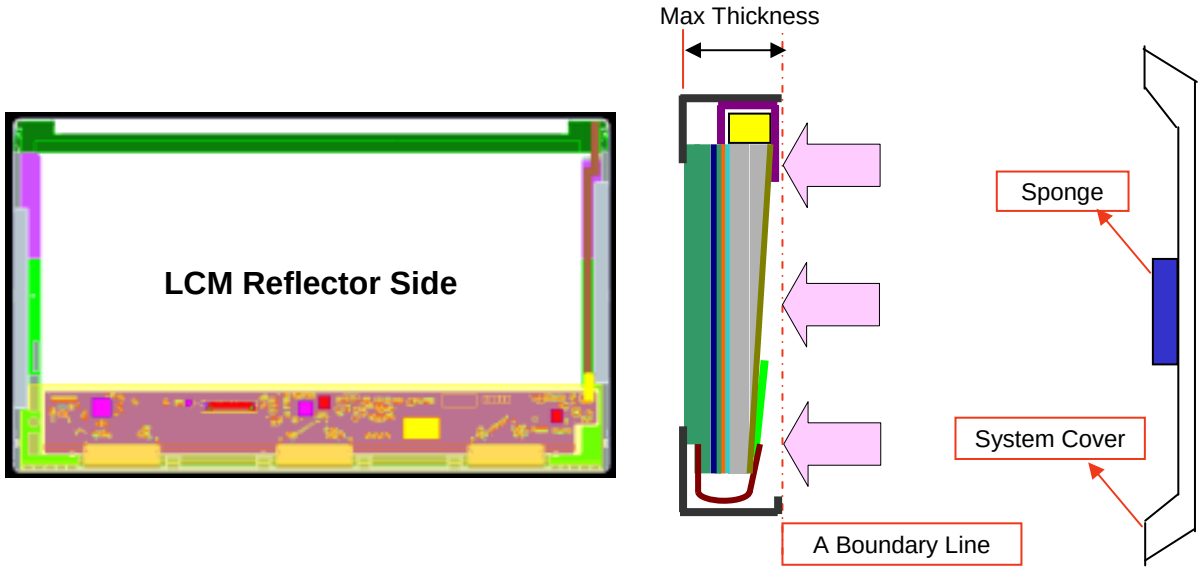
* Screw Length(A) : Max : 2.5, Min : 2.0
* Screw Depth(B) : Min 2.5
* Screw Torque : Max 2.5kgf.cm
(Measurement Gauge: Torque Meter)

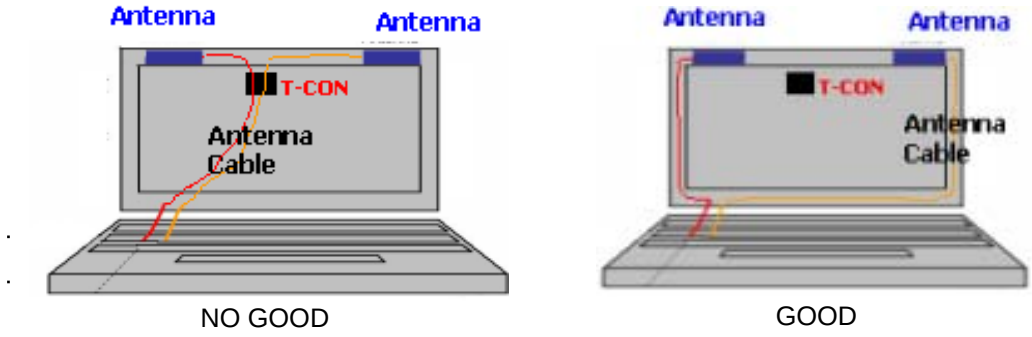
Notes : 1. Screw plated through the method of non-electrolytic nickel plating is preferred to reduce possibility that results in vertical and/or horizontal line defect due to the conductive particles from screw surface.

Note) Unit:[mm], General tolerance: ± 0.5mm

LGD Proposal for system cover design.(Appendix)

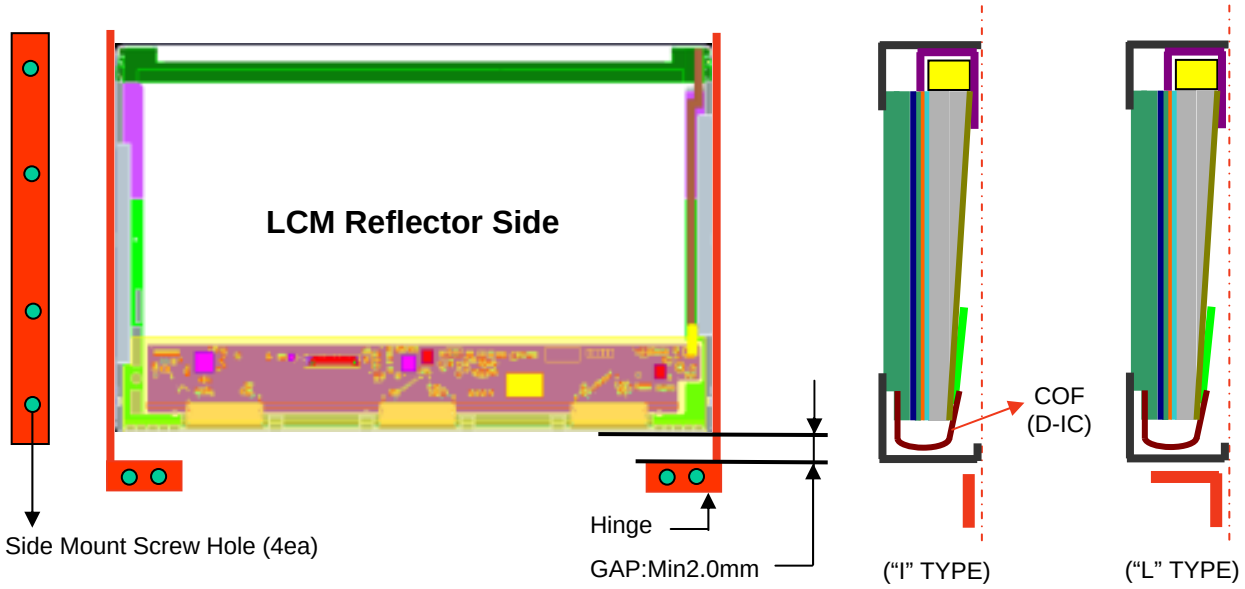
1	Gap check for securing the enough gap between LCM and System cover.	

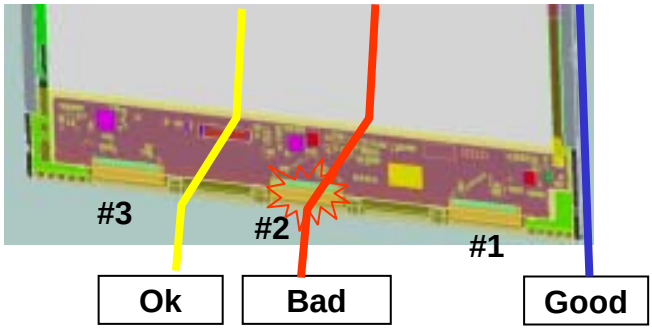


Define	1.Rear side of LCM is sensitive against external stress,and previous check about interference is highly needed. 2.In case there is something from system cover comes into the boundary above,mechanical interference may cause the FOS defects. (Eg:Ripple,White spot..)
2	Check if antenna cable is sufficiently apart from T-CON of LCD Module.
Define	
	1.If system antenna is overlapped with T-CON,it might be cause the noise.

LGD Proposal for system cover design.

3	Gap check for securing the enough gap between LCM and System hinge.	

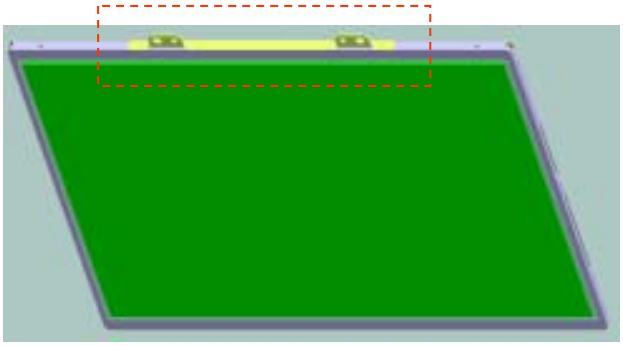


Define	1.At least 2.0mm of gap needs to be secured to prevent the shock related defects. 2."L" type of hinge is recommended than "I" type under shock test.
4	Checking the path of the System wire.
	
Define	1.COF area needs to be handled with care. 2.GOOD ➔Wire path design to system side. OK➔ Wire path is located between COFs. BAD➔Wire path overlapped with COF area.

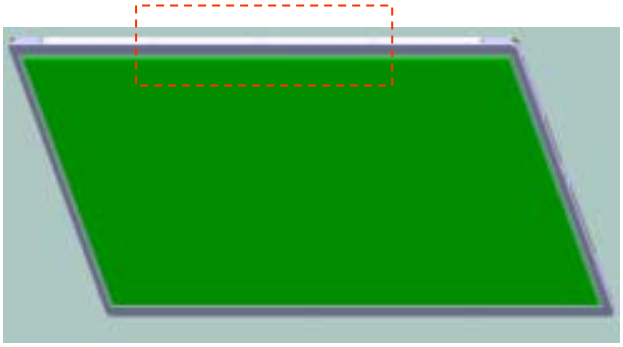
LGD Proposal for system cover design.

5	Using a bracket on the top of LCM is not recommended.	

bracket

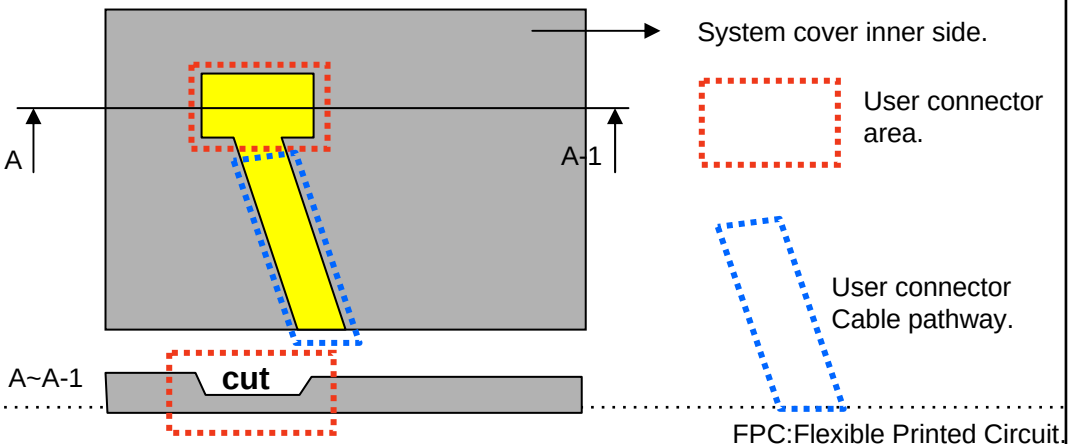


With bracket



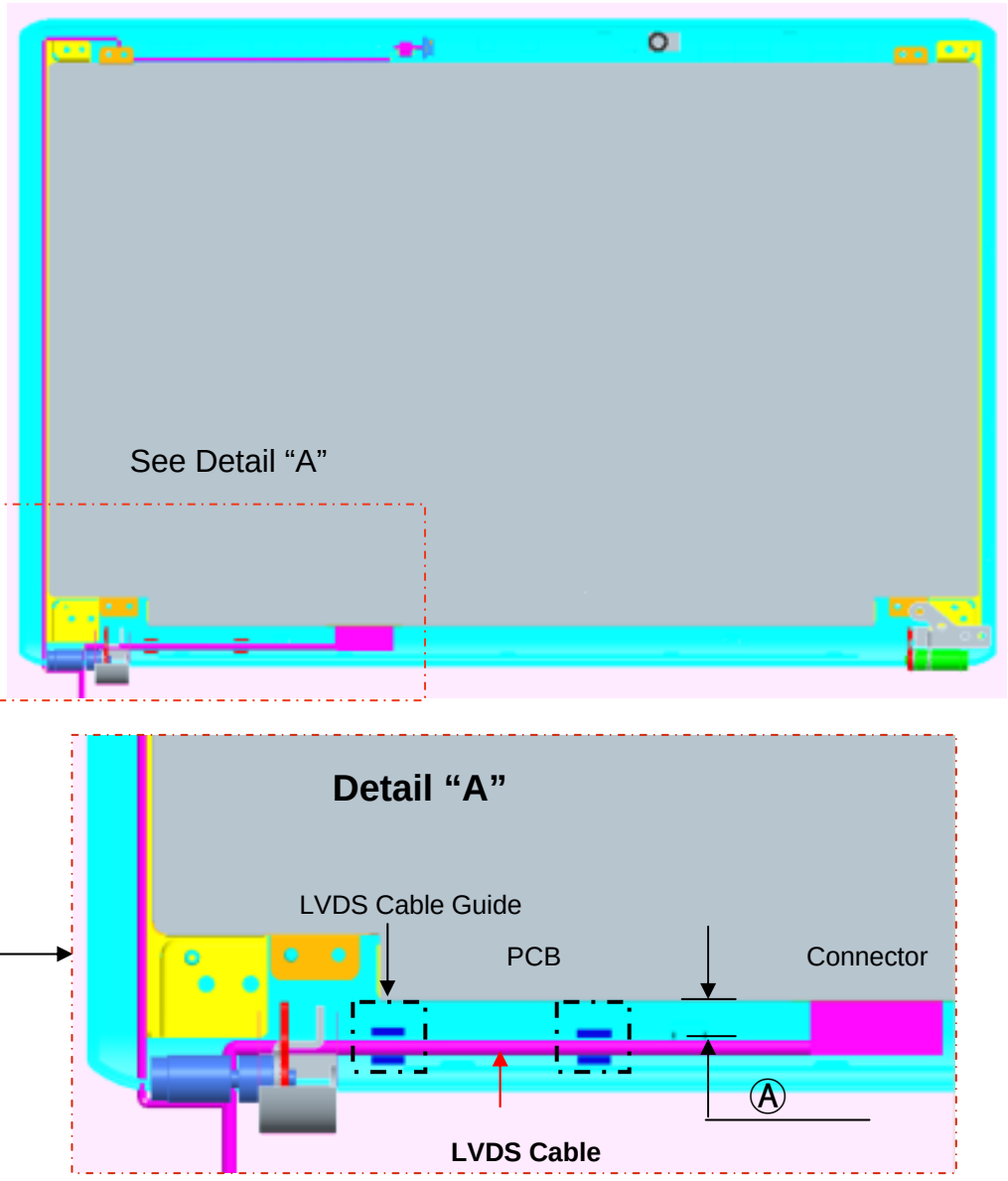
Without bracket

Define	1.Condition without bracket is good for mechanical noise,and can minimize the light leakage from deformation of bracket. 2.The results shows that there is no difference between the condition with or without bracket.
6	Securing additional gap on CNT area..



Define	1.CNT area is specially sensitive against external stress,and additional gap by cutting on system cover will be helpful on removing the Ripple. 2.Using a thinner CNT will be better. (eg: FPC type)

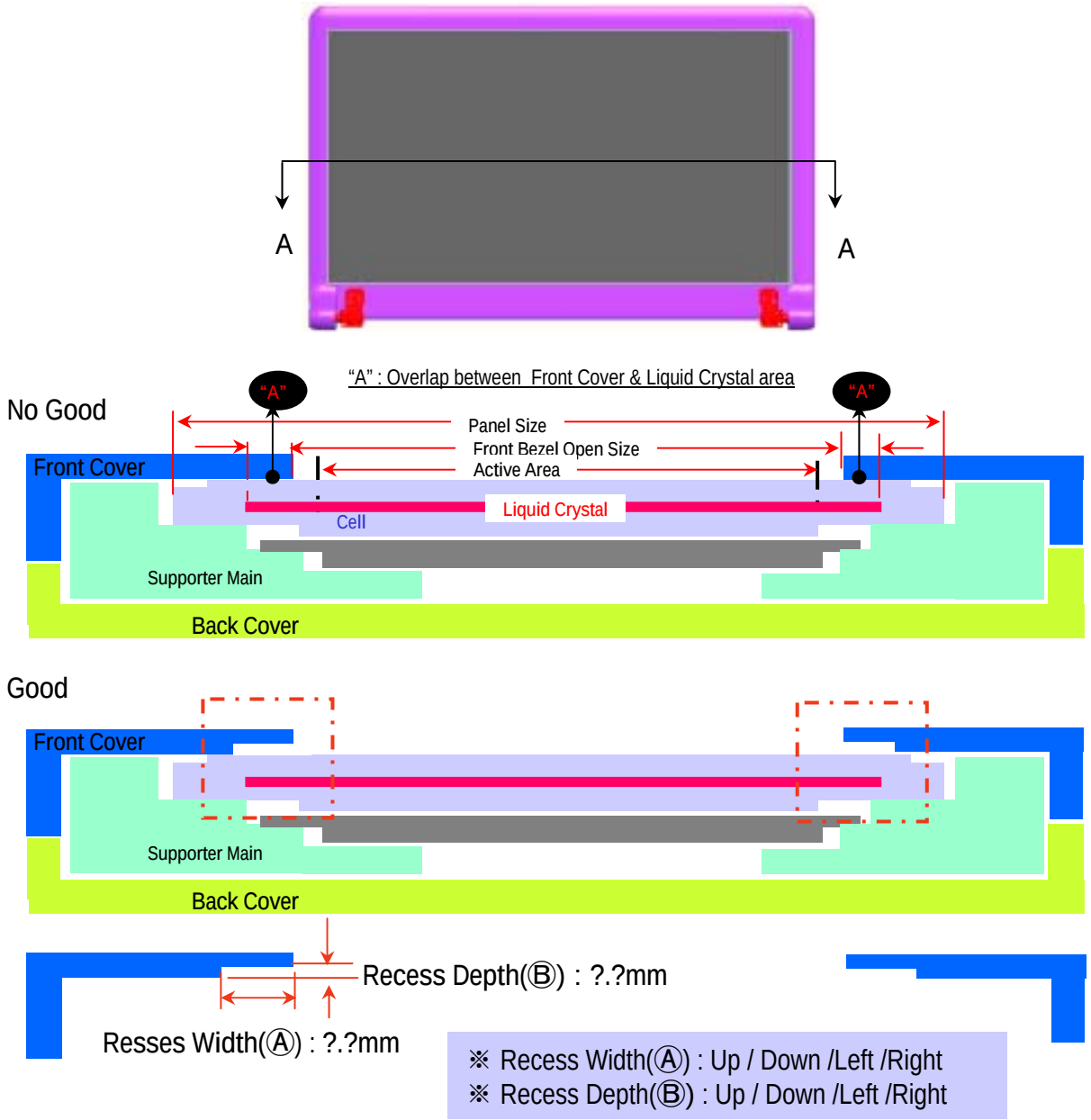
7	Checking the path of the System LVDS Cable.



Define	1.At least 1.0mm of gap needs to be secured to prevent the overlap between LVDS cable and PCB.(Ⓐ ≥ 1.0mm) (This overlap may cause a Abnormal Display after hinge test)
	2.”Flat” type of LVDS cable is recommended than “Cylinderical” type . 3. Making LVDS Cable Guide will be better.(Refer to detail “A”)

LGD Proposal for system cover design.

8	Securing additional gap between front cover & LCD at edge of front cover.



Define	1.Liquid Crystal area is sensitive against external stress, so additional gap by making recess area at the edge of front cover will be helpful on removing a Ripple.(Dimension of Recess depends on each model)

6. Reliability

Environment test condition

No.	Test Item	Conditions
1	High temperature storage test	Ta= 60°C, 240h
2	Low temperature storage test	Ta= -20°C, 240h
3	High temperature operation test	Ta= 50°C, 50%RH, 240h
4	Low temperature operation test	Ta= 0°C, 240h
5	Vibration test (non-operating)	Sine wave, 5 ~ 150Hz, 1.5G, 0.37oct/min 3 axis, 30min/axis
6	Shock test (non-operating)	- No functional or cosmetic defects following a shock to all 6 sides delivering at least 200 G in a half sine pulse no longer than 2 ms to the display module - No functional defects following a shock delivering at least 260 g in a half sine pulse no longer than 2 ms to each of 6 sides. Each of the 6 sides will be shock tested with one each display, for a total of 6 displays
7	Altitude operating storage / shipment	0 ~ 10,000 feet (3,048m) 24Hr 0 ~ 40,000 feet (12,192m) 24Hr

{ Result Evaluation Criteria }
There should be no change which might affect the practical display function when the display quality test is conducted under normal operating condition.

7. International Standards

7-1. Safety

a) UL 60950-1, Second Edition, Underwriters Laboratories Inc.
Information Technology Equipment - Safety - Part 1 : General Requirements.

b) CAN/CSA C22.2 No.60950-1-07, Second Edition, Canadian Standards Association.
Information Technology Equipment - Safety - Part 1 : General Requirements.

c) EN 60950-1:2006 + A11:2009, European Committee for Electrotechnical Standardization(CENELEC).
Information Technology Equipment - Safety - Part 1 : General Requirements.

d) IEC 60950-1:2005, Second Edition, The International Electrotechnical Commission (IEC).
Information Technology Equipment - Safety - Part 1 : General Requirements.

7-2. EMC

a) ANSI C63.4 – 2003 “American National Standard for Methods of Measurement of Radio-Noise Emissions from Low-Voltage Electrical and Electronic Equipment in the Range of 9 kHz to 40 GHz.” American National Standards Institute (ANSI), 2003.

b) C.I.S.P.R. Pub. 22. Limits and methods of measurement of radio interference characteristics of information technology equipment." International Special Committee on Radio Interference (C.I.S.P.R.), 2005.

c) EN 55022 "Limits and methods of measurement of radio interference characteristics of information technology equipment." European Committee for Electrotechnical Standardization (CENELEC), 2006.

7-3. Environment

a) RoHS, Directive 2002/95/EC of the European Parliament and of the council of 27 January 2003

8. Packing

8-1. Designation of Lot Mark

a) Lot Mark

A	B	C	D	E	F	G	H	I	J	K	L	M

A,B,C : SIZE(INCH)
D : YEAR
E : MONTH
F ~ M : SERIAL NO.

Note

1. YEAR

Year	2011	2012	2013	2014	2015	2016	2017	2018	2019	2020
Mark	A	B	C	D	E	F	G	H	J	K

2. MONTH

Month	Jan	Feb	Mar	Apr	May	Jun	Jul	Aug	Sep	Oct	Nov	Dec
Mark	1	2	3	4	5	6	7	8	9	A	B	C

b) Location of Lot Mark

Serial No. is printed on the label. The label is attached to the backside of the LCD module.
This is subject to change without prior notice.

8-2. Packing Form

a) Package quantity in one box : 20ea

b) Box Size : 480*380*280

9. PRECAUTIONS

Please pay attention to the followings when you use this TFT LCD module.

9-1. MOUNTING PRECAUTIONS

(1) You must mount a module using holes arranged in four corners or four sides.
(2) You should consider the mounting structure so that uneven force (ex. Twisted stress) is not applied to the module. And the case on which a module is mounted should have sufficient strength so that external force is not transmitted directly to the module.
(3) Please attach the surface transparent protective plate to the surface in order to protect the polarizer. Transparent protective plate should have sufficient strength in order to the resist external force.
(4) You should adopt radiation structure to satisfy the temperature specification.
(5) Acetic acid type and chlorine type materials for the cover case are not desirable because the former generates corrosive gas of attacking the polarizer at high temperature and the latter causes circuit break by electro-chemical reaction.
(6) Do not touch, push or rub the exposed polarizers with glass, tweezers or anything harder than HB pencil lead. And please do not rub with dust clothes with chemical treatment.
Do not touch the surface of polarizer for bare hand or greasy cloth.(Some cosmetics are detrimental to the polarizer.)
(7) When the surface becomes dusty, please wipe gently with absorbent cotton or other soft materials like chamois soaks with petroleum benzene. Normal-hexane is recommended for cleaning the adhesives used to attach front / rear polarizers. Do not use acetone, toluene and alcohol because they cause chemical damage to the polarizer.
(8) Wipe off saliva or water drops as soon as possible. Their long time contact with polarizer causes deformations and color fading.
(9) Do not open the case because inside circuits do not have sufficient strength.

9-2. OPERATING PRECAUTIONS

(1) The spike noise causes the mis-operation of circuits. It should be lower than following voltage :
V=± 200mV(Over and under shoot voltage)

(2) Response time depends on the temperature.(In lower temperature, it becomes longer.)
(3) Brightness depends on the temperature. (In lower temperature, it becomes lower.)
And in lower temperature, response time(required time that brightness is stable after turned on) becomes longer.
(4) Be careful for condensation at sudden temperature change. Condensation makes damage to polarizer or electrical contacted parts. And after fading condensation, smear or spot will occur.
(5) When fixed patterns are displayed for a long time, remnant image is likely to occur.
(6) Module has high frequency circuits. Sufficient suppression to the electromagnetic interference shall be done by system manufacturers. Grounding and shielding methods may be important to minimized the interference.

9-3. ELECTROSTATIC DISCHARGE CONTROL

Since a module is composed of electronic circuits, it is not strong to electrostatic discharge. Make certain that treatment persons are connected to ground through wrist band etc. And don't touch interface pin directly.

9-4. PRECAUTIONS FOR STRONG LIGHT EXPOSURE

Strong light exposure causes degradation of polarizer and color filter.

9-5. STORAGE

When storing modules as spares for a long time, the following precautions are necessary.

(1) Store them in a dark place. Do not expose the module to sunlight or fluorescent light. Keep the temperature between 5°C and 35°C at normal humidity.
(2) The polarizer surface should not come in contact with any other object.
It is recommended that they be stored in the container in which they were shipped.

9-6. HANDLING PRECAUTIONS FOR PROTECTION FILM

(1) When the protection film is peeled off, static electricity is generated between the film and polarizer. This should be peeled off slowly and carefully by people who are electrically grounded and with well ion-blown equipment or in such a condition, etc.
(2) The protection film is attached to the polarizer with a small amount of glue. If some stress is applied to rub the protection film against the polarizer during the time you peel off the film, the glue is apt to remain on the polarizer.
Please carefully peel off the protection film without rubbing it against the polarizer.
(3) When the module with protection film attached is stored for a long time, sometimes there remains a very small amount of glue still on the polarizer after the protection film is peeled off.
(4) You can remove the glue easily. When the glue remains on the polarizer surface or its vestige is recognized, please wipe them off with absorbent cotton waste or other soft material like chamois soaked with normal-hexane.

APPENDIX A. Enhanced Extended Display Identification Data (EEDID™) 1/3

EDID Data for *HP Dream Color* _ ver. 0.0

2010/10/27

	Byte (Dec)	Byte (Hex)	Field Name and Comments	Value (Hex)	Value (Bin)
Header	0	00	Header	00	00000000
	1	01	Header	FF	11111111
	2	02	Header	FF	11111111
	3	03	Header	FF	11111111
	4	04	Header	FF	11111111
	5	05	Header	FF	11111111
	6	06	Header	FF	11111111
	7	07	Header	00	00000000
Vendor / Product EDID Version	8	08	ID Manufacture Name LGD	30	00110000
	9	09	ID Manufacture Name	E4	11100100
	10	0A	ID Product Code 02FCh	FC	11111100
	11	0B	(Hex. LSB first)	02	00000010
	12	0C	ID Serial No. - Optional ("00h" If not used, Number Only and LSB First)	00	00000000
	13	0D	ID Serial No. - Optional ("00h" If not used, Number Only and LSB First)	00	00000000
	14	0E	ID Serial No. - Optional ("00h" If not used, Number Only and LSB First)	00	00000000
	15	0F	ID Serial No. - Optional ("00h" If not used, Number Only and LSB First)	00	00000000
	16	10	Week of Manufacture - Optinal 00 weeks	00	00000000
	17	11	Year of Manufacture 2010 years	14	00010100
	18	12	EDID structure version # = 1	01	00000001
	19	13	EDID revision # = 4	04	00000100
Display Parameters	20	14	Video input Definition = Input is a Digital Video signal Interface , Colo Bit Depth : 10 Bits per Primary Color , Digital Video Interface Standard Supported: Digital Interface is not defined	B0	10110000
	21	15	Horizontal Screen Size (Rounded cm) = 38 cm38 cm	26	00100110
	22	16	Vertical Screen Size (Rounded cm) = 21 cm21 cm	15	00010101
	23	17	Display Transfer Characteristic (Gamma) = (gamma*100)-100 = Example:(2.2*100)-100=120 = 2.2 Gamma	78	01111000
	24	18	Feature Support [Display Power Management(DPM) : Standby Mode is not supported, Suspend Mode is not supported, Active Off = Very Low Power is not supported ,Supportted Color Encoding Formats : RGB 4:4:4 & YCrCb 4:4:4 ,Other Feature Support Flags : No_sRGB, Preferred Timing Mode, No_Display is continuous frequency (Multi-mode_Base EDID and Extension Block).]	0A	00001010
Panel Color Coordinates	25	19	Red/Green Low Bits (RxRy/GxGy)	B8	10111000
	26	1A	Blue/White Low Bits (BxBy/WxWy)	25	00100101
	27	1B	Red X Rx = 0.686	AF	10101111
	28	1C	Red Y Ry = 0.308	4E	01001110
	29	1D	Green X Gx = 0.213	36	00110110
	30	1E	Green Y Gy = 0.715	B7	10110111
	31	1F	Blue X Bx = 0.145	25	00100101
	32	20	Blue Y By = 0.045	0B	00001011
	33	21	White X Wx = 0.313	50	01010000
	34	22	White Y Wy = 0.329	54	01010100
Established Timings	35	23	Established timing 1 (Optional_00h if not used)	00	00000000
	36	24	Established timing 2 (Optional_00h if not used)	00	00000000
	37	25	Manufacturer's timings (Optional_00h if not used)	00	00000000
Standard Timing ID	38	26	Standard timing ID1 (Optional_01h if not used)	01	00000001
	39	27	Standard timing ID1 (Optional_01h if not used)	01	00000001
	40	28	Standard timing ID2 (Optional_01h if not used)	01	00000001
	41	29	Standard timing ID2 (Optional_01h if not used)	01	00000001
	42	2A	Standard timing ID3 (Optional_01h if not used)	01	00000001
	43	2B	Standard timing ID3 (Optional_01h if not used)	01	00000001
	44	2C	Standard timing ID4 (Optional_01h if not used)	01	00000001
	45	2D	Standard timing ID4 (Optional_01h if not used)	01	00000001
	46	2E	Standard timing ID5 (Optional_01h if not used)	01	00000001
	47	2F	Standard timing ID5 (Optional_01h if not used)	01	00000001
	48	30	Standard timing ID6 (Optional_01h if not used)	01	00000001
	49	31	Standard timing ID6 (Optional_01h if not used)	01	00000001
	50	32	Standard timing ID7 (Optional_01h if not used)	01	00000001
	51	33	Standard timing ID7 (Optional_01h if not used)	01	00000001
	52	34	Standard timing ID8 (Optional_01h if not used)	01	00000001
	53	35	Standard timing ID8 (Optional_01h if not used)	01	00000001

APPENDIX A. Enhanced Extended Display Identification Data (EEDID™) 2/3

	Byte (Dec)	Byte (Hex)	Field Name and Comments	Value (Hex)	Value (Bin)
Timing Descriptor #1	54	36	Pixel Clock/10,000 (LSB) 138.7 MHz @ 60Hz	2E	00101110
	55	37	Pixel Clock/10,000 (MSB)	36	00110110
	56	38	Horizontal Active (lower 8 bits) 1920 Pixels	80	10000000
	57	39	Horizontal Blanking(Thp-HA) (lower 8 bits) 160 Pixels	A0	10100000
	58	3A	Horizontal Active / Horizontal Blanking(Thp-HA) (upper 4:4bits)	70	01110000
	59	3B	Vertical Avtive 1080 Lines	38	00111000
	60	3C	Vertical Blanking (Tvp-HA) (DE Blanking typ.for DE only panels) 31 Lines	1F	00011111
	61	3D	Vertical Active : Vertical Blanking (Tvp-HA) (upper 4:4bits)	40	01000000
	62	3E	Horizontal Sync. Offset (Thfp) 48 Pixels	30	00110000
	63	3F	Horizontal Sync Pulse Width (HSPW) 32 Pixels	20	00100000
	64	40	Vertical Sync Offset(Tvfp) : Sync Width (VSPW) 3 Lines : 5 Lines	35	00110101
	65	41	Horizontal Vertical Sync Offset/Width (upper 2bits)	00	00000000
	66	42	Horizontal Image Size (mm) 382 mm	7E	01111110
	67	43	Vertical Image Size (mm) 215 mm	D7	11010111
	68	44	Horizontal Image Size / Vertical Image Size	10	00010000
	69	45	Horizontal Border = 0 (Zero for Notebook LCD)	00	00000000
	70	46	Vertical Border = 0 (Zero for Notebook LCD)	00	00000000
	71	47	Non-Interlace, Normal display, no stereo, Digital Separate [Vsync_NEG, Hsync_NEG (outside of V-sync)]	19	00011001
Timing Descriptor #2	72	48	Pixel Clock/10,000 (LSB) 110.96 MHz @ 48Hz	58	01011000
	73	49	Pixel Clock/10,000 (MSB)	2B	00101011
	74	4A	Horizontal Active (lower 8 bits) 1920 Pixels	80	10000000
	75	4B	Horizontal Blanking(Thp-HA) (lower 8 bits) 160 Pixels	A0	10100000
	76	4C	Horizontal Active / Horizontal Blanking(Thp-HA) (upper 4:4bits)	70	01110000
	77	4D	Vertical Avtive 1080 Lines	38	00111000
	78	4E	Vertical Blanking (Tvp-HA) (DE Blanking typ.for DE only panels) 31 Lines	1F	00011111
	79	4F	Vertical Active : Vertical Blanking (Tvp-HA) (upper 4:4bits)	40	01000000
	80	50	Horizontal Sync. Offset (Thfp) 48 Pixels	30	00110000
	81	51	Horizontal Sync Pulse Width (HSPW) 32 Pixels	20	00100000
	82	52	Vertical Sync Offset(Tvfp) : Sync Width (VSPW) 3 Lines : 5 Lines	35	00110101
	83	53	Horizontal Vertical Sync Offset/Width (upper 2bits)	00	00000000
	84	54	Horizontal Image Size (mm) 382 mm	7E	01111110
	85	55	Vertical Image Size (mm) 215 mm	D7	11010111
	86	56	Horizontal Image Size / Vertical Image Size	10	00010000
	87	57	Horizontal Border = 0 (Zero for Notebook LCD)	00	00000000
	88	58	Vertical Border = 0 (Zero for Notebook LCD)	00	00000000
	89	59	Non-Interlace, Normal display, no stereo, Digital Separate [Vsync_NEG, Hsync_NEG (outside of V-sync)]	19	00011001
Timing Descriptor #3	90	5A	Maximum DCLK (T-CON to Driver IC) Integer Part 144.25 MHz	90	10010000
	91	5B	Maximum DCLK (T-CON to Driver IC) Fractional Part	19	00011001
	92	5C	Minimum DCLK (T-CON to Driver IC) Integer Part 133.15 MHz	85	10000101
	93	5D	Minimum DCLK (T-CON to Driver IC) Fractional Part	0F	00001111
	94	5E	Hblank Maximum Setting (High byte) 248 Pixels	00	00000000
	95	5F	Hblank Maximum Setting (Low Byte)	F8	11111000
	96	60	Hblank Minimum Setting (High byte) 80 Pixels	00	00000000
	97	61	Hblank Minimum Setting (Low Byte)	50	01010000
	98	62	Vblank Maximum Setting (High byte) 31 Pixels (Typical)	00	00000000
	99	63	Vblank Maximum Setting (Low Byte)	1F	00011111
	100	64	Vblank Minimum Setting (High byte) 31 Pixels (Typical)	00	00000000
	101	65	Vblank Minimum Setting (Low Byte)	1F	00011111
	102	66	Type of bus between T-CON and Driver IC Mini-LVDS	01	00000001
	103	67	DCLK Multiplier/Divider Integer between T-CON and Driver IC 1.00 Times	01	00000001
	104	68	DCLK Multiplier/Divider Fractional between T-CON and Driver IC	00	00000000
	105	69	Spread Spectrum Setting between T-Con and Driver IC SS Disabled	00	00000000
	106	6A	Flags	00	00000000
	107	6B	Flags	00	00000000

APPENDIX A. Enhanced Extended Display Identification Data (EEDID™) 3/3

	Byte (Dec)	Byte (Hex)	Field Name and Comments	Value (Hex)	Value (Bin)
Timing Descriptor #4	108	**6C**	Pixel Clock/10,000 (LSB) 115.58 MHz @ 50Hz	**26**	00100110
	109	**6D**	Pixel Clock/10,000 (MSB)	**2D**	00101101
	110	**6E**	Horizontal Active (lower 8 bits) 1920 Pixels	**80**	10000000
	111	**6F**	Horizontal Blanking(Thp-HA) (lower 8 bits) 160 Pixels	**A0**	10100000
	112	**70**	Horizontal Active / Horizontal Blanking(Thp-HA) (upper 4:4bits)	**70**	01110000
	113	**71**	Vertical Avtive 1080 Lines	**38**	00111000
	114	**72**	Vertical Blanking (Tvp-HA) (DE Blanking typ.for DE only panels) 31 Lines	**1F**	00011111
	115	**73**	Vertical Active : Vertical Blanking (Tvp-HA) (upper 4:4bits)	**40**	01000000
	116	**74**	Horizontal Sync. Offset (Thfp) 48 Pixels	**30**	00110000
	117	**75**	Horizontal Sync Pulse Width (HSPW) 32 Pixels	**20**	00100000
	118	**76**	Vertical Sync Offset(Tvfp) : Sync Width (VSPW) 3 Lines : 5 Lines	**35**	00110101
	119	**77**	Horizontal Vertical Sync Offset/Width (upper 2bits)	**00**	00000000
	120	**78**	Horizontal Image Size (mm) 382 mm	**7E**	01111110
	121	**79**	Vertical Image Size (mm) 215 mm	**D7**	11010111
	122	**7A**	Horizontal Image Size / Vertical Image Size	**10**	00010000
	123	**7B**	Horizontal Border = 0 (Zero for Notebook LCD)	**00**	00000000
	124	**7C**	Vertical Border = 0 (Zero for Notebook LCD)	**00**	00000000
	125	**7D**	Non-Interlace, Normal display, no stereo, Digital Separate [Vsync_NEG, Hsync_NEG (outside of V-sync)]	**19**	00011001
Checksum	126	**7E**	Extension flag (# of optional 128 panel ID extension block to follow, Typ = 0)	**00**	00000000
	127	**7F**	Check Sum (The 1-byte sum of all 128 bytes in this panel ID block shall = 0)	**46**	01000110