Voltage Detectors With Adjustable Delay Circuit External

■ General Description

The LN804 is a cost-effective system supervisor Integrated Circuit (IC) designed to monitor VCC in digital and mixed signal systems and provide a warning signal when the system power supply is out of working range, and a reset signal to the host processor when necessary.

It features low supply current. CMOS output configurations is available. Delay time can be set by a external capacitor.

■ Features

Precision VCC Monitor for 1.63,1,93,2.63V, 2.93V, 3.08V, 4.00V ,4.38V and4.63V

Highly Accurate: ± 2%

Low Power Consumption : typical 3μA

Operating Voltage Range: 1V ~ 6.0V

Detect Voltage Temperature Characteristics: ± 100ppm/℃(TYP.)

Output Configuration: CMOS

■ Applications

Microprocessor reset circuitry

Memory battery back-up circuits

Power-on reset circuits

Power failure detection

System battery life and charge voltage monitors

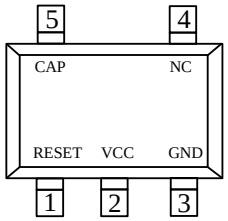
Delay circuitry

■ Ordering Information

LN804 ①②③④⑤⑥⑦

Designator	Description	Symbol	Description
①	Output Configuration	C	CMOS output
② ③④	Detect Voltage	263	2.63V
		293	2.93V
		308	3.08V
		400	4.00V
		438	4.38V
		463	4.63V
⑤	Detect Accuracy	1	Within ± 1.0%
		2	Within ± 2.0%
⑥	Package	M	SOT-23-5L
⑦	Device Orientation	R	Embossed tape, standard feed
		L	Embossed tape, reverse feed

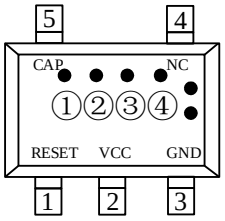
■ PIN Assignment



SOT23-5

PIN NO.	SYMBOL	DESCRIPTION
1	RESET	Output.Active High
2	VCC	Power
3	GND	Ground
4	N.C.	No Connected
5	CAP	Delay Timer set Pin

■ Marking



SOT23-5

① ② represent the Output type and Voltage thresthold.

CMOS(LN804C series)

SYMBOL	OUTPUT TYPE	VDET(V)
Ca	CMOS	4.63
Cb	CMOS	4.38
Cc	CMOS	4.00
Cd	CMOS	3.08
Ce	CMOS	2.93
Cf	CMOS	2.63
Cg	CMOS	1.93
Ch	CMOS	1.63

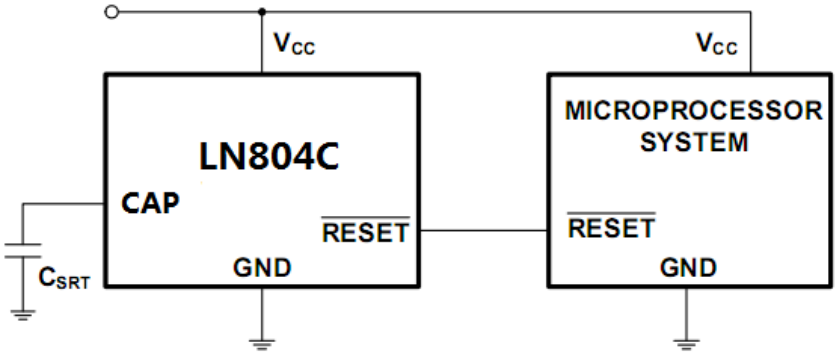
③：**Represent the** Accurate of the VDET.

SYMBOL	ACCURATE
2	±2%

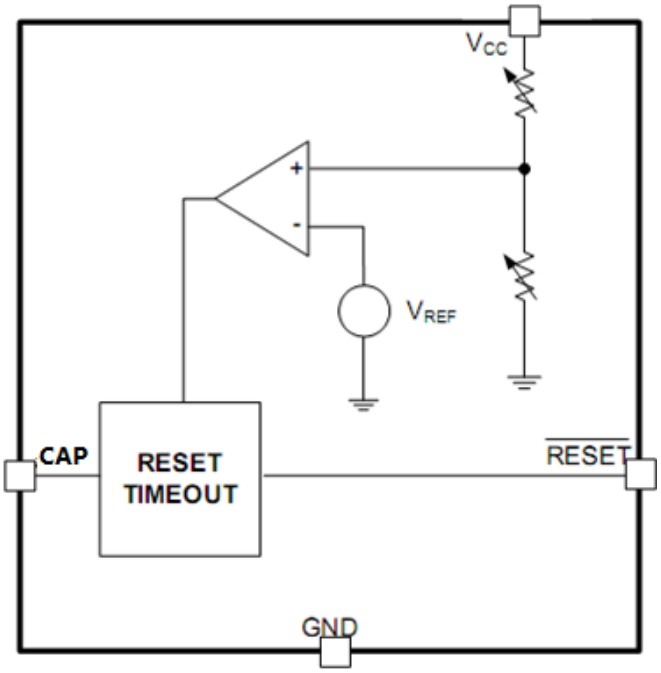
④ Represent the lot No

Note: six "." represent the information of product quality

■ Typical Application Circuit



■ Function Block Diagram



■ Absolute Maximum Ratings

Parameter		Symbol	Maximum Rating	Unit
Input Supply Voltage		V_{CC}	6	V
Output Current		IRESET	30	mA
Output Voltage	CMOS	RESET	VSS -0.3 ~ VCC + 0.3	V
Power Dissipation	SOT-23-5L	Pd	350	mW
Operating Temperature Range		Topr	-30～+85	℃
Storage Temperature Range		Tstg	-40～+125	℃

■ Electrical Characteristics

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Detect Voltage	VDF		VDF(T) x 0.98	VDF(T)	VDF(T) x 1.02	V
Hysteresis Range	VHYS		-	4*VDF	-	mV
Supply Current	ISS	VCC = 5V		3.0	5.0	μA
Operating Voltage	VCC	VDF= 2.63V to 4.63V	0.7		6	V
Output Current	IOUT	NMOS VCC=6V		30		mA
		PMOS VCC=6V		-30		
Detect Voltage Temperature Characteristics	ΔVDF ΔTopr· VDF			±100		ppm/℃

■ Operational Explanation

CMOS output(the 4th is the most important)

① When a voltage higher than the release voltage (VDR) is applied to the voltage input pin (VCC), the voltage will gradually fall. When a voltage higher than the detect voltage (VDF) is applied to VCC, output (RESET) will be equal to the input at VCC.

Note that high impedance exists at RESET with the N-channel open drain configuration. If the pin is pulled up, RESET will be equal to the pull up voltage.

② When VCC falls below VDF, RESET will be equal to the ground voltage (VSS) level (detect state). Note that this also applies to N-channel open drain configurations.

③ When VCC falls to a level below that of the minimum operating voltage (VMIN) output will become unstable. Because the output pin is generally pulled up with N-channel open drain configurations, output will be equal to pull up voltage.

④ When VCC rises above the VSS level (excepting levels lower than minimum operating voltage), RESET will be equal to VSS until VCC reaches the VDR level. But if the rising rate is fast enough, RESET is equal to the pull up voltage.

⑤ Although VCC will rise to a level higher than VDR, RESET maintains ground voltage level via the delay circuit.

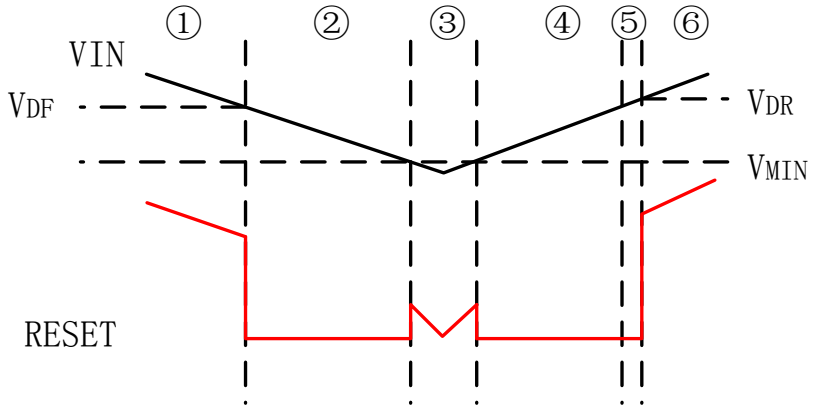
⑥ Following transient delay time, VCC will be output at RESET. Note that high impedance exists with the N-channel open drain configuration and that voltage will be dependent on pull up.

Notes:

1. The difference between VDR and VDF represents the hysteresis range.

2. Propagation delay time (tDLY) represents the time it takes for VCC to appear at RESET once the said voltage has exceeded the VDR level.

Timing Chart

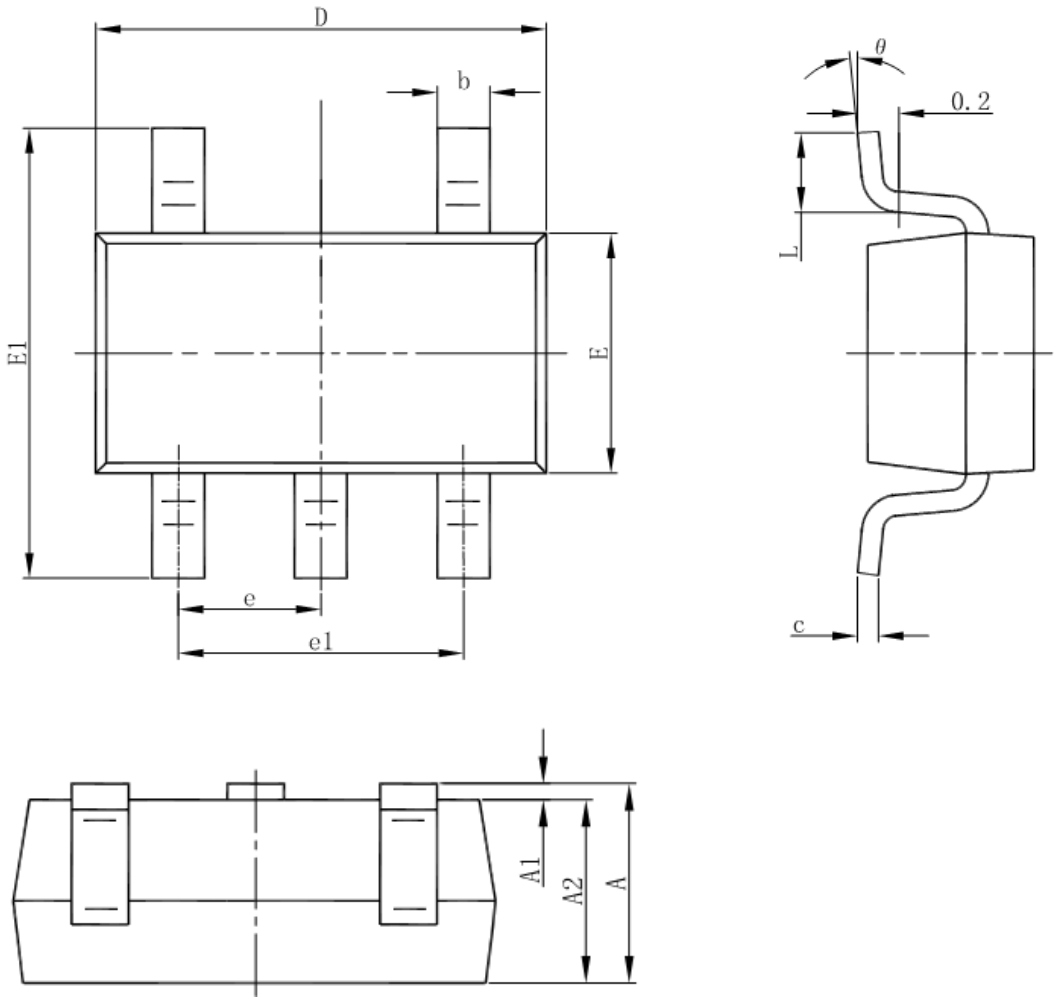


Delay time can be set by external capacitor

$T_{dly}=3.8x10^{-6}xC_{SR.}$

■ Package Information

- SOT-23-5L



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	1.050	1.250	0.041	0.049
A1	0.000	0.100	0.000	0.004
A2	1.050	1.150	0.041	0.045
b	0.300	0.500	0.012	0.020
c	0.100	0.200	0.004	0.008
D	2.820	3.020	0.111	0.119
E	1.500	1.700	0.059	0.067
E1	2.650	2.950	0.104	0.116
e	0.950(BSC)		0.037(BSC)	
e1	1.800	2.000	0.071	0.079
L	0.300	0.600	0.012	0.024
θ	0°	8°	0°	8°