National Semiconductor

PRELIMINARY
January 2005

LMP8272, LMP8277
High Common Mode, Gain of 14, Precision Voltage Difference Amplifiers

General Description

The LMP™8272, LMP8277 are fixed gain differential amplifiers with a -2V to 27V input common mode voltage range and a supply voltage range of 4.5V to 5.5V. The LMP8272, LMP8277 are precision amplifiers which will detect, amplify and filter small differential signals in the presence of high common mode voltages. The gain is fixed at 14 and is adequate to drive an ADC to full scale in most cases. This fixed gain is achieved in two separate stages, a pre-amplifier with gain of +7 and a second stage amplifier with a gain of +2. The internal signal path between these two stages is brought out on two pins that provide a connection for a filter network.

The LMP8272, LMP8277 will function with reduced specifications over the extended common mode input voltage range of -5 to 36 Volts. This feature makes the device suitable for applications with load dump in automotive systems.

Features

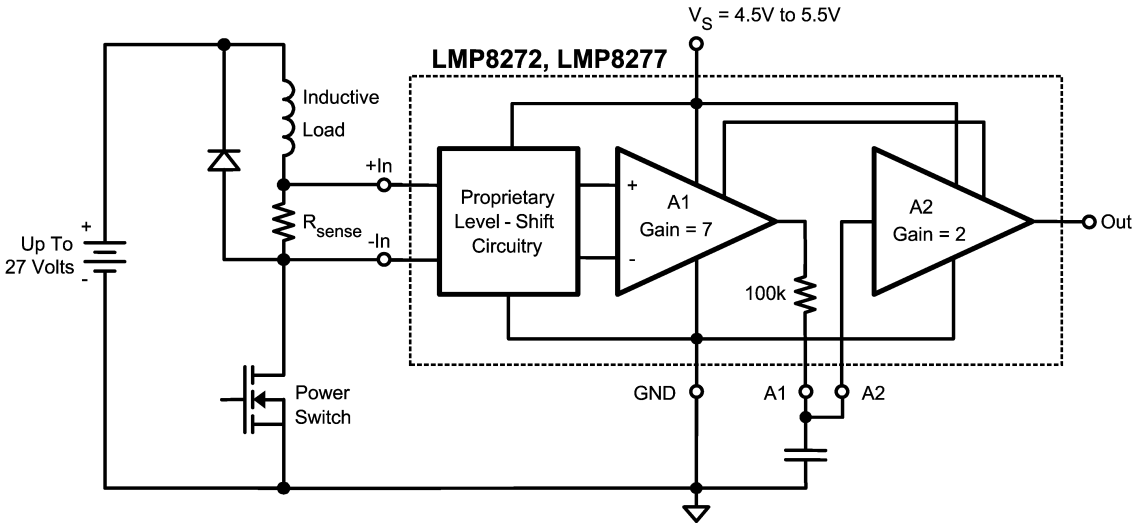
- Typical Values, TA = 25˚C
- Input Offset Voltage 1mV max
- TCVos (LMP8272) 15µV/˚C max
- TCVos (LMP8277) 30µV/˚C max
- CMRR 80dB Min
- Extended CMVR -5V to 36V
- Output Voltage Swing Rail to Rail
- Bandwidth 80KHz
- Operating Temperature Range (Ambient) -40˚C to 125˚C
- Operating Temperature Range (bare die) -40˚C to 150˚C
- Supply Voltage 4.5V to 5.5V
- Supply Current 1mA

Applications

- Fuel Injection Control
- Low Side Driver Configuration Current Sensing
- Power Management Systems

Typical Application

Typical Application: Low side Current Sensing



LMP™ is a trademark of National Semiconductor Corporation.

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

ESD Tolerance (Note 2)	
Human Body Model	
For input pins only	±4000V
For All other pins	±2000V
Machine Model	200V
Supply Voltage (V_S - GND)	5.75V
CMVR Continuous	-5 to 42 Volts
Transient (300 ms)	-TBD to 45 Volts
Storage Temperature Range	-65˚C to +150˚C
Junction Temperature (Note 3)	+150˚C max
Soldering Information	
Infrared or Convection (20 sec)	235˚C
Wave Soldering Lead Temp. (10 sec)	260˚C

Operating Ratings (Note 1)

Temperature Range (Note 3)	
Packaged devices(Note 3)	-40˚C to +125˚C
Bare Die Junction Temperature(Note 3)	-40˚C to +150˚C
Supply Voltage (V_S – GND)	4.5V to 5.5V
Package Thermal Resistance (θ_{JA} (Note 3))	
8–Pin SOIC	190˚C/W

5V Electrical Characteristics (Note 7)

Unless otherwise specified, all limits guaranteed for T_A = 25˚C, V_S = 5V, GND= 0, -2V≤V_{CM} ≤27V. **Boldface** limits apply at the temperature extremes.

Symbol	Parameter	Conditions		Min	Typ (Note 4)	Max	Units
V_{OS}	Input Offset Voltage	V_{CM} = Vs/2			±0.25	1.0	mV
TC V_{OS}	Input Offset Voltage Drift	LMP8272			±6	**±15**	µV/˚C
TC V_{OS}	Input Offset Voltage Drift	LMP8277			±6	**±30**	µV/˚C
A2 I_B	Input Bias Current of A2	(Note 5)				**±20**	µA
I_S	Supply Current			0.6 **TBD**	1.0	1.2 **TBD**	mA
R_{CM}	Input impedance Common Mode			**160**	200	**240**	KΩ
R_{DM}	Input impedance Differential Mode			**320**	400	**480**	KΩ
CMVR	Input Common-Mode Voltage Range	Continuous		**-2**		**+27**	V
ECMVR	Extended Common-Mode Voltage Range			-5		36	V
DC CMRR	DC Common Mode Rejection Ratio	-2V≤V_{CM}≤ 27V -5V≤V_{CM}≤ 36V		**80** **80**			dB
AC CMRR	AC Common Mode Rejection Ratio	-2V≤V_{CM}≤ 27V	f = 1KHz	TBD			dB
		-2V≤V_{CM}≤ 27V	f = 10KHz	TBD			
PSRR	Power Supply Rejection Ratio	4.5V≤V_S≤ 5.5V		TBD **TBD**			dB
R_{F-INT}	Filter Resistor			**97**	100	**103**	KΩ
TCR_{F-INT}	Filter Resistor Drift				TBD		ppm/˚C
A_V	Total Gain				14		V/V
	Gain Error					±1	%
	Gain Drift					**±25**	ppm/˚C
A1 V_{OUT}	A1 Output Voltage Swing	R_L= 100KΩ on Output	VOL			**0.01**	Volts
			VOH	**4.80**			
A2 V_{OUT}	A2 Output Voltage Swing	R_L= 100KΩ on Output	VOL			**0.01**	Volts
			VOH	**4.80**			
SR	Slew Rate (Note 6)				0.7		V/µs
BW	Bandwidth				80		KHz

5V Electrical Characteristics (Note 7) (Continued)

Unless otherwise specified, all limits guaranteed for T_A = 25˚C, V_S = 5V, GND= 0, -2V≤V_{CM} ≤27V. **Boldface** limits apply at the temperature extremes.

Symbol	Parameter	Conditions	Min	Typ (Note 4)	Max	Units
Noise	0.1Hz ro 10Hz			TBD		µVpp
	Spectral Density			TBD		nV/√Hz

Note 1: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is intended to be functional, but specific performance is not guaranteed. For guaranteed specifications and the test conditions, see the Electrical Characteristics Tables.

Note 2: Human body model, 1.5 kΩ in series with 100 pF. Machine model: 0Ω in series with 200 pF.

Note 3: The maximum power dissipation is a function of $T_{J(MAX)}$, θ_{JA}, and T_A. The maximum allowable power dissipation at any ambient temperature is $P_D = (T_{J(MAX)} - T_A)/ \theta_{JA}$. All numbers apply for packages soldered directly onto a PC board.

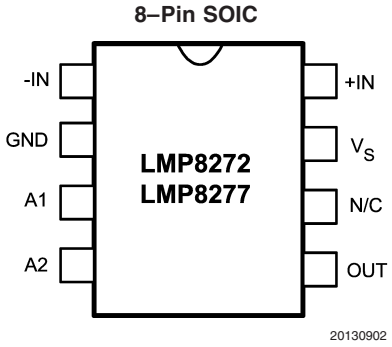
Note 4: Typical values represent the most likely parametric norm.

Note 5: Positive current corresponds to current flowing into the device.

Note 6: Slew rate is the average of the rising and falling slew rates.

Note 7: Electrical table values apply only for factory testing conditions at the temperature indicated. Factory testing conditions result in very limited self-heating of the device.

Connection Diagram



Top View

Application Note

The LMP8272, LMP8277 are single supply amplifier with a fixed gain of 14 and an extended common mode voltage range of -2V to 36V. The fixed gain is achieved in two separate stages, a pre-amplifier with gain of +7 and a second stage amplifier with gain of +2. A block diagram of the LMP8272, LMP8277 is shown in Figure 1.

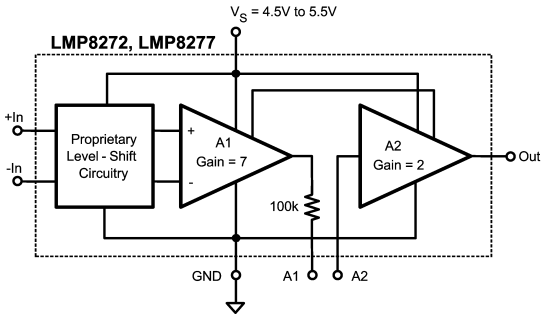


FIGURE 1.

The overall offset of the LMP8272, LMP8277 is minimized by trimming amplifier A1. This is done so that the output referred offset of A1 cancels the input referred offset of A2 or $7V_{OS1} = -V_{OS2}$

Because of this offset voltage relationship, the offset of each individual amplifier stage maybe more than the limit specified for the overall system in the datasheet tables. Care must be given when pin 3 and 4, A1 and A2, are connected to each other. If the signal going from A1 to A2 is amplified or attenuated (by use of amplifiers and resistors), the overall LMP8272, LMP8277 offset will be affected as a result. Filtering the signal between A1 and A2 or simply connecting the two pins will not change the offset of the LMP8272, LMP8277.

Referencing input referred offset voltages, the following relationship holds:

$$\frac{(7V_{OS1}) + (V_{OS2})}{7} = V_{OS}(\text{LMP8272, LMP8277})$$

If the signal on pin 3 is scaled, attenuated or amplified, by a factor **X**, then the offset of the overall system will become:

$$\frac{(7V_{OS1}).(X) + (V_{OS2})}{7} = V_{OS}(\text{LMP8272, LMP8277})$$

Application Note (Continued)

This represents a value that the LMP8272 and LMP8277 have not been optimized and trimmed for and may very well be above the limits indicated in the electrical characteristics tables.

National Semiconductor
Americas Customer
Support Center
Email: new.feedback@nsc.com
Tel: 1-800-272-9959

www.national.com

National Semiconductor
Europe Customer Support Center
Fax: +49 (0) 180-530 85 86
Email: europe.support@nsc.com
Deutsch Tel: +49 (0) 69 9508 6208
English Tel: +44 (0) 870 24 0 2171
Français Tel: +33 (0) 1 41 91 8790

National Semiconductor
Asia Pacific Customer
Support Center
Email: ap.support@nsc.com

National Semiconductor
Japan Customer Support Center
Fax: 81-3-5639-7507
Email: jpn.feedback@nsc.com
Tel: 81-3-5639-7560