LMP4435SSF 30V P-Channel MOSFET

Features

- -30V/-9A, $R_{DS(ON)}$<18mΩ@V_{GS}=-10V
- -30V/-7A, $R_{DS(ON)}$<26mΩ@V_{GS}=-4.5V
- Super high density cell design for extremely low $R_{DS\ (ON)}$
- SOP-8 package design

Product Description

LMP4435SSF, P-Channel enhancement mode MOSFET, uses Advanced Trench Technology to provide excellent $R_{DS(ON)}$, low gate charge.

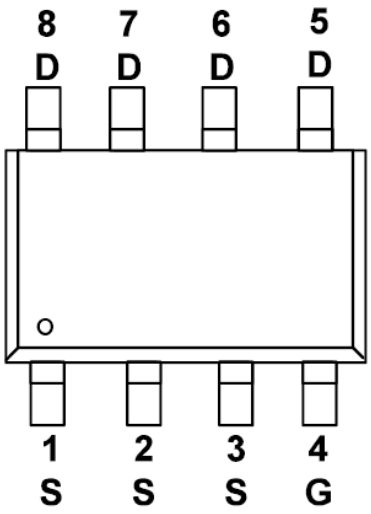
These devices are particularly suited for low voltage power management, such as smart phone and notebook computer, and low in-line power loss are needed in commercial industrial surface mount applications.

Applications

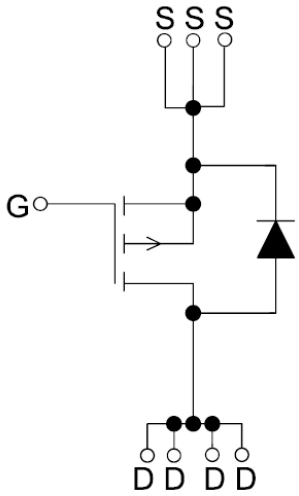
- LED Display
- CCFL Inverter
- Power Management in Notebook computer
- Load/Power Switching

Pin Configuration

LMP4435SSF (SOP-8)



PIN	Description
1	Source
2	Source
3	Source
4	Gate
5	Drain
6	Drain
7	Drain
8	Drain



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Ordering Information

Ordering Information					
Part Number	P/N	PKG code	Pb Free code	Package	Quantity
LMP4435SSF	LMP4435S	S	F	SOP-8	4000

Marking Information

Marking Information		
Part Marking	Part Number	LFC code
4435S AAAAAA BBBBBB	AAAAAA	BBBBBB

Absolute Maximum Ratings

(T_C=25ºC Unless otherwise noted)

Symbol	Parameter		Typical	Unit
V_{DSS}	Drain-Source Voltage		-30	V
V_{GSS}	Gate Source Voltage		±20	V
I_D	Continuous Drain Current(T_J=150ºC)	T_A=25ºC	-8.6	A
		T_A=70ºC	-6.8	
I_{DM}	Pulsed Drain Current		-32	A
I_S	Continuous Source Current(Diode Conduction)		-2	A
P_D	Power Dissipation	T_A=25ºC	2	W
		T_A=70ºC	1.28	
T_J	Operating Junction Temperature		-55/150	ºC
T_{STG}	Storage Temperature Range		-55/150	ºC
R	Thermal Resistance-Junction to Ambient		62.5	ºC/W
$R_{\theta C}$	Thermal Resistance-Junction to Case		38	ºC/W

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Electrical Characteristics

(T_C=25ºC Unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Static						
$V_{(BR)DSS}$	Drain-Source Breakdown Voltage	V_{GS}=0V, I_D=-250uA	-30			V
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS}=V_{GS}, I_D=-250uA	-1.0		-2.0	
I_{GSS}	Gate Leakage Current	V_{DS}=0V, V_{GS}=±25V			±100	nA
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS}=-24V, V_{GS}=0V			-1	uA
		V_{DS}=-24V, V_{GS}=0V, T_J=85ºC			-30	
$I_{D(on)}$	On-State Drain Current	V_{DS} -10V, V_{GS}=-10V	-30			A
		V_{DS} -5V, V_{GS}=-4.5V	-5			
$R_{DS(on)}$	Drain-Source On-Resistance	V_{GS}=-10V, I_D=-9A		10	18	mΩ
		V_{GS}=-4.5V, I_D=-7A		16	26	
g_{FS}	Forward Transconductance	V_{DS}=-10V, I_D=-9A		22		S
V_{SD}	Diode Forward Voltage	I_S=-2.3A, V_{GS}=0V		-0.7	-1.3	V
Dynamic						
Q_g	Total Gate Charge	V_{DS}=-15V, V_{GS}=-4.5V, I_D=-6A		20	30	nC
Q_{gs}	Gate-Source Charge			6		
Q_{gd}	Gate-Drain Charge			10		
C_{iss}	Input Capacitance	V_{DS}=-15V, V_{GS}=0V, f=1MHz		1600		pF
C_{oss}	Output Capacitance			350		
C_{rss}	Reverse Transfer Capacitance			300		
$t_{d(on)}$	Turn-On Time	V_{DD}=-15V, R_L=3Ω , I_D=-5A, V_{GEN}=-10V,R_G=1Ω		10	20	ns
t_r				12	24	
$t_{d(off)}$	Turn-Off Time			30	45	
t_f				10	20	

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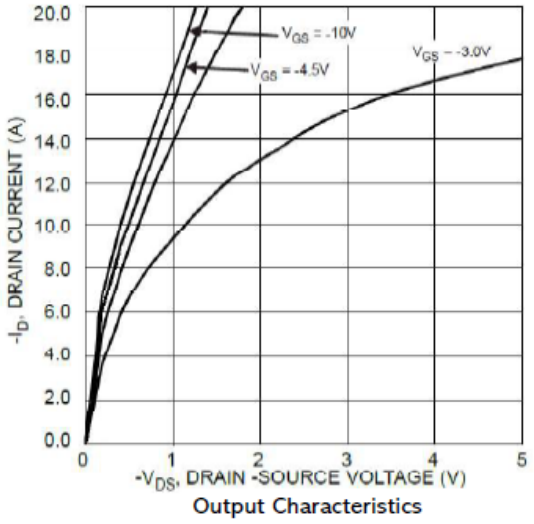
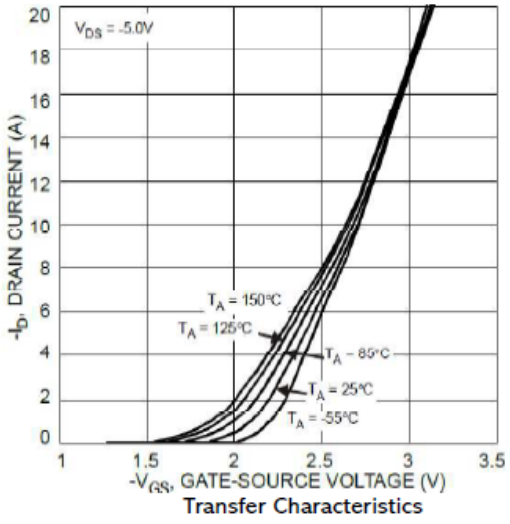
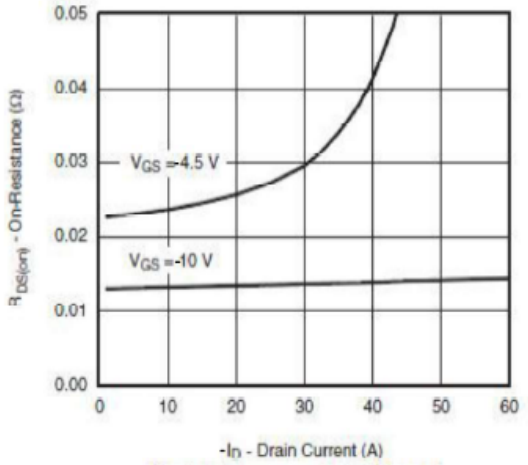
Typical Performance Characteristics



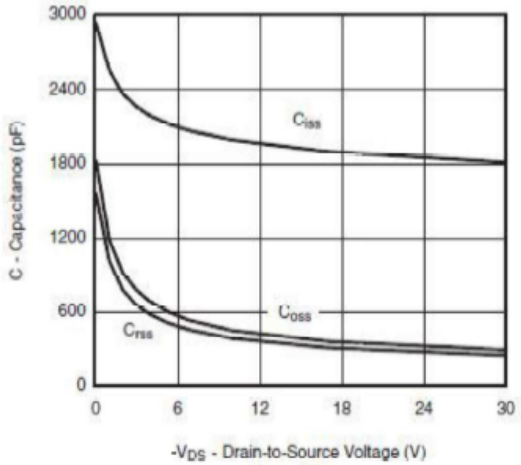
Output Characteristics



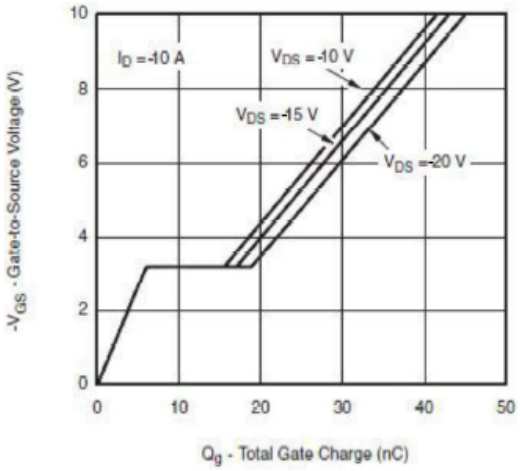
Transfer Characteristics

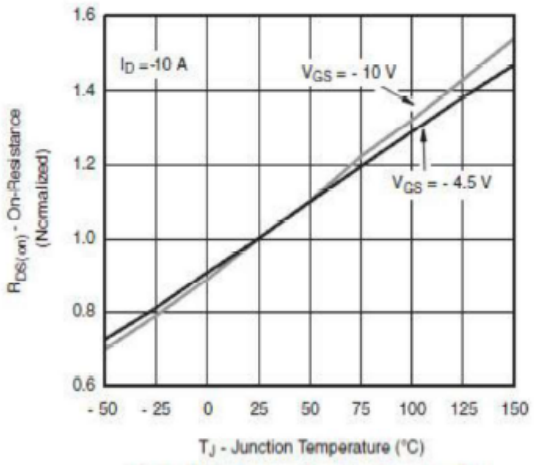


On-Resistance vs. Drain Current



capacitance





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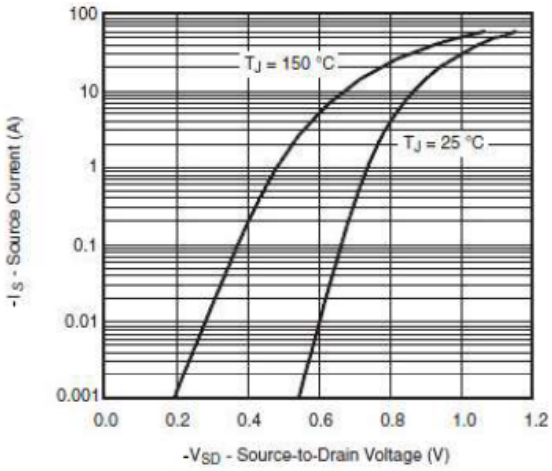
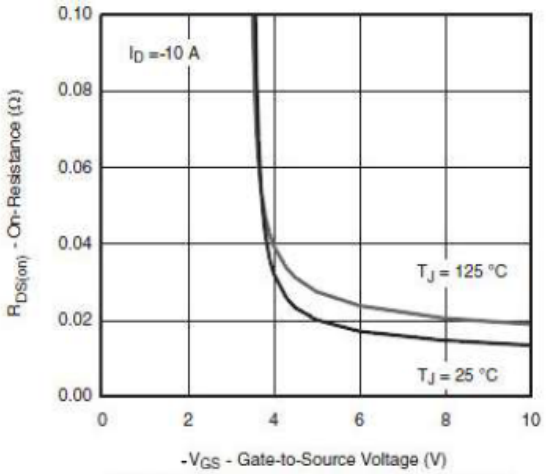
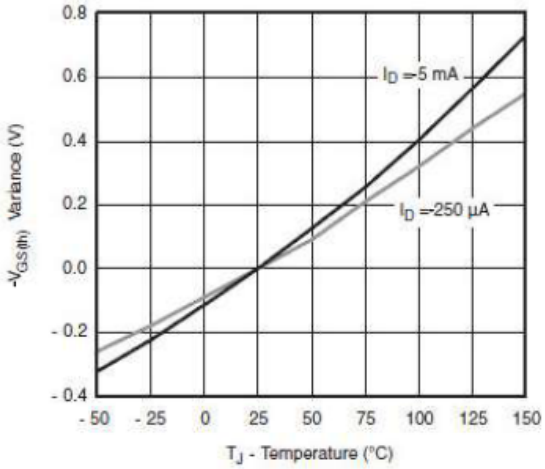
Typical Performance Characteristics(continue)



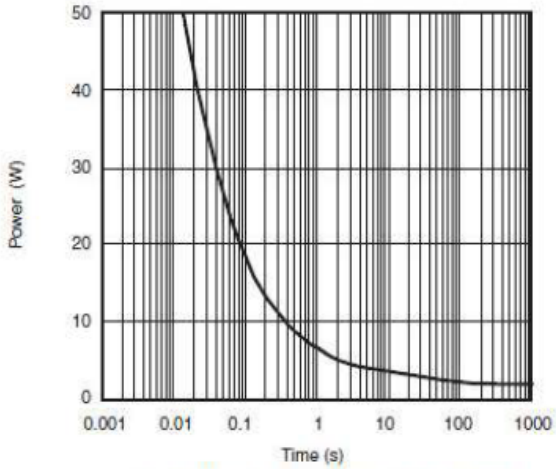
Source-Drain Diode Forward Voltage



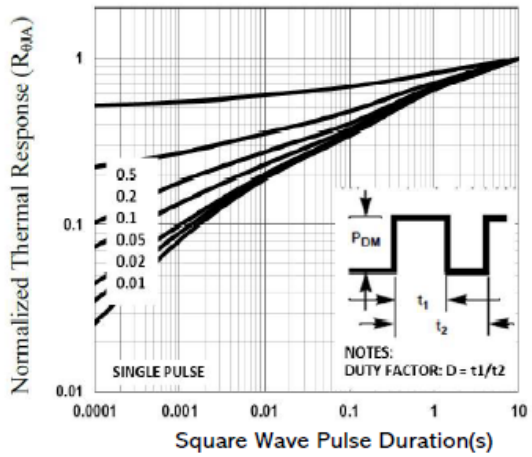
On-Resistance vs. Gate-to-Source Voltage

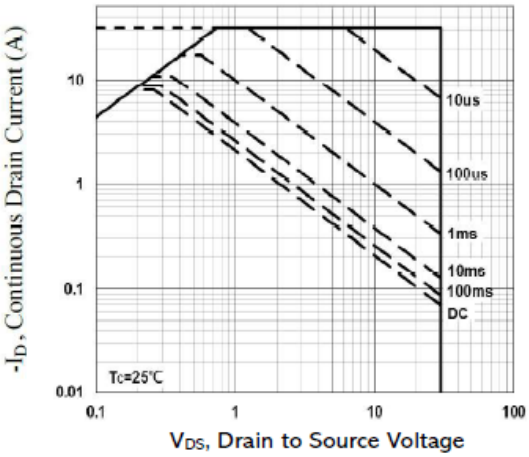


Threshold Voltage



Single Pulse Power, Junction-to-Ambient





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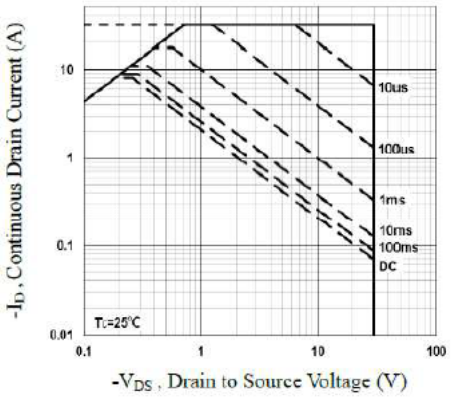
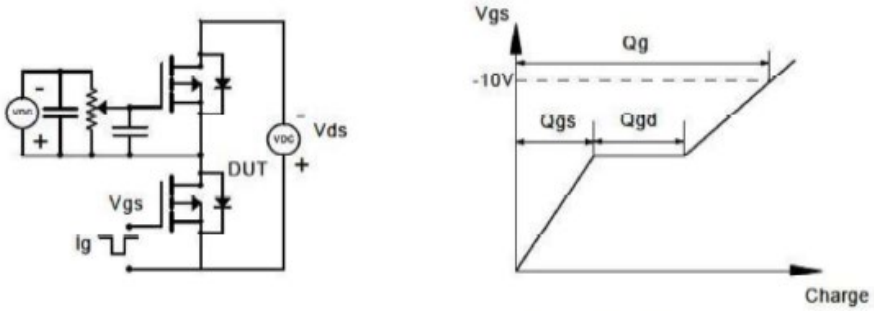
Typical Performance Characteristics(continue)

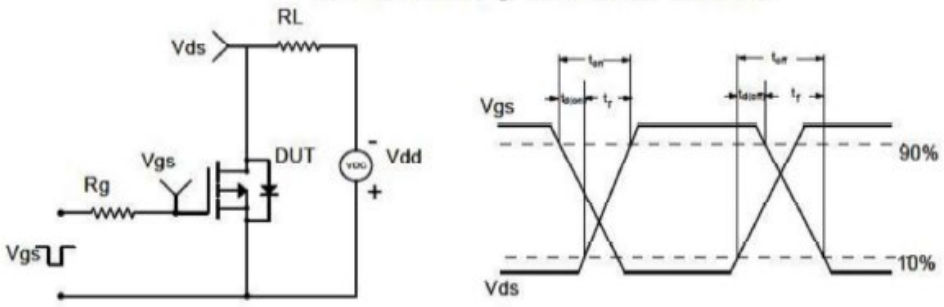


Maximum Safe Operation Area

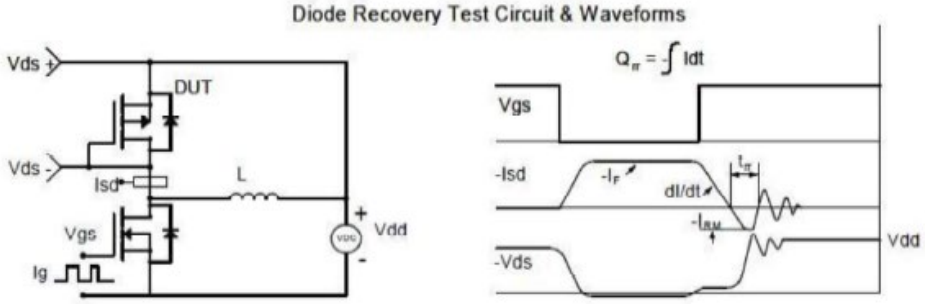
Gate Charge Test Circuit & Waveform



Resistive Switching Test Circuit & Waveforms



Diode Recovery Test Circuit & Waveforms



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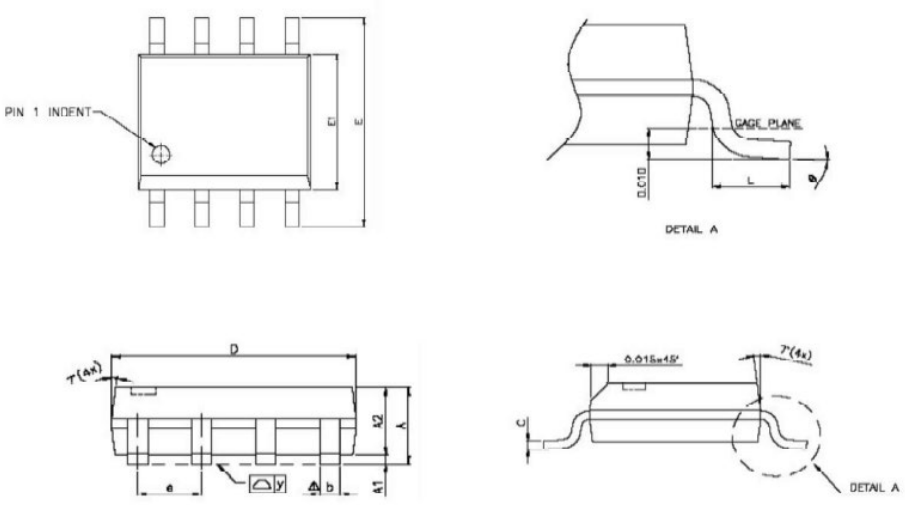
Package Dimension:

SOP-8



DIMENSION D AND E1 DO NOT INCLUDE MOLD FLASH, TIE BAR BURRS，GATE BURRS，AND INTERLEAD FLASH, NOT INCLUDING ANY MISMATCH BETWEEN THE TOP AND BOTTOM OF THE PLASTIC BODY.

Dimensions						
Symbol	Millimeters			Inches		
	Min	Nom	Max	Min	Nom	Max
A	1.47	1.60	1.73	0.058	0.063	0.068
A1	0.10	-	0.25	0.004	-	0.010
A2	-	1.45	-	-	0.057	-
b	0.33	0.41	0.51	0.013	0.016	0.020
C	0.19	0.20	0.25	0.0075	0.008	0.0098
D	4.80	4.85	4.95	0.189	0.191	0.195
E	5.80	6.00	6.20	0.228	0.236	0.244
E1	3.80	3.90	4.00	0.150	0.154	0.157
e	-	1.27	-	-	0.050	-
L	0.38	0.71	1.27	0.015	0.028	0.050
θ	0°	-	8 °	0 °	-	8 °

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