LMP3335SF 30V P-Channel Enhancement Mode MOSFET

Features

- $R_{DS(ON)}$=5mΩ@V_{GS}=-10V
- $R_{DS(ON)}$=7.8mΩ@V_{GS}=-4.5V
- Fast switching
- Suit for -4.5V Gate Drive Applications
- Green Device Available

Product Description

The P-Channel enhancement mode power field effect transistor is using trench DMOS technology. This advanced technology has been especially tailored to minimize on-state resistance, provide superior switching performance, and withstand high energy pulse in the avalanche and commutation mode.

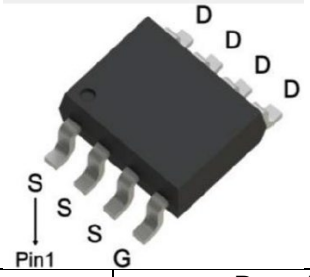
This device is well suited for high efficiency fast switching applications.

Applications

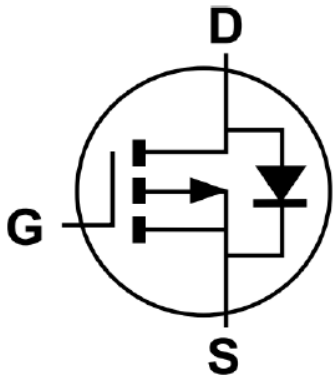
- Motor Driver Applications
- POL Applications
- Load Switch
- LED Application

Pin Configuration

LMP3335SF (SOP-8)



PIN	Description
1	Source
2	Source
3	Source
4	Gate
5	Drain
6	Drain
7	Drain
8	Drain



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Ordering Information

Ordering Information					
Part Number	P/N	PKG code	Pb Free code	Package	Quantity
LMP3335SF	LMP3335	S	F	SOP-8	4000pcs

Marking Information

Marking Information	
Part Number	LFC code
LMP3335SF	□□□□□□

Absolute Maximum Ratings

(T_C=25ºC Unless otherwise noted)

Symbol	Parameter		Typical	Unit
V_{DS}	Drain-Source Voltage		-30	V
V_{GS}	Gate-Source Voltage		±20	V
I_D	Continuous Drain Current	T_A=25℃	-20	A
		T_A=70℃	-16	
I_{DM}	Pulsed Drain Current		-100	A
P_D	Power Dissipation	T_A=25℃	3.1	W
		T_A=70℃	2	
T_J	Operating Junction Temperature		-55 to +150	℃
T_{STG}	Storage Temperature Range		-55 to +150	℃
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient (t ≦10s)		40	℃/W
	Thermal Resistance, Junction to Ambient (Steady State)		75	℃/W
$R_{\theta JC}$	Thermal Resistance, Junction to Case		24	℃/W

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Electrical Characteristics

(T_C=25ºC Unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Static characteristics						
BV_{DSS}	Drain-Source Breakdown Voltage	V_{GS}=0V, I_D=-250uA	-30			V
$V_{GS\ (th)}$	Gate Threshold Voltage	V_{DS}=V_{GS}, I_D=-250uA	-1.2		-2.5	V
I_{GSS}	Gate Leakage Current	V_{DS}=0V, V_{GS}=±25V			±100	nA
I_{DSS}	Drain-Source Leakage Current	V_{DS}=-30V, V_{GS}=0V			-1	uA
V_{SD}	Diode Forward Voltage	I_S=-1A, V_{GS}=0V			-1	V
$R_{DS(on)}$	Drain-Source On-Resistance	V_{GS}=-10V, I_D=-20A		4.5	5	mΩ
		V_{GS}=-4.5V, I_D=-10A		6.3	7.8	
Gate charge characteristics						
Q_g	Total Gate Charge	V_{DD}=-15V, V_{GS}=-10V, I_D=-10A		150		nC
Q_{gs}	Gate-Source Charge			24		
Q_{gd}	Gate-Drain Charge			28		
Dynamic characteristics						
C_{iss}	Input Capacitance	V_{DS}=-15V, V_{GS}=0V, f=1.0MHz		7500		pF
C_{oss}	Output Capacitance			1200		
C_{rss}	Reverse Transfer Capacitance			940		
$t_{d(on)}$	Turn-On Time	V_{DD}=-15V, V_{GS}=-10V, I_{DS}=-1A, R_g=6Ω		25		ns
t_r				35		
$t_{d(off)}$	Turn-Off Time			100		
t_f				50		

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Typical Performance Characteristics

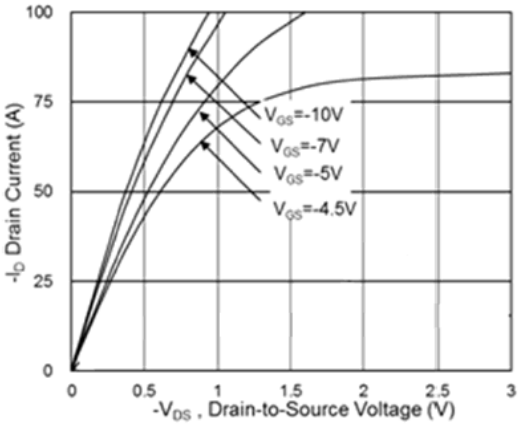

Figure 1. Output Characteristics

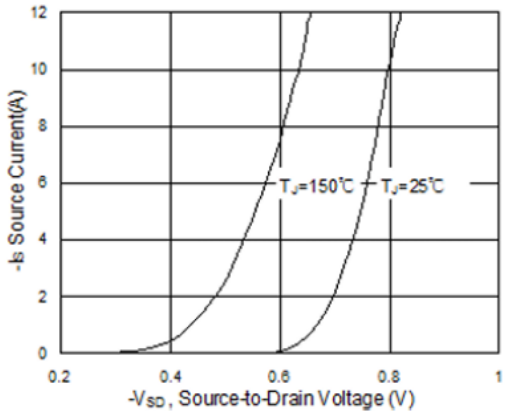

Figure 2. Forward Characteristics of Reverse

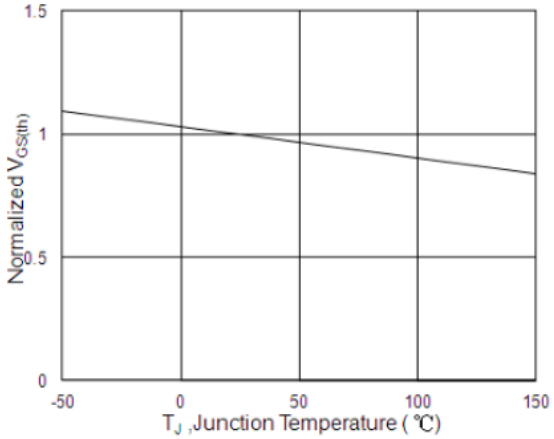

Figure 3. Normalized $V_{GS(th)}$ vs. T_J

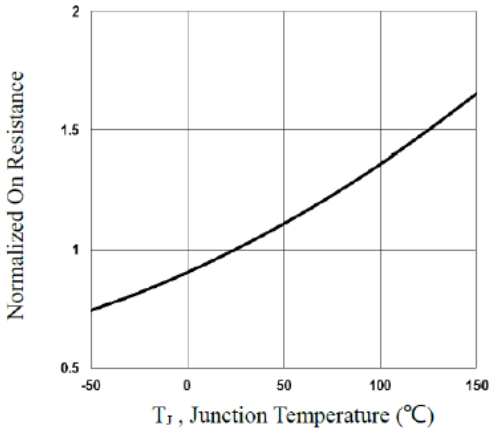

Figure 4. Normalized R_{DSON} vs. T_J

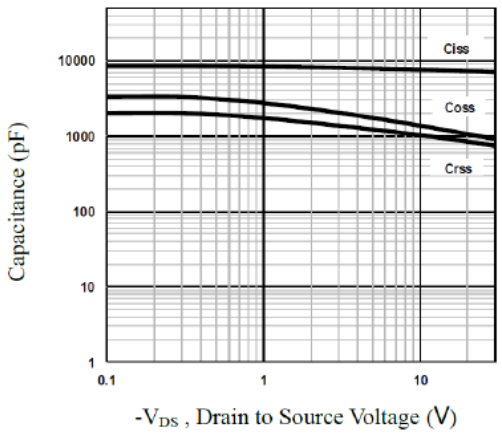

Figure 5. Capacitance

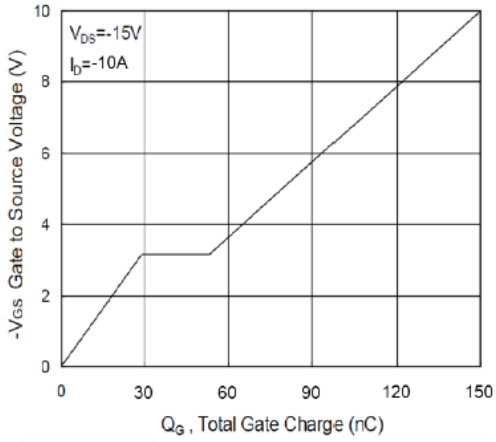

Figure 6. Gate Charge

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Typical Performance Characteristics(continue)

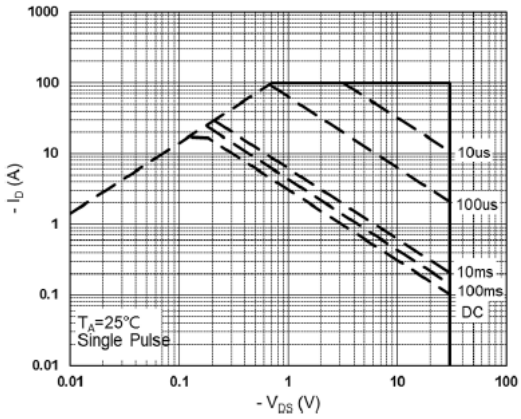

Figure 7. Maximum Safe Operating Area

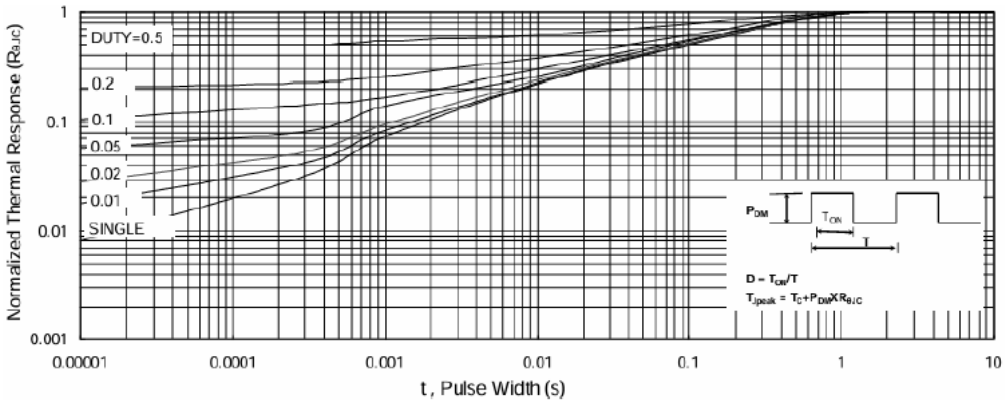

Figure 8. Normalized Transient Thermal Resistance

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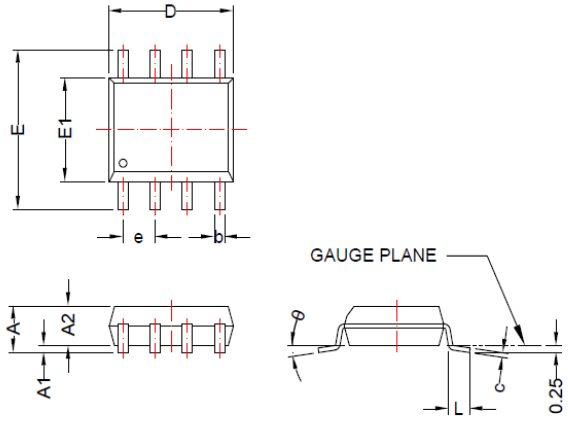
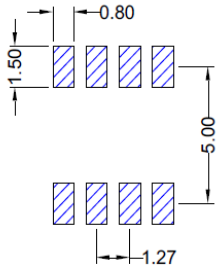
Package Dimension:

SOP-8

Package Dimension



Recommended Land Pattern



Dimensions				
Symbol	Millimeters		Inches	
	Min	Max	Min	Max
A	-	1.75	-	0.069
A1	0.10	0.15	0.004	0.006
A2	1.25	-	0.049	-
b	0.31	0.51	0.012	0.020
c	0.10	0.25	0.004	0.010
D	4.70	5.10	0.185	0.201
D1	1.50	-	0.059	-
E	5.80	6.20	0.228	0.244
E1	3.80	4.00	0.150	0.157
E2	1.00	-	0.039	-
e	1.27 BSC		0.050 BSC	
L	0.40	1.27	0.016	0.050
θ	0°	8°	0°	8°

NOTE:
Dimensions are exclusive of Burrs, Mold Flash & Tie Bar extrusions.

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