LMP3117XF 30V P-Channel MOSFET

Features

- -30V/-42A, $R_{DS(ON)}$=14.5mΩ@V_{GS}=-10V
- Fast switching
- Suit for -4.5V Gate Drive Applications
- Green Device Available
- DFN5X6-8L package design

Product Description

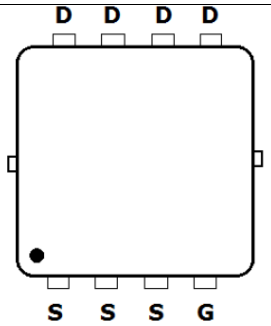
These P-Channel enhancement mode power field effect transistors are using trench DMOS technology. This advanced technology has been especially tailored to minimize on-state resistance, provide superior switching performance, and withstand high energy pulse in the avalanche and commutation mode.
These devices are well suited for high efficiency fast switching applications..

Applications

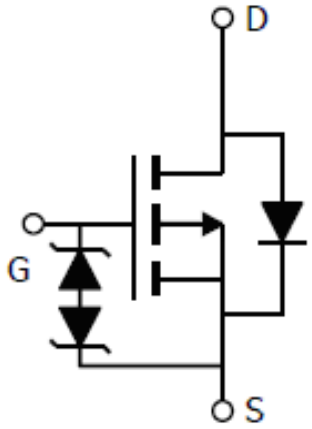
- MB / VGA / Vcore
- POL Applications
- Load Switch
- LED Application

Pin Configuration

LMP3117XF (DFN5X6-8L)



PIN	Description
1	Source
2	Source
3	Source
4	Gate
5	Drain
6	Drain
7	Drain
8	Drain



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Ordering Information

Ordering Information					
Part Number	P/N	PKG code	Pb Free code	Package	Quantity
LMP3117XF	LMP3117	X	F	DFN5X6-8L	3000

Marking Information

Marking Information		
Part Marking	Part Number	LFC code
3117XF XWMMMM	3117XF	XWMMMM

Absolute Maximum Ratings

(T_C=25ºC Unless otherwise noted)

Symbol	Parameter		Typical	Unit
V_{DS}	Drain-Source Voltage		-30	V
V_{GS}	Gate-Source Voltage		±25	V
I_D	Continuous Drain Current	TC=25℃	-42	A
		TC=100℃	-27	
I_{DM}	Pulsed Drain Current		-140	A
P_D	Power Dissipation	TC=25℃	42	W
		TC=100℃	17	
T_J	Operating Junction Temperature		-55 to +150	℃
T_{STG}	Storage Temperature Range		-55 to +150	℃
$R_{\theta JA}$	Thermal Resistance-Junction to Ambient		50	℃/W
$R_{\theta JC}$	Thermal Resistance-Junction to Case		3	℃/W

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Electrical Characteristics

(T_C=25ºC Unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Static						
$V_{(BR)DSS}$	Drain-Source Breakdown Voltage	V_{GS}=0V, I_D=-250uA	-30			V
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS}=V_{GS}, I_D=-250uA	-1.2	-1.6	-2.5	
I_{GSS}	Gate Leakage Current	V_{DS}=0V, V_{GS}=±25V			±100	uA
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS}=-30V, V_{GS}=0V			-1	uA
$R_{DS(on)}$	Drain-Source On-Resistance	V_{GS}=-10V, I_D=-10A		11.9	14.5	mΩ
		V_{GS}=-4.5V, I_D=-6A		19	23	
V_{SD}	Diode Forward Voltage	I_S=-1A, V_{GS}=0V			-1	V
Dynamic						
Q_g	Total Gate Charge	V_{DS}=-15V, V_{GS}=-4.5V, I_D=-15A		22		nC
Q_{gs}	Gate-Source Charge			8.7		
Q_{gd}	Gate-Drain Charge			7.2		
C_{iss}	Input Capacitance	V_{DS}=-15V, V_{GS}=0V f=1MHz		2215		pF
C_{oss}	Output Capacitance			310		
C_{rss}	Reverse Transfer Capacitance			237		
$t_{d(on)}$	Turn-On Time	V_{DD}=-15V, I_D=-15A V_{GS}=-10V, R_G=3.3Ω		8		ns
t_r				73.67		
$t_{d(off)}$	Turn-Off Time			61.8		
t_f				24.4		

Note

1. The data tested by surface mounted on a 1 inch2 FR-4 board with 2oz copper.
2. The EAS data shows Max. rating . The test condition is VDD=-20V, VGS=-10V, L=0.1mH, IAS=-19A.
3. The data tested by pulsed , pulse width ≦300us , duty cycle ≦2%.

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Typical Performance Characteristics

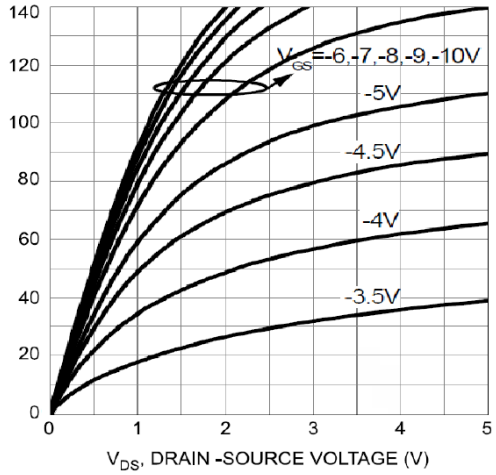

Figure 1. Output Characteristics

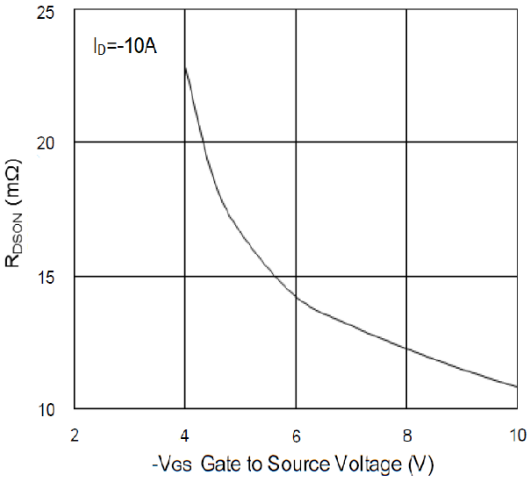

Figure 2. On-Resistance Variation with V_{GS}

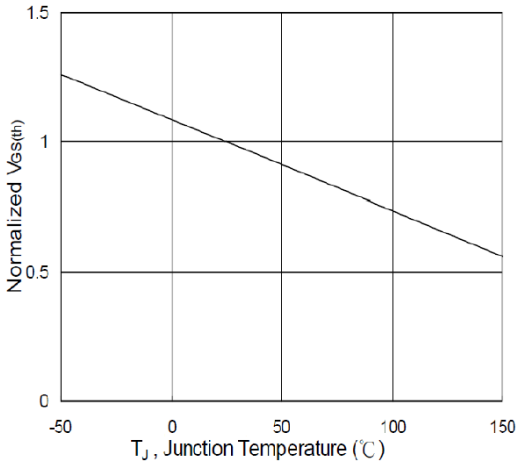

Figure 3. Normalized $V_{GS(th)}$ vs. T_J

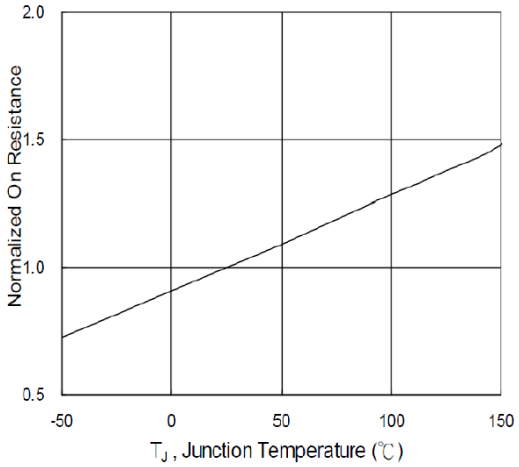

Figure 4. Normalized R_{DSON} vs. T_J

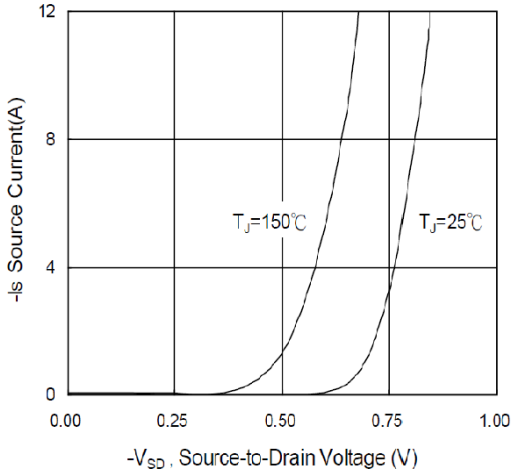

Figure 5. Diode Forward Voltage vs. Current

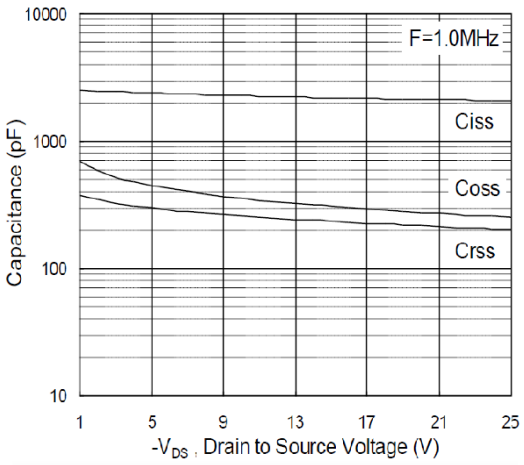

Figure 6. Capacitance

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Typical Performance Characteristics(continue)

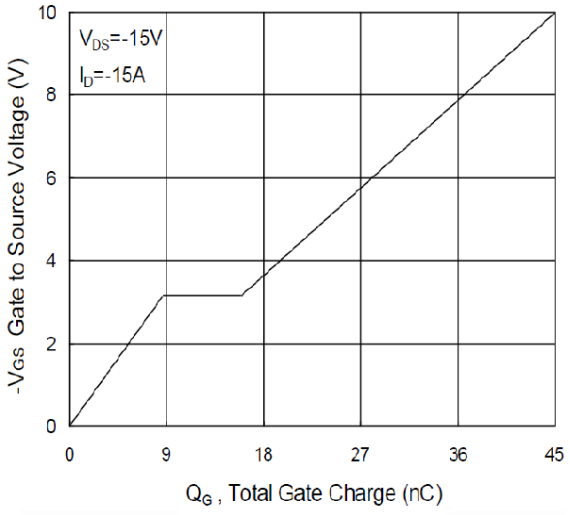

Figure 7. Gate Charge Waveform

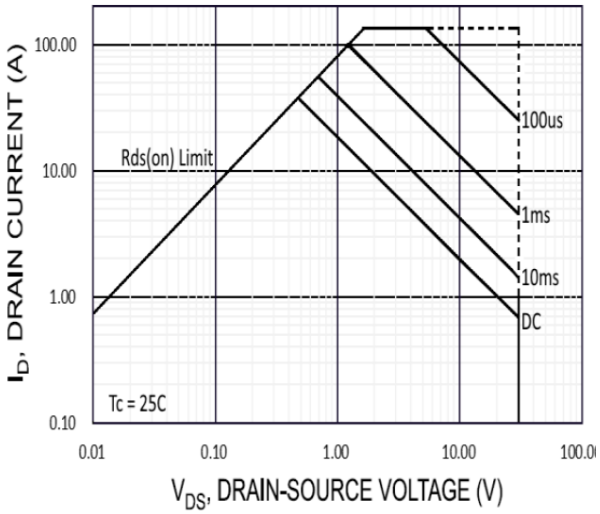

Figure 8. Maximum Safe Operating Area

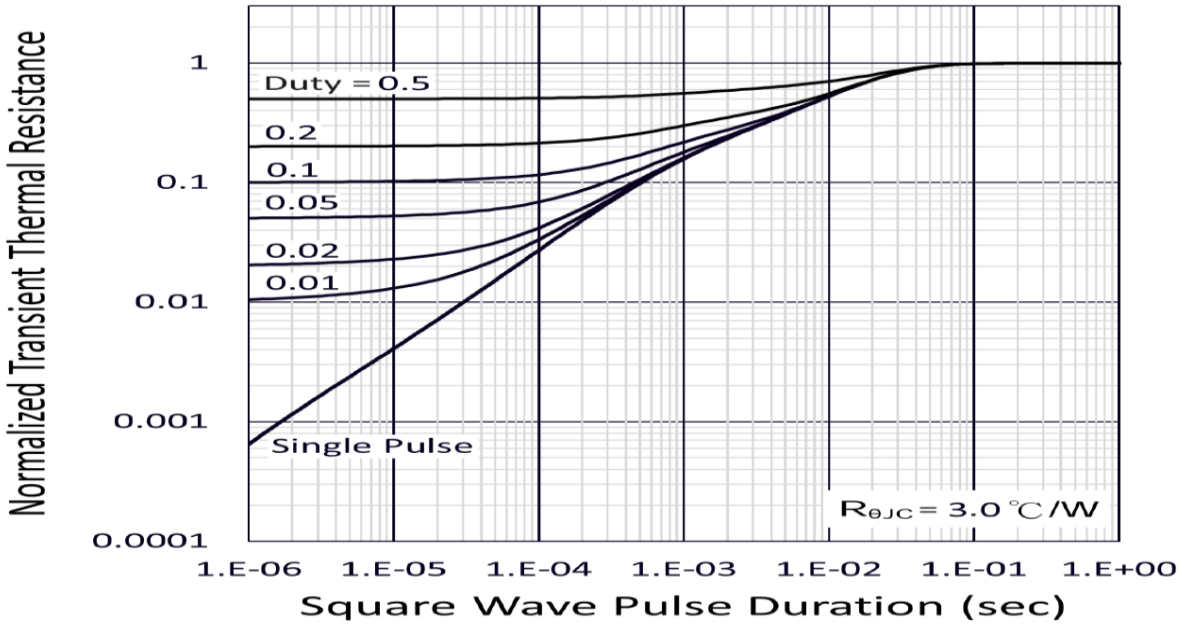

Figure 9. Normalized Transient Thermal Resistance

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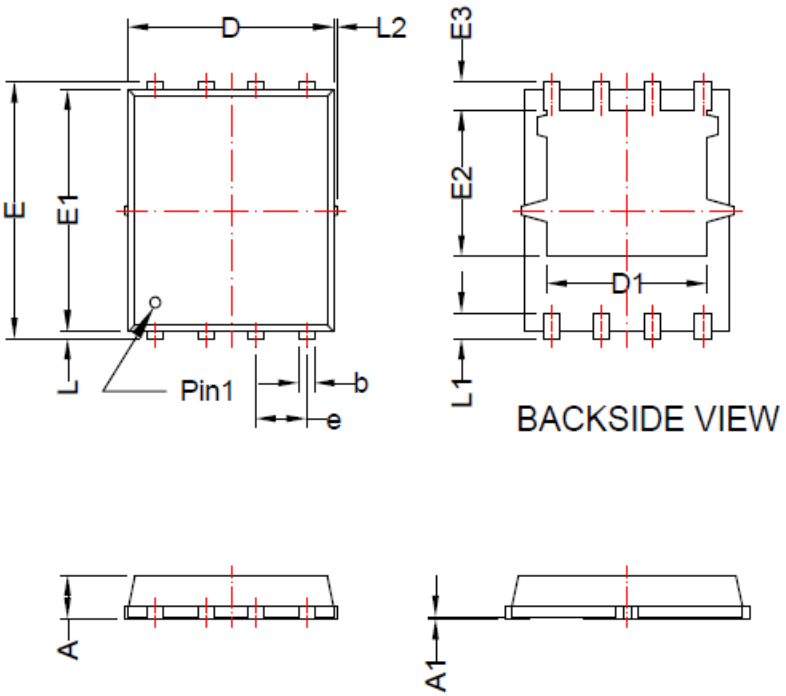
Package Dimension:

DFN5X6-8L



DIMENSION D AND E1 DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS.MOLD FLASH, PROTRUSIONS OR GATE BURRS SHALL HOT EXCEED 0.5mm PER INTERLEAD FLASH OR PROTRUSIOB SHALL NOT EXCEED 0.5mm PER SIDE

Dimensions				
Symbol	Millimeters		Inches	
	Min	Max	Min	Max
A	0.80	1.20	0.031	0.047
A1	0.00	0.05	0.000	0.002
b	0.25	0.51	0.010	0.020
c	0.20	0.35	0.008	0.014
D	4.90	5.40	0.193	0.213
D1	3.40	4.60	0.134	0.181
e	1.27 BSC		0.050 BSC	
L	0.1	0.25	0.004	0.010
L1	0.45	0.75	0.018	0.030
L2	---	0.15	---	0.006

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