LMN3368ASF 30V N-Channel Enhancement Mode MOSFETs

Features

- $R_{DS(ON)}$ =6mΩ @ V_{GS}=10V
- $R_{DS(ON)}$ =9.8mΩ @ V_{GS}=4.5V
- SOP-8 Package

Product Description

The N-Channel enhancement mode power field effect transistor is using trench DMOS technology. This advanced technology has been especially tailored to minimize on-state resistance, provide superior switching performance, and withstand high energy pulse in the avalanche and commutation mode.

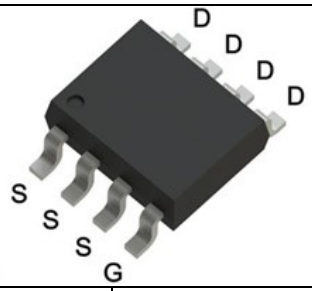
The device is well suited for high efficiency fast switching applications.

Applications

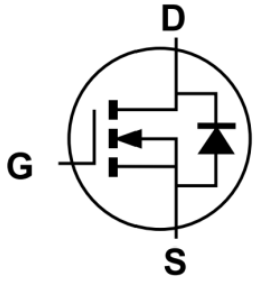
- MB / VGA / Vcore
- POL
- SMPS

Pin Configuration

LMN3368ASF (SOP-8)



PIN	Description
1,2,3	Source
4	Gate
5,6,7,8	Drain



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Ordering Information

Part Number	Part Marking	Package	Quantity
LMN3368ASF	3368ASF	SOP-8	4000 PCS

Marking Information

Part Marking	Package Code	Green Level:	Product Code:
3368ASF	1 is S for SOP-8	2 is F for RoHS Compliant and Halogen Free	LMN3368ASF

Absolute Maximum Ratings

(T_C=25ºC Unless otherwise noted)

Symbol	Parameter		Typical	Unit
V_{DSS}	Drain-Source Voltage		30	V
V_{GSS}	Gate-Source Voltage		±20	V
I_D	Continuous Drain Current[1]	T_A=25ºC	13	A
		T_A=70ºC	10	
I_{DM}	Pulsed Drain Current[2]		65	A
P_D	Power Dissipation[3]	T_A=25ºC	1.5	W
		T_A=70ºC	1	
T_J	Operating Junction Temperature		-55 to +150	℃
T_{STG}	Storage Temperature Range		-55 to +150	℃
$R_{\theta JA}$	Thermal Resistance-Junction to Case[1]		80	℃/W

Note:
1. The data tested by surface mounted on a 1 inch2 FR-4 board with 2oz copper.
2. The data tested by pulsed, pulse width ≤ 300us, duty cycle ≤ 2%.
3. The power dissipation is limited by 150ºC junction temperature.

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Electrical Characteristics

(T_C=25ºC Unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Static						
BV_{DSS}	Drain-Source Breakdown Voltage	V_{GS}=0V, I_D=250uA	30			V
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS}=V_{GS}, ID=250uA	1.2		2.5	
I_{GSS}	Gate Leakage Current	V_{DS}=0V, V_{GS}=±20V			±100	nA
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS}=30V, V_{GS}=0V			1	uA
$R_{DS(on)}$	Drain-Source On-Resistance	V_{GS}=10V, I_D=15A		4.2	6	mΩ
		V_{GS}=4.5V, I_D=10A		5.6	9.8	
V_{SD}	Diode Forward Voltage	I_S=20A, V_{GS}=0V			1.2	V
Dynamic						
Q_g	Total Gate Charge	V_{DS}=15V, V_{GS}=10V, I_D=15A		39		nC
Q_{gs}	Gate-Source Charge			7.6		
Q_{gd}	Gate-Drain Charge			7.2		
C_{iss}	Input Capacitance	V_{DS}=15V, V_{GS}=0V, f=1MHz		2295		pF
C_{oss}	Output Capacitance			267		
C_{rss}	Reverse Transfer Capacitance			210		
$t_{d(on)}$	Turn-On Time	V_{DD}=15V, I_D=15A, V_{GS}=10V, R_G=3.3Ω		7.8		ns
t_r				15		
$t_{d(off)}$	Turn-Off Time			37		
t_f				11		
R_g	Gate Resistance	V_{DS}=0V, V_{GS}=0V, f=1MHz		1.7		Ω

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Typical Performance Characteristics

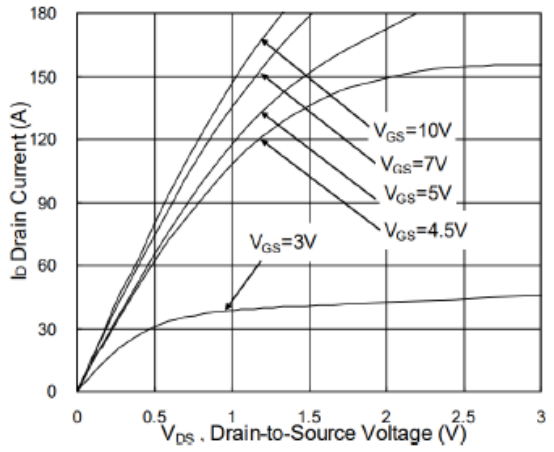

Figure 1. Typical Output Characteristics

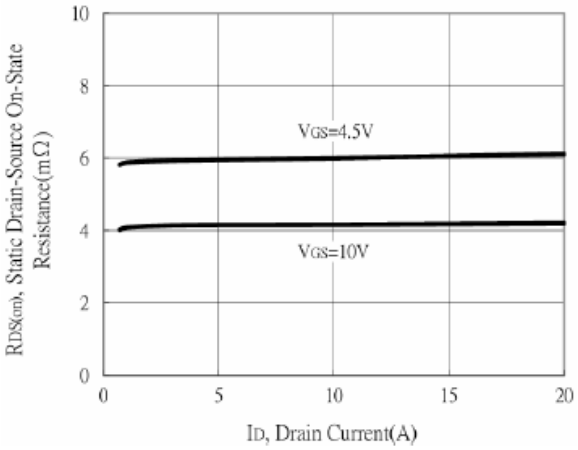

Figure 2. Drain-Source On-State resistance vs Drain Current

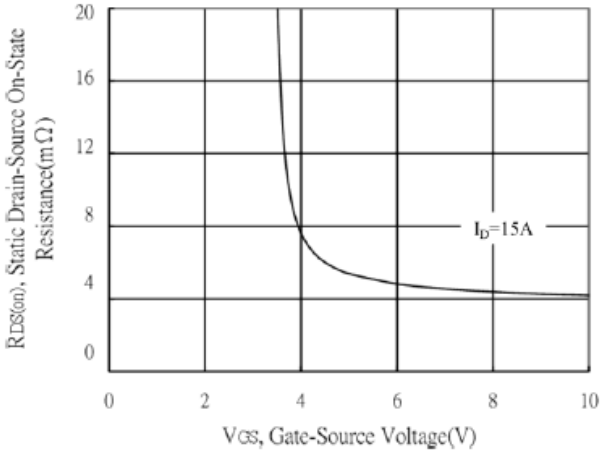

Figure 3. Drain-Source On-State Resistance vs Gate-Source Voltage

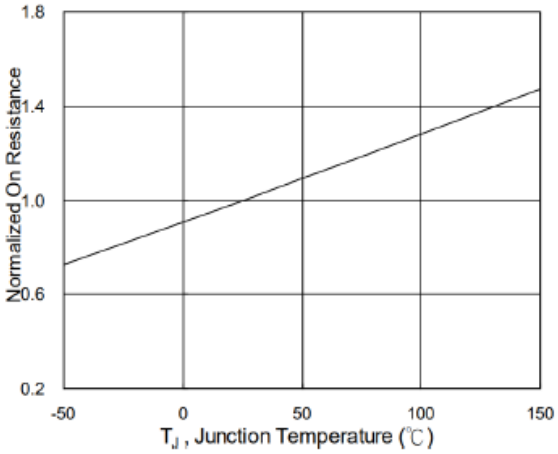

Figure 4. Drain-Source On-State Resistance vs Junction Temperature

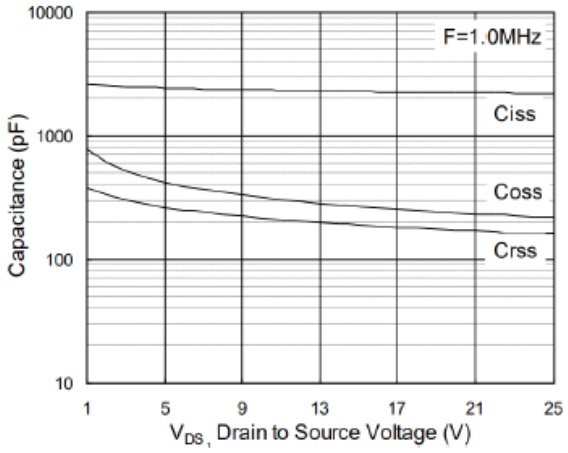

Figure 5. Capacitance vs Drain-to-Source Voltage

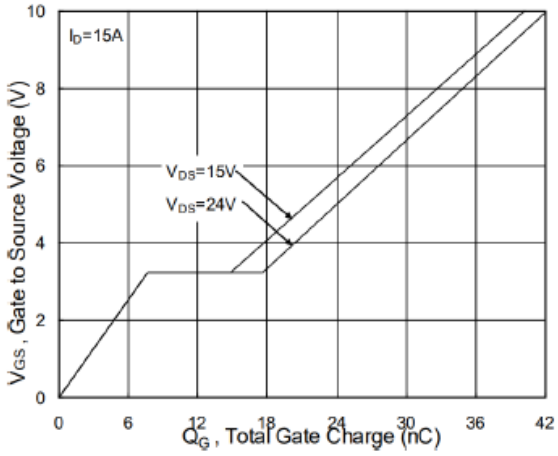

Figure 6. Gate Charge

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Typical Performance Characteristics(continue)

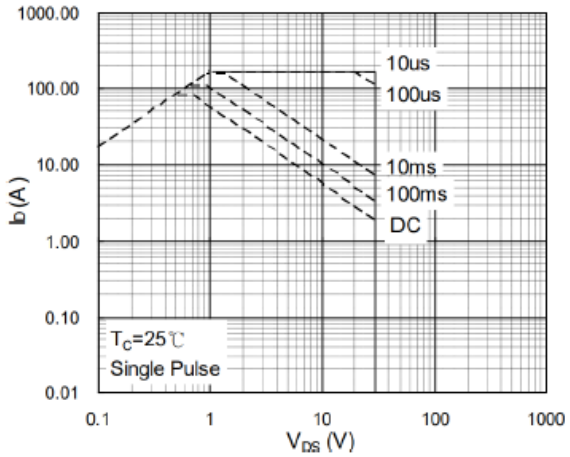

Figure 7. Maximum Safe Operating Area

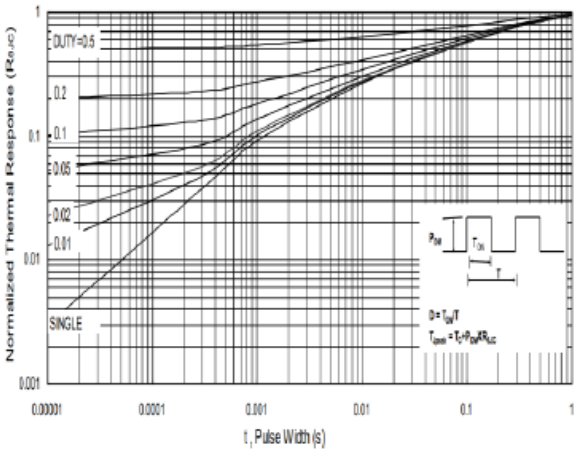

Figure 8. Normalized Transient Thermal Resistance

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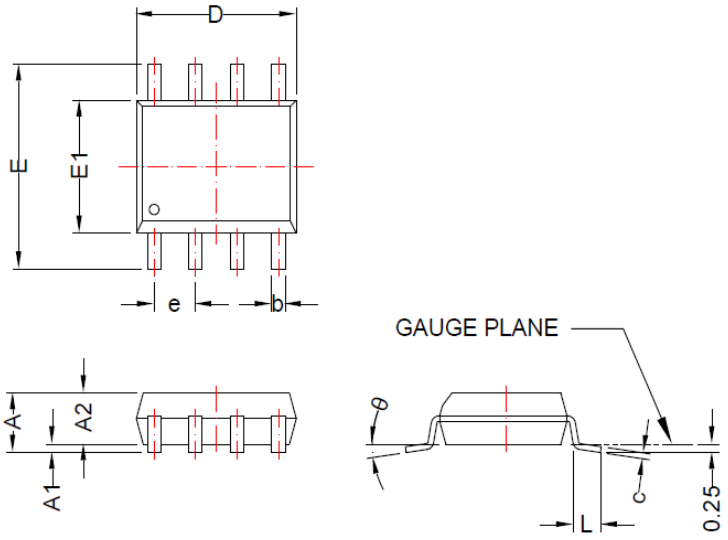
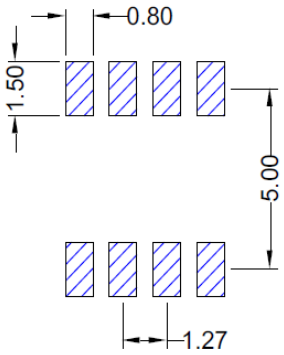
Package Dimension:

SOP-8

Package Dimension



Recommended Land Pattern



Dimensions				
Symbol	Millimeters		Inches	
	Min	Max	Min	Max
A	-	1.75	-	0.069
A1	0.10	0.25	0.004	0.010
A2	1.25	-	0.049	-
b	0.31	0.51	0.012	0.020
c	0.10	0.25	0.004	0.010
D	4.70	5.10	0.185	0.201
E	5.80	6.20	0.228	0.244
E1	3.80	4.00	0.150	0.157
e	1.27BSC		0.050BSC	
L	0.40	1.27	0.016	0.050
θ	0°	8°	0°	8°

NOTE:
DIMENSION D DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH, PROTRUSIONS OR GATE BURRS SHALL NOT EXCEED 0.15 mm PER END.

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