LMH6628QML Dual Wideband, Low Noise, Voltage Feedback Op Amp

Check for Samples: LMH6628QML

FEATURES

- **Available with Radiation Ensured 300 krad(Si)**
- **Wide Unity Gain Bandwidth: 300MHz**
- **Low Noise: 2nV/√Hz**
- **Low Distortion: −65/−74dBc (10MHz)**
- **Settling Time: 12ns to 0.1%**
- **Wide Supply Voltage Range: ±2.5V to ±6V**
- **High Output Current: ±85mA**
- **Improved Replacement for CLC428**

APPLICATIONS

- **High Speed Dual Op Amp**
- **Low Noise Integrators**
- **Low Noise Active Filters**
- **Driver/Receiver for Transmission Systems**
- **High Speed Detectors**
- **I/Q Channel Amplifiers**

DESCRIPTION

The LMH6628 is a high speed dual op amp that offers a traditional voltage feedback topology featuring unity gain stability and slew enhanced circuitry. The LMH6628's low noise and very low harmonic distortion combine to form a wide dynamic range op amp that operates from a single (5V to 12V) or dual (±5V) power supply.

Each of the LMH6628's closely matched channels provides a 300MHz unity gain bandwidth and low input voltage noise density (2nV/√Hz). Low 2nd/3rd harmonic distortion (−65/−74dBc at 10MHz) make the LMH6628 a perfect wide dynamic range amplifier for matched I/Q channels.

With its fast and accurate settling (12ns to 0.1%), the LMH6628 is also an excellent choice for wide dynamic range, anti-aliasing filters to buffer the inputs of hi resolution analog-to-digital converters. Combining the LMH6628's two tightly matched amplifiers in a single package reduces cost and board space for many composite amplifier applications such as active filters, differential line drivers/receivers, fast peak detectors and instrumentation amplifiers.

The LMH6628 is fabricated using Texas Instruments' VIP10 complimentary bipolar process.

To reduce design times and assist in board layout, the LMH6628 is supported by an evaluation board (LMH730036).

CONNECTION DIAGRAMS

Top View

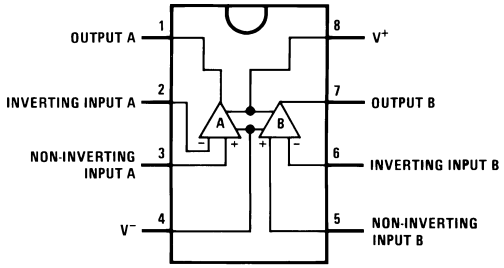

Figure 1. 8 Lead CDIP Package
See Package Number NAB0008A

Top View

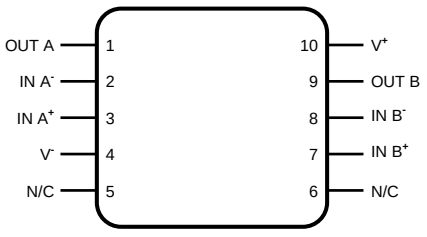

Figure 2. 10 Lead CLGA Package
See Package Number NAC0010A

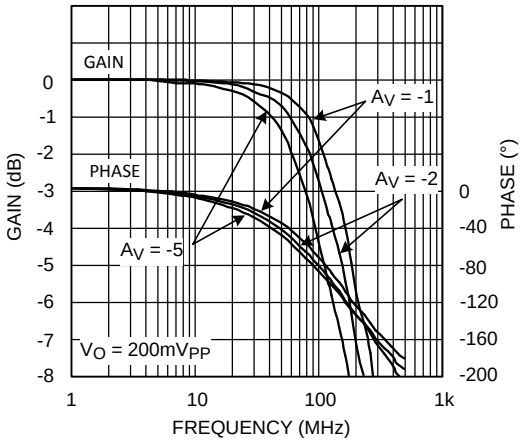

Figure 3. Inverting Frequency Response

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

ABSOLUTE MAXIMUM RATINGS (1)

Supply Voltage			$\pm 7V_{DC}$
Maximum Junction temperature (2)			+175°C
Lead temperature (Soldering, 10 seconds)			+300°C
Differential input voltage			$V^+ - V^-$
Common mode input voltage			$V^+ - V^-$
Storage temperature range			$-65°C \le T_A \le +150°C$
Power Dissipation (2)			1.0W
Short circuit current (3)			
Thermal Resistance	θ_{JA}	CDIP (Still Air)	135°C/W
		CDIP (500LF/Min Air Flow)	75°C/W
		CLGA (Still Air)	200°C/W
		CLGA (500LF/Min Air Flow)	145°C/W
	θ_{JC}	CDIP	30°C/W
		CLGA	19°C/W
Package Weight (typical)			
CDIP			TBD
CLGA			TBD
ESD Tolerance (4)			4000V

(1) Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is intended to be functional, but do not ensure specific performance limits. For specifications and test conditions, see the Electrical Characteristics. The specifications apply only for the test conditions listed. Some performance characteristics may degrade when the device is not operated under the listed test conditions.

(2) The maximum power dissipation must be derated at elevated temperatures and is dictated by T_{Jmax} (maximum junction temperature), θ_{JA} (package junction to ambient thermal resistance), and T_A (ambient temperature). The maximum allowable power dissipation at any temperature is $P_{Dmax} = (T_{Jmax} - T_A)/\theta_{JA}$ or the number given in the Absolute Maximum Ratings, whichever is lower.

(3) Output is short circuit protected to ground, however maximum reliability is obtained if output current does not exceed 160mA.

(4) Human body model, 1.5kΩ in series with 100pF.

MAXIMUM OPERATING RATINGS

Supply Voltage	±2.5V to ±6.0V
Ambient Operating Temperture Range	$-55°C \le T_A \le +125°C$

QUALITY CONFORMANCE INSPECTION

MIL-STD-883, Method 5005 - Group A

Subgroup	Description	Temp (°C)
1	Static tests at	+25
2	Static tests at	+125
3	Static tests at	-55
4	Dynamic tests at	+25
5	Dynamic tests at	+125
6	Dynamic tests at	-55
7	Functional tests at	+25
8A	Functional tests at	+125
8B	Functional tests at	-55
9	Switching tests at	+25
10	Switching tests at	+125
11	Switching tests at	-55

LMH6628QML ELECTRICAL CHARACTERISTICS DC PARAMETERS STATIC AND DC TESTS

The following conditions apply, unless otherwise specified.
V_{CC} = +5V_{DC}, A_V = +2V, R_L = 100Ω, R_F = 100Ω, −55°C ≤ T_A ≤ +125°C

Symbol	Parameter	Conditions	Notes	Min	Max	Unit	Sub-groups
I_B	Input Bias Current		(1)	-10	+10	µA	1
				-20	+20	µA	2
				-20	+20	µA	3
V_{IO}	Input Offset Voltage		(1)	-2	+2	mV	1
				-2.6	+2.6	mV	2, 3
I_{CC}	Supply Current	R_L = ∞	(1)		24	mA	1
					24	mA	2
					25	mA	3
PSRR	Power Supply Rejection Ratio	+V_S = +4.0V to +5.0V, -V_S = -4.0V to -5.0V		60		dB	1
				55		dB	2, 3
V_{OUT}	Output Voltage Range	R_L = ∞		-5.0	+5.0	V	1, 2, 3

(1) Pre and post irradiation limits are identical to those listed under electrical characteristics. These parts may be dose rate sensitive in a space environment and demonstrate enhanced low dose rate effect. Radiation end point limits for the noted parameters are specified only for the conditions as specified in MIL-STD-883, Method 1019.

LMH6628QML ELECTRICAL CHARACTERISTICS AC PARAMETERS FREQUENCY DOMAIN RESPONSE

The following conditions apply, unless otherwise specified.
V_{CC} = +5V_{DC}, A_V = +2V, R_L = 100Ω, R_F = 100Ω, −55°C ≤ T_A ≤ +125°C

Symbol	Parameter	Conditions	Notes	Min	Max	Unit	Sub-groups
SSBW	Small Signal Bandwith	-3 dB BW, V_O < 0.5 V_{PP}	(1)	50		MHz	4
GFP	Gain Flatness Peaking	0.1 MHz to 200 MHz, V_O ≤0.5 V_{PP}	(1)		0.6	dB	4
GFR	Gain Flatness Rolloff	0.1 MHz to 20 MHz, V_O ≤0.5 V_{PP}	(1)		0.6	dB	4
A_{OL}	Open Loop Gain		(1)	55		dB	4

(1) Group A testing only.

LMH6628QML ELECTRICAL CHARACTERISTICS AC PARAMETERS DISTORTION AND NOISE TESTS

The following conditions apply, unless otherwise specified.
V_{CC} = +5V_{DC}, A_V = +2V, R_L = 100Ω, R_F = 100Ω, −55°C ≤ T_A ≤ +125°C

Symbol	Parameter	Conditions	Notes	Min	Max	Unit	Sub-groups
HD_2	Second Harmonic Distortion	1 V_{PP}at10 MHz	(1)		50	dBc	4
HD_3	Third Harmonic Distortion	1 V_{PP}at10 MHz	(1)		60	dBc	4

(1) Group A testing only.

LMH6628QML ELECTRICAL CHARACTERISTICS DC PARAMETERS DRIFT VALUES

The following conditions apply, unless otherwise specified.
Deltas not required on B Level product. Deltas required for S Level product at Group B5 only, or as specified on the Internal Processing Instructions (IPI).

Symbol	Parameter	Conditions	Notes	Min	Max	Unit	Sub-groups
I_B	Input Bias Current		(1)	-1.0	+1.0	µA	1
V_{IO}	Input Offset Voltage		(1)	-0.2	+0.2	mV	1
I_{CC}	Supply Current	R_L = ∞	(1)	-1	+1	mA	1

(1) If not tested, shall be ensured to the limits specified.

TYPICAL PERFORMANCE CHARACTERISTICS

(T_A = +25°, A_V = +2, V_{CC} = ±5V, R_F =100Ω, R_L = 100Ω, unless specified)

Non-Inverting Frequency Response

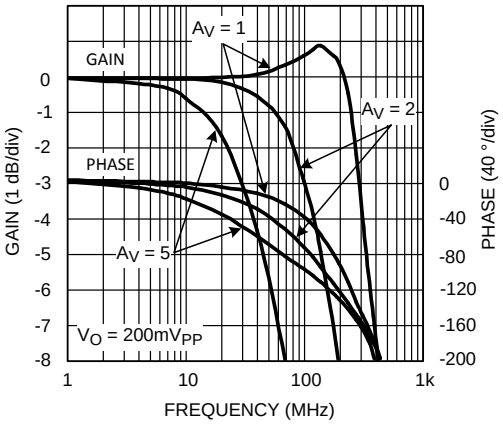

Figure 4.

Inverting Frequency Response

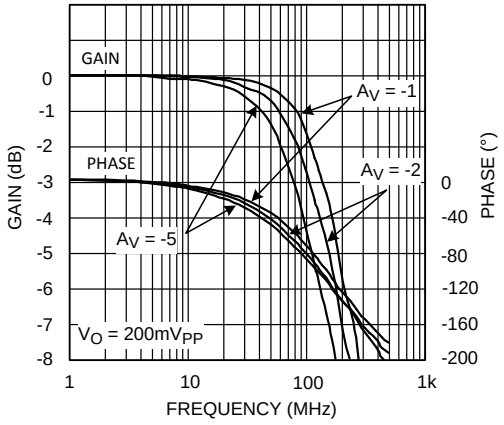

Figure 5.

Frequency Response vs. Load Resistance

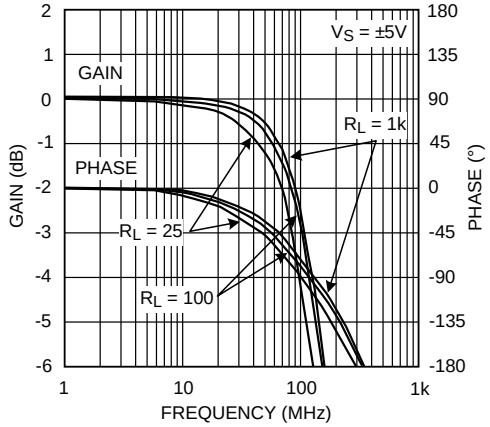

Figure 6.

Frequency Response vs. Output Amplitude

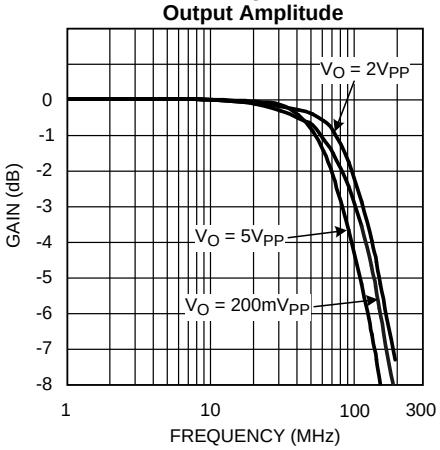

Figure 7.

Frequency Response vs. Capacitive Load

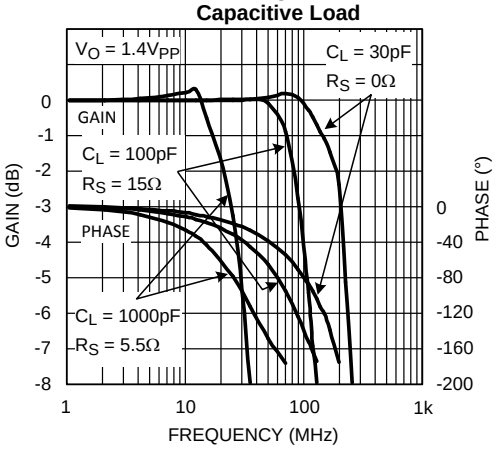

Figure 8.

Gain Flatness & Linear Phase

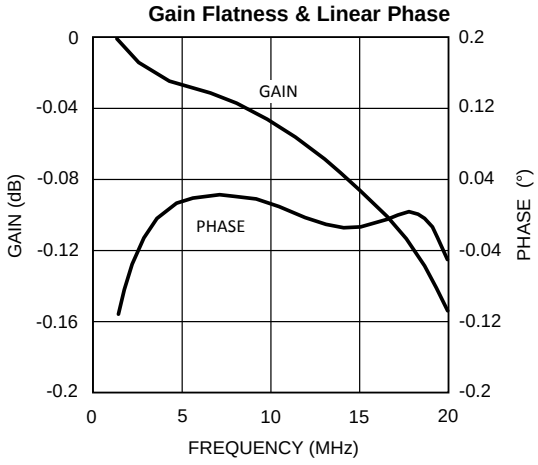

Figure 9.

TYPICAL PERFORMANCE CHARACTERISTICS (continued)

(T_A = +25°, A_V = +2, V_{CC} = ±5V, R_F =100Ω, R_L = 100Ω, unless specified)

Channel Matching

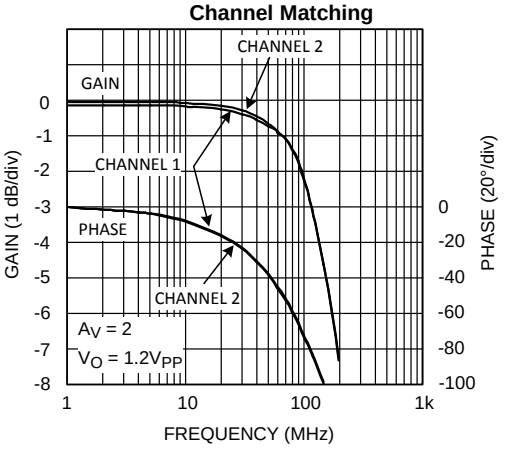

Figure 10.

Channel to Channel Crosstalk

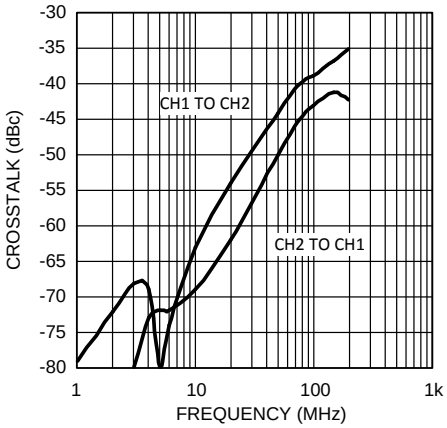

Figure 11.

Pulse Response (V_O = 2V)

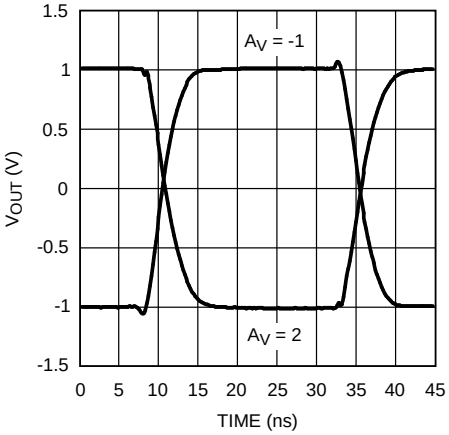

Figure 12.

Pulse Response (V_O = 100mV)

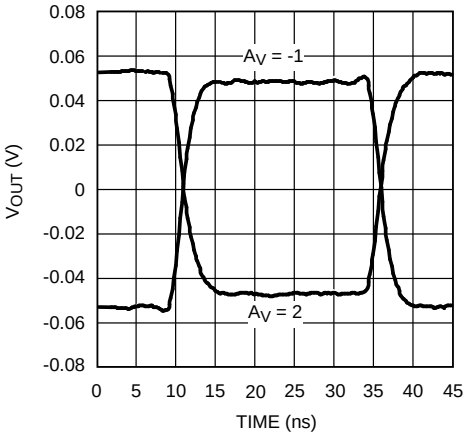

Figure 13.

2nd Harmonic Distortion vs. Output Voltage

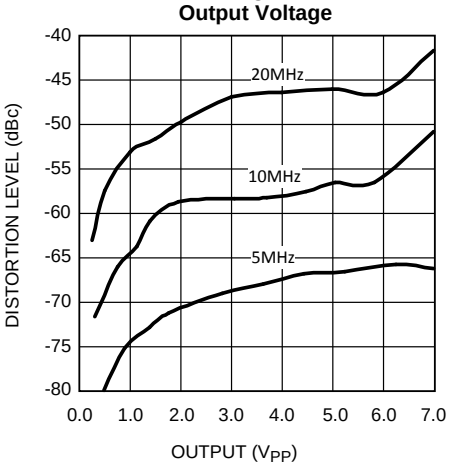

Figure 14.

3rd Harmonic Distortion vs. Output Voltage

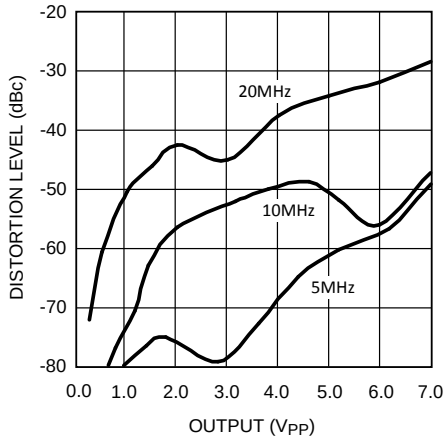

Figure 15.

TYPICAL PERFORMANCE CHARACTERISTICS (continued)

(T_A = +25°, A_V = +2, V_{CC} = ±5V, R_F =100Ω, R_L = 100Ω, unless specified)

2nd & 3rd Harmonic Distortion vs. Frequency

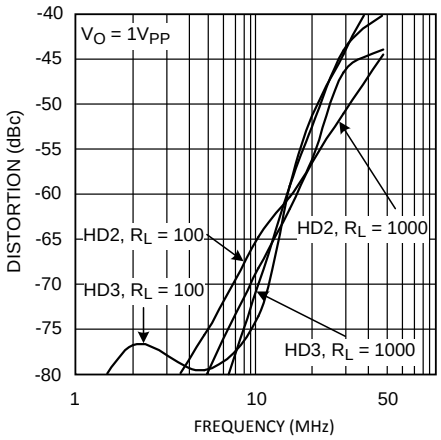

Figure 16.

PSRR and CMRR (±5V)

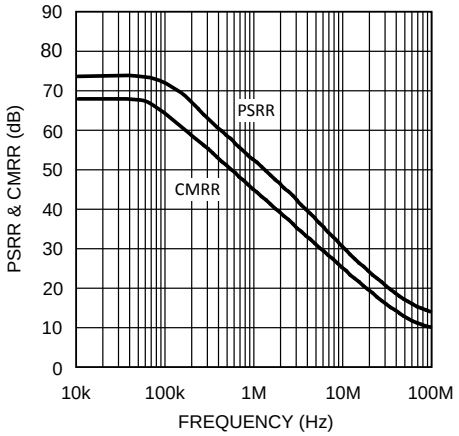

Figure 17.

PSRR and CMRR (±2.5V)

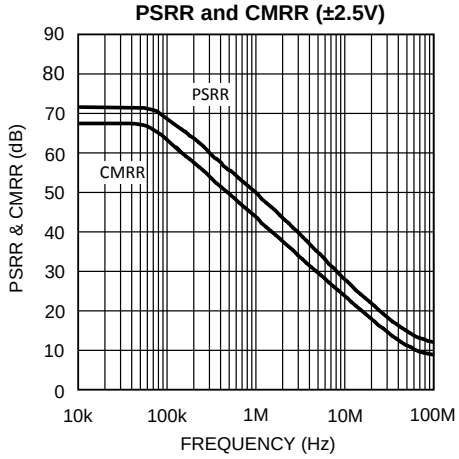

Figure 18.

Closed Loop Output Resistance (±2.5V)

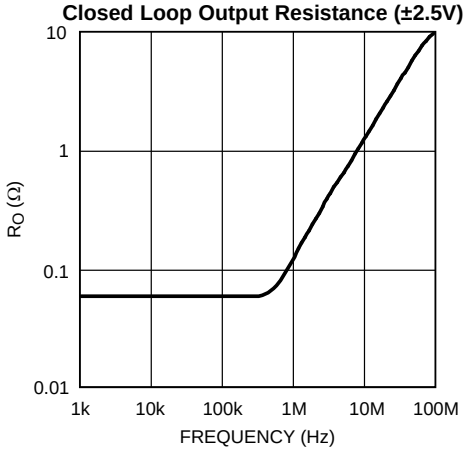

Figure 19.

Closed Loop Output Resistance (±5V)

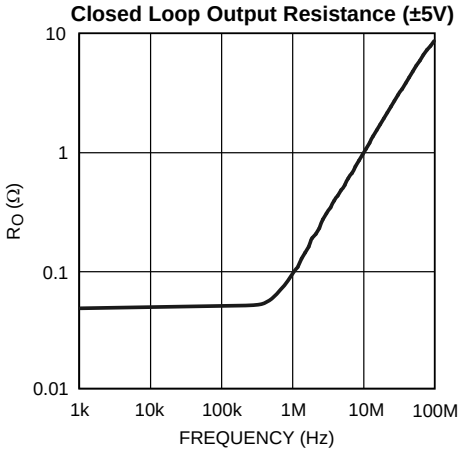

Figure 20.

Open Loop Gain & Phase (±2.5V)

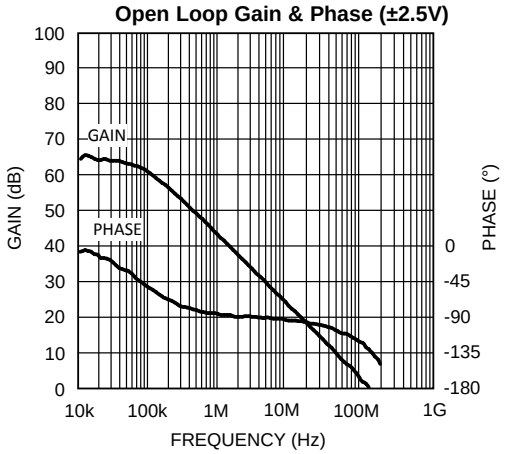

Figure 21.

TYPICAL PERFORMANCE CHARACTERISTICS (continued)

(T_A = +25°, A_V = +2, V_{CC} = ±5V, R_F =100Ω, R_L = 100Ω, unless specified)

Open Loop Gain & Phase (±5V)

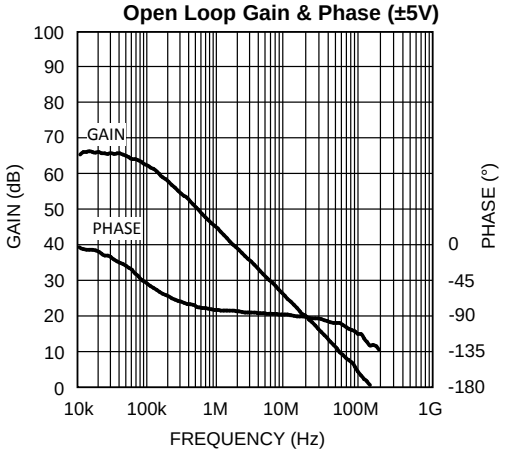

Figure 22.

Recommended R_S vs. C_L

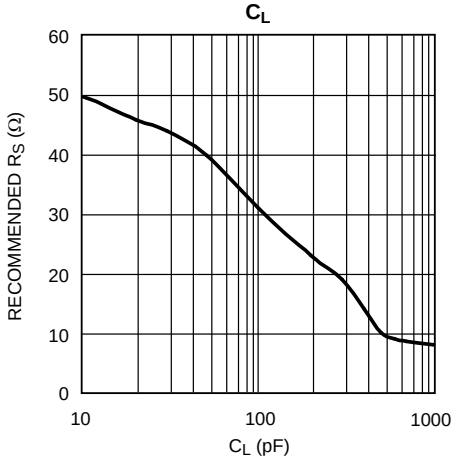

Figure 23.

DC Errors vs. Temperature

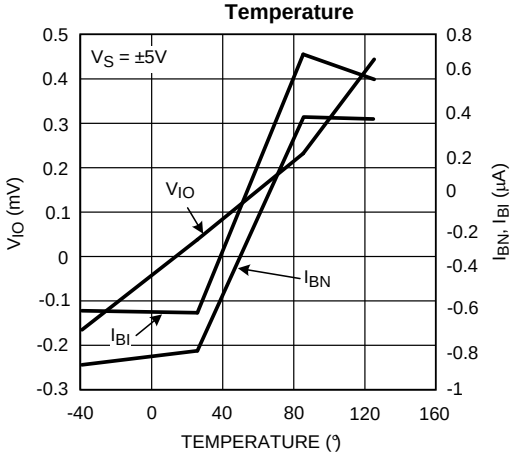

Figure 24.

Maximum V_O vs. R_L

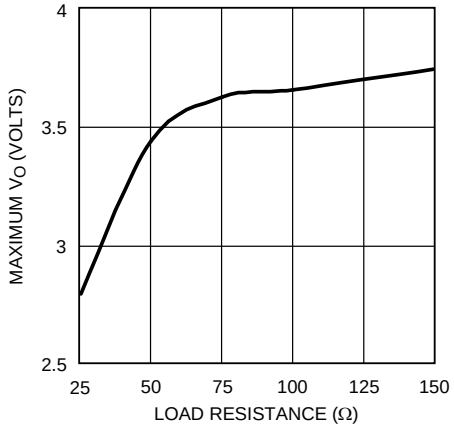

Figure 25.

2-Tone, 3rd Order Intermodulation Intercept

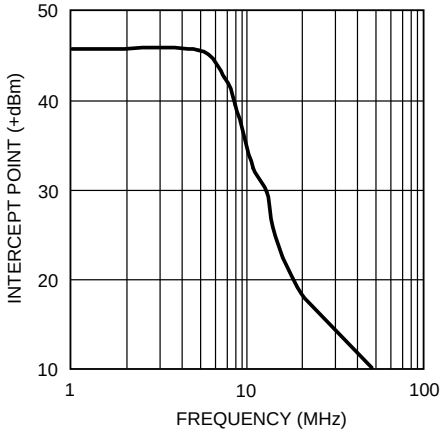

Figure 26.

Voltage & Current Noise vs. Frequency

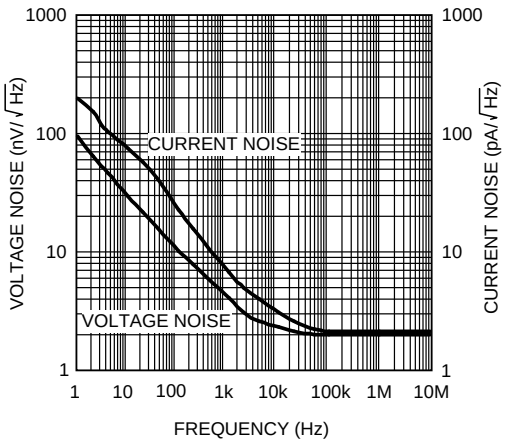

Figure 27.

TYPICAL PERFORMANCE CHARACTERISTICS (continued)

(T_A = +25°, A_V = +2, V_{CC} = ±5V, R_F =100Ω, R_L = 100Ω, unless specified)

Settling Time vs. Accuracy

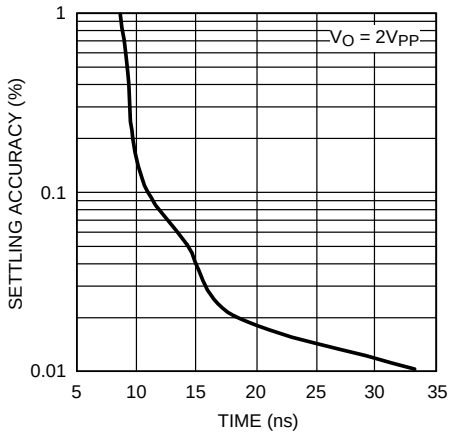

Figure 28.

APPLICATION SECTION

LOW NOISE DESIGN

Ultimate low noise performance from circuit designs using the LMH6628 requires the proper selection of external resistors. By selecting appropriate low valued resistors for R_F and R_G, amplifier circuits using the LMH6628 can achieve output noise that is approximately the equivalent voltage input noise of 2nV/√Hz multiplied by the desired gain (A_V).

DC BIAS CURRENTS AND OFFSET VOLTAGES

Cancellation of the output offset voltage due to input bias currents is possible with the LMH6628. This is done by making the resistance seen from the inverting and non-inverting inputs equal. Once done, the residual output offset voltage will be the input offset voltage (V_{OS}) multiplied by the desired gain (A_V). Texas Application Note OA-07 offers several solutions to further reduce the output offset.

OUTPUT AND SUPPLY CONSIDERATIONS

With ±5V supplies, the LMH6628 is capable of a typical output swing of ±3.8V under a no-load condition. Additional output swing is possible with slightly higher supply voltages. For loads of less than 50Ω, the output swing will be limited by the LMH6628's output current capability, typically 85mA.

Output settling time when driving capacitive loads can be improved by the use of a series output resistor. See the plot labeled Figure 23 in the TYPICAL PERFORMANCE CHARACTERISTICS.

LAYOUT

Proper power supply bypassing is critical to insure good high frequency performance and low noise. De-coupling capacitors of 0.1µF should be placed as close as possible to the power supply pins. The use of surface mounted capacitors is recommended due to their low series inductance.

A good high frequency layout will keep power supply and ground traces away from the inverting input and output pins. Parasitic capacitance from these nodes to ground causes frequency response peaking and possible circuit oscillation. See OA-15 for more information. Texas Instruments suggests the LMH730036 (SOIC) dual op amp evaluation board as a guide for high frequency layout and as an aid in device evaluation.

ANALOG DELAY CIRCUIT (ALL-PASS NETWORK)

The circuit in Figure 29 implements an all-pass network using the LMH6628. A wide bandwidth buffer (LM7121) drives the circuit and provides a high input impedance for the source. As shown in Figure 30, the circuit provides a 13.1ns delay (with R = 40.2Ω, C = 47pF). R_F and R_G should be of equal and low value for parasitic insensitive operation.

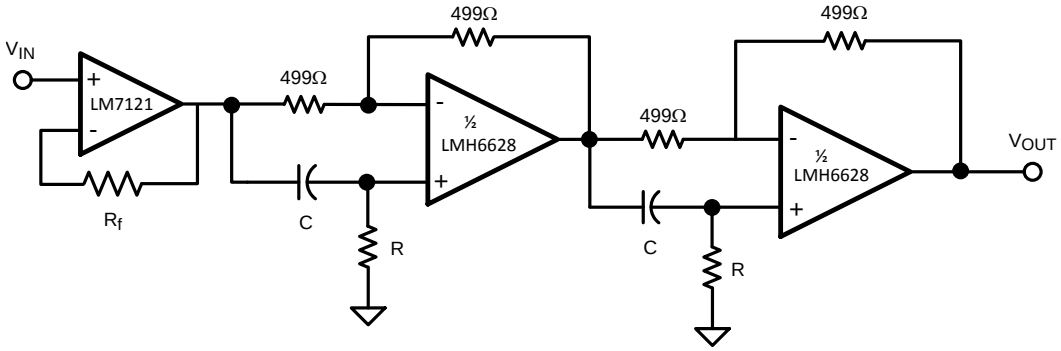

Figure 29. Circuit That Implements an All-pass Network Using the LMH6628

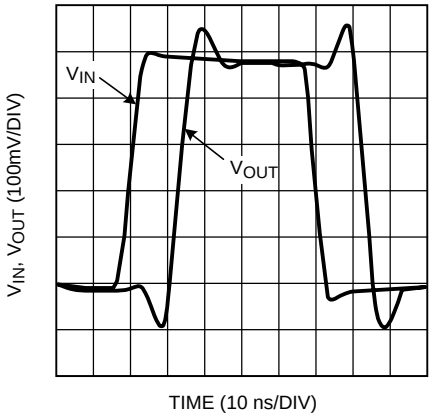

Figure 30. Delay Circuit Response to 0.5V Pulse

The circuit gain is +1 and the delay is determined by the following equations.

$$\tau delay = 2(2RC + T_d) \quad (1)$$

$$T_d = \frac{1}{360}\frac{d\phi}{df}; \quad (2)$$

where

- T_d is the delay of the op amp at A_V = +1

The LMH6628QML provides a typical delay of 2.8ns at its −3dB point.

FULL DUPLEX DIGITAL OR ANALOG TRANSMISSION

Simultaneous transmission and reception of analog or digital signals over a single coaxial cable or twisted-pair line can reduce cabling requirements. The LMH6628's wide bandwidth and high common-mode rejection in a differential amplifier configuration allows full duplex transmission of video, telephone, control and audio signals.

In the circuit shown in Figure 31, one of the LMH6628's amps is used as a "driver" and the other as a difference "receiver" amplifier. The output impedance of the "driver" is essentially zero. The two R's are chosen to match the characteristic impedance of the transmission line. The "driver" op amp gain can be selected for unity or greater.

Receiver amplifier A_2 (B_2) is connected across R and forms differential amplifier for the signals transmitted by driver A_2 (B_2). If R_F equals R_G, receiver A_2 (B_1) will then reject the signals from driver A_1 (B_1) and pass the signals from driver B_1 (A_1).

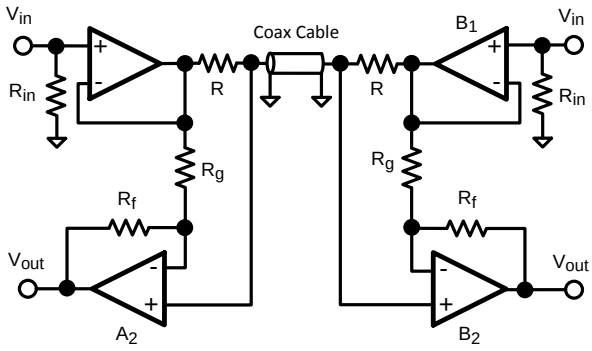

Figure 31. Full Duplex Transmit and Receive using the LMH6628

The output of the receiver amplifier will be:

$$V_{out_{A(B)}} = \frac{1}{2} V_{in_{A(B)}} \left[1 - \frac{R_f}{R_g}\right] + \frac{1}{2} V_{in_{B(A)}} \left[1 + \frac{R_f}{R_g}\right] \quad (3)$$

Care must be given to layout and component placement to maintain a high frequency common-mode rejection. The plot of Figure 32 shows the simultaneous reception of signals transmitted at 1MHz and 10MHz.

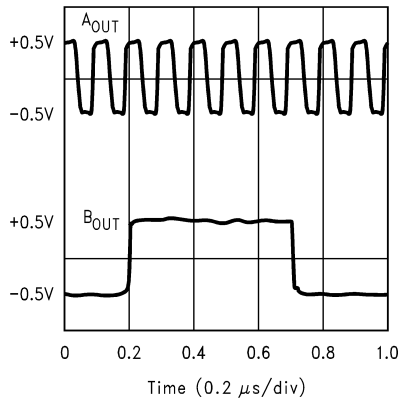

Figure 32. Simultaneous Reception of Signals Transmitted at 1MHz and 10MHz

POSITIVE PEAK DETECTOR

The LMH6628's dual amplifiers can be used to implement a unity-gain peak detector circuit as shown in Figure 33.

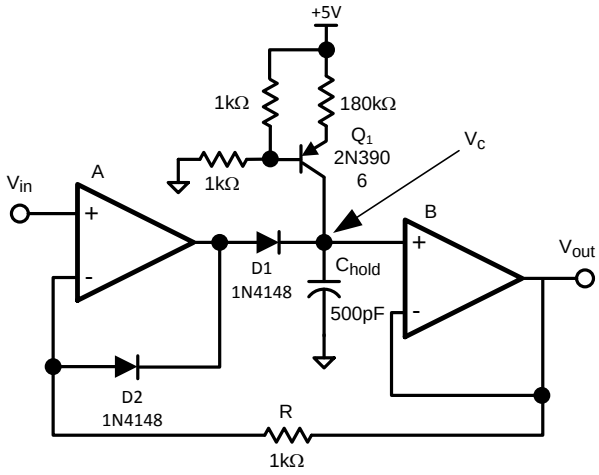

Figure 33. LMH6628's Dual Amplifiers Used to Implement a Unity-Gain Peak Detector Circuit

The acquisition speed of this circuit is limited by the dynamic resistance of the diode when charging C_{hold}. A plot of the circuit's performance is shown in Figure 34 with a 1MHz sinusoidal input.

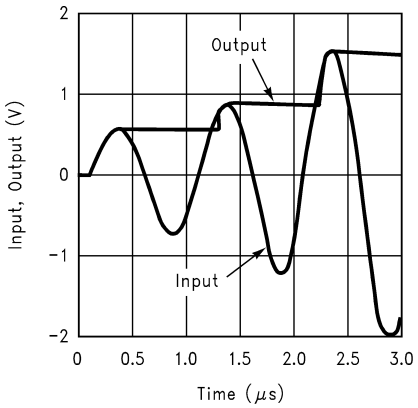

Figure 34. Circuit's Performance With a 1MHz Sinusoidal Input

A current source, built around Q1, provides the necessary bias current for the second amplifier and prevents saturation when power is applied. The resistor, R, closes the loop while diode D2 prevents negative saturation when V_{IN} is less than V_C. A MOS-type switch (not shown) can be used to reset the capacitor's voltage.

The maximum speed of detection is limited by the delay of the op amps and the diodes. The use of Schottky diodes will provide faster response.

ADJUSTABLE OR BANDPASS EQUALIZER

A "boost" equalizer can be made with the LMH6628 by summing a bandpass response with the input signal, as shown in Figure 35.

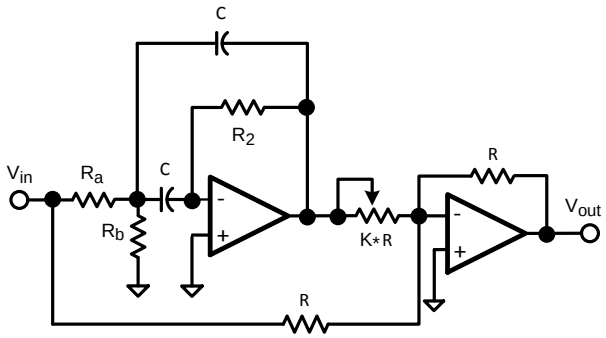

Figure 35. "Boost" Equalizer Made With the LMH6628 by Summing a Bandpass Response With the Input Signal

The overall transfer function is shown in Equation 4.

$$\frac{V_{out}}{V_{in}} = \left[\frac{R_b}{K(R_a + R_b)}\right] \frac{s2Q\omega_o}{s^2 + s\frac{\omega_o}{Q} + \omega_o{}^2} - 1 \quad (4)$$

To build a boost circuit, use the design equations Equation 5 and Equation 6.

$$\frac{R_2 C}{2} = \frac{Q}{\omega_o} \quad (5)$$

$$2C\,(R_a \| R_b) = \frac{1}{Q\omega_o} \quad (6)$$

Select R_2 and C using Equation 5. Use reasonable values for high frequency circuits - R_2 between 10Ω and 5kΩ, C between 10pF and 2000pF. Use Equation 6 to determine the parallel combination of R_a and R_b. Select R_a and R_b by either the 10Ω to 5kΩ criteria or by other requirements based on the impedance V_{in} is capable of driving. Finish the design by determining the value of K from Equation 7.

$$\text{Peak Gain} = \frac{V_{out}}{V_{in}}(\omega_o) = \frac{R_2}{2KR_a} - 1 \tag{7}$$

Figure 36 shows an example of the response of the circuit of Figure 35, where f_o is 2.3MHz. The component values are as follows: R_a=2.1kΩ, R_b = 68.5Ω, R_2 = 4.22kΩ, R = 500Ω, KR = 50Ω, C = 120pF.

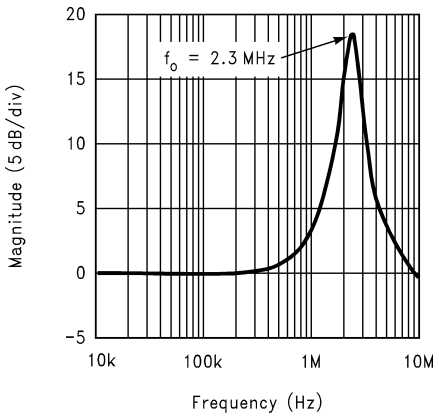

Figure 36. Example of Response of Circuit of Figure 35, Where f_o is 2.3MHz

REVISION HISTORY

Date Released	Revision	Section	Changes
12/03/2010	A	New Corporate Format Release	1 MDS data sheet converted into a Corp. data sheet format. Following MDS data sheet will be Archived MNLMH6628-X-RH, Rev. 0A0
07/12/2011	B	Connection Diagrams	Replaced 8 Lead CDIP (NAB0008A) diagram depicting single Op Amp with diagram depicting dual Op Amp. Also replaced 10 Lead CLGA (NAC0010A) diagram depicting single Op Amp with diagram depicting dual Op Amp.
05/02/2013	B	All	Changed layout of National Data Sheet to TI format

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
5962-0254501MZA	ACTIVE	CFP	NAC	10	54	Non-RoHS & Green	Call TI	Level-1-NA-UNLIM	-55 to 125	LMH6628 WG-QML Q 5962-02545 01MZA ACO 01MZA >T	Samples
5962-0254501VPA	ACTIVE	CDIP	NAB	8	40	Non-RoHS & Green	Call TI	Level-1-NA-UNLIM	-55 to 125	LMH6628J-QV 5962-02545 01VPA Q ACO 01VPA Q >T	Samples
5962F0254501VZA	ACTIVE	CFP	NAC	10	54	Non-RoHS & Green	Call TI	Level-1-NA-UNLIM	-55 to 125	LMH6628 WGFQMLV Q 5962F02545 01VZA ACO 01VZA >T	Samples
LMH6628J-QMLV	ACTIVE	CDIP	NAB	8	40	Non-RoHS & Green	Call TI	Level-1-NA-UNLIM	-55 to 125	LMH6628J-QV 5962-02545 01VPA Q ACO 01VPA Q >T	Samples
LMH6628WG-QML	ACTIVE	CFP	NAC	10	54	Non-RoHS & Green	Call TI	Level-1-NA-UNLIM	-55 to 125	LMH6628 WG-QML Q 5962-02545 01MZA ACO 01MZA >T	Samples
LMH6628WGFQMLV	ACTIVE	CFP	NAC	10	54	Non-RoHS & Green	Call TI	Level-1-NA-UNLIM	-55 to 125	LMH6628 WGFQMLV Q 5962F02545 01VZA ACO 01VZA >T	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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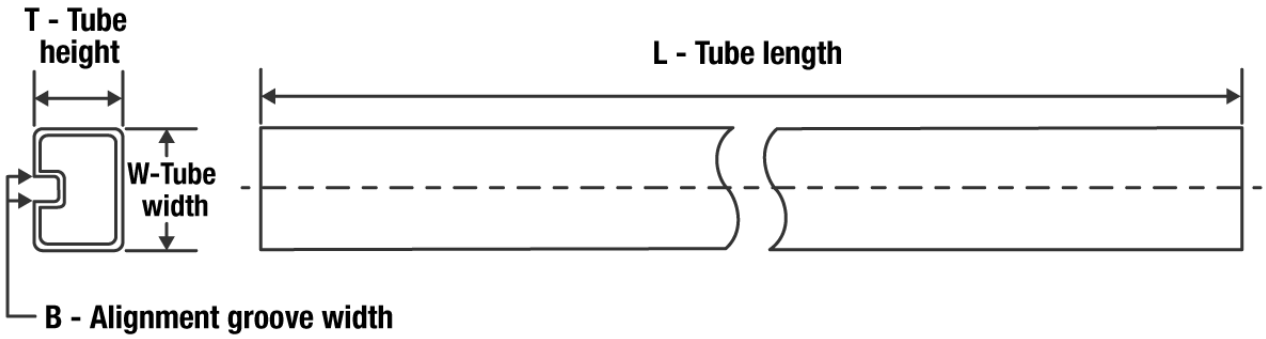
OTHER QUALIFIED VERSIONS OF LMH6628QML, LMH6628QML-SP :

- Military : LMH6628QML
- Space : LMH6628QML-SP

NOTE: Qualified Version Definitions:

- Military - QML certified for Military and Defense Applications
- Space - Radiation tolerant, ceramic packaging and qualified for use in Space-based application

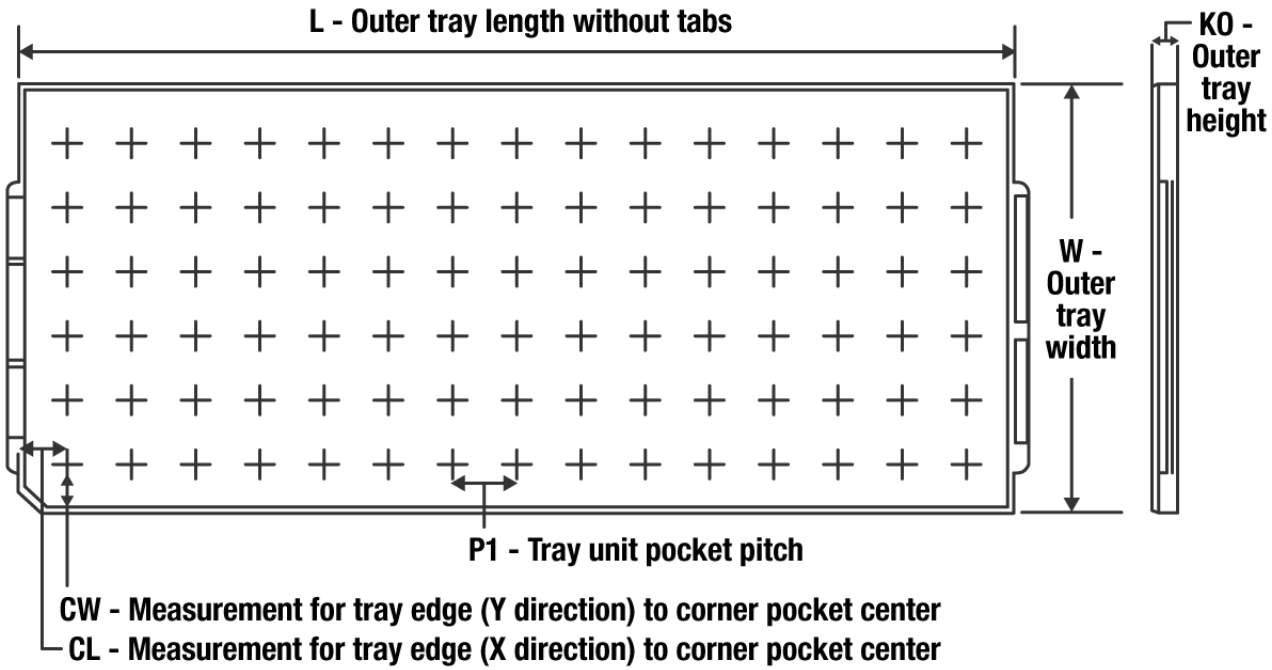
TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
5962-0254501VPA	NAB	CDIP	8	40	502	14	10668	4.32
LMH6628J-QMLV	NAB	CDIP	8	40	502	14	10668	4.32

TRAY

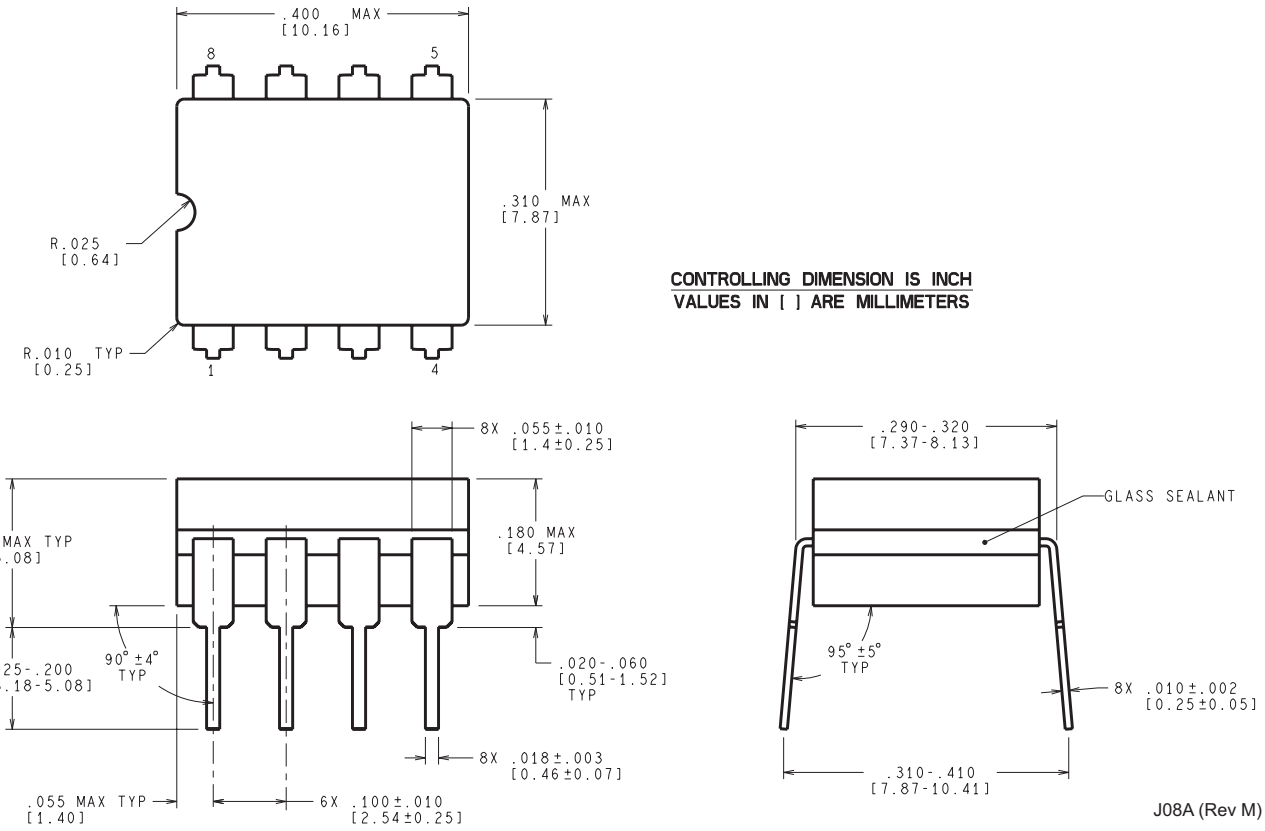


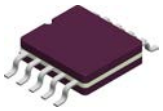
Chamfer on Tray corner indicates Pin 1 orientation of packed units.

*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	Unit array matrix	Max temperature (°C)	L (mm)	W (mm)	K0 (µm)	P1 (mm)	CL (mm)	CW (mm)
5962-0254501MZA	NAC	CFP	10	54	6 X 9	100	101.6	101.6	8001	2.78	16.08	16.08
5962F0254501VZA	NAC	CFP	10	54	6 X 9	100	101.6	101.6	8001	2.78	16.08	16.08
LMH6628WG-QML	NAC	CFP	10	54	6 X 9	100	101.6	101.6	8001	2.78	16.08	16.08
LMH6628WGFQMLV	NAC	CFP	10	54	6 X 9	100	101.6	101.6	8001	2.78	16.08	16.08

NAB0008A


.400 MAX
[10.16]
8
5
.310 MAX
[7.87]
R.025
[0.64]
R.010 TYP
[0.25]
1
4
CONTROLLING DIMENSION IS INCH
VALUES IN [ ] ARE MILLIMETERS
8X .055±.010
[1.4±0.25]
.200 MAX TYP
[5.08]
.180 MAX
[4.57]
8X .125-.200
[3.18-5.08]
90° ±4°
TYP
.020-.060
[0.51-1.52]
TYP
8X .018±.003
[0.46±0.07]
.055 MAX TYP
[1.40]
6X .100±.010
[2.54±0.25]
.290-.320
[7.37-8.13]
GLASS SEALANT
95° ±5°
TYP
8X .010±.002
[0.25±0.05]
.310-.410
[7.87-10.41]
J08A (Rev M)

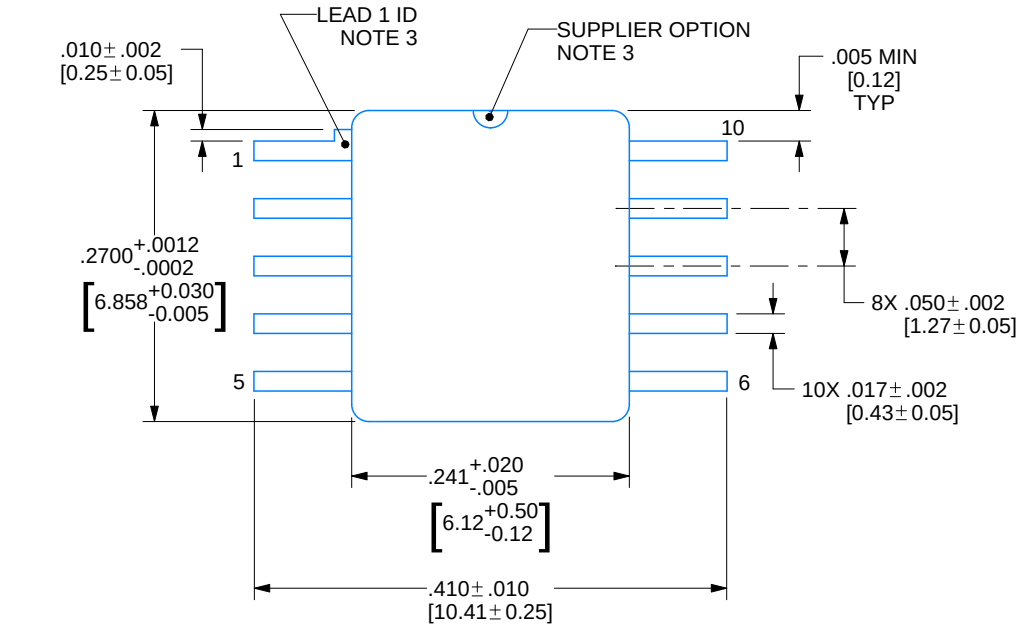


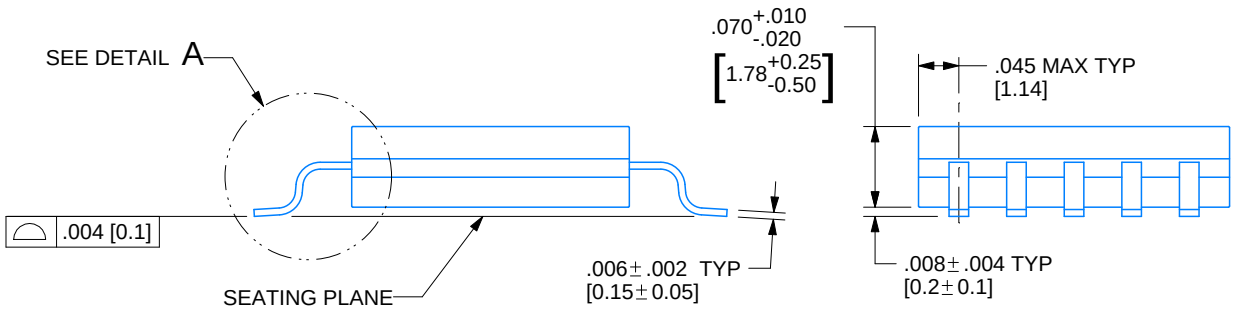
PACKAGE OUTLINE

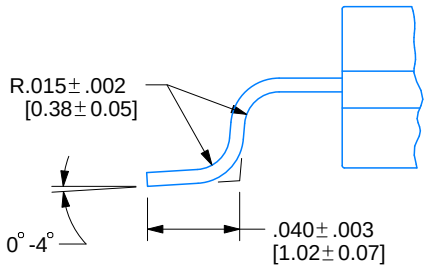
NAC0010A

CFP - 2.33mm max height

CERAMIC FLATPACK







DETAIL A
TYPICAL

4215196/C 02/2022

NOTES:

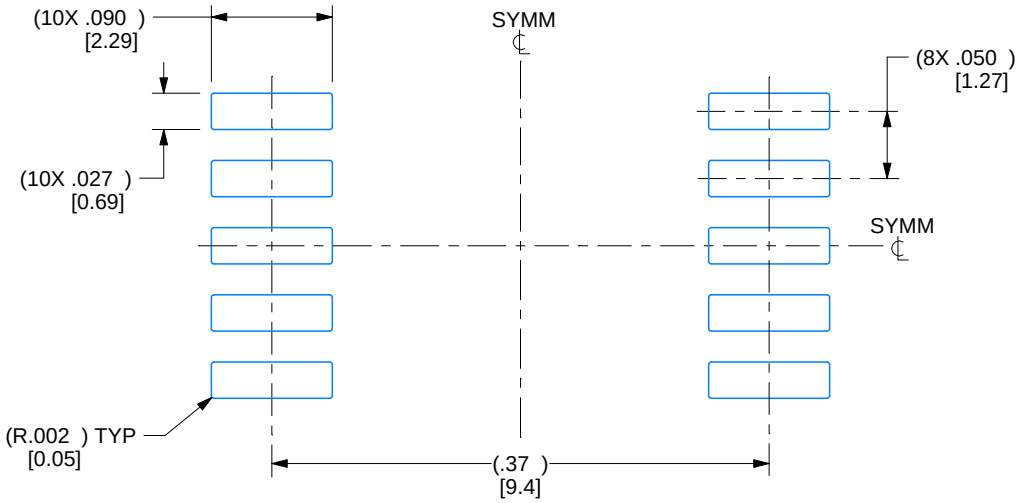
1. All controlling linear dimensions are in inches. Dimensions in brackets are in millimeters. Any dimension in brackets or parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. For solder thickness and composition, see the "Lead Finish Composition/Thickness" link in the packaging section of the Texas Instruments website
3. Lead 1 identification shall be:
   a) A notch or other mark within this area
   b) A tab on lead 1, either side
4. No JEDEC registration as of December 2021

EXAMPLE BOARD LAYOUT

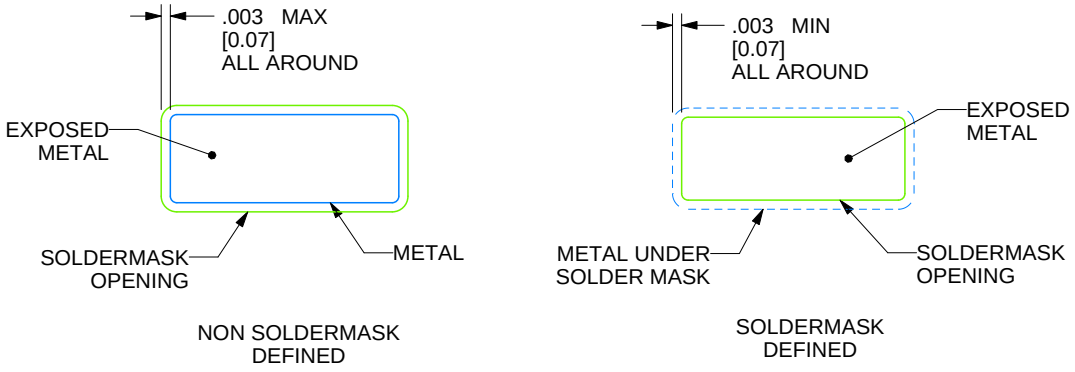
NAC0010A

CFP - 2.33mm max height

CERAMIC FLATPACK



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 7X



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