National Semiconductor

LMH2190

PRELIMINARY
June 4, 2009

Quad Channel 26 MHz Clock Tree Driver with I²C Interface

General Description

The LMH2190 is a quad channel configurable clock distribution device which supplies the system clock to peripherals in mobile handsets or other applications. It provides a solution to clocking issues such as drive capability for fanout or longer traces, protection of the master clock from varying loads and frequency pulling effects, isolation buffering from noisy modules, and crosstalk isolation. It has very low phase noise which enables it to drive sensitive modules such as Wireless LAN and Bluetooth.

The LMH2190 can be clocked up to 26 MHz, and has an independent clock request pin for each clock output which allows the peripheral to control the clock. It features an integrated LDO which provides an ultra low noise voltage supply with 10 mA external load current which can be used to supply the TCXO or other clock source.

The I²C serial interface can be used to override the default configuration of the device to optimize the LMH2190 for the application. Some of these programmable features include setting the polarity of both the clock and the clock request inputs. In addition, the clock outputs have programmable output drive current to optimize for the connected load. EMI switching noise can be controlled by configuring output drive and skew settings.

The LMH2190 quad clock distributor is offered in a tiny 1.5mm x 1.5mm 16 bump microSMD package. Its' small size and low supply current make it ideal for portable applications.

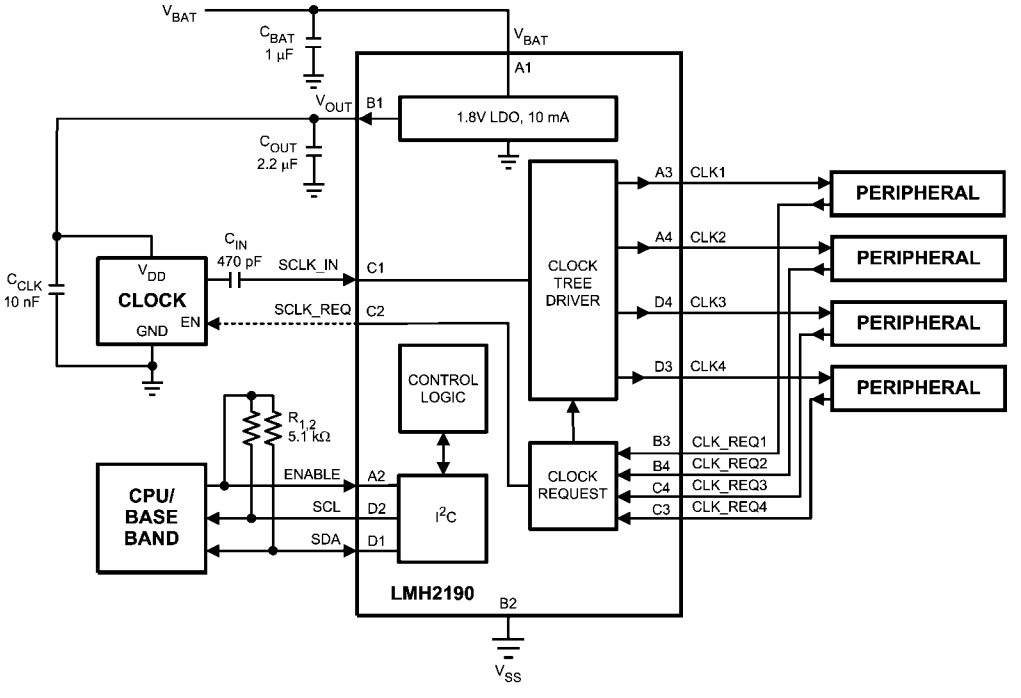
Features

- 1 Input Clock, 4 Output Clocks
- Independent clock request
- Support both square or sine wave input
- Skewed clock outputs
- High isolation of supply noise to clock input
- High output to output Isolation
- Output Drive up to 50 pF
- EMI controlled output edges and EMI filtering
- Integrated Low-Dropout Regulator
  - — Low Output Noise Voltage
  - — 10 mA load current
- I²C Configurable up to 400 kHz (Fast Mode)
- Ultra low standby current
- V_{BAT} range = 2.5V to 5.5V

Applications

- Mobile handsets
- PDAs
- Portable Equipment

Typical Application



Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Supply Voltage	
V_{BAT} - V_{SS}	-0.3V to 6V
LVCMOS port IO voltage	-0.3V to (V_{OUT} + 0.3V)
ESD Tolerance (Note 2)	
Human Body Model	2000V
Machine Model	200V
Charge Device Model	1000V
Storage Temperature Range	−65°C to 150°C
Junction Temperature (Note 3)	150°C
Maximum Lead Temperature (Soldering,10 sec)	230°C

Operating Ratings (Note 1)

Supply Voltage (V_{BAT} - V_{SS})	2.5V to 5.5V
V_{ENABLE}	0 to 2V
Input Clock, SCLK_IN	
DC Mode	13 to 26 MHz
AC Mode	32 kHz to 26 MHz
Duty Cycle	45% to 55%
Temperature Range	-20°C to +85°C
Package Thermal Resistance θ_{JA} (Note 3)	113.6°C/W

3.5 V DC and AC Electrical Characteristics (Notes 4, 11)

Unless otherwise specified, all limits are guaranteed at T_A = 25°C, V_{BAT} = 3.5V, f_{SCLK_IN} = 26 MHz, C_{OUT} = 2.2 µF, V_{DD_IO} = 1.8V (See *Block Diagram* and (Note 9)), Registers are in default setting. **Boldface** limits apply at the temperature extremes.

Symbol	Parameter	Condition	Min (Note 6)	Typ (Note 5)	Max (Note 6)	Units
Supply Current (Note 8)						
I_{DD}	Supply Current	Clock outputs toggling at 26 MHz without external capacitors on CLK1/2/3/4, LDO is ON, I_{OUT} = 0 mA.		3		mA
		In Shutdown. No clocks toggling. LDO is OFF		0.1	**2**	µA
		In Shutdown. Input CLK toggling, no Clock outputs toggling. LDO is OFF.		0.1	**10**	µA
I_{DDQ}	Quiescent Current	No Clock outputs toggling. LDO is ON, I_{OUT} = 0 mA.		37	**70**	µA
		No Clock outputs toggling, LDO is ON, I_{OUT} = 10 mA.		50	**180**	
I_{DDEN}	Current to Enable pin	I²C port is operational.			**2**	mA
I_{DDEN}	Current to Enable pin	I²C port is idle.			**2**	µA
C_{PD}	Power Dissipation Capacitance per CLK output	Defined with respect to V_{OUT}= 1.8V		15	**tbd**	pF
Clock Outputs (CLK1/2/3/4)						
tp_{LH}	Propagation Delay SCLK_IN to CLK1 - Low to High, *Figure 1* (Note 7)	50% to 50%		6	**tbd**	ns
tp_{HL}	Propagation Delay SCLK_IN to CLK1 - High to Low, *Figure 1* (Note 7)	50% to 50%		7	**tbd**	
t_{SKEW}	Skew Between Outputs (Either Edge), (Note 7)	CLK1 to CLK2. 50% to 50%	**tbd**	6	**tbd**	
		CLK2 to CLK3 and CLK3 to CLK4. 50% to 50%	**tbd**	3.5	**tbd**	
t_{RISE}	Rise Time, (Note 13)	C_L = 10 pF to 50 pF, 20% to 80%	**1**	3	**5**	ns
t_{FALL}	Fall Time, (Note 13)	C_L = 10 pF to 50 pF, 20% to 80%	**1**	3	**5**	
CLK_DC	Output Clock Duty Cycle, *Figure 3* (Note 7)	C_L = 10 pF to 50 pF	**43**	50	**57**	%

Symbol	Parameter	Condition		Min (Note 6)	Typ (Note 5)	Max (Note 6)	Units
$Jitter_{RMS}$	Additive RMS period Jitter	BW = 100 Hz to 1 MHz	CLK1		343		fs
			CLK2		403		
			CLK3		456		
			CLK4		506		
$Jitter_{P2P}$	Additive Peak-to-Peak Period Jitter	CLK1			tbd		ps
		CLK2			tbd		
		CLK3			tbd		
		CLK4			tbd		
Phase Noise	CLK1 Additive Phase Noise with Output	f = 100 Hz			-130		dBc/Hz
		f = 1 kHz			-144		
		f = 10 kHz			-152		
		f = 100 kHz			-158		
		f = 1 MHz			-165		
	CLK2 Additive Phase Noise with Output	f = 100 Hz			-128		
		f = 1 kHz			-139		
		f = 10 kHz			-146		
		f = 100 kHz			-151		
		f = 1 MHz			-153		
	CLK3 Additive Phase Noise with Output	f = 100 Hz			-127		
		f = 1 kHz			-138		
		f = 10 kHz			-144		
		f = 100 kHz			-148		
		f = 1 MHz			-150		
	CLK4 Additive Phase Noise with Output	f = 100 Hz			-125		
		f = 1 kHz			-135		
		f = 10 kHz			-142		
		f = 100 kHz			-147		
		f = 1 MHz			-148		
V_{OH}	CLK1/2/3/4 Output Voltage High Level	CLK1/2/3/4 = -2 mA		**1.6**			V
V_{OL}	CLK1/2/3/4 Output voltage Low Level	CLK1/2/3/4 = 2 mA				**0.2**	
System Clock Input (SCLK_IN)							
V_{IH}	SCLK_IN Input Voltage High Level	DC Mode		**0.65 x V_{DD_IO}**		**2.0**	V
		AC Mode		**1.2**		**1.8**	
V_{IL}	SCLK_IN Input Voltage Low Level	DC Mode		**0**		**0.35 x V_{DD_IO}**	V
		AC Mode		**0**		**0.6**	
I_{IH}	SCLK_IN Input Current High Level	SCLK_IN = 1.8V, Clock path disabled		**-1**	0	**+1**	µA
I_{IL}	SCLK_IN Input Current Low Level	SCLK_IN = V_{SS}, Clock path disabled		**-1**	0	**+1**	µA
C_{IN}	Input Capacitance (Note 7)				7.5	**tbd**	pF
V_{BIAS}	DC Bias Voltage	AC Mode			0.9		V
R_{IN}	Input Resistance	AC Mode, Clock path enabled.			30	**tbd**	kΩ

Symbol	Parameter	Condition	Min (Note 6)	Typ (Note 5)	Max (Note 6)	Units
Clock Request Output (SCLK_REQ)						
tp_{LH}	Propagation Delay, Push-Pull and Open Source, (Note 7)	50% to 50%		21	**tbd**	ns
tp_{HL}	Propagation Delay, Push-Pull and Open Drain, (Note 7)	50% to 50%		15	**tbd**	ns
V_{OH}	SCLK_REQ Output Voltage High Level	SCLK_REQ = -500 µA, Push-Pull Output	**1.6V**			V
		SCLK_REQ = -500 µA, Open Source Output	**1.6V**			V
V_{OL}	SCLK_REQ Output Voltage Low Level	SCLK_REQ = 500 µA, Push-Pull Output			**0.2**	V
		SCLK_REQ = 500 µA, Open Drain Output			**0.2**	V
Clock Request Inputs (CLK_REQ1/2/3/4)						
t_{SET}	Setup Time from CLK_REQx to SCLK_IN, to enable CLKx (Note 7)		**tbd**			ns
V_{IH}	CLK_REQ1/2/3/4 Input Voltage High Level		**0.65 x V_{DD_IO}**			V
V_{IL}	CLK_REQ1/2/3/4 Input Voltage Low Level				**0.35 x V_{DD_IO}**	V
I_{IH}	CLK_REQ1/2/3/4 Input Current High Level	200 kΩ internal pull down resistor. CLK_REQ1/2/3/4 = 1.8V	**-1**	8.6	**10**	µA
		Without internal / external pull down resistor.CLK_REQ1/2/3/4 = 1.8V	**-1**	0	**1**	µA
I_{IL}	CLK_REQ1/2/3/4 Input Current Low Level	$V_{IL} = V_{SS}$	**-1**	0	**1**	µA
SCL and SDA Inputs, V_{ENABLE} = 1.8V (Note 10)						
V_{IH}	SCL and SDA Input Voltage High Level		**0.8 x V_{ENABLE}**			V
V_{IL}	SCL and SDA Input Voltage Low Level				**0.2 x V_{ENABLE}**	V
I_{IH}	SCL and SDA Input Current High Level	SCL/SDA = V_{ENABLE}		0	**1**	µA
I_{IL}	SCL and SDA Input Current Low Level	100 kΩ internal Pull-up resistor, SCL/SDA = V_{SS}	**-25**	-19		µA
V_{OL}	SDA Output Voltage Low Level	SDA = 3 mA			**0.2**	V
ENABLE Input						
V_{IH}	ENABLE Input Voltage High Level		**1.65**		**2**	V
V_{IL}	ENABLE Input Voltage Low Level				**0.5**	V
I_{IH}	ENABLE Input Current High Level	ENABLE = V_{OUT}			**1**	µA
I_{IL}	ENABLE Input Current Low Level	ENABLE = V_{SS}	**-1**			µA
LDO						
V_{OUT}	Output Voltage		**1.746**	1.8	**1.854**	V
I_{LOAD}	Load Current (Note 12)	V_{OUT} > 1.7V	0		10	mA
V_{DO}	Dropout Voltage (Note 14)	I_{OUT} = 10 mA		80		mV
I_{SC}	Short Circuit Current Limit			300		mA

Symbol	Parameter	Condition		Min (Note 6)	Typ (Note 5)	Max (Note 6)	Units
PSRR	Power Supply Rejection Ratio	V_{BAT} ripple = 200 mV_{PP}, I_{OUT} = 10 mA	f = 100 Hz		93		dB
			f = 217.5 Hz		90		
			f = 1 kHz		79		
			f = 10 kHz		62		
			f = 50 kHz		53		
			f = 100 kHz		50		
			f = 1 MHz		42		
			f = 3.25 MHz		35		
E_N	Output Noise Voltage	BW = 10Hz to 100 kHz, V_{IN} = 4.2V, C_{OUT} = 2.2 µF, All Outputs are Off			10		μV_{RMS}
T_{SHTDWN}	Thermal Shutdown (Note 7)	Temperature			160		°C
		Hysteresis			20		
ΔV_{OUT}	Line Transient (Note 7)	V_{IN} = ($V_{OUT\ (NOM)}$ + 1.0V) to ($V_{OUT\ (NOM)}$ + 1.6V) in 30 µs, I_{OUT} = 1 mA		**-1**			mV
		V_{IN} = ($V_{OUT\ (NOM)}$ + 1.6V) to ($V_{OUT\ (NOM)}$ + 1.0V) in 30 µs, I_{OUT} = 1 mA				**1**	
	Load Transient (Note 7)	I_{OUT} = 0 mA to 10 mA in 10 µs		**-70**			mV
		I_{OUT} = 10 mA to 0 mA in 10 µs				**30**	
	Overshoot on Startup (Note 7)					**100**	mV
R_{OUT}	DC Output Resistance				5		Ω
T_{ON}	Turn on Time (Note 7)	to 95% of $V_{OUT\ (NOM)}$			180	300	µs

Note 1: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is intended to be functional, but specific performance is not guaranteed. For guaranteed specifications and the test conditions, see the Electrical Characteristics Tables.

Note 2: Human body model, applicable std. MIL-STD-883, Method 3015.7. Machine model, applicable std. JESD22–A115–A (ESD MM std of JEDEC). Field-Induced Charge-Device Model, applicable std. JESD22–C101–C. (ESD FICDM std. of JEDEC)

Note 3: The maximum power dissipation is a function of $T_{J(MAX)}$, θ_{JA} and T_A. The maximum allowable power dissipation at any ambient temperature is $P_D = (T_{J(MAX)} - T_A)/\theta_{JA}$. All numbers apply for packages soldered directly onto a PC board.

Note 4: Electrical Table values apply only for factory testing conditions at the temperature indicated. Factory testing conditions result in very limited self-heating of the device such that $T_J = T_A$. No guarantee of parametric performance is indicated in the electrical tables under conditions of internal self-heating where $T_J > T_A$.

Note 5: Typical values represent the most likely parametric norm as determined at the time of characterization. Actual typical values may vary over time and will also depend on the application and configuration. The typical values are not tested and are not guaranteed on shipped production material.

Note 6: Limits are 100% production tested at 25°C. Limits over temperature range are guaranteed through correlations using statistical quality control (SQC) method.

Note 7: This parameter is guaranteed by design and/or characterization and is not tested in production.

Note 8: I_{DD} current depends on switching frequency and load.

Note 9: V_{DD_IO} is equal to V_{OUT} when the LDO is enabled and it is equal to V_{ENABLE} when it is disabled.

Note 10: I^2C interface uses IO cells guaranteed for 1.8V typical supply (1.6V Min - 2.0V Max).

Note 11: C_{BAT}, C_{OUT}: Low-ESR Surface-Mount Ceramic Capacitors (MLCCs) used in setting electrical characteristics.

Note 12: The device maintains stable, regulated output voltage without a load.

Note 13: Appropriate output load register must be set.

Note 14: Dropout voltage is the voltage difference between the input and the output at which the output voltage drops to 100 mV below its nominal value.

Timing Waveforms

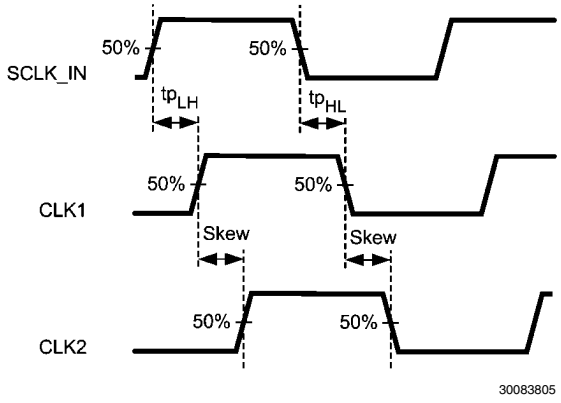


FIGURE 1. Clock Output Timing Waveforms

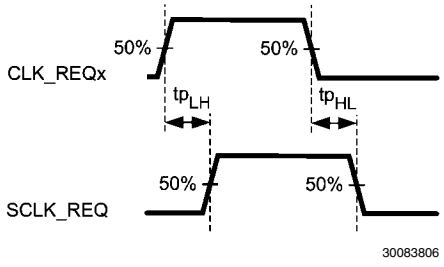


FIGURE 2. Clock Request Timing Waveforms

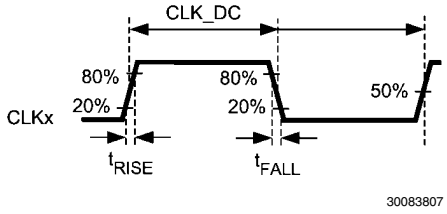


FIGURE 3. Rise / Fall Time and Duty Cycle Waveform for Clock Outputs

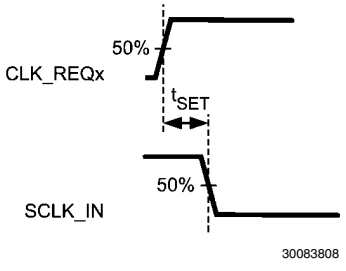
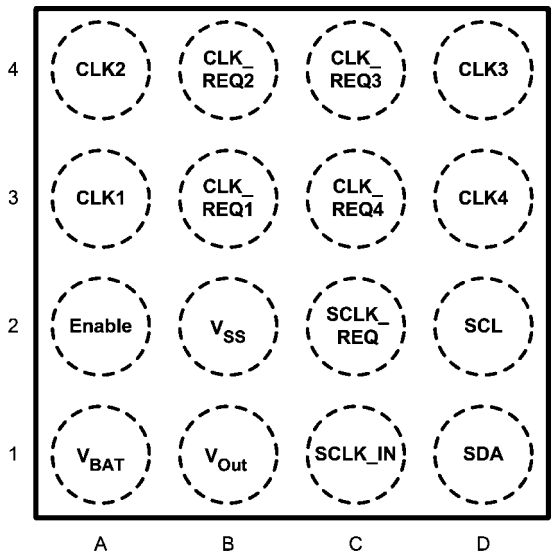


FIGURE 4. Setup Time from SCLK_IN to CLK_REQ

Connection Diagram

16-Bump micro SMD



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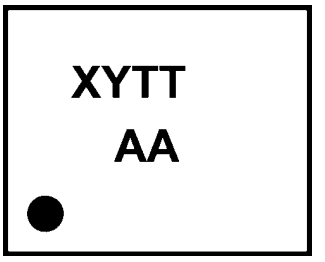
Top View

16–Bump micro SMD Marking



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Top View
XY = Date Code
TT = Die Tracebility
AA = LMH2190TM

Pin Descriptions

Pin	Pin Name	Port / Direction	Type	Description
C1	SCLK_IN	Host	I	Source Clock Input
C2	SCLK_REQ	Host	O	Source Clock Request
A3	CLK1	Peripheral	O	Clock Output 1
B3	CLK_REQ1	Peripheral	I	Clock Request Input 1
A4	CLK2	Peripheral	O	Clock Output 2
B4	CLK_REQ2	Peripheral	I	Clock Request Input 2
D4	CLK3	Peripheral	O	Clock Output 3
C4	CLK_REQ3	Peripheral	I	Clock Request Input 3
D3	CLK4	Peripheral	O	Clock Output 4
C3	CLK_REQ4	Peripheral	I	Clock Request Input 4
A2	Enable	Host	I	Enable Device, Active High
D2	SCL	Host	I	I²C Clock Input, 100 kΩ Pull-up to ENABLE
D1	SDA	Host / Bidirectional	I/O	I²C Data I/O, 100 kΩ Pull-up to ENBALE
A1	V_{BAT}	Battery / Input	Power	Power Supply
B1	V_{OUT}	LDO / Output	Power	Power Supply to Clock Source and Clock Outputs
B2	V_{SS}	Ground	Ground	Ground Pin

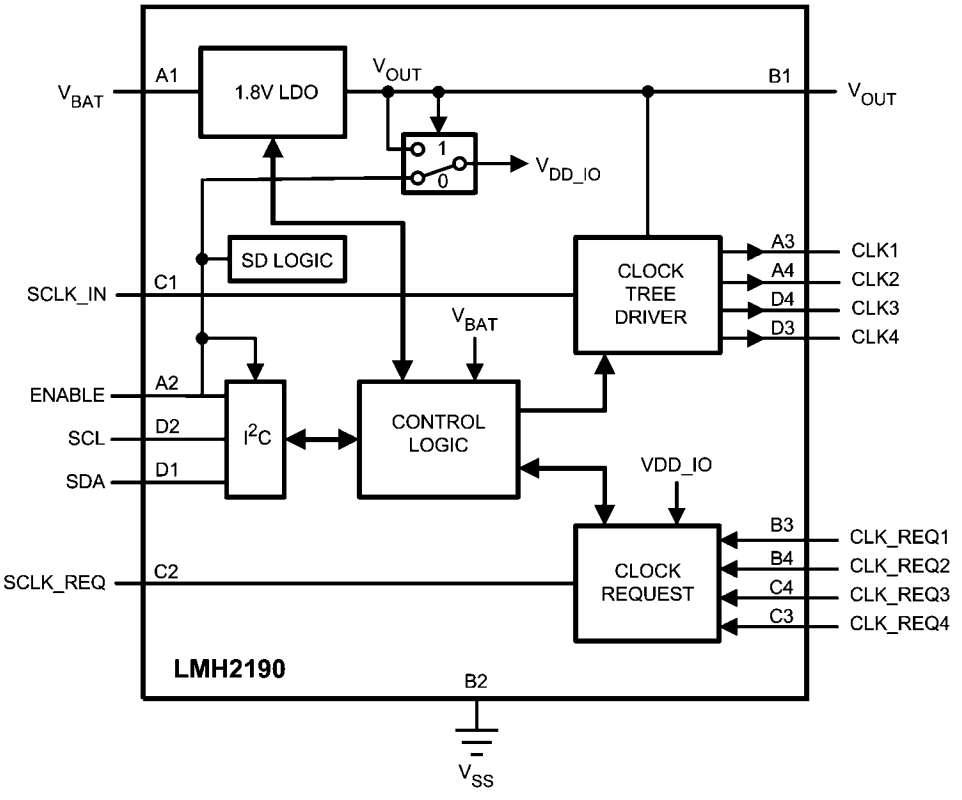
I = Input, O = Output, I/O = Input / Output

Ordering Information

Package	Part Number	I²C Address	Package Marking	Transport Media	NSC Drawing
16-Bump Thin microSMD	LMH2190TM-38	38	AA	250 Units Tape and Reel	TMD16AAA
	LMH2190TMX-38			3000 Units Tape and Reel	

Note: For other I²C addresses please contact your local sales office.

Block Diagram

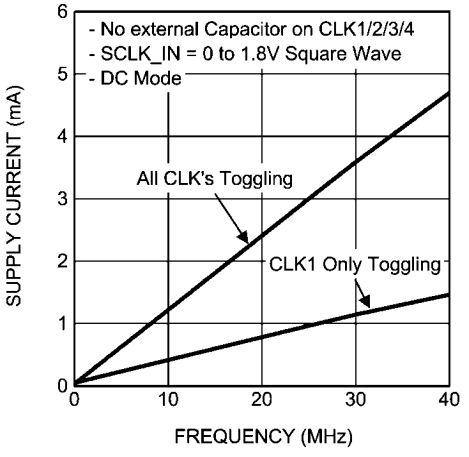


LMH2190

Typical Performance Characteristics

Unless otherwise specified, T_A = 25°C, V_{BAT} = 3.5V, f_{SCLK_IN} = 26 MHz, C_{OUT} = 2.2 µF, V_{DD_IO} = 1.8V (See *Block Diagram*, Registers are in default configuration.

Supply Current vs. Input Clock Frequency



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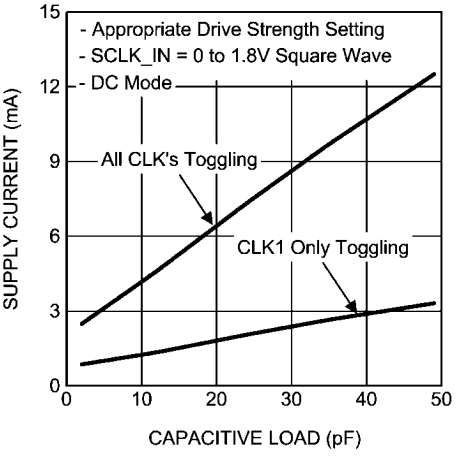
Supply Current vs. Capacitive Load



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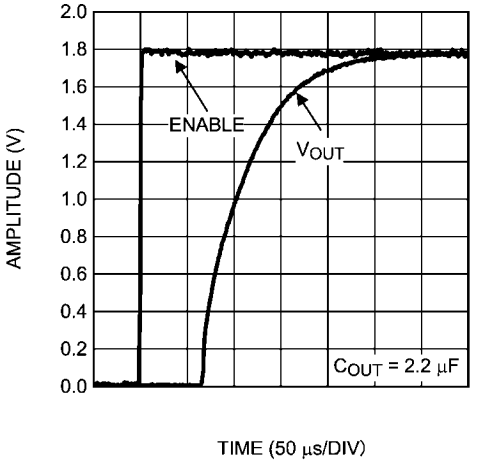
LDO Output Voltage vs. Time



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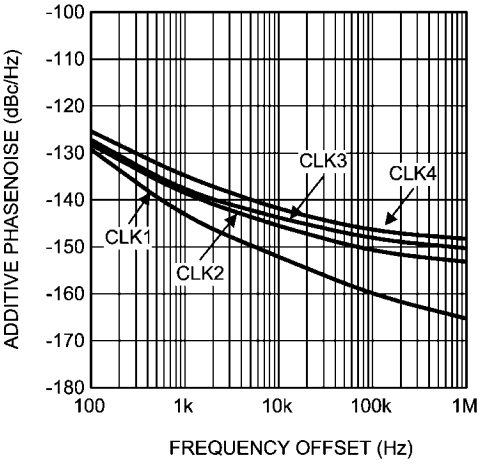
Additive Phase Noise vs. Frequency Offset



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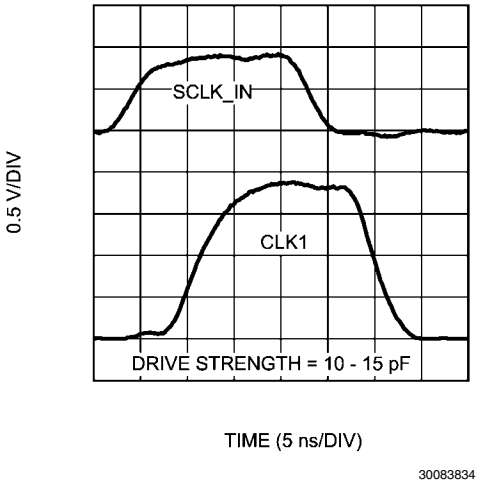
CLK1 Response, C_L = 10 pF



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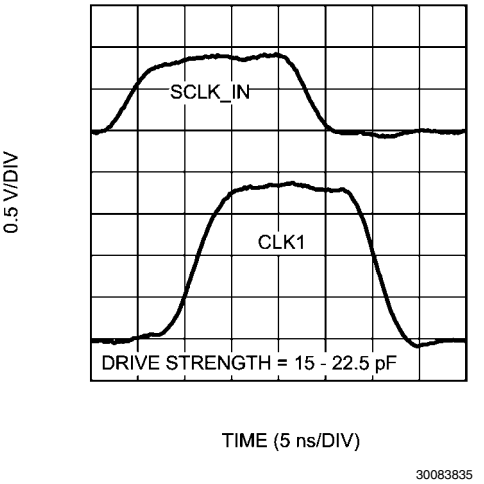
CLK1 Response, C_L = 22pF



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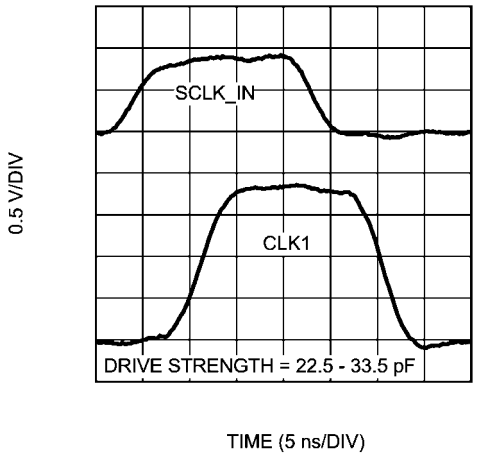
CLK1 Response, C_L = 33 pF



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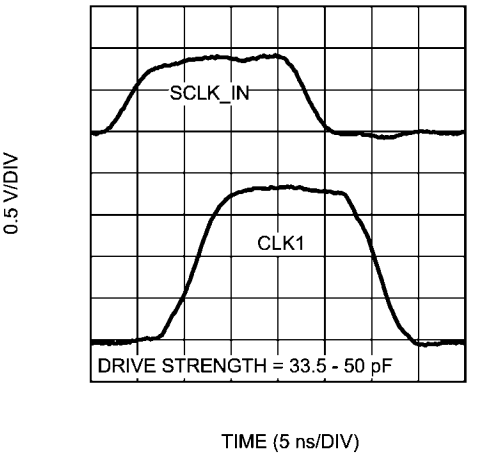
CLK1 Response, C_L = 50 pF



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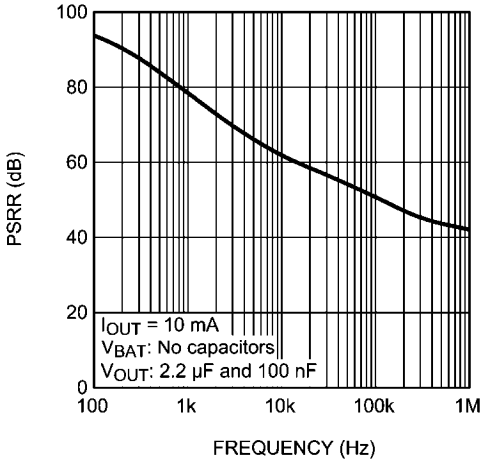
Power Supply Rejection Ratio vs. Frequency



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Application Information

The LMH2190 is a complete 26 MHz clocking conditioner and clock tree driver. The LMH2190 is used to supply a common clock to a number of mobile phone peripherals such as Bluetooth, Wireless LAN, and/or Digital Video Broadcast-H (DVB-H). The high isolation between the clock outputs achieves that the peripherals don't disrupt each other. It's excellent phase noise characteristics ensures that the clock quality doesn't get degraded. A typical LMH2190 setup is depicted in *Figure 5*.

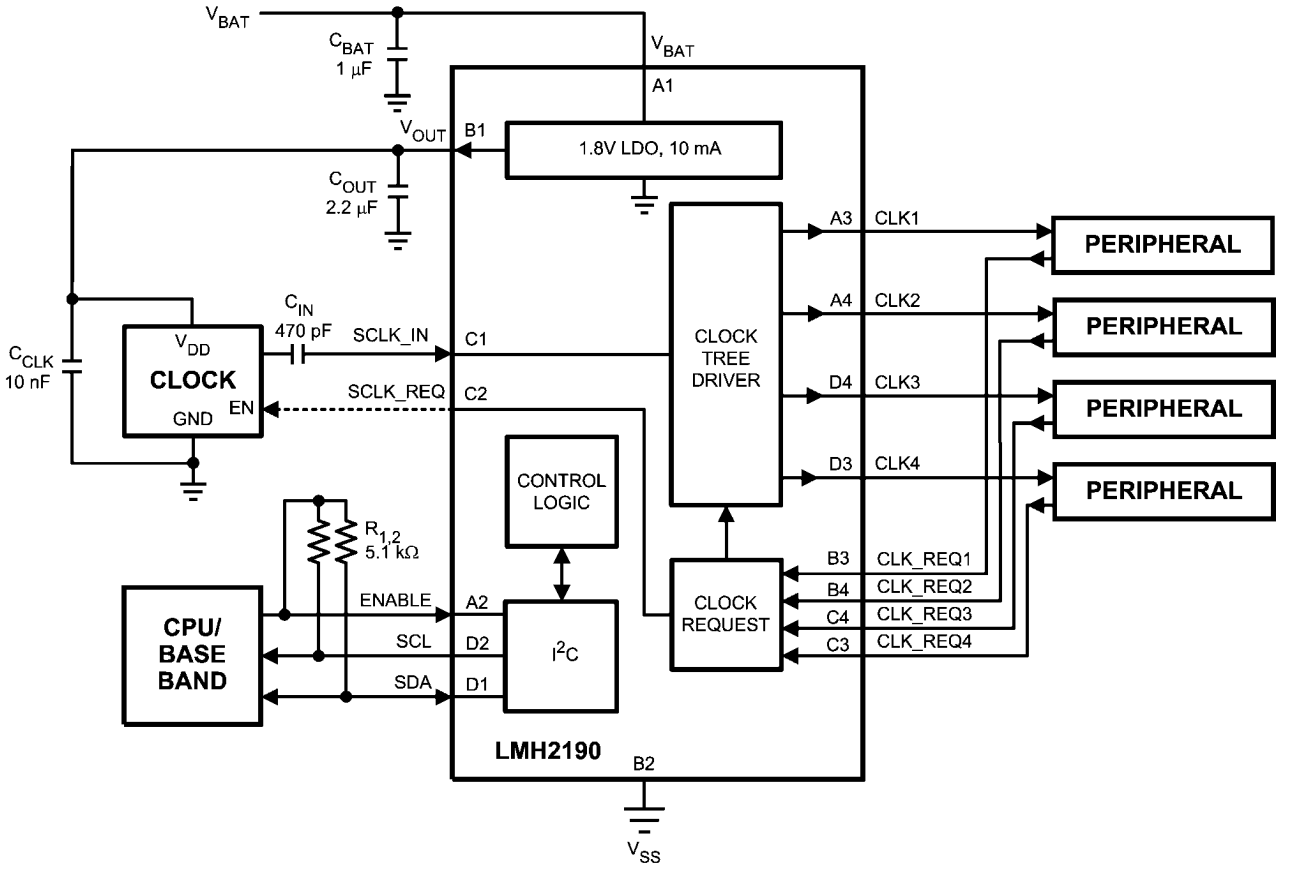


FIGURE 5. Typical LMH2190 Setup

The LMH2190 clock conditioner and clock tree driver can be described into 4 blocks:

- Clock tree driver
- Clock request logic
- Low Dropout (LDO) regulator
- I²C Control logic

The clock tree driver provides a clean clock to a maximum of 4 separately connected peripheral devices. Independent clock request inputs allows the peripheral to control when the particular clock should be enabled. Furthermore the clock request inputs together control the source clock request (SCLK_REQ). The LDO provides a low noise, high PSRR supply voltage that enables low phase noise on the clock outputs, and low quiescent current for portable applications. It can also be used to supply the TCXO. An I²C control port enables re-configuration of settings of many features of the device in order to optimize the device performance based on the application. All the blocks can be place into a low power consumptions mode to save energy. This functionality is controlled by the ENABLE pin. The following sections provide a detail description of each block.

CLOCK TREE DRIVER

The clock tree driver consists of one input that drives 4 outputs. It is supplied by the highly accurate 1.8V LDO. In default configuration the outputs are switched on when the clock request inputs are high. The input as well as the output can be configured in several ways though I²C programming.

Clock Tree Driver Input

The source clock input (SCLK_IN) is the input for the clock tree driver. It can be configured to DC or AC coupled mode. In shutdown mode, the input stage is completely switched off to prevent unnecessary power consumption when the source clock is still present.

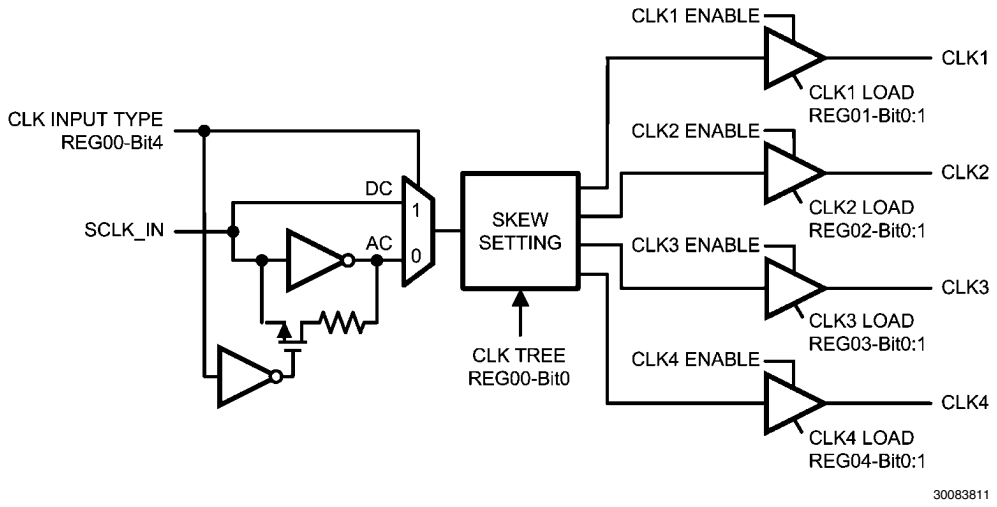


FIGURE 6. Clock Tree Driver

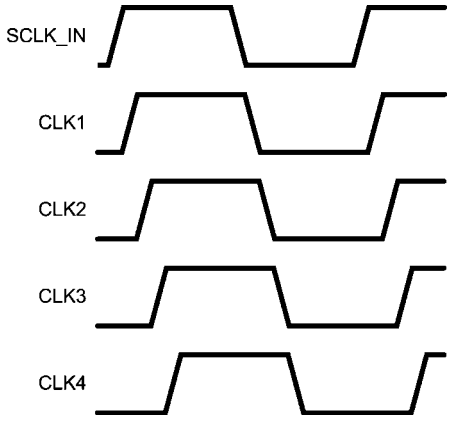
In the DC coupled mode, the clock input may range from 32 kHz to 26 MHz. DC coupling mode requires that the input is a square wave.

In AC mode an external capacitor needs to be connected in series with the clock source and the SCLK_IN pin to block external DC. Internally, an DC bias network centered at about $V_{OUT}/2$ is provided for a sine wave clock source (0.8 V_{PP} to 1.8 V_{PP}). The bias voltage is enabled only when the clock request output is asserted in order to eliminate the DC power. In the AC coupled mode, the clock input may range from 13 MHz up to 26 MHz. It is assumed to be a sine wave. Signals with sharp edges, such as square wave signals, should be prevented as the DC control loop can't maintain its internal DC level then.

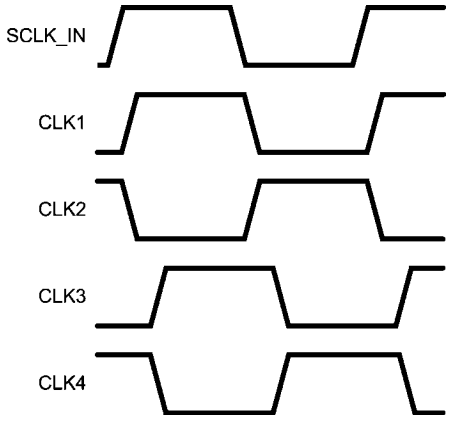
Clock Tree Driver Outputs

The LMH2190's clock tree driver outputs have many modes of operation to reduce power consumption and minimize EMI. The output drive strength of the LMH2190 can be selected in 4 steps based on the load capacitance it needs to drive. The configuration can be done by means of I²C.

There are two dedicated methods for reducing EMI that can be selected through the I²C interface. As shown in *Figure 7* the first method skews all of the clock edges individually, so that the EMI generated by the switching is spread out over time. The second method inverts two of the outputs and also skews one pair from the other.



(a) Outputs with Skew only



(b) Outputs with Skew and Inversion

FIGURE 7. Clock Outputs Timing

CLOCK REQUEST LOGIC

The clock request logic enables an independent control of the clock tree driver outputs (CLK1 to CLK4) as well as an overall source clock request (SCLK_REQ). Since the clock request logic always needs to be active, it is supplied by either the output of the LDO (V_{OUT}) or by the external ENABLE. Further details about the selection between V_{OUT} and ENABLE can be found in the LDO section.

Clock Request Inputs

A clock request input is provided for each clock output. This allows the peripheral device to control when it wants to receive a clock. In case the peripheral device does not have clock request functionality, the CLKx_REQ can be wired to a logic high level to enable the clock output (default register setting). Alternatively, it can be controlled through ²C. The input can also be configured to be active high or low. When the LDO is off, they still need to be able to function such that they can turn on the LDO. This is why the ENABLE input is used to supply the Clock Request Logic in case the LDO is off.

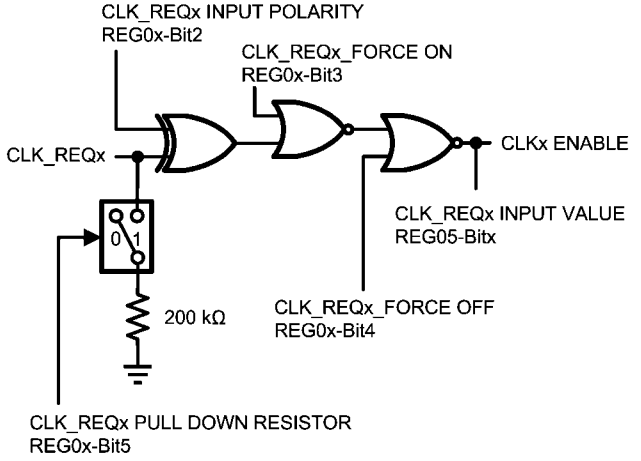


FIGURE 8. Clock Request Input

To prevent glitches on CLK outputs, enabling of the outputs is done synchronously. A latch, is used to ensure that the CLK outputs will be enabled on the falling edge of the source clock input (SCLK_IN).

System Clock Request Output

In the typical mode of operation, the clock request output will be asserted if one of the 4 CLK_REQ inputs is asserted. However, this can be overridden by the I²C interface which has a register bit that forces the output to be asserted. The polarity of the output is controlled by the I²C (CLK_REQ Output Polarity) along with whether the output is configured as push/pull, open drain or open source.

For the open drain case, there needs to be an external resistor that pulls the SCLK_REQ to a high level. This high level may be greater than the LDO voltage of 1.8V, but not more than the supply voltage (V_{BAT}) of the LMH2190.

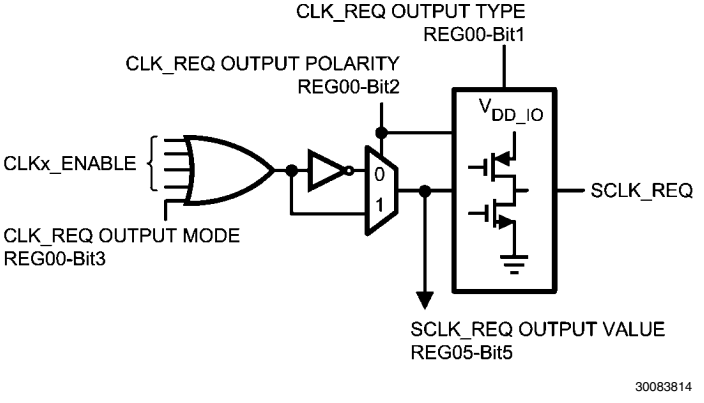


FIGURE 9. System Clock Request Output

The System Clock Request Output pin can be used to enable or disable an external TCXO to save power consumption. A typical application diagram is shown in *Figure 10*. The LDO powers the TCXO, while the SCLK_REQ enables or disables the TCXO. If the TXCO doesn't have an enable pin, power

savings can be realized by switching off the LMH2190's LDO and therewith the TCXO.

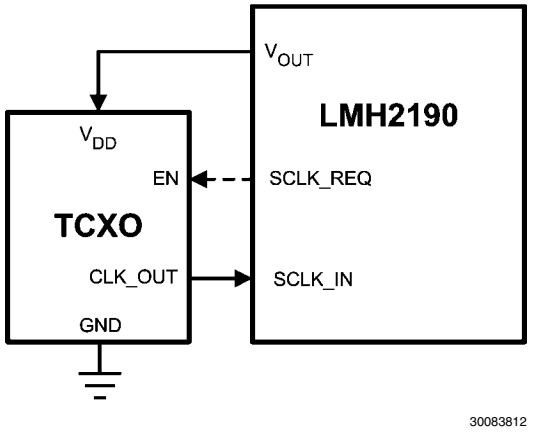


FIGURE 10. TCXO Powered from LMH2190's LDO

Please note that the LMH2190 initializes to its default settings when V_{BAT} is powered-up. It should be realized that the LMH2190 is in it's default state until it is configured through I²C. Because of this configuration the CLK1/2/3/4 outputs may transmit the clock to a peripheral when it is not requested upon startup and before the device is initialized through the I²C port. This may happen for instance when the default settings of the device for SCLK_REQ and CLK_REQ1/2/3/4 polarities do not correspond to what is expected by the TCXO and the peripheral. Care must be taken to prevent any unwanted behavior in the peripheral device until the I²C port correctly configures the device. The setting of the registers is maintained as long as the V_{BAT} voltage is present.

LOW DROPOUT REGULATOR

The linear and Low Dropout regulator (LDO) is used to regulate the input voltage, V_{BAT}, to generate a well defined 1.8V supply voltage. This allows the LMH2190 to suppress V_{BAT} voltage ripple. A voltage ripple would distort clock edges causing phase noise on the distributed clock signal.

In default mode the LDO is powered-up whenever a Clock Request is active. Therefore the Clock Request Logic needs to be powered continuously such that it can wake-up the LMH2190. The V_{DD_IO} that takes care of supplying the Clock Request Logic can therefore be drive by either the LDO output voltage or the ENABLE signal. Normally the V_{DD_IO} signal comes from the LDO output, unless the LDO is in a low power shutdown mode. In this case the ENABLE signal will drive the V_{DD_IO} (*Figure 11*). As soon as there is a clock request, the built in LDO will power up and takes over the sourcing of V_{DD_IO} from the ENABLE signal.

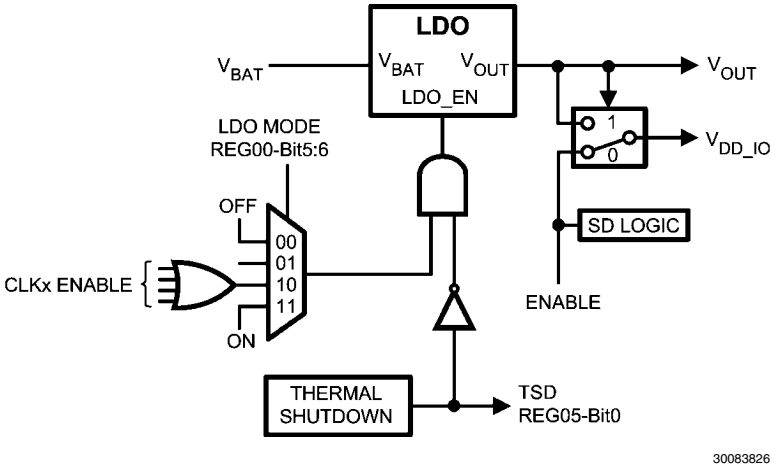


FIGURE 11. Linear Regulator Block Diagram

The LDO contains thermal overheating detection. If it does overheat, the LMH2190 will shutdown and set a status bit in the I²C status register.

The LDO can be configured to be always On for the case when it needs to supply power to the TCXO even when the LMH2190 is not requesting any clocks to be distributed.

It is possible to use an external 1.8V supply connected to V_{OUT} and shut off the internal LDO, although it is highly recommended to use the internally generated 1.8V. If an external supply is used, care should be taken during startup as the default configuration is for the internal LDO to be enabled. In this case, there could be contention between the two supplies which could cause excessive current to be consumed between them.

I²C CONTROL LOGIC

The LMH2190 operation is controlled from a host device by a register set, accessed via the I²C interface. The I²C communication is based on a READ/WRITE structure, following the I²C transmission protocol. According to the I²C specification one set of pull-up resistors need to be present on the I²C bus.

Some of the features are for instance the polarity of the clock request inputs and output and the drive strength of the clock outputs. It also allows direct control of the clock request signals and the LDO via the I²C. The I²C interface is supplied by the ENABLE, while the control logic and registers are supplied by the V_{BAT}.

I²C Data Validity

The data on SDA line must be stable during the HIGH period of the clock signal (SCL). In other words, state of the data line can only be changed when SCL is LOW (*Figure 12*).

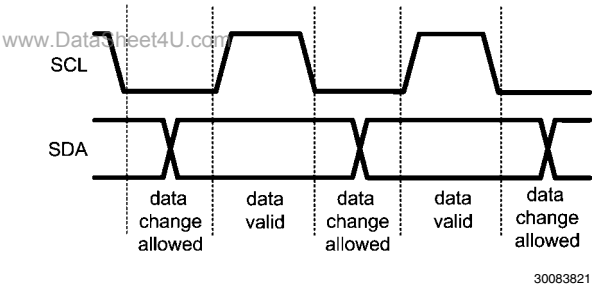


FIGURE 12. I²C Signals: Data Validity

I²C Start and Stop Condition

START and STOP bits classify the beginning and the end of the I²C session. START condition is defined as SDA signal transitioning from HIGH to LOW while SCL line is HIGH (*Figure 13*). STOP condition is defined as the SDA transitioning from LOW to HIGH while SCL is HIGH. The I²C master always generates START and STOP bits. The I²C bus is considered to be busy after START condition and free after STOP condition. During data transmission, I²C master can generate repeated START conditions. First START and repeated START conditions are equivalent, function-wise.

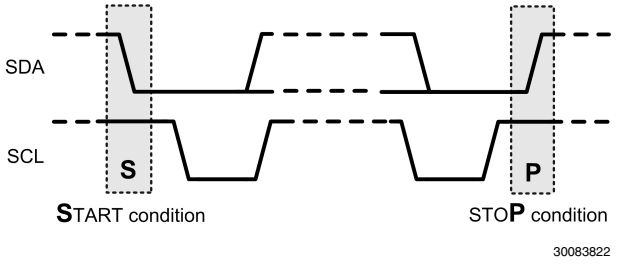


FIGURE 13. I²C Start and Stop Conditions

Transferring Data

Every byte put on the SDA line must be eight bits long, with the most significant bit (MSB) being transferred first. Each byte of data has to be followed by an acknowledge bit. The acknowledge related clock pulse is generated by the master. The transmitter releases the SDA line (HIGH) during the acknowledge clock pulse. The receiver must pull down the SDA line during the 9th clock pulse, signifying an acknowledge. A receiver which has been addressed must generate an acknowledge after each byte has been received.

After the START condition, the I²C master sends a chip address. This address is seven bits long followed by an eight bit which is a data direction bit (R/W). For the eighth bit, a "0" indicates a WRITE and a "1" indicates a READ. The second byte selects the register to which the data will be written. The third byte contains data to write to the selected register.

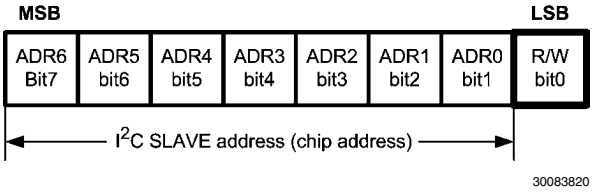


FIGURE 14. I²C Chip Address

Register changes take effect at the SCL rising edge during the last ACK from slave. An example of a WRITE cycle is given in *Figure 15*. When a READ function is to be accomplished, a WRITE function must precede the READ function, as shown in the Read Cycle waveform (*Figure 16*).

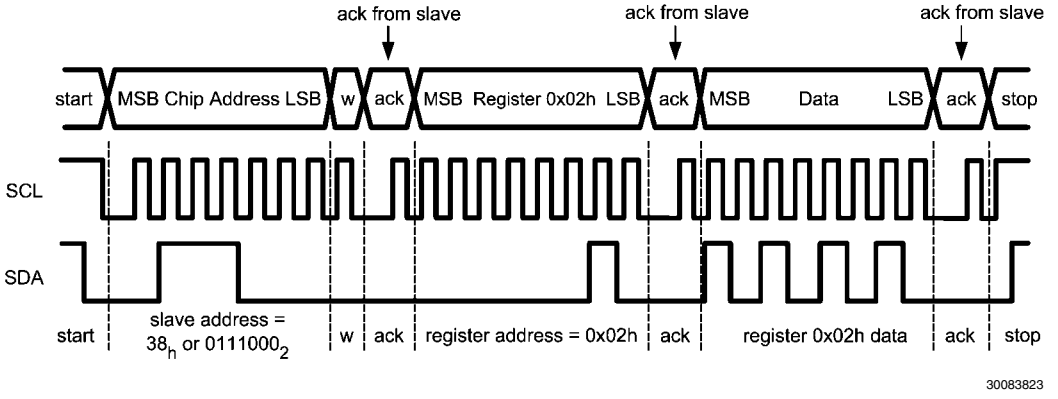


FIGURE 15. Example I²C Write Cycle

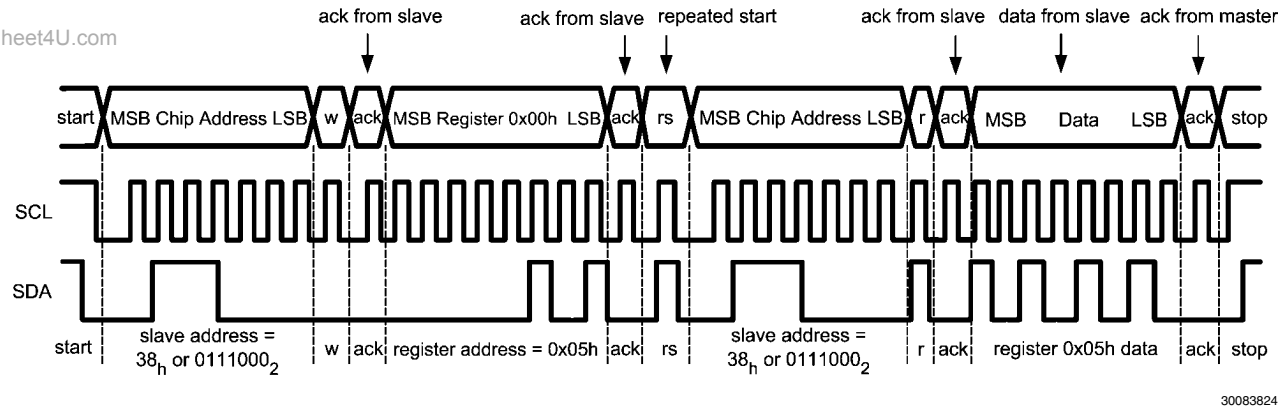


FIGURE 16. Example I²C Read Cycle

I²C Timing

The timing of the SDA and SCL signals is depicted in *Figure 17* and the parameters are given in table below.

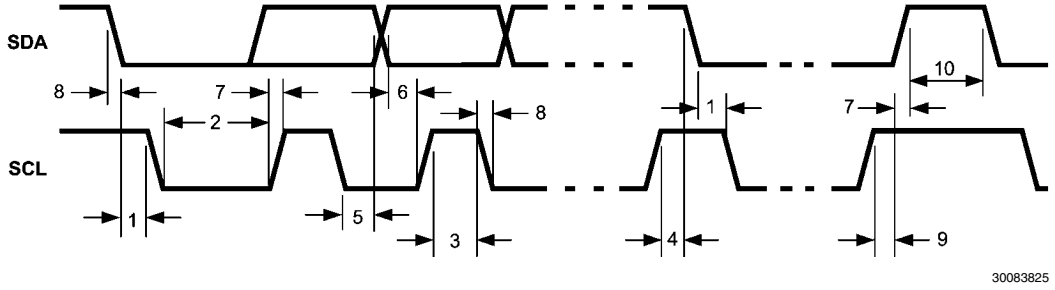


FIGURE 17. I²C Timing Diagram

TABLE 1. I²C Timing

Symbol	Parameter	Limit		Units
		Min	Max	
f_{SCL}	Clock Frequency		400	kHz
1	Hold Time (repeated) START Condition	0.6		µs
2	Clock Low Time	1.3		ns
3	Clock High Time	600		ns
4	Setup Time for a Repeated START Condition	600		ns
5	Data Hold Time (Output direction, delay generated by LMH2190)	300	900	µs
5	Data Hold Time (Input direction, delay generated by the Master)	0	900	ns
6	Data Setup Time	100		ns
7	Rise Time of SDA and SCL	20+0.1 C_b	300	ns
8	Fall Time of SDA and SCL	10+0.1 C_b	300	ns
9	Set-up Time for STOP condition	600		ns
10	Bus Free Time between a STOP and a START Condition	1.3		µs
C_b	Capacitive Load for Each Bus Line	10	200	pF

I²C Registers

TABLE 2. Configuration Register

Address = 00H, type = R/W, reset value = 44H, 0100_0100, **Bold** face settings are the default configuration.

Field	Bits	Description
Output Mode	[0]	Sets the timing relationship of the clock outputs (*Figure 7*). **0** - All 4 outputs are skewed from each other 1 - Two pair of outputs where one output of the pair is the inversion of the other and the second pair is skewed from the first pair.
Clock Request Output Type	[1]	Sets whether the output is push-pull or open drain. **0** - Push-Pull Output 1 - Open Drain/Source Output (Open drain with Active low output, Open source with Active high output).
Clock Request Output Polarity	[2]	Sets whether the clock Request output is active low or active high. 0 - Active low output **1** - Active high output
Clock Request Output Mode	[3]	Sets how the clock request output operates. **0** - Use clock request inputs 1 - Force the clock request output to be asserted.
Clock Input Type	[4]	Sets whether the input is AC or DC coupled. **0** - AC coupled 1 - DC coupled
LDO Mode	[6-5]	Sets the regulator mode of operation. 00 - OFF 01 - Reserved **10** - Track Clock Requests 11 - Force ON
Reserved	[7]	

TABLE 3. CLK1 Output Register

Address = 01H, type = R/W, reset value = 06H, 0000_0110, **Bold** face settings are the default configuration.

Field	Bits	Description
CLK1 Load	[1-0]	Sets the drive strength of the clock outputs based on the capacitive load. 00 - 10pF to 15pF 01 - 15pF to 22.5pF **10** - 22.5pF to 33.5pF 11 - 33.5pF to 50pF
CLK_REQ1 Input Polarity	[2]	Sets whether a logic low or high enables the clock output. 0 - Logic low enables the clock output. **1** - Logic high enables the clock output.
CLK_REQ1 Force ON Control	[3]	Selects whether to use a clock request or I²C logic to enable the output. **0** - Use the clock request pin to control the output. 1 - Force the clock output to be enabled (Force ON).
CLK_REQ1 Force OFF Control	[4]	Selects whether to use a clock request or I²C logic to disable the output. **0** - Use the clock request pin to control the output. 1 - Force the clock output to be enabled (Force OFF). ”Force OFF" overrides ”Force ON".
CLK_REQ1 Pull down Resistor	[5]	Selects whether an internal 200 kΩ pull down resistor on the clock request input to GND is present. **0** - No internal pull down resistor is present. 1 - Internal 200 kΩ pull-down resistor is present.
Reserved	[6]	
Reserved	[7]	

TABLE 4. CLK2 Output Register

Address = 02H, type = R/W, reset value = 06H, 0000_0110, **Bold** face settings are the default configuration.

Field	Bits	Description
CLK2 Load	[1-0]	Sets the drive strength of the clock outputs based on the capacitive load. 00 - 10pF to 15pF 01 - 15pF to 22.5pF **10** - 22.5pF to 33.5pF 11 - 33.5pF to 50pF
CLK_REQ2 Input Polarity	[2]	Sets whether a logic low or high enables the clock output. 0 - Logic low enables the clock output. **1** - Logic high enables the clock output.
CLK_REQ2 Force ON Control	[3]	Selects whether to use a clock request or I²C logic to enable the output. **0** - Use the clock request pin to control the output. 1 - Force the clock output to be enabled (Force ON).
CLK_REQ2 Force OFF Control	[4]	Selects whether to use a clock request or I²C logic to disable the output. **0** - Use the clock request pin to control the output. 1 - Force the clock output to be enabled (Force OFF). ”Force OFF" overrides ”Force ON".
CLK_REQ2 Pull down Resistor	[5]	Selects whether an internal 200 kΩ pull down resistor on the clock request input to GND is present. **0** - No internal pull down resistor is present. 1 - Internal 200 kΩ pull-down resistor is present.
Reserved	[6]	
Reserved	[7]	

TABLE 5. CLK3 Output Register

Address = 03H, type = R/W, reset value = 06H, 0000_0110, **Bold** face settings are the default configuration.

Field	Bits	Description
CLK3 Load	[1-0]	Sets the drive strength of the clock outputs based on the capacitive load. 00 - 10pF to 15pF 01 - 15pF to 22.5pF **10** - 22.5pF to 33.5pF 11 - 33.5pF to 50pF
CLK_REQ3 Input Polarity	[2]	Sets whether a logic low or high enables the clock output. 0 - Logic low enables the clock output. **1** - Logic high enables the clock output.
CLK_REQ3 Force ON Control	[3]	Selects whether to use a clock request or I²C logic to enable the output. **0** - Use the clock request pin to control the output. 1 - Force the clock output to be enabled (Force ON).
CLK_REQ3 Force OFF Control	[4]	Selects whether to use a clock request or I²C logic to disable the output. **0** - Use the clock request pin to control the output. 1 - Force the clock output to be enabled (Force OFF). ”Force OFF" overrides ”Force ON".
CLK_REQ3 Pull down Resistor	[5]	Selects whether an internal 200 kΩ pull down resistor on the clock request input to GND is present. **0** - No internal pull down resistor is present. 1 - Internal 200 kΩ pull-down resistor is present.
Reserved	[6]	
Reserved	[7]	

TABLE 6. CLK4 Output Register

Address = 04H, type = R/W, reset value = 06H, 0000_0110, **Bold** face settings are the default configuration.

Field	Bits	Description
CLK4 Load	[1-0]	Sets the drive strength of the clock outputs based on the capacitive load. 00 - 10pF to 15pF 01 - 15pF to 22.5pF **10** - 22.5pF to 33.5pF 11 - 33.5pF to 50pF
CLK_REQ4 Input Polarity	[2]	Sets whether a logic low or high enables the clock output. 0 - Logic low enables the clock output. **1** - Logic high enables the clock output.
CLK_REQ4 Force ON Control	[3]	Selects whether to use a clock request or I²C logic to enable the output. **0** - Use the clock request pin to control the output. 1 - Force the clock output to be enabled (Force ON).
CLK_REQ4 Force OFF Control	[4]	Selects whether to use a clock request or I²C logic to disable the output. **0** - Use the clock request pin to control the output. 1 - Force the clock output to be enabled (Force OFF). ”Force OFF" overrides ”Force ON".
CLK_REQ4 Pull down Resistor	[5]	Selects whether an internal 200 kΩ pull down resistor on the clock request input to GND is present. **0** - No internal pull down resistor is present. 1 - Internal 200 kΩ pull-down resistor is present.
Reserved	[6]	
Reserved	[7]	

TABLE 7. Status Register

Address = 05H, type = R

Field	Bits	Description
Thermal Shutdown (TSD)	[0]	Indicates if a thermal shutdown event has occurred. 0 - Thermal shutdown has not occurred. 1 - Thermal shutdown has occurred
CLK_REQ1 Input Value	[1]	Captures the state of the clock request input value. 0 - Clock request is low. 1 - Clock request is high.
CLK_REQ2 Input Value	[2]	Captures the state of the clock request input value. 0 - Clock request is low. 1 - Clock request is high.
CLK_REQ3 Input Value	[3]	Captures the state of the clock request input value. 0 - Clock request is low. 1 - Clock request is high.
CLK_REQ4 Input Value	[4]	Captures the state of the clock request input value. 0 - Clock request is low. 1 - Clock request is high.
SCLK_REQ Output Value	[5]	Captures the state of the system clock request output value. 0 - System clock request is low. 1 - System clock request is high.
Reserved	[6]	
Reserved	[7]	

LAYOUT RECOMMENDATIONS

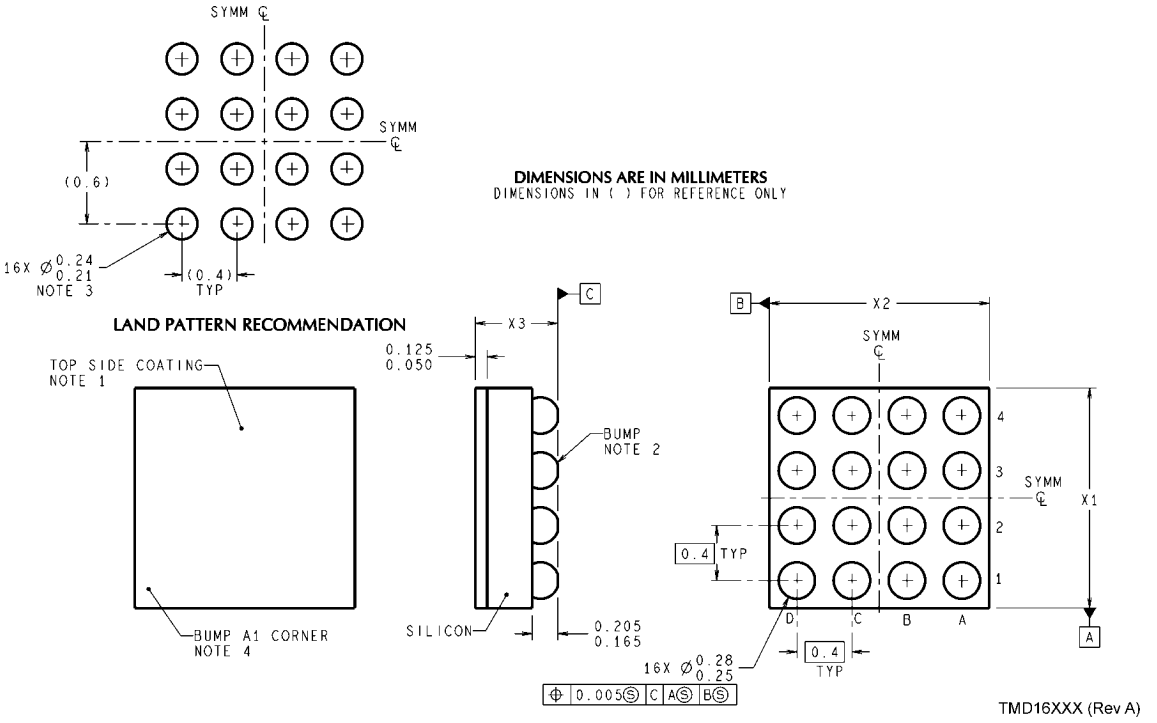
As with any other device, careful attention must be paid to the board layout. If the board isn't properly designed, the performance of the device can be less than may be expected. Especially the input clock trace (SCLK_IN) and output traces (CLK1/2/3/4) should be as short as possible to reduce the capacitive load observed by the clock outputs. Also proper decoupling close to the device is necessary. *Table 8* depicts the advised component values.

TABLE 8. Recommended Component Values

Symbol	Parameter	Min	Typ	Max	Units
C_{BAT}	Capacitor on V_{BAT}	0.47	1		µF
C_{OUT}	Capacitor on V_{OUT}	1	2.2		
ESR	Equivalent Series Resistance	5		500	mΩ
C_{SCLK_IN}	Input AC Coupling Capacitor	330	470	10000	pF

C_{BAT}, C_{OUT}: Low-ESR Surface-Mount Ceramic Capacitors (MLCC's) used in setting electrical characteristics.

Physical Dimensions inches (millimeters) unless otherwise noted



6-Bump micro SMD
NS Package Number TMD16AAA
X1 = 1.615 ± 0.030 mm, X2 = 1.615 ± 0.030 mm, X3 = 0.600 ± 0.075 mm

Notes

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Interface	www.national.com/interface	Eval Boards	www.national.com/evalboards
LVDS	www.national.com/lvds	Packaging	www.national.com/packaging
Power Management	www.national.com/power	Green Compliance	www.national.com/quality/green
Switching Regulators	www.national.com/switchers	Distributors	www.national.com/contacts
LDOs	www.national.com/ldo	Quality and Reliability	www.national.com/quality
LED Lighting	www.national.com/led	Feedback/Support	www.national.com/feedback
Voltage Reference	www.national.com/vref	Design Made Easy	www.national.com/easy
PowerWise® Solutions	www.national.com/powerwise	Solutions	www.national.com/solutions
Serial Digital Interface (SDI)	www.national.com/sdi	Mil/Aero	www.national.com/milaero
Temperature Sensors	www.national.com/tempsensors	SolarMagic™	www.national.com/solarmagic
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