LME49610 High Performance, High Fidelity, High Current Audio Buffer

Check for Samples: LME49610

FEATURES

- **Pin-Selectable Bandwidth and Quiescent Current**
- **Pure Fidelity. Pure Performance**
- **Short Circuit Protection**
- **Thermal Shutdown**
- **TO–263 Surface-Mount Package**

APPLICATIONS

- **Headphone Amplifier Output Drive Stage**
- **Line Drivers**
- **Low Power Audio Amplifiers**
- **High-Current Operational Amplifier Output Stage**
- **ATE Pin Driver Buffer**
- **Power Supply Regulator**

DESCRIPTION

The LME49610 is a high performance, low distortion high fidelity 250mA audio buffer. The LME49610 is designed for a wide range of applications. When used inside the feedback loop of an op amp, it increases output current, improves capacitive load drive, and eliminates thermal feedback.

The LME49610 offers a pin-selectable bandwidth: a low current, 120MHz bandwidth mode that consumes 13mA and a wide 200MHz bandwidth mode that consumes 19mA. In both modes the LME49610 has a nominal 2000V/µs slew rate. Bandwidth is easily adjusted by either leaving the BW pin unconnected, connecting it to the V_{EE} pin or connecting a resistor between the BW pin and the V_{EE} pin.

The LME49610 is fully protected through internal current limit and thermal shutdown.

Table 1. KEY SPECIFICATIONS

		VALUE	UNIT
Low THD+N	(V_{OUT} = 3V_{RMS}, f = 1kHz, Figure 27)	0.00003	% (typ)
Slew Rate		2000	V/µs (typ)
High Output Current		250	mA (typ)
Bandwidth	BW pin floating	120	MHz (typ)
	BW connected to V_{EE}	200	MHz (typ)
Supply Voltage Range		±2.25V ≤ V_{DD} ≤ ±22	V

FUNCTIONAL BLOCK DIAGRAM

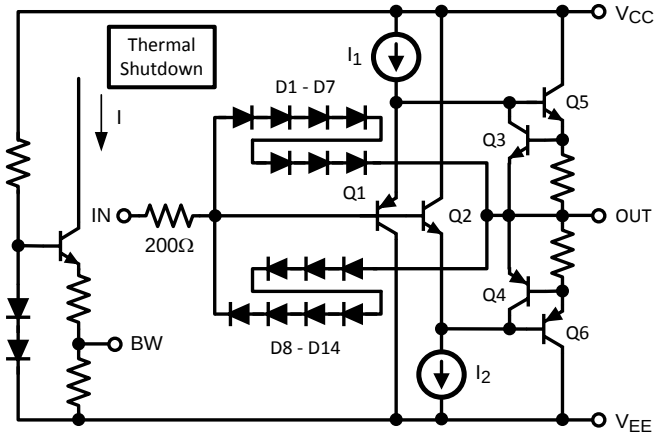

Figure 1. Functional Block Diagram

CONNECTION DIAGRAM

Top View

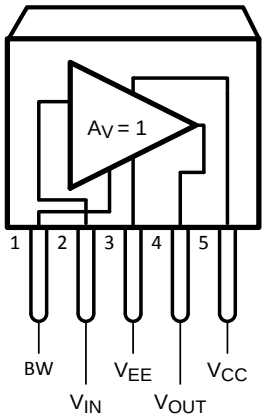

Figure 2. DDPAK/TO-263 Package
See Package Number KTT0005B(1)

(1) The KTT0005B package is a non-isolated package. The package's metal back and any heat sink to which it is mounted are connected to the same potential as the $-V_{EE}$ pin.

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

ABSOLUTE MAXIMUM RATINGS (1)(2)(3)

Supply Voltage		46V
ESD Rating (4)		2000V
ESD Rating (5)		200V
Storage Temperature		−40°C to +150°C
Junction Temperature		150°C
Thermal Resistance	θ_{JC}	4°C/W
	θ_{JA}	65°C/W
	θ_{JA} (6)	20°C/W
Soldering Information: DDPAK/TO–263 Package (10 seconds)		260°C

(1) "*Absolute Maximum Ratings*" indicate limits beyond which damage to the device may occur, including inoperability and degradation of device reliability and/or performance. Functional operation of the device and/or non-degradation at the Absolute Maximum Ratings or other conditions beyond those indicated in the *Recommended Operating Conditions* is not implied. The *Recommended Operating Conditions* indicate conditions at which the device is functional and the device should not be operated beyond such conditions. All voltages are measured with respect to the ground pin, unless otherwise specified

(2) The *Electrical Characteristics* tables list specifications under the listed *Recommended Operating Conditions* except as otherwise modified or specified by the *Electrical Characteristics Conditions* and/or Notes. Typical specifications are estimations only and are not ensured.

(3) If Military/Aerospace specified devices are required, please contact the Texas Instruments Sales Office/ Distributors for availability and specifications.

(4) Human body model, applicable std. JESD22-A114C.

(5) Machine model, applicable std. JESD22-A115-A.

(6) The maximum power dissipation must be derated at elevated temperatures and is dictated by T_{JMAX}, θ_{JA}, and the ambient temperature, T_A. The maximum allowable power dissipation is $P_{DMAX} = (T_{JMAX} - T_A) / \theta_{JA}$ or the number given in *Absolute Maximum Ratings*, whichever is lower. For the LME49610, typical application shown in Figure 27 with $|V_{EE}| = V_{CC} = 15V$, $R_L = 32\Omega$, the total power dissipation is 1.9W. $\theta_{JA} = 20°C/W$ for the DDPAK/TO-263 package mounted to 16in^2 (103.2 cm^2) 1oz. copper surface heat sink area.

OPERATING RATINGS (1)(2)

Temperature Range	$T_{MIN} \le T_A \le T_{MAX}$	$-40°C \le T_A \le 85°C$
Supply Voltage		±2.25V to ±22V

(1) "*Absolute Maximum Ratings*" indicate limits beyond which damage to the device may occur, including inoperability and degradation of device reliability and/or performance. Functional operation of the device and/or non-degradation at the Absolute Maximum Ratings or other conditions beyond those indicated in the *Recommended Operating Conditions* is not implied. The *Recommended Operating Conditions* indicate conditions at which the device is functional and the device should not be operated beyond such conditions. All voltages are measured with respect to the ground pin, unless otherwise specified

(2) The *Electrical Characteristics* tables list specifications under the listed *Recommended Operating Conditions* except as otherwise modified or specified by the *Electrical Characteristics Conditions* and/or Notes. Typical specifications are estimations only and are not ensured.

ELECTRICAL CHARACTERISTICS

The following specifications apply for V_S = ±22V, f_{IN} = 1kHz, R_L = 1kΩ, unless otherwise specified. Typicals and limits apply for T_A = 25°C.

Parameter		Test Conditions	LME49610		Units (Limits)
			Typ (1)	Limit (2)	
I_Q	Total Quiescent Current	I_{OUT} = 0 BW pin: No connect BW pin: Connected to V_{EE} pin	 13 19	 15 23	 mA (max) mA (max)
THD+N	Total Harmonic Distortion + Noise (3)	A_V = 1, V_{OUT} = 3V_{RMS}, R_L = 32Ω, BW = 80kHz, closed loop (see Figure 27.) f = 1kHz f = 20kHz	 0.000035 0.0005	 	 % %
SR	Slew Rate	30 ≤ BW ≤ 180MHz V_{OUT} = 20V_{P-P}, R_L = 100Ω	2000		V/µs
BW	Bandwidth	A_V = –3dB			
		BW pin: No Connect R_L = 100Ω R_L = 1kΩ	 110 120	 	 MHz MHz
		BW pin: Connected to V_{EE} pin R_L = 100Ω R_L = 1kΩ	 180 200	 	 MHz MHz
	Voltage Noise Density	f = 10kHz BW pin: No Connect	3.0	8.5	nV/√Hz (max)
		f = 10kHz BW pin: Connected to V_{EE} pin	2.7	6.5	nV/√Hz (max)
t_s	Settling Time	ΔV = 10V, R_L = 100Ω 1% Accuracy BW pin: No connect BW pin: Connected to V_{EE} pin	 200 60	 	 ns ns
A_V	Voltage Gain	V_{OUT} = ±10V R_L = 67Ω R_L = 100Ω R_L = 1kΩ	 0.93 0.95 0.99	 0.90 0.92 0.98	 V/V (min) V/V (min) V/V (min)
V_{OUT}	Voltage Output	Positive I_{OUT} = 10mA I_{OUT} = 100mA I_{OUT} = 150mA	 V_{CC} –1.2 V_{CC} –1.5 V_{CC} –1.7	 V_{CC} –1.4 V_{CC} –1.8 V_{CC} –2.1	 V (min) V (min) V (min)
		Negative I_{OUT} = –10mA I_{OUT} = –100mA I_{OUT} = –150mA	 V_{EE} +1.2 V_{EE} +1.6 V_{EE} +2.2	 V_{EE} +1.4 V_{EE} +1.9 V_{EE} +2.5	 V (min) V (min) V (min)
I_{OUT}	Output Current		±250		mA
I_{OUT-SC}	Short Circuit Output Current	BW pin: No Connect BW pin: Connected to V_{EE} pin	±750 ±750	 ±785	mA mA (max)
I_B	Input Bias Current	V_{IN} = 0V BW pin: No Connect BW pin: Connected to V_{EE} pin	 ±1.0 ±3.0	 ±2.5 ±5.0	 µA (max) µA (max)
Z_{IN}	Input Impedance	R_L = 100Ω BW pin: No Connect BW pin: Connected to V_{EE} pin	 7.5 5.5	 	 MΩ MΩ
V_{OS}	Offset Voltage		±17	±60	mV (max)
V_{OS}/°C	Offset Voltage vs Temperature	40°C ≤ T_A ≤ +125°C	±100		µV/°C
V_{SUPPLY}	Power Supply Voltage Operating Range		±2.25 ±22		V V

(1) Typical values represent most likely parametric norms at T_A = +25ºC, and at the Recommended Operation Conditions at the time of product characterization and are not ensured.
(2) Datasheet min/max specification limits are specified by test or statistical analysis.
(3) This is the distortion of the LME49610 operating in a closed loop configuration with an LME49710. When operating in an operational amplifier's feedback loop, the amplifier's open loop gain dominates, linearizing the system and determining the overall system distortion.

TYPICAL PERFORMANCE CHARACTERISTICS

Gain vs Frequency vs Quiescent Current V_S = ±22V

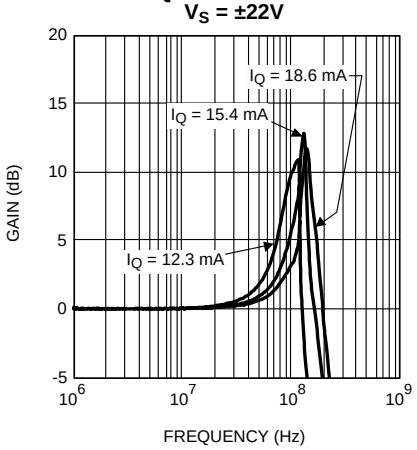

Figure 3.

Phase vs Frequency vs Quiescent Current V_S = ±22V

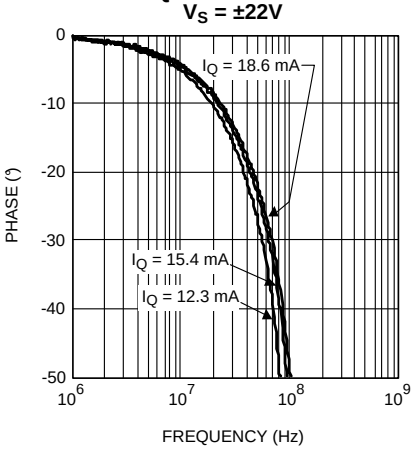

Figure 4.

Gain vs Frequency vs Power Supply Voltage Wide BW Mode (BW pin = V_{EE})

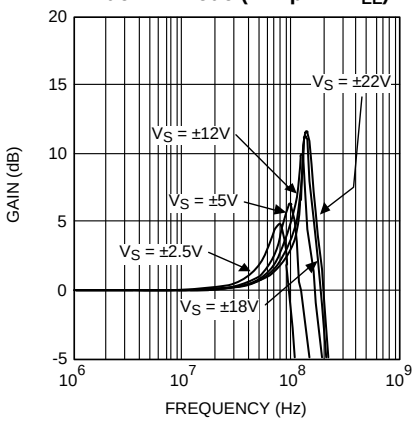

Figure 5.

Phase vs Frequency vs Supply Voltage Wide BW Mode (BW pin = V_{EE})

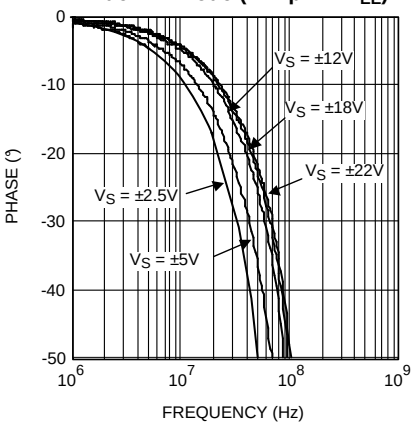

Figure 6.

Gain vs Frequency vs Power Supply Voltage Low I_Q Mode (BW pin = Float)

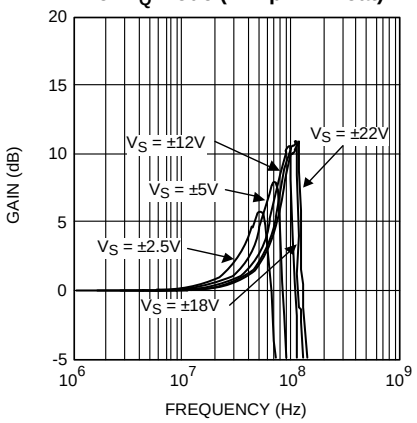

Figure 7.

Phase vs Frequency vs Power Supply Voltage Low I_Q Mode (BW pin = Float)

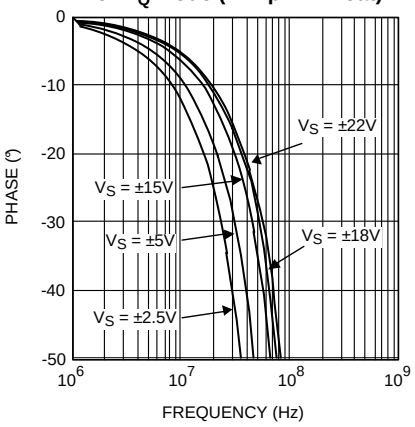

Figure 8.

TYPICAL PERFORMANCE CHARACTERISTICS (continued)

Gain vs Frequency vs R_{LOAD} Wide BW Mode (BW pin = V_{EE}), V_S = ±22V

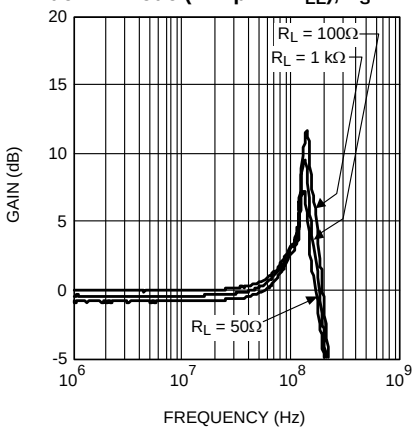

Figure 9.

Phase vs Frequency vs R_{LOAD} Wide BW Mode (BW pin = V_{EE}), V_S = ±22V

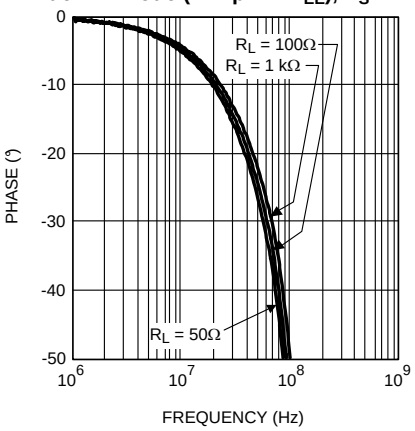

Figure 10.

Gain vs Frequency vs R_{LOAD} Low I_Q Mode (BW pin = Float), V_S = ±22V

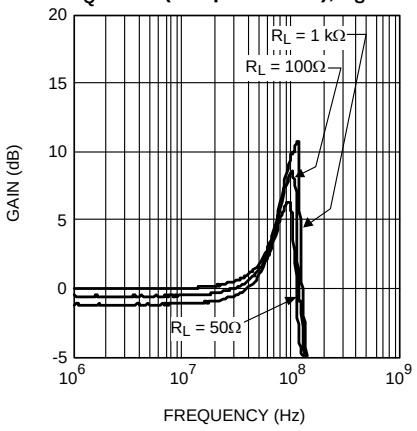

Figure 11.

Phase vs Frequency vs R_{LOAD} Low I_Q Mode (BW pin = Float), V_S = ±22V

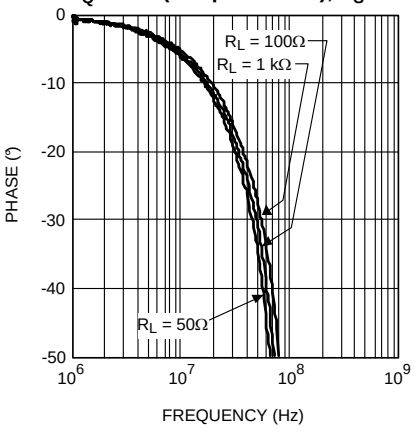

Figure 12.

Gain vs Frequency vs Quiescent Current V_S = ±15V

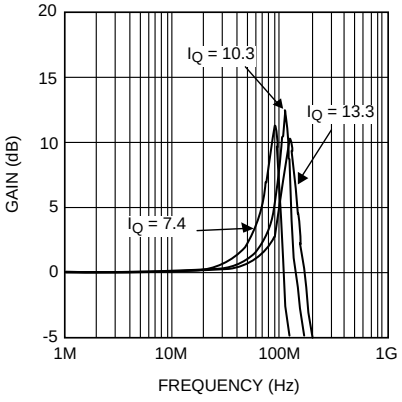

Figure 13.

Phase vs Frequency vs Quiescent Current V_S = ±15V

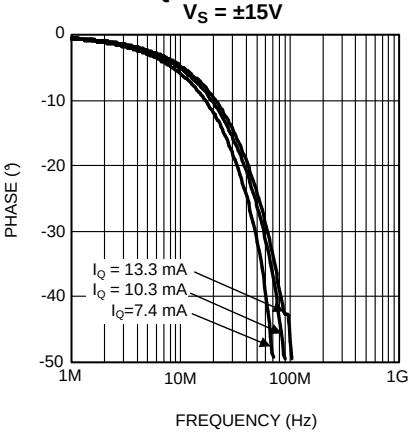

Figure 14.

TYPICAL PERFORMANCE CHARACTERISTICS (continued)

Gain vs Frequency vs R_{LOAD} Wide BW Mode (BW pin = V_{EE}), V_S = ±15V

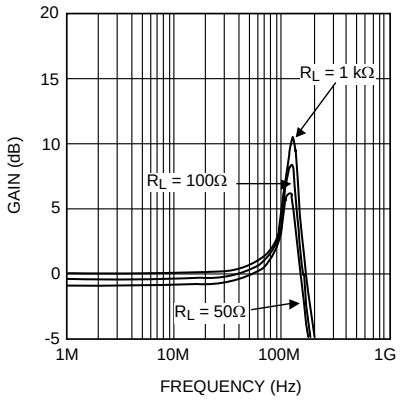

Figure 15.

Phase vs Frequency vs R_{LOAD} Wide BW Mode (BW pin = V_{EE}), V_S = ±15V

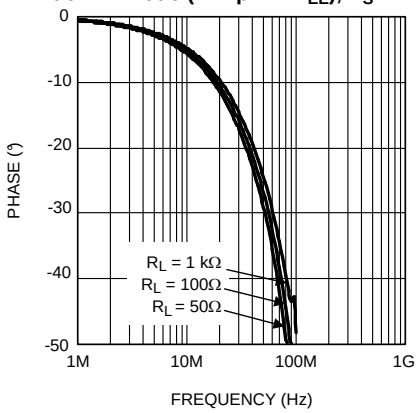

Figure 16.

Gain vs Frequency vs R_{LOAD} Low I_Q Mode (BW pin = Float), V_S = ±15V

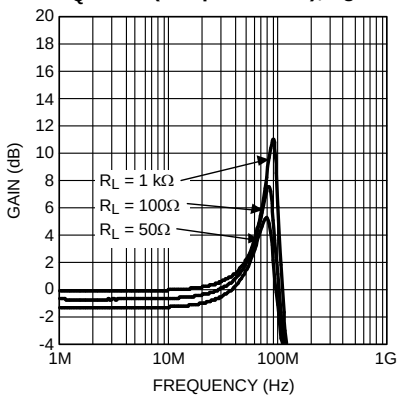

Figure 17.

Phase vs Frequency vs R_{LOAD} Low I_Q Mode (BW pin = Float), V_S = ±15V

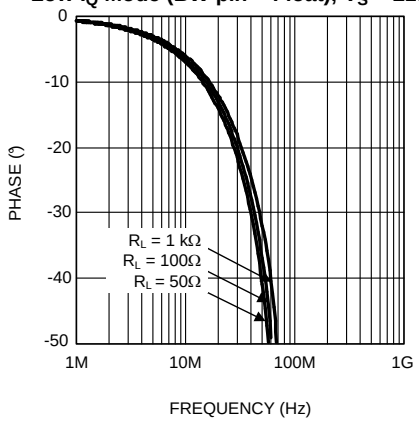

Figure 18.

+PSRR vs Frequency V_S = +15V and ±22V, Wide BW Mode (BW pin = V_{EE})

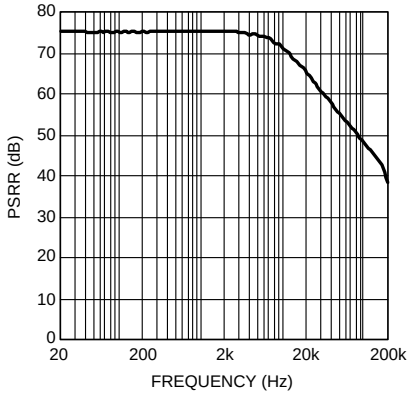

Figure 19.

+PSRR vs Frequency V_S = ±15V and ±22V, Low I_Q Mode (BW pin = Float)

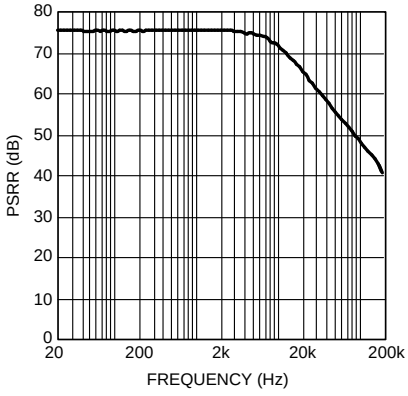

Figure 20.

TYPICAL PERFORMANCE CHARACTERISTICS (continued)

−PSRR vs Frequency
V_S = ±15V and ±22V, Wide BW Mode
(BW pin = V_{EE})

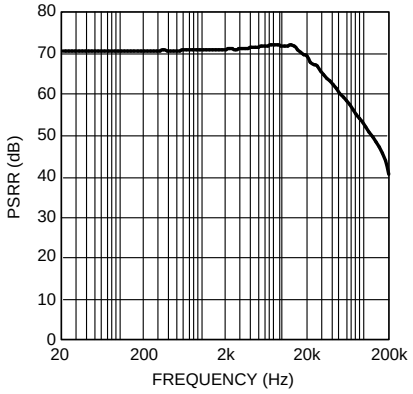

Figure 21.

−PSRR vs Frequency
V_S = ±15V and ±22V, Low I_Q Mode
(BW pin = Float)

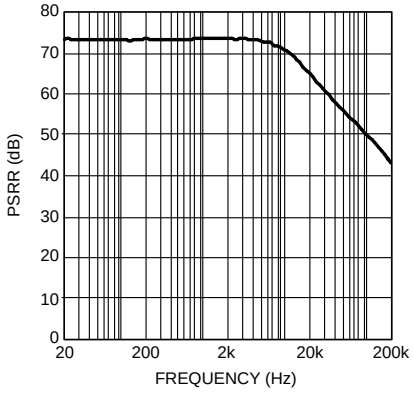

Figure 22.

Quiescent Current vs
Bandwidth Control Resistance
V_S = ±15V (Bottom) & V_S = ±22V (Top)

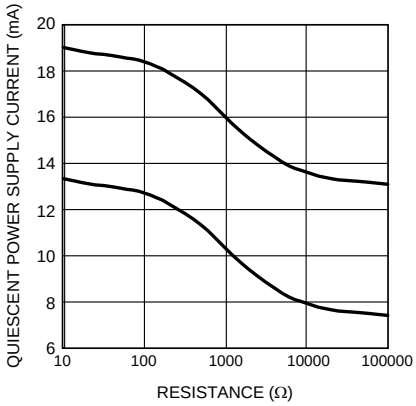

Figure 23.

THD+N vs Output Voltage
V_S = ±15V, R_L = 32Ω, f = 1kHz

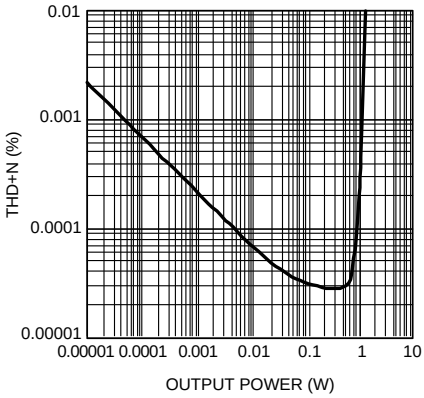

Figure 24.

Wide BW Noise Curve
(BW pin = V_{EE})

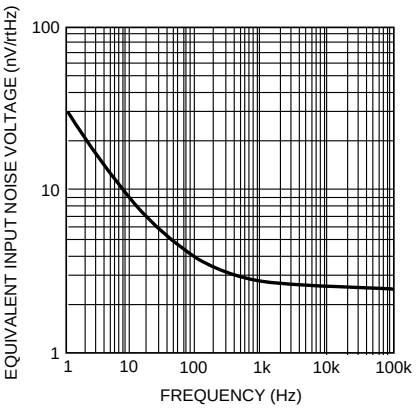

Figure 25.

Low I_Q Noise Curve
(BW pin = Float)

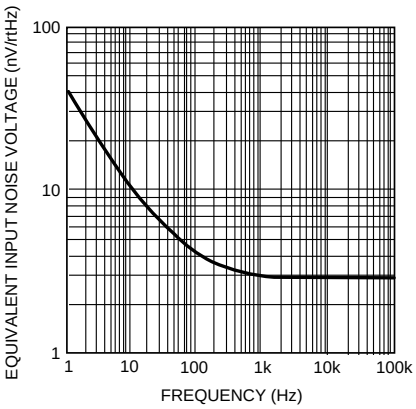

Figure 26.

TYPICAL APPLICATION DIAGRAM

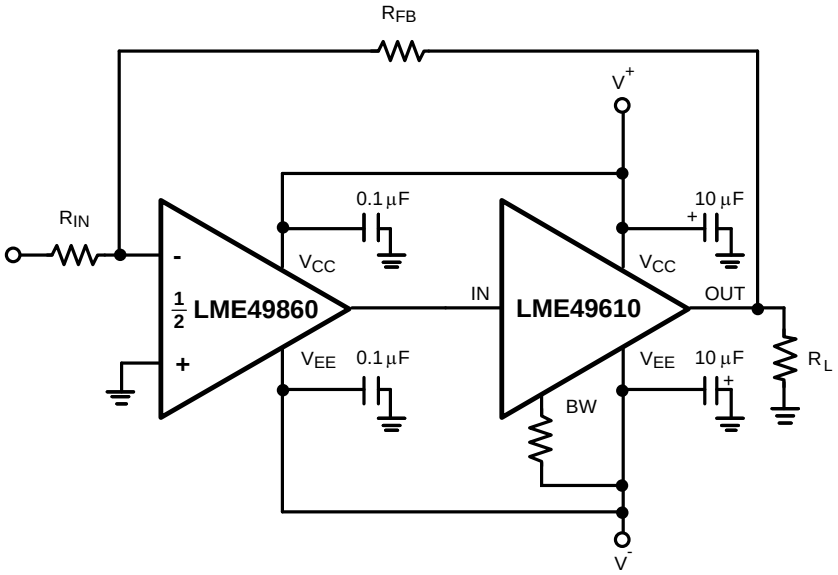

Figure 27. High Performance, High Fidelity LME49610 Audio Buffer Application

APPLICATION INFORMATION

HIGH PERFORMANCE, HIGH FIDELITY HEADPHONE AMPLIFIER

The LME49610 is the ideal solution for high output, high performance high fidelity headphone amplifiers. When placed in the feedback loop of the LME49710, LME49720 or LME49740 High Performance, High Fidelity audio operational amplifier, the LME49610 is able to drive 32Ω headphones to a dissipation of greater than 500mW at 0.00003% THD+N while operating on ±15V power supply voltages. The circuit schematic for a typical headphone amplifier is shown in Figure 28.

Operation

The following describes the circuit operation for the headphone amplifier's Left Channel. The Right Channel operates identically.

The audio input signal is applied to the input jack (HP31 or J1/J2) and dc-coupled to the volume control, VR1. The output signal from VR1's wiper is applied to the non-inverting input of U2-A, an LME49720 High Performance, High Fidelity audio operational amplifier. U2-A's signal gain is set by resistors R2 and R4. To allow for a DC-coupled signal path and to ensure minimal output DC voltage regardless of the closed-loop gain, the other half of the U2 is configured as a DC servo. By constantly monitoring U2-A's output, the servo creates a voltage that compensates for any DC voltage that may be present at the output. A correction voltage is generated and applied to the feedback node at U2-A, pin 2. The servo ensures that the gain at DC is unity. Based on the values shown in Figure 28, the RC combination formed by R11 and C7 sets the servo's high-pass cutoff at 0.16Hz. This is over two decades below 20Hz, minimizing both amplitude and phase perturbations in the audio frequency band's lowest frequencies.

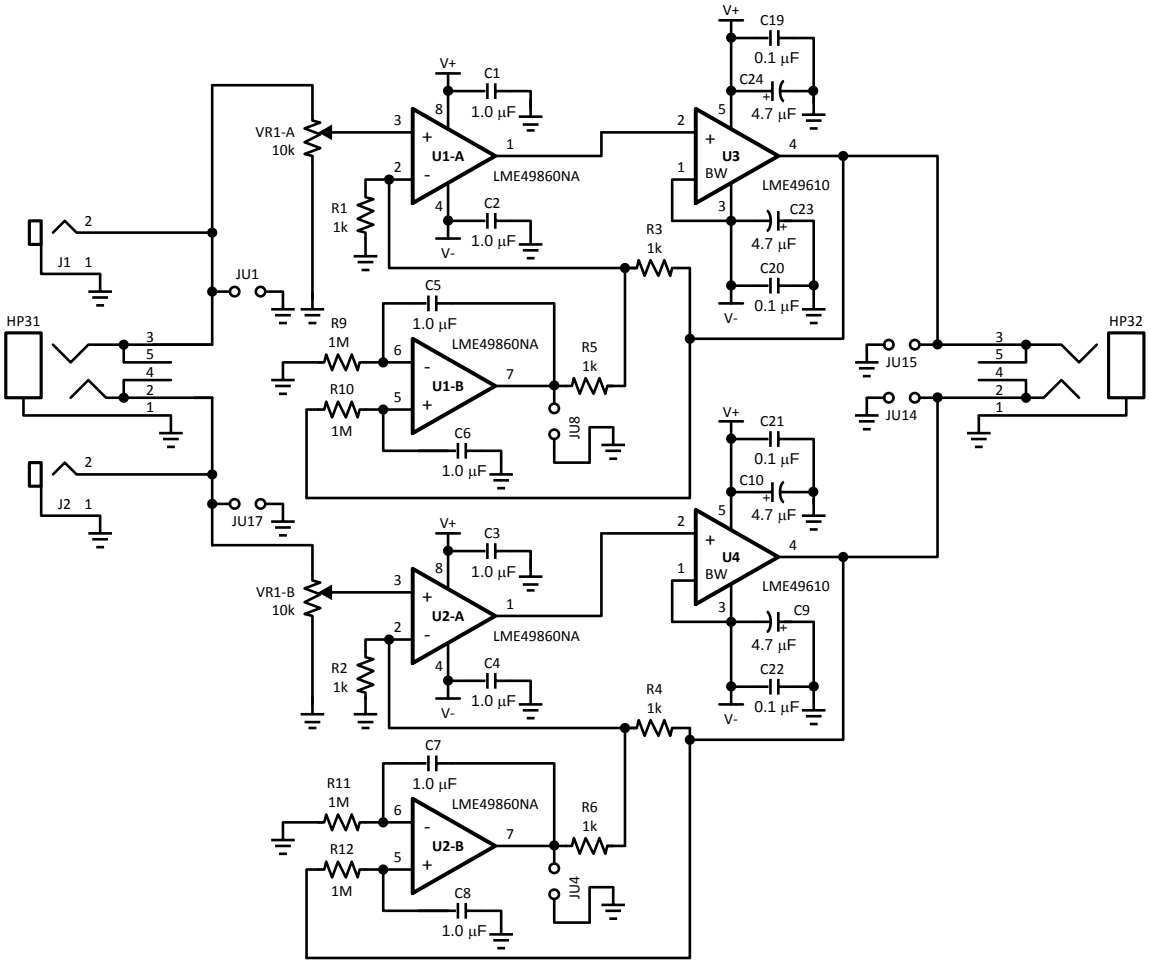

Figure 28. LME49610 Delivers High Output Current for this High Performance Headphone Amplifier

AUDIO BUFFERS

Audio buffers or unity-gain followers, have large current gain and a voltage gain of one. Audio buffers serve many applications that require high input impedance, low output impedance and high output current. They also offer constant gain over a very wide bandwidth.

Buffers serve several useful functions, either in stand-alone applications or in tandem with operational amplifiers. In stand-alone applications, their high input impedance and low output impedance isolates a high impedance source from a low impedance load.

SUPPLY BYPASSING

The LME49610 will place great demands on the power supply voltage source when operating in applications that require fast slewing and driving heavy loads. These conditions can create high amplitude transient currents. A power supply's limited bandwidth can reduce the supply's ability to supply the needed current demands during these high slew rate conditions. This inability to supply the current demand is further exacerbated by PCB trace or interconnecting wire inductance. The transient current flowing through the inductance can produce voltage transients.

For example, the LME49610's output voltage can slew at a typical 2000V/µs. When driving a 100Ω load, the di/dt current demand is 20 A/µs. This current flowing through an inductance of 50nH (approximately 1.5" of 22 gage wire) will produce a 1V transient. In these and similar situations, place the parallel combination of a solid 5µF to 10µF tantalum capacitor and a ceramic 0.1µF capacitor as close as possible to the device supply pins.

Ceramic capacitor have very lower ESR (typically less than 10mΩ) and low ESL when compared to the same valued tantalum capacitor. The ceramic capacitors, therefore, have superior AC performance for bypassing high frequency noise.

In less demanding applications that have lighter loads or lower slew rates, the supply bypassing is not as critical. Capacitor values in the range of 0.01µF to 0.1µF are adequate.

SIMPLIFIED LME49610 CIRCUIT DIAGRAM

The LME49610's simplified circuit diagram is shown in Figure 29. The diagram shows the LME49610's complementary emitter follower design, bias circuit and bandwidth adjustment node.

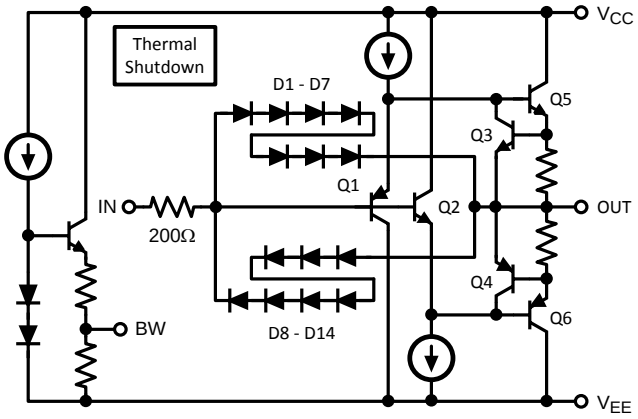

Figure 29. Simplified Circuit Diagram

Figure 30 shows the LME49610 connected as an open-loop buffer. The source impedance and optional input resistor, R_S, can alter the frequency response. As previously stated, the power supplies should be bypassed with capacitors connected close to the LME49610's power supply pins. Capacitor values as low as 0.01µF to 0.1µF will ensure stable operation in lightly loaded applications, but high output current and fast output slewing can demand large current transients from the power supplies. Place a recommended parallel combination of a solid tantalum capacitor in the 5µF to 10µF range and a ceramic 0.1µF capacitor as close as possible to the device supply pins.

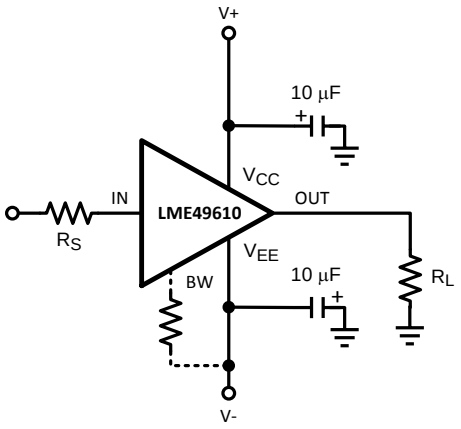

Figure 30. Buffer Connections

OUTPUT CURRENT

The LME49610 can continuously source or sink 250mA. Internal circuitry limits the short circuit output current to approximately ±450mA. For many applications that fully utilize the LME49610's current source and sink capabilities, thermal dissipation may be the factor that limits the continuous output current.

The maximum output voltage swing magnitude varies with junction temperature and output current. Using sufficient PCB copper area as a heatsink when the metal tab of the LME49610's surface mount DDPAK/TO-263 package is soldered directly to the circuit board reduces thermal impedance. This in turn reduces junction temperature. The PCB copper area should be in the range of $2in^2$ to $6in^2$.

THERMAL PROTECTION

LME49610 power dissipated will cause the buffer's junction temperature to rise. A thermal protection circuit in the LME49610 will disable the output when the junction temperature exceeds 150°C. When the thermal protection is activated, the output stage is disabled, allowing the device to cool. The output circuitry is enabled when the junction temperature drops below 150°C.

The DSDPAK/TO-263 package has excellent thermal characteristics. To minimize thermal impedance, its exposed die attach paddle should be soldered to a circuit board copper area for good heat dissipation. Figure 31 shows typical thermal resistance from junction to ambient as a function of the copper area. The DDPAK/TO-263's exposed die attach paddle is electrically connected to the V_{EE} power supply pin.

LOAD IMPEDANCE

The LME49610 is stable under any capacitive load when driven by a source that has an impedance of 50Ω or less. When driving capacitive loads, any overshoot that is present on the output signal can be reduced by shunting the load capacitance with a resistor.

OVERVOLTAGE PROTECTION

If the input-to-output differential voltage exceeds the LME49610's Absolute Maximum Rating of 3V, the internal diode clamps shown in Figure 1 conduct, diverting current around the compound emitter followers of Q1/Q5 (D1 – D7 for positive input), or around Q2/Q6 (D8 – D14 for negative inputs). Without this clamp, the input transistors Q1/Q2 and Q5/Q6 will zener and damage the buffer.

To ensure that the current flow through the diodes is held to a save level, the internal 200Ω resistor in series with the input limits the current through these clamps. If the additional current that flows during this situation can damage the source that drives the LME49610's input, add an external resistor in series with the input see Figure 30.

BANDWIDTH CONTROL PIN

The LME49610's –3dB bandwidth is approximately 110MHz in the low quiescent-current mode (13mA typical). Select this mode by leaving the BW pin unconnected.

Connect the BW pin to the V_{EE} pin to extend the LME49610's bandwidth to a nominal value of 180MHz. In this mode, the quiescent current increases to approximately 19mA. Bandwidths between these two limits are easily selected by connecting a series resistor between the BW pin and V_{EE} .

Regardless of the connection to the LME49610's BW pin, the rated output current and slew rate remain constant. With the power supply voltage held constant, the wide-bandwidth mode's increased quiescent current causes a corresponding increase in quiescent power dissipation. For all values of the BW pin voltage, the quiescent power dissipation is equal to the total supply voltage times the quiescent current (I_Q * (V_{CC} + |V_{EE} |)).

BOOSTING OP AMP OUTPUT CURRENT

When placed in the feedback loop, the LME49610 will increase an operational amplifier's output current. The operational amplifier's open loop gain will correct any LME49610 errors while operating inside the feedback loop.

To ensure that the operational amplifier and buffer system are closed loop stable, the phase shift must be low. For a system gain of one, the LME49610 must contribute less than 20° at the operational amplifier's unity-gain frequency. Various operating conditions may change or increase the total system phase shift. These phase shift changes may affect the operational amplifier's stability.

Unity gain stability is preserved when the LME49610 is placed in the feedback loop of most general-purpose or precision op amps. When the LME46900 is driving high value capacitive loads, the BW pin should be connected to the V_{EE} pin for wide bandwidth and stable operation. The wide bandwidth mode is also suggested for high speed or fast-settling operational amplifiers. This preserves their stability and the ability to faithfully amplify high frequency, fast-changing signals. Stability is ensured when pulsed signals exhibit no oscillations and ringing is minimized while driving the intended load and operating in the worst-case conditions that perturb the LME49610's phase response.

HIGH FREQUENCY APPLICATIONS

The LME49610's wide bandwidth and very high slew rate make it ideal for a variety of high-frequency open-loop applications such as an ADC input driver, 75Ω stepped volume attenuator driver, and other low impedance loads. Circuit board layout and bypassing techniques affect high frequency, fast signal dynamic performance when the LME49610 operates open-loop.

A ground plane type circuit board layout is best for very high frequency performance results. Bypass the power supply pins (V_{CC} and V_{EE}) with 0.1µF ceramic chip capacitors in parallel with solid tantalum 10µF capacitors placed as close as possible to the respective pins.

Source resistance can affect high-frequency peaking and step response overshoot and ringing. Depending on the signal source, source impedance and layout, best nominal response may require an additional resistance of 25Ω to 200Ω in series with the input. Response with some loads (especially capacitive) can be improved with an output series resistor in the range of 10Ω to 150Ω.

THERMAL MANAGEMENT

Heat Sinking

For some applications, the LME49610 may require a heat sink. The use of a heat sink is dependent on the maximum LME49610 power dissipation and a given application's maximum ambient temperature. In the DDPAK/TO-263 package, heat sinking the LME49610 is easily accomplished by soldering the package's tab to a copper plane on the PCB. (Note: The tab on the LME49610's DDPAK/TO-263 package is electrically connected to V_{EE}.)

Through the mechanisms of convection, heat conducts from the LME49610 in all directions. A large percentage moves to the surrounding air, some is absorbed by the circuit board material and some is absorbed by the copper traces connected to the package's pins. From the PCB material and the copper, it then moves to the air. Natural convection depends on the amount of surface area that contacts the air.

If a heat conductive copper plane has perfect thermal conduction (heat spreading) through the plane's total area, the temperature rise is inversely proportional to the total exposed area. PCB copper planes are, in that sense, an aid to convection. These planes, however, are not thick enough to ensure perfect heat conduction. Therefore, eventually a point of diminishing returns is reached where increasing copper area offers no additional heat conduction to the surrounding air. This is apparent in Figure 31. 2 oz copper boards will have decrease thermal resistance providing a better heat sink compared to 1oz. copper. Beyond 1oz or 2oz copper plane areas, external heatsinks are required. Ultimately, the 1oz copper area attains a nominal value of 20°C/W junction to ambient thermal resistance (θ_{JA}) under zero air flow.

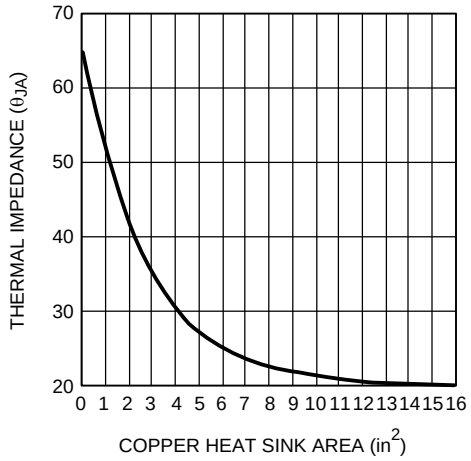

Figure 31. Thermal Resistance (Typ) for 5 Lead DDPAK/TO-263 Package Mounted on 1 Ounce of Copper

A copper plane may be placed directly beneath the tab. Additionally, a matching plane can be placed on the opposite side. If a plane is placed on the side opposite of the LME49610, connect it to the plane to which the buffer's metal tab is soldered with a matrix of thermal vias per JEDEC Standard JESD51-5.

Determining Copper Area

Find the required copper heat sink area using the following guidelines:

1. Determine the maximum power dissipation of the LME49610, P_D.
2. Specify a maximum operating ambient temperature, $T_{A(MAX)}$. Note that the die temperature, T_J, will be higher than T_A by an amount that is dependent on the thermal resistance from junction to ambient, θ_{JA}. Therefore, T_A must be specified such that T_J does not exceed the absolute maximum die temperature of 150°C.
3. Specify a maximum allowable junction temperature, $T_{J(MAX)}$, This is the LME49610's die temperature when the buffer is drawing maximum current (quiescent and load). It is prudent to design for a maximum continuous junction temperature of 100°C to 130°C. Ensure, however, that the junction temperature never exceeds the 150°C absolute maximum rating for the part.
4. alculate the value of junction to ambient thermal resistance, θ_{JA}.
5. θ_{JA} as a function of copper area in square inches is shown in Figure 31. Choose a copper area that will ensure the specified $T_{J(MAX)}$ for the calculated θ_{JA}. The maximum value of junction to ambient thermal resistance, θ_{JA}, is defined as:

   $\theta_{JA} = (T_{J(MAX)} - T_{A(MAX)}) / P_{D(MAX)}$ (°C/W)

   where

   - $T_{J(MAX)}$ = the maximum recommended junction temperature
   - $T_{A(MAX)}$ = the maximum ambient temperature in the LME49610's environment
   - $P_{D(MAX)}$ = the maximum recommended power dissipation
   - The allowable thermal resistance is determined by the maximum allowable temperature increase:

   $T_{RISE} = T_{J(MAX)} - T_{A(MAX)}$ (2) (2)

Thus, if ambient temperature extremes force T_{RISE} to exceed the design maximum, the part must be de-rated by either decreasing P_D to a safe level, reducing θ_{JA} further, or, if available, using a larger copper area.

Procedure

1. First determine the maximum power dissipated by the LME49610, $P_{D(MAX)}$. For the simple case of the buffer driving a resistive load, and assuming equal supplies, $P_{D(MAX)}$ is given by:

$$P_{DMAX(AC)} = (I_S \times V_S) + (V_S)^2 / (2\pi^2 R_L) \quad \text{(Watts)} \tag{3}$$

$$P_{DMAX(DC)} = (I_S \times V_S) + (V_S)^2 / R_L \quad \text{(Watts)}$$

where

- $V_S = |V_{EE}| + V_{CC}$ (V)
- I_S = quiescent supply current (A)

Equation 3 is for sinusoidal output voltages and Equation 4 is for DC output voltages (4)

2. Determine the maximum allowable die temperature rise,

$$T_{RISE(MAX)} = T_{J(MAX)} - T_{A(MAX)} \quad °C \tag{5}$$

3. Using the calculated value of $T_{RISE(MAX)}$ and $P_{D(MAX)}$, find the required value of junction to ambient thermal resistance combining Equation 1 and Equation 4 to derive Equation 6:

$$\theta_{JA} = T_{RISE(MAX)} / P_{D(MAX)} \quad (°C/W) \tag{6}$$

4. Finally, choose the minimum value of copper area from Figure 31 based on the value for θ_{JA}.

Example

Assume the following conditions: $V_S = |V_{EE}| + V_{CC} = 30V$, $R_L = 32\Omega$, $I_S = 15mA$, sinusoidal output voltage, $T_{J(MAX)} = 125°C$, $T_{A(MAX)} = 85°C$

Applying Equation 3:

$$P_{DMAX} = (I_S \times V_S) + (V_S)^2 / 2\pi^2 R_L \tag{7}$$

$$= (15mA)(30V) + 900V^2 / 632\Omega$$

$$= 1.87W$$

Applying Equation 4:

$$T_{RISE(MAX)} = 125°C – 85°C \tag{8}$$

$$= 40°C$$

Applying Equation 6:

$$\theta_{JA} = 40°C/1.87W \tag{9}$$

$$= 21.4°C/W$$

Examining the Copper Area vs. θ_{JA} plot (see Figure 31) indicates that a thermal resistance of 21.4°C/W is possible with a 8–10in^2 plane of one layer of 1oz copper. Other solutions include using two layers of 1oz copper or the use of 2oz copper. Higher dissipation may require forced air flow. As a safety margin, an extra 15% heat sinking capability is recommended.

When amplifying AC signals, wave shapes and the nature of the load (reactive, non-reactive) also influence dissipation. Peak dissipation can be several times the average with reactive loads. It is particularly important to determine dissipation when driving large load capacitance.

The LME49610's dissipation in DC circuit applications is easily computed using Equation 3. After the value of dissipation is determined, the heat sink copper area calculation is the same as for AC signals.

SLEW RATE

A buffer's voltage slew rate is its output signal's rate of change with respect to an input signal's step changes. For resistive loads, slew rate is limited by internal circuit capacitance and operating current (in general, the higher the operating current for a given internal capacitance, the higher the slew rate).

However, when driving capacitive loads, the slew rate may be limited by the available peak output current according to the following expression.

$$dv/dt = I_{PK} / C_L \tag{10}$$

Output voltages with high slew rates will require large output load currents. For example if the part is required to slew at 1000V/µs with a load capacitance of 1nF, the current demanded from the LME49610 is 1A. Therefore, fast slew rate is incompatible with a capacitive load of this value. Also, if C_L is in parallel with the load, the peak current available to the load decreases as C_L increases.

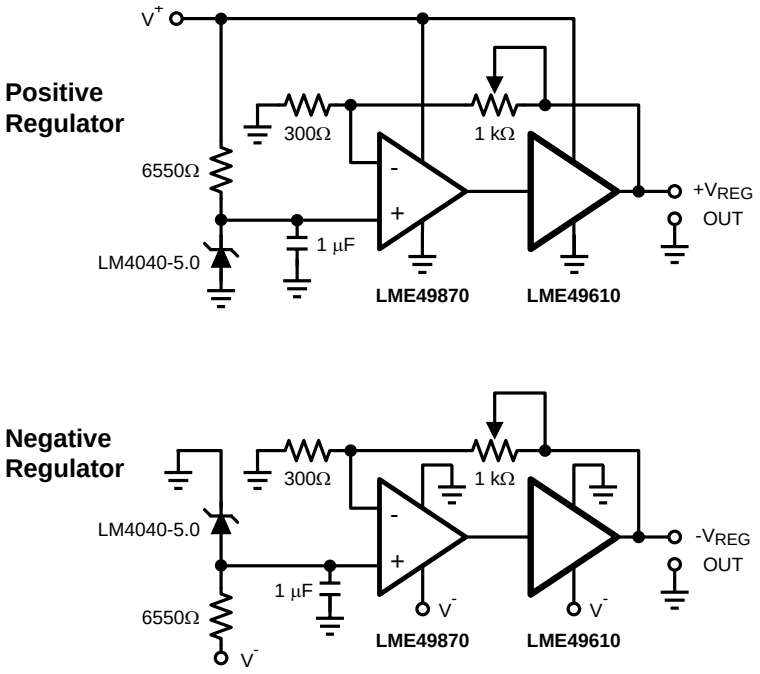

Figure 32. High Speed Positive and Negative Regulator

REVISION HISTORY

Rev	Date	Description
1.0	04/09/08	Initial WEB released.
1.01	10/28/09	Typical and Limit changes on the Short Circuit Output current.
B	04/04/13	Changed layout of National Data Sheet to TI format.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LME49610TS/NOPB	LIFEBUY	DDPAK/ TO-263	KTT	5	45	Pb-Free (RoHS Exempt)	CU SN	Level-3-245C-168 HR	-40 to 85	LME49610 TS	

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
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(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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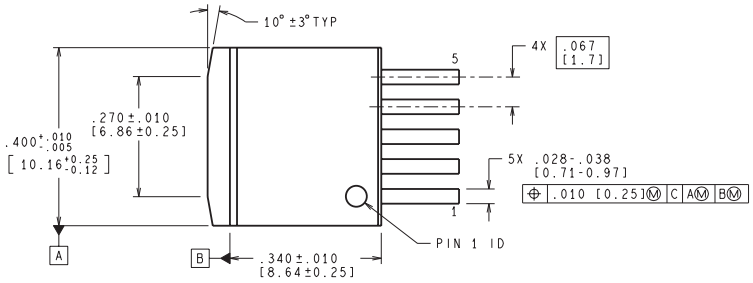

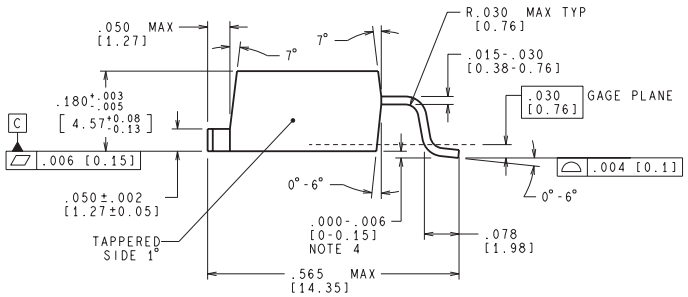

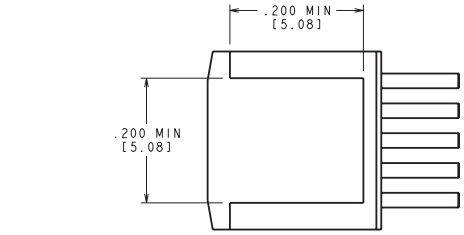

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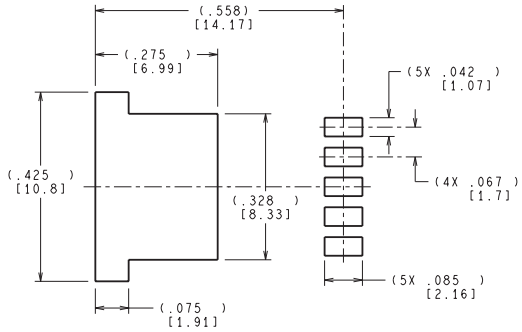

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