LM25115 Secondary Side Post Regulator Controller

Check for Samples: LM25115

FEATURES

- Self-synchronization to Main Channel Output
- Free-run Mode for Buck Regulation of DC Input
- Leading Edge Pulse Width Modulation
- Voltage-mode Control with Current Injection and Input Line Feed-forward
- Operates from AC or DC Input up to 42V
- Wide 4.5V to 30V Bias Supply Range
- Wide 0.75V to 13.5V Output Range.
- Top and Bottom Gate Drivers Sink 2.5A Peak
- Adaptive Gate Driver Dead-time Control
- Wide Bandwidth Error Amplifier (4MHz)
- Programmable Soft-start
- Thermal Shutdown Protection
- TSSOP-16 or Thermally Enhanced WSON-16 Packages

DESCRIPTION

The LM25115 controller contains all of the features necessary to implement multiple output power converters utilizing the Secondary Side Post Regulation (SSPR) technique. The SSPR technique develops a highly efficient and well regulated auxiliary output from the secondary side switching waveform of an isolated power converter. Regulation of the auxiliary output voltage is achieved by leading edge pulse width modulation (PWM) of the main channel duty cycle. Leading edge modulation is compatible with either current mode or voltage mode control of the main output. The LM25115 drives external high side and low side NMOS power switches configured as a synchronous buck regulator. A current sense amplifier provides overload protection and operates over a wide common mode input range. Additional features include a low dropout (LDO) bias regulator, error amplifier, precision reference, adaptive dead time control of the gate signals and thermal shutdown.

Typical Application Circuit

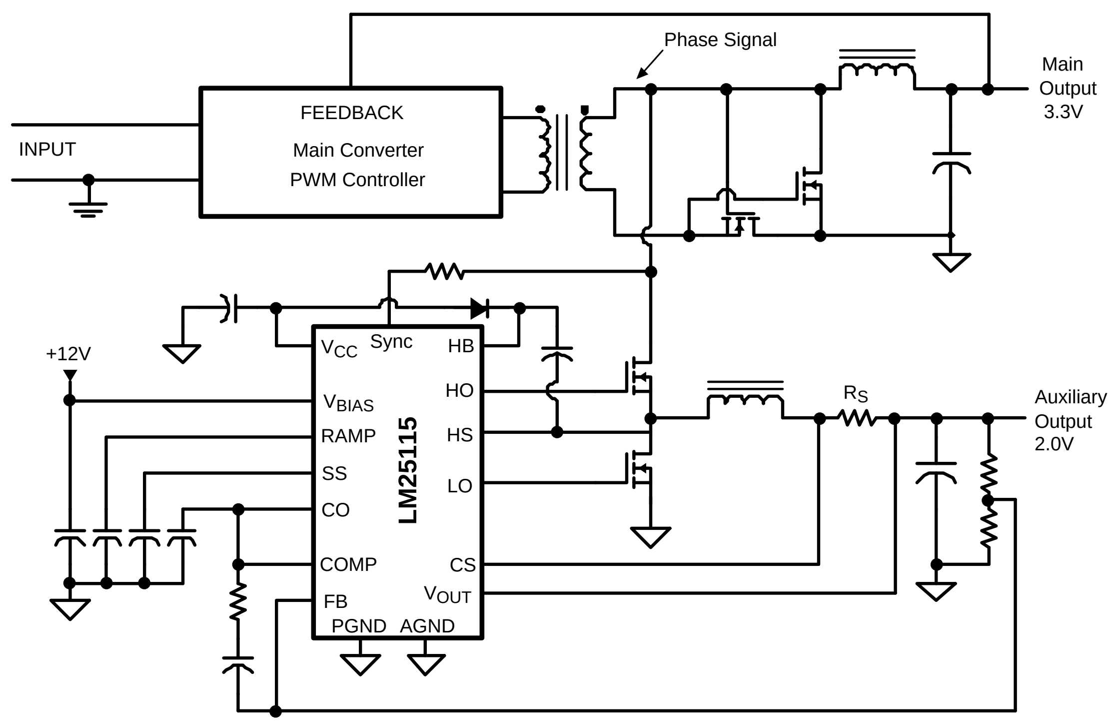


Figure 1. Simplified Multiple Output Power Converter Utilizing SSPR Technique

Connection Diagram

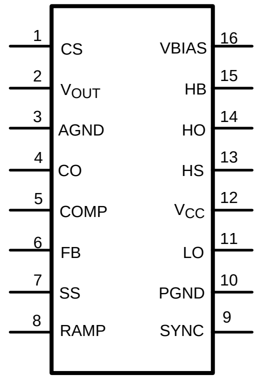


Figure 2. 16-Lead TSSOP, WSON
See Package Numbers PW0016A and NHQ0016A

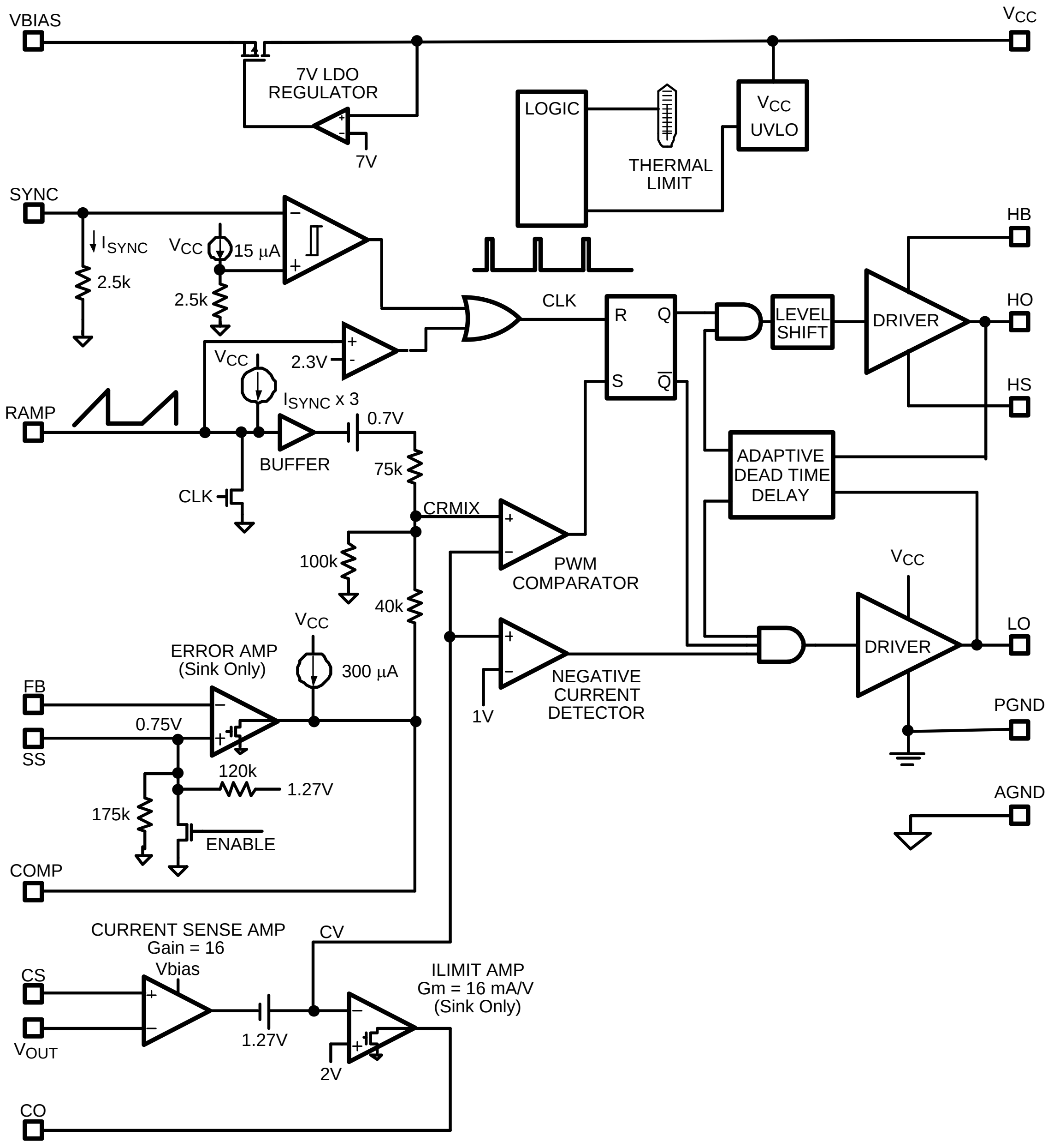
PIN DESCRIPTIONS

Pin	Name	Description	Application Information
1	CS	Current Sense amplifier positive input	A low inductance current sense resistor is connected between CS and VOUT. Current limiting occurs when the differential voltage between CS and VOUT exceeds 45mV (typical).
2	VOUT	Current sense amplifier negative input	Connected directly to the output voltage. The current sense amplifier operates over a voltage range from 0V to 13.5V at the VOUT pin.
3	AGND	Analog ground	Connect directly to the power ground pin (PGND).
4	CO	Current limit output	For normal current limit operation, connect the CO pin to the COMP pin. Leave this pin open to disable the current limit function.
5	COMP	Compensation. Error amplifier output	COMP pin pull-up is provided by an internal 300uA current source.
6	FB	Feedback. Error amplifier inverting input	Connected to the regulated output through the feedback resistor divider and compensation components. The non-inverting input of the error amplifier is internally connected to the SS pin.
7	SS	Soft-start control	An external capacitor and the equivalent impedance of an internal resistor divider connected to the bandgap voltage reference set the soft-start time. The steady state operating voltage of the SS pin equal to 0.75V (typical).
8	RAMP	PWM Ramp signal	An external capacitor connected to this pin sets the ramp slope for the voltage mode PWM. The RAMP capacitor is charged with a current that is proportional to current into the SYNC pin. The capacitor is discharged at the end of every cycle by an internal MOSFET.
9	SYNC	Synchronization input	A low impedance current input pin. The current into this pin sets the RAMP capacitor charge current and the frequency of an internal oscillator that provides a clock for the free-run (DC input) mode .
10	PGND	Power Ground	Connect directly to the analog ground pin (AGND).
11	LO	Low side gate driver output	Connect to the gate of the low side synchronous MOSFET through a short, low inductance path.
12	VCC	Output of bias regulator	Nominal 7V output from the internal LDO bias regulator. Locally decouple to PGND using a low ESR/ESL capacitor located as close to controller as possible.
13	HS	High side MOSFET source connection	Connect to negative terminal of the bootstrap capacitor and the source terminal of the high side MOSFET.
14	HO	High side gate driver output	Connect to the gate of high side MOSFET through a short, low inductance path.
15	HB	High side gate driver bootstrap rail	Connect to the cathode of the bootstrap diode and the positive terminal of the bootstrap capacitor. The bootstrap capacitor supplies current to charge the high side MOSFET gate and should be placed as close to controller as possible.

PIN DESCRIPTIONS (continued)

Pin	Name	Description	Application Information
16	VBIAS	Supply Bias Input	Input to the LDO bias regulator and current sense amplifier that powers internal blocks. Input range of VBIAS is 4.5V to 30V.
-	Exposed Pad (WSON Package Only)	Exposed Pad, underside of WSON package	Internally bonded to the die substrate. Connect to system ground for low thermal impedance.

Block Diagram



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

ABSOLUTE MAXIMUM RATINGS(1)(2)

VBIAS to GND	–0.3V to 32V
VCC to GND	–0.3V to 9V
HS to GND	–1V to 45V
VOUT, CS to GND	– 0.3V to 15V
All other inputs to GND	−0.3V to 7.0V
Storage Temperature Range	–55°C to +150°C
Junction Temperature	+150°C
ESD Rating HBM (3)	2 kV

(1) Absolute Maximum Ratings indicate limits beyond which damage to the component may occur. Operating Ratings are conditions under which operation of the device is specified. Operating Ratings do not imply ensured performance limits. For ensured performance limits and associated test conditions, see the Electrical Characteristics tables.
(2) If Military/Aerospace specified devices are required, please contact the Texas Instruments Sales Office/Distributors for availability and specifications.
(3) The human body model is a 100 pF capacitor discharged through a 1.5kΩ resistor into each pin.

OPERATING RATINGS

VBIAS supply voltage	5V to 30V
VCC supply voltage	5V to 7.5V
HS voltage	0V to 42V
HB voltage	VCC + HS
Operating Junction Temperature	–40°C to +125°C

TYPICAL OPERATING CONDITIONS

Parameter	Min	Typ	Max	Units
Supply Voltage, VBIAS	4.5		30	V
Supply Voltage, VCC	4.5		7	V
Supply voltage bypass, CVBIAS	0.1	1		µF
Reference bypass capacitor, CVCC	0.1	1	10	µF
HB-HS bootstrap capacitor	0.047			µF
SYNC Current Range (VCC = 4.5V)	50		150	µA
RAMP Saw Tooth Amplitude	1		1.75	V
VOUT regulation voltage (VBIAS min = 3V + VOUT)	0.75		13.5	V

ELECTRICAL CHARACTERISTICS

Unless otherwise specified, T_J = –40°C to +125°C, VBIAS = 12V, No Load on LO or HO.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
VBIAS SUPPLY						
Ibias	VBIAS Supply Current	F_{SYNC} = 200kHz			4	mA
VCC LOW DROPOUT BIAS REGULATOR						
VccReg	VCC Regulation	VCC open circuit. Outputs not switching	**6.65**	7	**7.15**	V
	VCC Current Limit	((1))		40		mA
	VCC Under-voltage Lockout Voltage	Positive going VCC	**4**		**4.5**	V
	VCC Under-voltage Hysteresis		**0.2**	0.25	**0.3**	V

(1) Device thermal limitations may limit usable range.

ELECTRICAL CHARACTERISTICS (continued)

Unless otherwise specified, T_J = –40°C to +125°C, VBIAS = 12V, No Load on LO or HO.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
SOFT-START						
	SS Source Impedance		43	60	77	kΩ
	SS Discharge Impedance			100		Ω
ERROR AMPLIFIER and FEEDBACK REFERENCE						
VREF	FB Reference Voltage	Measured at FB pin	**0.737**	0.75	**0.763**	V
	FB Input Bias Current	FB = 2V		0.2	**0.5**	µA
	COMP Source Current			300		µA
	Open Loop Voltage Gain			60		dB
GBW	Gain Bandwidth Product			4		MHz
Vio	Input Offset Voltage		**-7**	0	**7**	mV
	COMP Offset	Threshold for V_{HO} = high RAMP = CS = VOUT = 0V		2		V
	RAMP Offset	Threshold for V_{HO} = high COMP = 1.5V, CS = VOUT = 0V		1.1		V
CURRENT SENSE AMPLIFIER						
	Current Sense Amplifier Gain			16		V/V
	Output DC Offset			1.27		V
	Amplifier Bandwidth			500		kHz
CURRENT LIMIT						
	ILIMIT Amp Transconductance			16		mA / V
	Overall Transconductance			237		mA / V
	Positive Current Limit	$V_{CL} = V_{CS} - V_{VOUT}$ VOUT = 6V and CO/COMP = 1.5V	**37**	45	**53**	mV
	Positive Current Limit Foldback	$V_{CL} = V_{CS} - V_{VOUT}$ VOUT = 0V and CO/COMP = 1.5V	**31**	38	**45**	mV
VCLneg	Negative Current Limit	VOUT = 6V $V_{CL} = V_{CS} - V_{VOUT}$ to cause LO to shutoff		-17		mV
RAMP GENERATOR						
	SYNC Input Impedance			2.5		kΩ
	SYNC Threshold	End of cycle detection threshold		15		µA
	Free Run Mode Peak Threshold	RAMP peak voltage with dc current applied to SYNC.			**2.3**	V
	Current Mirror Gain	Ratio of RAMP charge current to SYNC input current.	**2.7**		**3.3**	A/A
	Discharge Impedance			100		Ω
LOW SIDE GATE DRIVER						
V_{OLL}	LO Low-state Output Voltage	I_{LO} = 100mA		0.2	**0.5**	V
V_{OHL}	LO High-state Output Voltage	I_{LO} = -100mA, $V_{OHL} = V_{CC} - V_{LO}$		0.4	**0.8**	V
	LO Rise Time	C_{LOAD} = 1000pF		15		ns
	LO Fall Time	C_{LOAD} = 1000pF		12		ns
I_{OHL}	Peak LO Source Current	V_{LO} = 0V		2		A
I_{OLL}	Peak LO Sink Current	V_{LO} = 12V		2.5		A

ELECTRICAL CHARACTERISTICS (continued)

Unless otherwise specified, T_J = –40°C to +125°C, VBIAS = 12V, No Load on LO or HO.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
HIGH SIDE GATE DRIVER						
V_{OLH}	HO Low-state Output Voltage	I_{HO} = 100mA		0.2	**0.5**	V
V_{OHH}	HO High-state Output Voltage	I_{HO} = -100mA, $V_{OHH} = V_{HB} – V_{HO}$		0.4	**0.8**	V
	HO Rise Time	C_{LOAD} = 1000pF		15		ns
	HO High Side Fall Time	C_{LOAD} = 1000pF		12		ns
I_{OHH}	Peak HO Source Current	V_{HO} = 0V		2		A
I_{OLH}	Peak HO Sink Current	V_{HO} = 12V		2.5		A
SWITCHING CHARACTERISITCS						
	LO Fall to HO Rise Delay	C_{LOAD} = 0		70		ns
	HO Fall to LO Rise Delay	C_{LOAD} = 0		50		ns
	SYNC Fall to HO Fall Delay	C_{LOAD} = 0		120		ns
	SYNC Rise to LO Fall Delay	C_{LOAD} = 0		50		ns
THERMAL SHUTDOWN						
T_{SD}	Thermal Shutdown Temp.		150	165		°C
	Thermal Shutdown Hysteresis			25		°C
THERMAL RESISTANCE						
θ_{JA}	Junction to Ambient	PW Package		125		°C/W
θ_{JA}	Junction to Ambient	NHQ Package		32		°C/W

TYPICAL PERFORMANCE CHARACTERISTICS

VCC Regulator Start-Up Characteristics, VCC vs VBIAS

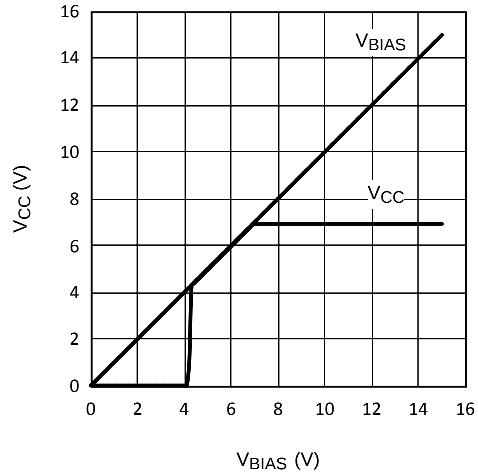


Figure 3.

VCC Load Regulation to Current Limit

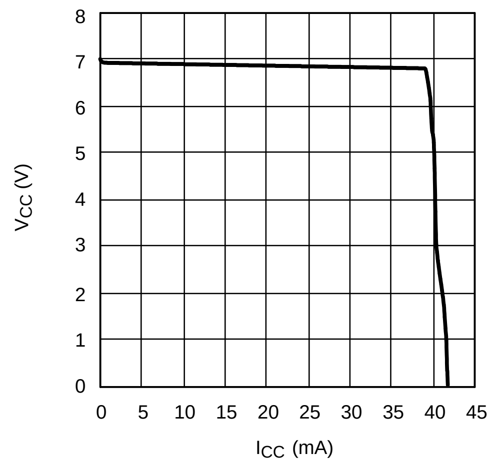


Figure 4.

Current Value (CV) vs Current Limit (V_{CL})

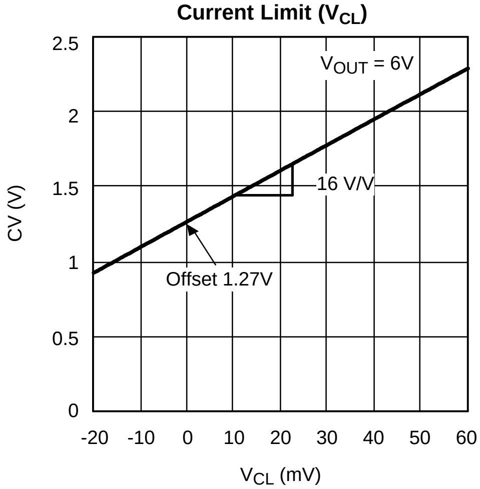


Figure 5.

Current Sense Amplifier Gain and Phase vs Frequency

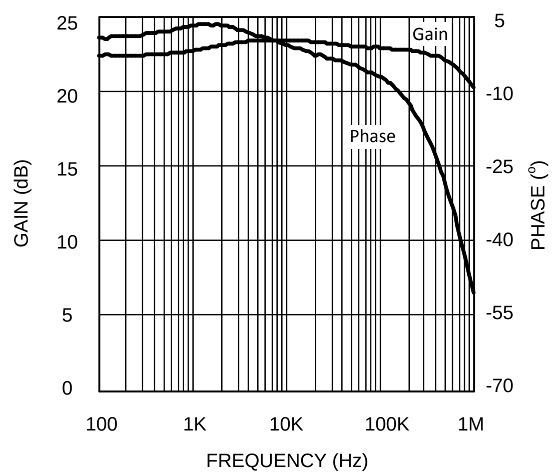


Figure 6.

TYPICAL PERFORMANCE CHARACTERISTICS (continued)

Current Error Amplifier Transconductance

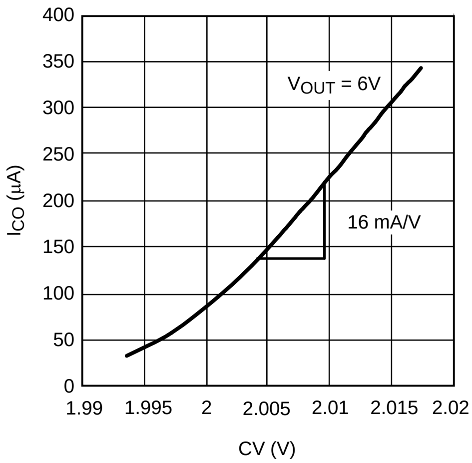


Figure 7.

Overall Current Amplifier Transconductance

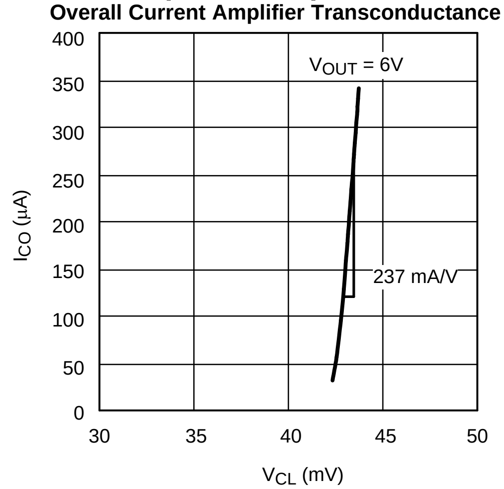


Figure 8.

Common Mode Output Voltage vs Positive Current Limit

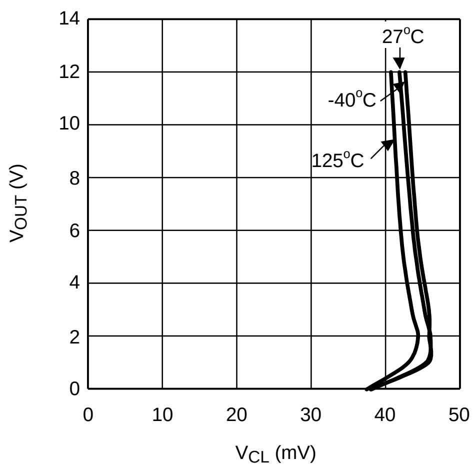


Figure 9.

Common Mode Output Voltage vs Negative Current Limit (Room Temp)

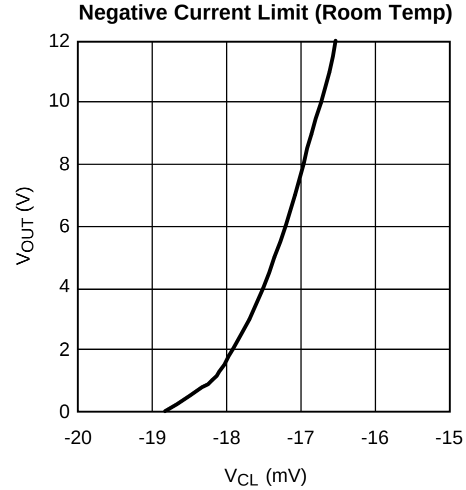


Figure 10.

DETAILED OPERATING DESCRIPTION

The LM25115 controller contains all of the features necessary to implement multiple output power converters utilizing the Secondary Side Post Regulation (SSPR) technique. The SSPR technique develops a highly efficient and well regulated auxiliary output from the secondary side switching waveform of an isolated power converter. Regulation of the auxiliary output voltage is achieved by leading edge pulse width modulation (PWM) of the main channel duty cycle. Leading edge modulation is compatible with either current mode or voltage mode control of the main output. The LM25115 drives external high side and low side NMOS power switches configured as a synchronous buck regulator. A current sense amplifier provides overload protection and operates over a wide common mode input range from 0V to 13.5V. Additional features include a low dropout (LDO) bias regulator, error amplifier, precision reference, adaptive dead time control of the gate driver signals and thermal shutdown. A programmable oscillator provides a PWM clock signal when the LM25115 is powered by a dc input (free-run mode) instead of the phase signal of the main channel converter (SSPR mode).

Low Drop-out Bias Regulator (VCC)

The LM25115 contains an internal LDO regulator that operates over an input supply range from 4.5V to 30V. The output of the regulator at the VCC pin is nominally regulated at 7V and is internally current limited to 40mA. VCC is the main supply to the internal logic, PWM controller, and gate driver circuits. When power is applied to the VBIAS pin, the regulator is enabled and sources current into an external capacitor connected to the VCC pin. The recommended output capacitor range for the VCC regulator is 0.1uF to 100uF. When the voltage at the VCC pin reaches the VCC under-voltage lockout threshold of 4.25V, the controller is enabled. The controller is disabled if VCC falls below 4.0V (250mV hysteresis). In applications where an appropriate regulated dc bias supply is available, the LM25115 controller can be powered directly through the VCC pin instead of the VBIAS pin. In this configuration, it is recommended that the VCC and the VBIAS pins be connected together such that the external bias voltage is applied to both pins. The allowable VCC range when biased from an external supply is 4.5V to 7V.

Synchronization (SYNC) and Feed-forward (RAMP)

The pulsing “phase signal” from the main converter synchronizes the PWM ramp and gate drive outputs of the LM25115. The phase signal is the square wave output from the transformer secondary winding before rectification (Figure 1). A resistor connected from the phase signal to the low impedance SYNC pin produces a square wave current (I_{SYNC}) as shown in Figure 11. A current comparator at the SYNC input monitors I_{SYNC} relative to an internal 15µA reference. When I_{SYNC} exceeds 15µA, the internal clock signal (CLK) is reset and the capacitor connected to the RAMP begins to charge. The current source that charges the RAMP capacitor is equal to 3 times the I_{SYNC} current. The falling edge of the phase signal sets the CLK signal and discharges the RAMP capacitor until the next rising edge of the phase signal. The RAMP capacitor is discharged to ground by a low impedance (100Ω) n-channel MOSFET. The input impedance at SYNC pin is 2.5kΩ which is normally much less than the external SYNC pin resistance.

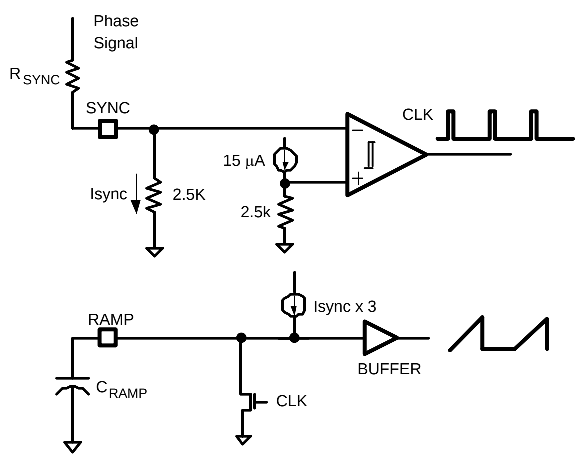


Figure 11. Line Feed-forward Diagram

The RAMP and SYNC functions illustrated in Figure 11 provide line voltage feed-forward to improve the regulation of the auxiliary output when the input voltage of the main converter changes. Varying the input voltage to the main converter produces proportional variations in amplitude of the phase signal. The main channel PWM controller adjusts the pulse width of the phase signal to maintain constant volt*seconds and a regulated main output as shown in Figure 12. The variation of the phase signal amplitude and duration are reflected in the slope and duty cycle of the RAMP signal of the LM25115 (I_{SYNC} α phase signal amplitude). As a result, the duty cycle of the LM25115 is automatically adjusted to regulate the auxiliary output voltage with virtually no change in the PWM threshold voltage. Transient line regulation is improved because the PWM duty cycle of the auxiliary converter is immediately corrected, independent of the delays of the voltage regulation loop.

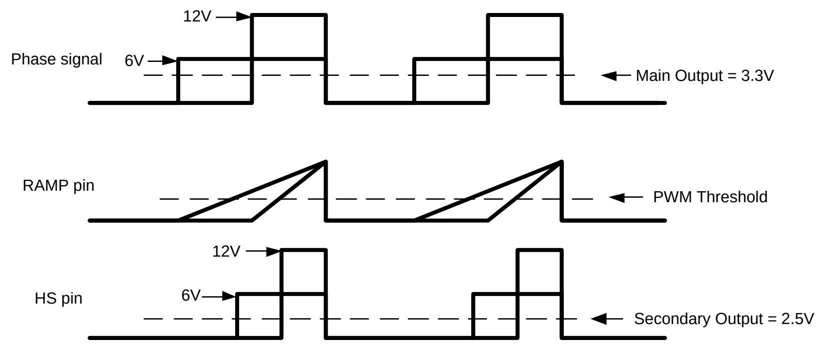


Figure 12. Line Feed-forward Waveforms

The recommended SYNC input current range is 50µA to 150µA. The SYNC pin resistor (R_{SYNC}) should be selected to set the SYNC current (I_{SYNC}) to 150µA with the maximum phase signal amplitude, $V_{PHASE(max)}$. This will ensure that I_{SYNC} stays within the recommended range over a 3:1 change in phase signal amplitude. The SYNC pin resistor is therefore:

$$R_{SYNC} = (V_{PHASE(max)} / 150\mu A) - 2.5k\Omega$$

Once I_{SYNC} has been established by selecting R_{SYNC}, the RAMP signal amplitude may be programmed by selecting the proper RAMP pin capacitor value. The recommended peak amplitude of the RAMP waveform is 1V to 1.75V. The C_{RAMP} capacitor is chosen to provide the desired RAMP amplitude with the nominal phase signal voltage and pulse width.

$$C_{RAMP} = (3 \times I_{SYNC} \times T_{ON}) / V_{RAMP}$$

where

- C_{RAMP} = RAMP pin capacitance
- I_{SYNC} = SYNC pin current current
- T_{ON} = corresponding phase signal pulse width
- V_{RAMP} = desired RAMP amplitude (1V to 1.75V)

For example,

Main channel output = 3.3V. Phase signal maximum amplitude = 12V. Phase signal frequency = 250kHz

- Set I_{SYNC} = 150µA with phase signal at maximum amplitude (12V):
  – $I_{SYNC} = 150\mu A = V_{PHASE(max)} / (R_{SYNC} + 2.5\ k\Omega) = 12V / (R_{SYNC} + 2.5\ k\Omega)$
  – $R_{SYNC} = 12V/150\mu A - 2.5k\Omega = 77.5k\Omega$
- T_{ON} = Main channel duty cycle / Phase frequency = (3.3V/12V) / 250kHz = 1.1µs
- Assume desired V_{RAMP} = 1.5V
- $C_{RAMP} = (3 \times I_{SYNC} \times T_{ON}) / V_{RAMP} = (3 \times 150\mu A \times 1.1\mu s) / 1.5V$
- C_{RAMP} = 330pF

Error Amplifier and Soft-Start (FB, CO, & COMP, SS)

An internal wide bandwidth error amplifier is provided within the LM25115 for voltage feedback to the PWM controller. The amplifier's inverting input is connected to the FB pin. The output of the auxiliary converter is regulated by connecting a voltage setting resistor divider between the output and the FB pin. Loop compensation networks are connected between the FB pin and the error amplifier output (COMP). The amplifier's non-inverting input is internally connected to the SS pin. The SS pin is biased at 0.75V by a resistor divider connected to the internal 1.27V bandgap reference. When the VCC voltage is below the UVLO threshold, the SS pin is discharged to ground. When VCC rises and exceeds the positive going UVLO threshold (4.25V), the SS pin is released and allowed to rise. If an external capacitor is connected to the SS pin, it will be charged by the internal resistor divider to gradually increase the non-inverting input of the error amplifier to 0.75V. The equivalent impedance of the SS resistor divider is nominally 60kΩ which determines the charging time constant of the SS capacitor. During start-up, the output of the LM25115 converter will follow the exponential equation:

$$VOUT(t) = VOUT(final) \times (1 - \exp(-t/R_{SS} \times C_{SS}))$$

where

- Rss = internal resistance of SS pin (60kΩ)
- Css = external Soft-Start capacitor
- VOUT(final) = regulator output set point

The initial Δv / Δt of the output voltage is VOUT(final) / Rss x Css and VOUT will be within 1% of the final regulation level after 4.6 time constants or when t = 4.6 x Rss x Css.

Pull-up current for the error amplifier output is provided by an internal 300µA current source. The PWM threshold signal at the COMP pin can be controlled by either the open drain error amplifier or the open drain current amplifier connected through the CO pin to COMP. Since the internal error amplifier is configured as an open drain output it can be disabled by connecting FB to ground. The current sense amplifier and current limiting function will be described in a later section.

Leading Edge Pulse Width Modulation

Unlike conventional voltage mode controllers, the LM25115 implements leading edge pulse width modulation. A current source equal to 3 times the I_{SYNC} current is used to charge the capacitor connected to the RAMP pin as shown in Figure 13. The ramp signal and the output of the error amplifier (COMP) are combined through a resistor network to produce a voltage ramp with variable dc offset (CRMIX in Figure 13). The high side MOSFET which drives the HS pin is held in the off state at the beginning of the phase signal. When the voltage of CRMIX exceeds the internal threshold voltage CV, the PWM comparator turns on the high side MOSFET. The HS pin rises and the MOSFET delivers current from the main converter phase signal to the output of the auxiliary regulator. The PWM cycle ends when the phase signal falls and power is no longer supplied to the drain of the high side MOSFET.

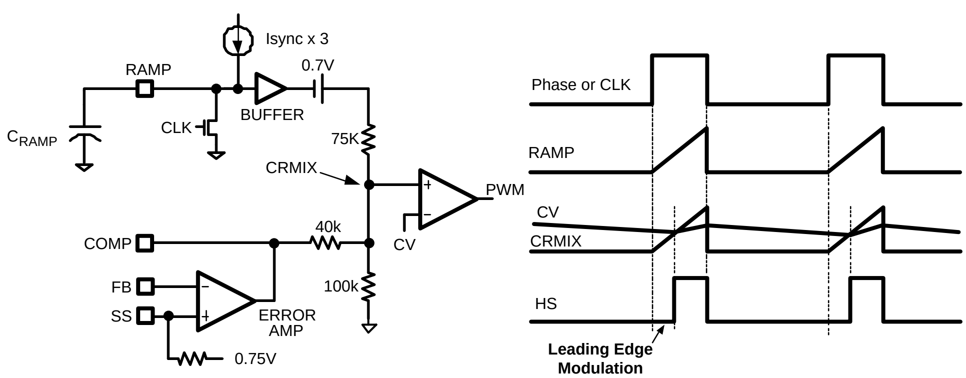


Figure 13. Synchronization and Leading Edge Modulation

Leading edge modulation of the auxiliary PWM controller is required if the main converter is implemented with peak current mode control. If trailing edge modulation were used, the additional load on the transformer secondary from the auxiliary channel would be drawn only during the first portion of the phase signal pulse. Referring to Figure 14, the turn off the high side MOSFET of the auxiliary regulator would create a non-monotonic negative step in the transformer current. This negative current step would produce instability in a peak current mode controller. With leading edge modulation, the additional load presented by the auxiliary regulator on the transformer secondary will be present during the latter portion of the phase signal. This positive step in the phase signal current can be accommodated by a peak current mode controller without instability.

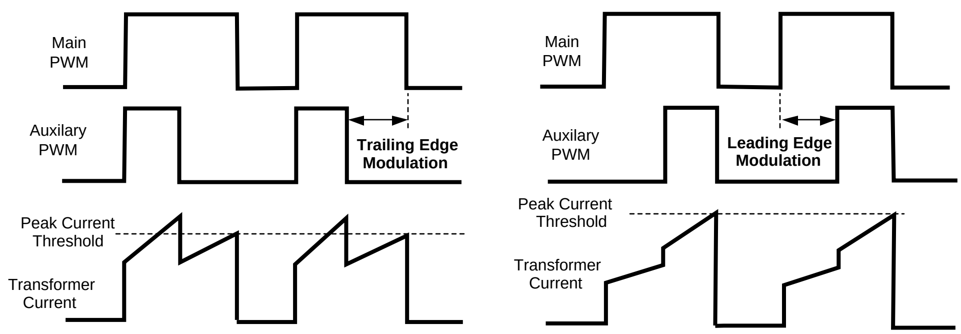


Figure 14. Leading versus Trailing Edge Modulation

Voltage Mode Control with Current Injection

The LM25115 controller uniquely combines elements and benefits of current mode control in a voltage mode PWM controller. The current sense amplifier shown in Figure 15 monitors the inductor current as it flows through a sense resistor connected between CS and VOUT. The voltage gain of the sense amplifier is nominally equal to 16. The current sense output signal is shifted by 1.27V to produce the internal CV reference signal. The CV signal is applied to the negative input of the PWM comparator and compared to CRMIX as illustrated in Figure 13. Thus the PWM threshold of the voltage mode controller (CV) varies with the instantaneous inductor current. Insure that the Vbias voltage is at least 3V above the regulated output voltage (VOUT).

Injecting a signal proportional to the instantaneous inductor current into a voltage mode controller improves the control loop stability and bandwidth. This current injection eliminates the lead R-C lead network in the feedback path that is normally required with voltage mode control (see Figure 16). Eliminating the lead network not only simplifies the compensation, but also reduces sensitivity to output noise that could pass through the lead network to the error amplifier.

The design of the voltage feedback path through the error amp begins with the selection of R1 and R2 in Figure 16 to set the regulated output voltage. The steady state output voltage after soft-start is determined by the following equation:

$$VOUT(final) = 0.75V \times (1+R1/R2)$$

The parallel impedance of the R1, R2 resistor divider should be approximately 2kΩ (between 0.5kΩ and 5kΩ). Lower resistance values may not be properly driven by the error amplifier output and higher feedback resistances can introduce noise sensitivity. The next step in the design process is selection of R3, which sets the ac gain of the error amplifier. The ac gain is given by the following equation and should be set to a value less than 30.

$$GAIN(ac) = R3/(R1 \| R2) < 30$$

The capacitor C1 is connected in series with R3 to increase the dc gain of the voltage regulation loop and improve output voltage accuracy. The corner frequency set by R3 x C1 should be less than 1/10th of the cross-over frequency of the overall converter such that capacitor C1 does not add phase lag at the crossover frequency. Capacitor C2 is added to reduce the noise in the voltage control loop. The value of C2 should be less than 500pF and C2 may not be necessary with very careful PC board layout.

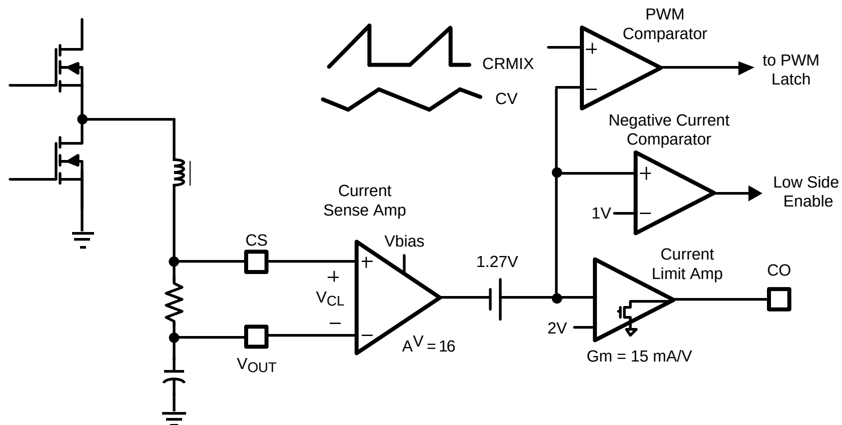


Figure 15. Current Sensing and Limiting

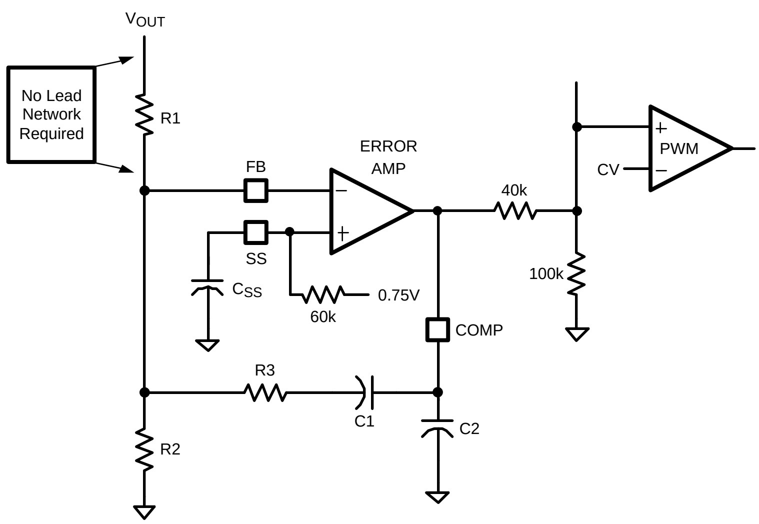


Figure 16. Voltage Sensing and Feedback

Current Limiting (CS, CO and VOUT)

Current limiting is implemented through the current sense amplifier as illustrated in Figure 15. The current sense amplifier monitors the inductor current that flows through a sense resistor connected between CS and VOUT. The voltage gain of the current sense amplifier is nominally equal to 16. The output of current sense amplifier is level shifted by 1.27V to produce the internal CV reference signal. The CV signal drives a current limit amplifier with nominal transconductance of 16mA/V. The current limit amplifier has an open drain (sink only) output stage and its output pin, CO is typically connected to the COMP pin. During normal operation, the voltage error amplifier controls the COMP pin voltage which adjusts the PWM duty cycle by varying the internal CRMIX level (Figure 13). However, when the current sense input voltage V_{CL} exceeds 45mV, the current limit amplifier pulls down on COMP through the CO pin. Pulling COMP low reduces the CRMIX signal below the CV signal level. When CRMIX does not exceed the CV signal, the PWM comparator inhibits output pulses until the CRMIX signal increases to a normal operating level.

A current limit fold-back feature is provided by the LM25115 to reduce the peak output current delivered to a shorted load. When the common mode input voltage to the current sense amplifier (CS and VOUT pins) falls below 2V, the current limit threshold is reduced from the normal level. At common mode voltages > 2V, the current limit threshold is nominally 45mV. When VOUT is reduced to 0V the current limit threshold drops to 36mV to reduce stress on the inductor and power MOSFETs.

Negative Current Limit

When inductor current flows from the regulator output through the low side MOSFET, the input to the current sense comparator becomes negative. The intent of the negative current comparator is to protect the low-side MOSFET from excessive currents. Negative current can lead to large negative voltage spikes on the output at turn off which can damage circuitry powered by the output. The negative current comparator threshold is sufficiently negative to allow inductor current to reverse at no load or light load conditions. It is not intended to support discontinuous conduction mode with diode emulation by the low-side MOSFET. The negative current comparator illustrated in Figure 15 monitors the CV signal and compares this signal to a fixed 1V threshold. This corresponds to a negative V_{CL} voltage between CS and VOUT of -17mV. The negative current limit comparator turns off the low-side MOSFET for the remainder of the cycle when the V_{CL} input falls below this threshold.

Gate Drivers Outputs (HO & LO)

The LM25115 provides two gate driver outputs, the floating high-side gate driver HO and the synchronous rectifier low-side driver LO. The low-side driver is powered directly by the VCC regulator. The high-side gate driver is powered from a bootstrap capacitor connected between HB and HS. An external diode connected between VCC and HB charges the bootstrap capacitor when the HS is low. When the high-side MOSFET is turned on, HB rises with HS to a peak voltage equal to VCC + V_{HS} - V_D where V_D is the forward drop of the external bootstrap diode. Both output drivers have adaptive dead-time control to avoid shoot through currents. The adaptive dead-time control circuit monitors the state of each driver to ensure that the opposing MOSFET is turned off before the other is turned on. The HB and VCC capacitors should be placed close to the pins of the LM25115 to minimize voltage transients due to parasitic inductances and the high peak output currents of the drivers. The recommended range of the HB capacitor is 0.047µF to 0.22µF.

Both drivers are controlled by the PWM logic signal from the PWM latch. When the phase signal is low, the outputs are held in the reset state with the low-side MOSFET on and the high-side MOSFET off. When the phase signal switches to the high state, the PWM latch reset signal is de-asserted. The high-side MOSFET remains off until the PWM latch is set by the PWM comparator (CRMIX > CV as shown in Figure 13). When the PWM latch is set, the LO driver turns off the low-side MOSFET and the HO driver turns on the high-side MOSFET. The high-side pulse is terminated when the phase signal falls and the SYNC input comparator resets the PWM latch.

Free-Run Mode

The LM25115 can be operated as a conventional synchronous buck controller with a dc input supply instead of the square wave phase signal. In the dc or free-run mode, the LM25115 PWM controller synchronizes to an internal clock signal instead of the phase signal pulses. The clock frequency in the free-run mode is programmed by the SYNC pin resistor and RAMP pin capacitor. Connecting a resistor between a dc bias supply and the SYNC pin produces a current I_{SYNC} which controls the charging current of the RAMP pin capacitor . The RAMP capacitor is charged until its voltage reaches the free-run mode peak threshold of 2.25V. The RAMP capacitor is then discharged for 300ns before beginning a new PWM cycle. The 300ns reset time of the RAMP pin sets the minimum off time of the PWM controller in the free-run mode. The internal clock frequency in the free-run mode is set by the synchronization current, ramp capacitor, free-run peak threshold, and 300ns deadtime.

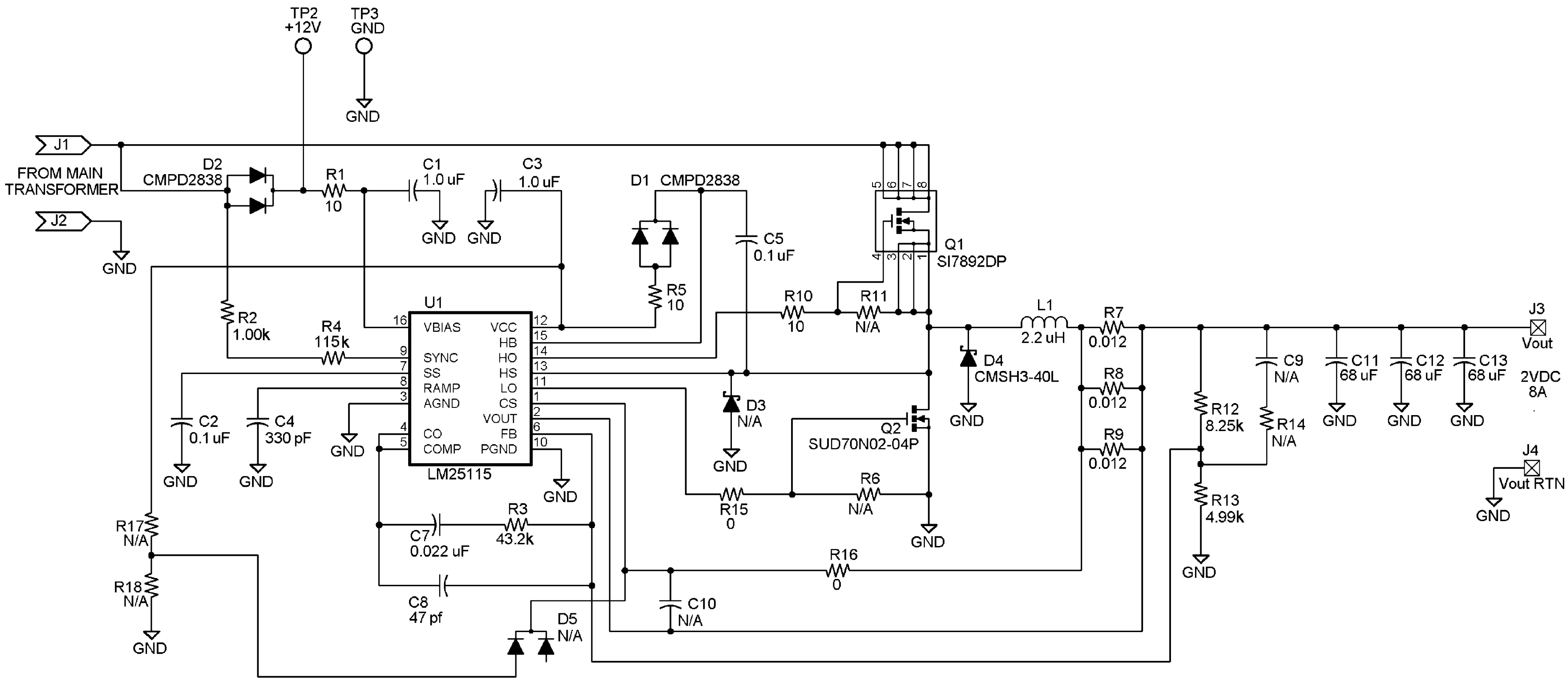
$$F_{CLK} \approxeq 1 / ((C_{RAMP} \text{ x } 2.25V) / (I_{SYNC} \text{ x } 3) + 300ns)$$

Note that the VCC supply can be used as the dc bias to produce I_{SYNC}. Note that the input voltage feedforward is no longer functional in this operating mode, so the loop gain will vary as a function of Vin. The LM25115 controls the buck power stage with leading edge pulse width modulaton to hold off the high-side driver until the necessary volt*seconds is established for regulation. Other features described for the secondary side post regulator apply in the free run mode operation. They include voltage mode control with current injection, positive and negative current limit, programmable soft-start, adaptive delays for outputs, and thermal protection.

Thermal Protection

Internal thermal shutdown circuitry is provided to protect the integrated circuit in the event the maximum junction temperature limit is exceeded. When activated, typically at 165 degrees Celsius, the controller is forced into a low power standby state with the output drivers and the bias regulator disabled. The device will restart when the junction temperature falls below the thermal shutdown hysteresis, which is typically 25 degrees. The thermal protection feature is provided to prevent catastrophic failures from accidental device overheating.

Application Circuit



(Inputs from LM5025 Forward Active Clamp Converter, 36V to 78V)

Figure 17. LM25115 Secondary Side Post Regulator

REVISION HISTORY

Changes from Original (March 2013) to Revision A	Page
• Changed layout of National Data Sheet to TI format	14

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LM25115MT/NOPB	ACTIVE	TSSOP	PW	16	92	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 125	L25115 MT	Samples
LM25115SDX/NOPB	ACTIVE	WSON	NHQ	16	4500	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 125	L25115	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

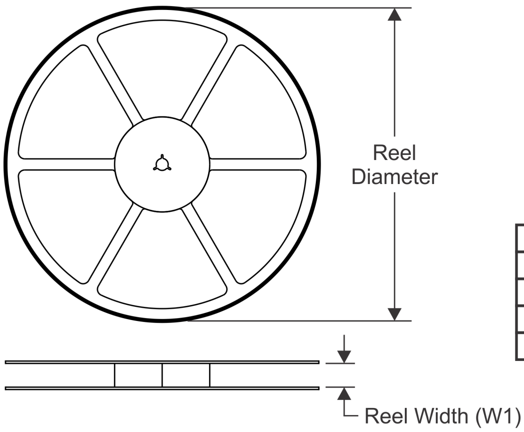
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

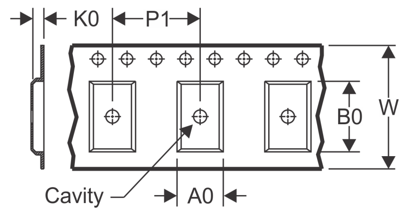
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

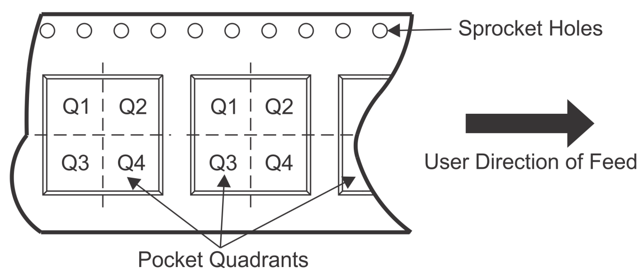


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

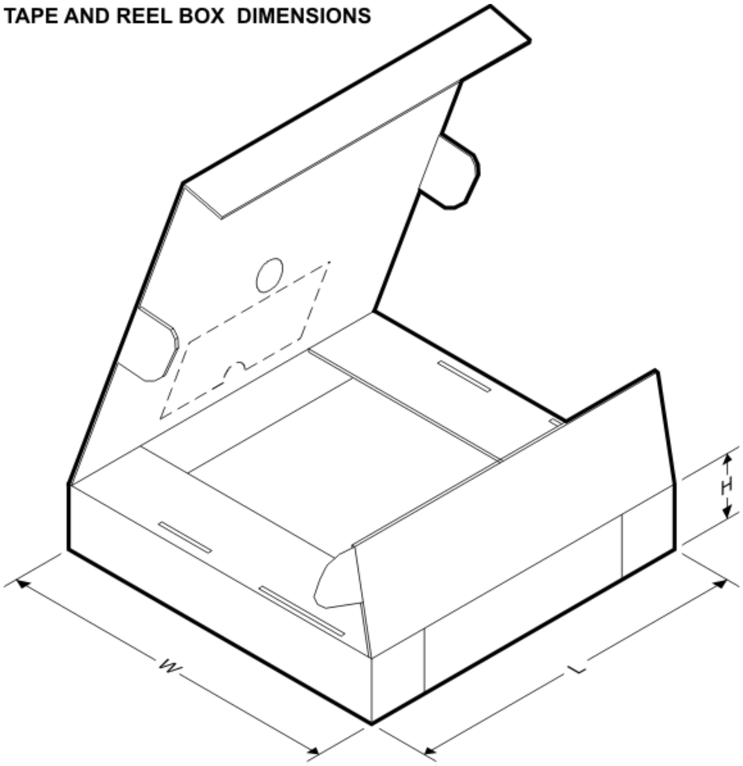
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LM25115SDX/NOPB	WSON	NHQ	16	4500	330.0	12.4	5.3	5.3	1.3	8.0	12.0	Q1

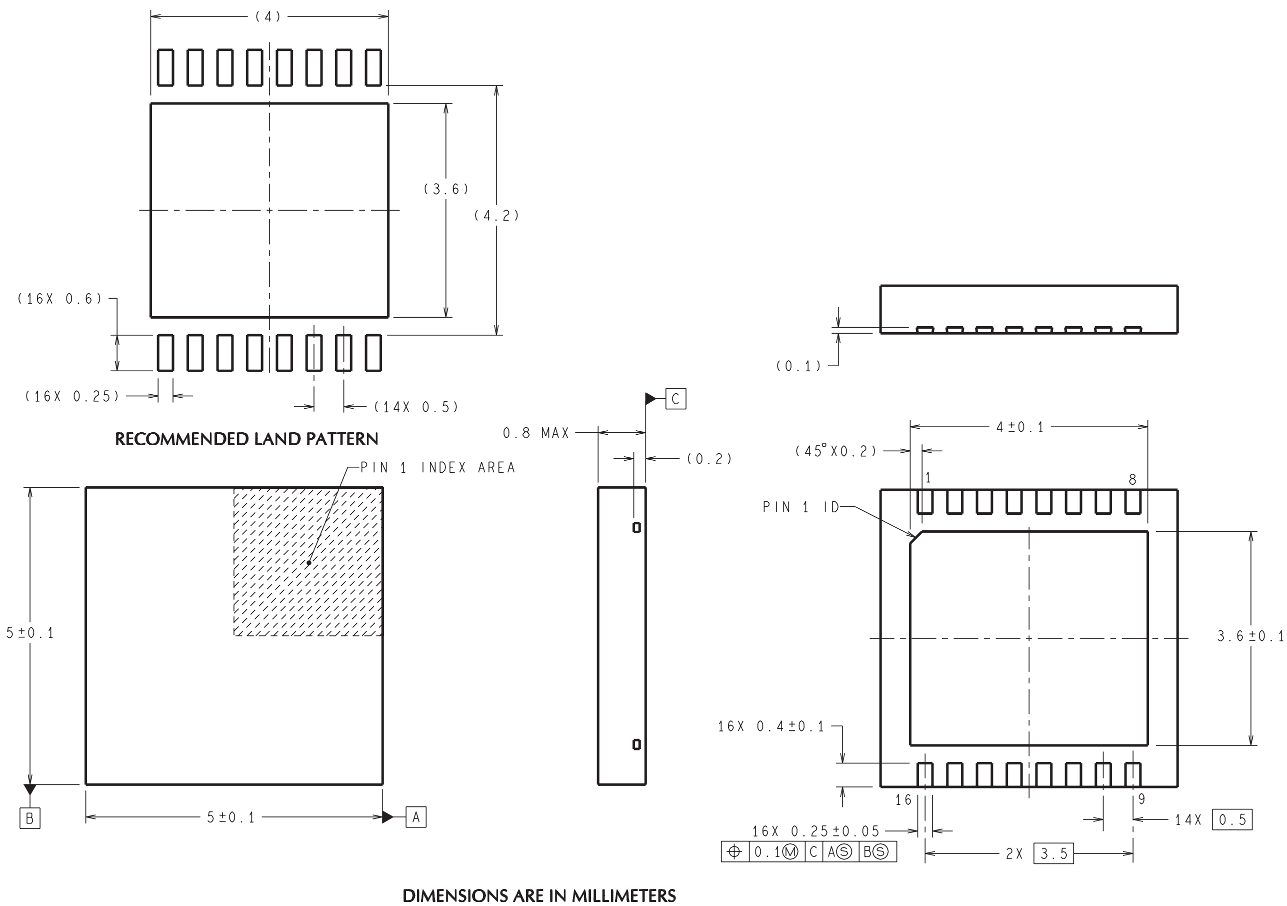
TAPE AND REEL BOX DIMENSIONS



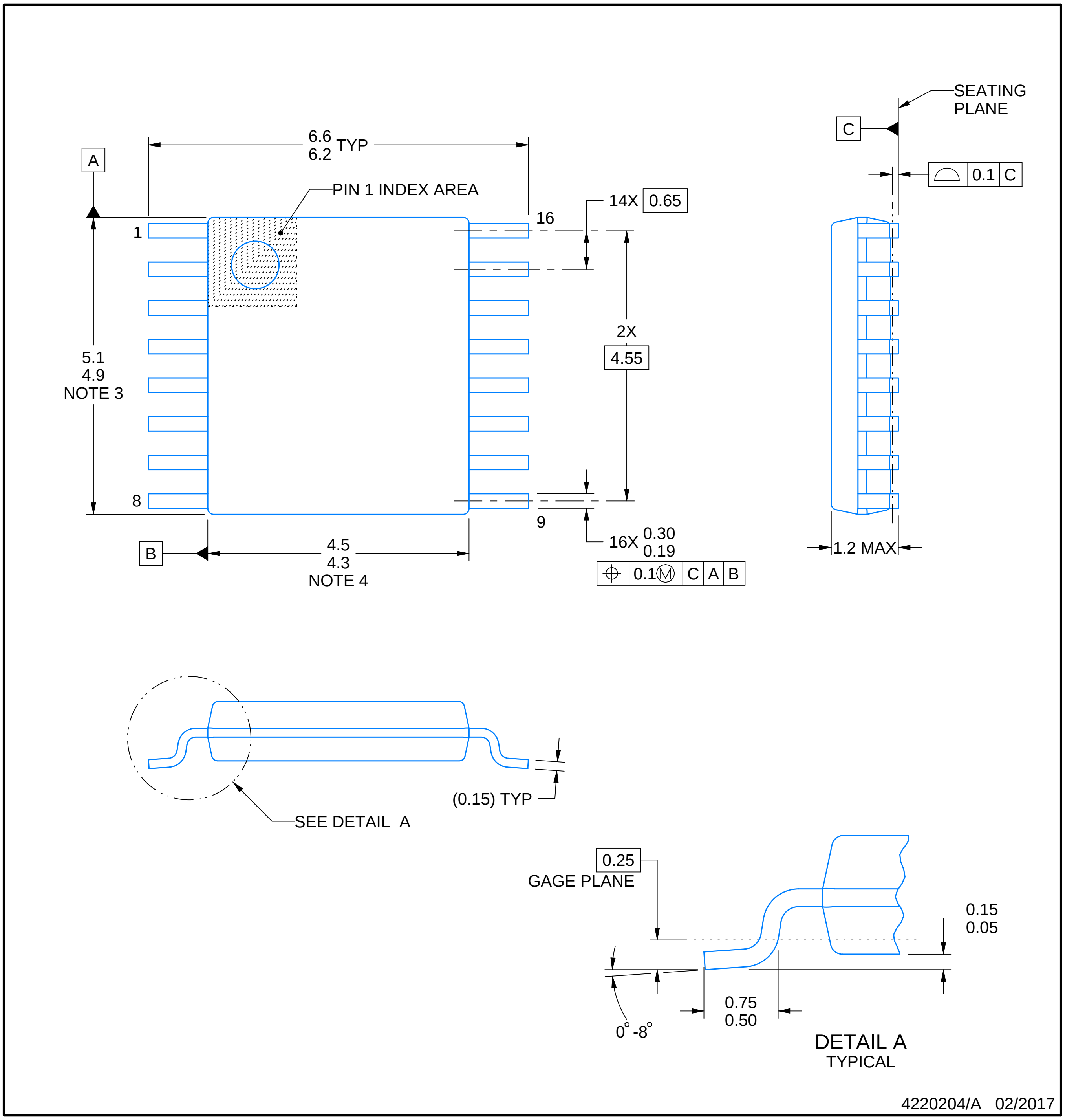
*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LM25115SDX/NOPB	WSON	NHQ	16	4500	367.0	367.0	35.0

NHQ0016A

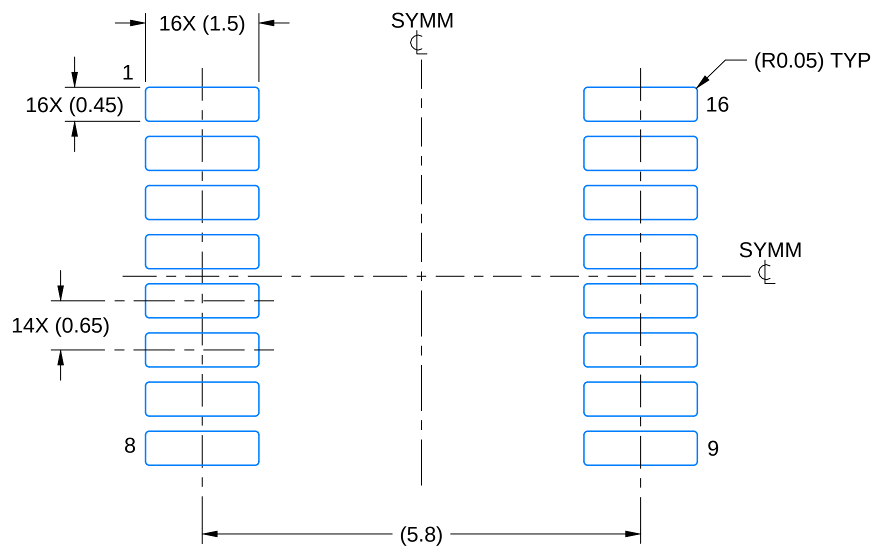


SDA16A (Rev A)

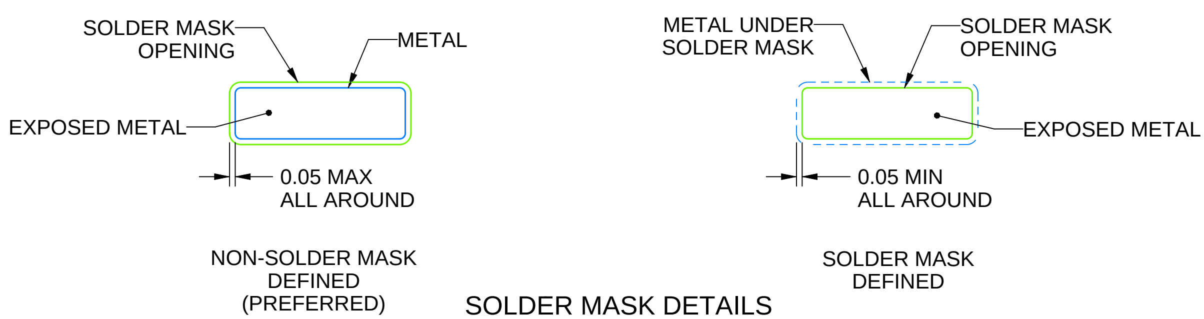


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X

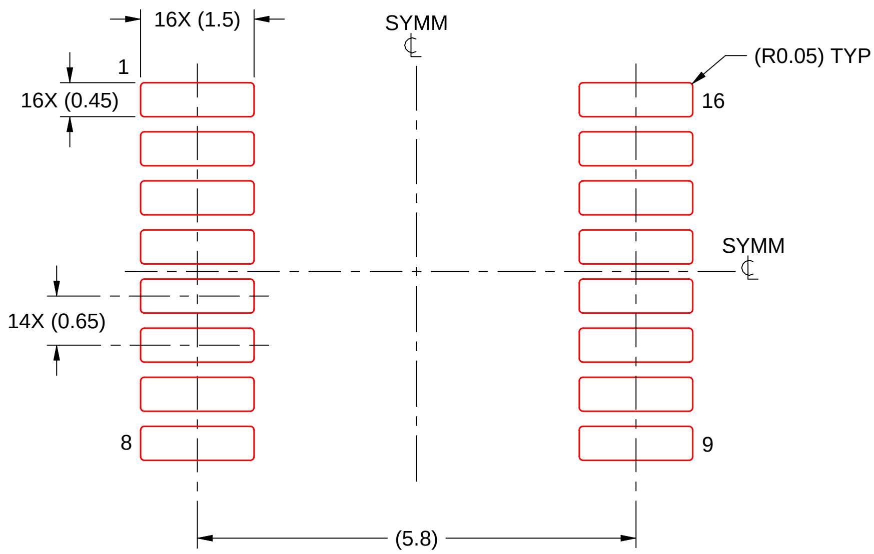


SOLDER MASK DETAILS

4220204/A 02/2017

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220204/A 02/2017

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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