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LM2507
Low Power Mobile Pixel Link (MPL) Level 0, 16-bit CPU Display interface Serializer and Deserializer

General Description

The LM2507 device adapts i80 CPU style display interfaces to the Mobile Pixel Link (MPL) Level zero serial link. When using smart CPU type interfaces, two chip selects support a main and sub display. A mode pin configures the device as a Master (MST) or Slave (SLV) so the same chip can be used on both sides of the interface.

The interconnect is reduced from 21 signals to only 3 active signals with the LM2507 chipset easing flex interconnect design, size constraints and cost.

The LM2507 in MST mode resides beside an application, graphics or baseband processor and translates a parallel bus from LVCMOS levels to serial Mobile Pixel Link levels for transmission over a flex cable (or coax) and PCB traces to the SLV located near the display module(s).

When the Power_Down (PD*) input is asserted on the Master, the MDn and MC line drivers are powered down to save current. The Slave is controlled by a separate Power_Down input.

The LM2507 implements the physical layer of the MPL Level 0 Standard (MPL-0) and a 150 µA I_B current (Class 0).

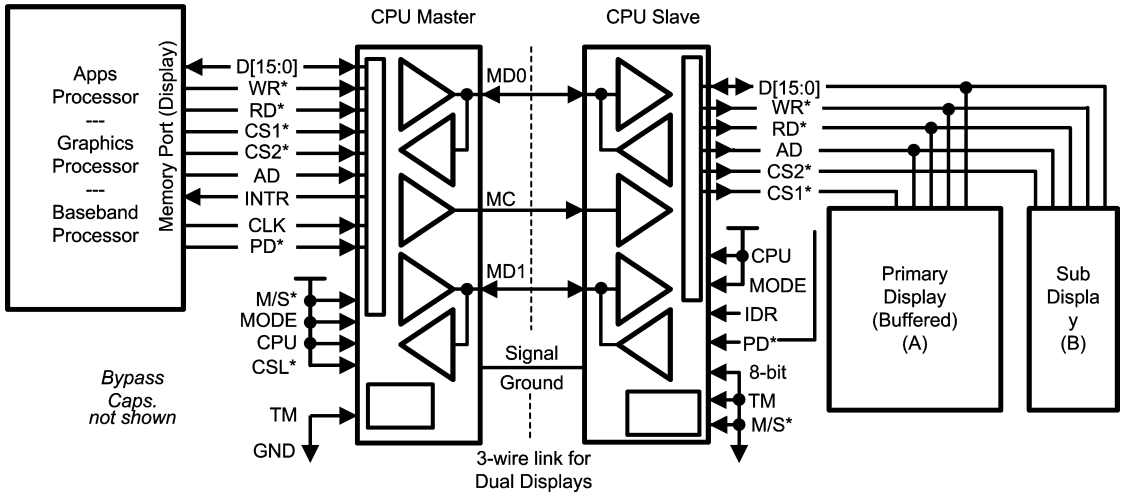
Features

- CPU Display Interface support up to 800 x 300 ½SVGA formats
- Dual displays supported – CS1* & CS2*
- MPL-Level 0 Physical Layer using two data and one clock signal
- Low Power Consumption
- Pinout mirroring enables straight through layout with minimal vias
- Level translation between host and display
- Link power down mode reduces quiescent power under < 10 µA
- 1.74V to 2.0V core / analog supply voltage range
- 1.74V to 3.0V I/O supply voltage range

System Benefits

- Small Interface
- Low Power
- Low EMI
- Intrinsic Level Translation

Typical Application Diagram - CPU Mode



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Pin Descriptions — CPU

Pin Name	No. of Pins	I/O, Type	Description	
			CPU Master (MST)	CPU Slave (SLV)
MPL SERIAL BUS PINS				
MD[1:0]	2	IO, MPL	MPL Data Line Driver/Receiver	MPL Data Receiver/Line Driver
MC	1	IO, MPL	MPL Clock Line Driver	MPL Clock Receiver
V_{SSA}		Ground	MPL Ground - see Power/Ground Pins	
CONFIGURATION/PARALLEL BUS PINS				
CPU	1	I, LVCMOS	CPU mode configuration input **Tie High**	
M/S*	1	I, LVCMOS	Tie High for Master	Tie Low for Slave
TM	1	I, LVCMOS	Test Mode control input **Tie Low for normal mode** (High reserved for factory test)	
Mode	1	I, LVCMOS	CPU Mode input **Tie High for i80 mode**	
CSL*/IDR	1	I, LVCMOS	Local Chip Select input, Reserved - **Tie High.**	Insert Dummy Read control input, H = inserts dummy read cycle in all READ transactions L = uses one READ cycle for every READ transaction
CLOCK / POWER DOWN SIGNALS				
CLK	1	I, LVCMOS	CLK input	NA
PD*	1	I, LVCMOS	Power Down input, L = Powered down (sleep mode) H = active mode	
PARALLEL INTERFACE SIGNALS				
D[15:0]	16	IO, LVCMOS	CPU Data Bus inputs / outputs	CPU Data Bus outputs / inputs
MF0 (RD*)	1	IO, LVCMOS	Multi Function input - Read input (RD*) for i80 I/F	Multi Function output - Read output (RD*) for i80 I/F
MF1 (WR*)	1	IO, LVCMOS	Multi Function input - Write input (WR*) for i80 I/F	Multi Function output - Write output (WR*) for i80 I/F
CS1*	1	IO, LVCMOS	Chip Select One input Active Low	Chip Select One output Active Low
CS2*	1	IO, LVCMOS	Chip Select Two input Active Low	Chip Select Two output Active Low
A/D	1	IO, LVCMOS	Address / Data selector input	Address / Data selector output
INTR/8-bit	1	IO, LVCMOS	Interrupt Output Active High, is asserted when READ data is ready and de-asserted upon send READ cycle **OPTIONAL**	8-bit Mode Input **Tie Low for 16-bit mode** 8-bit mode is reserved.

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Pin Descriptions — CPU (Continued)

Pin Name	No. of Pins	I/O, Type	Description	
			CPU Master (MST)	CPU Slave (SLV)
POWER/GROUND PINS				
V_{DDA}	1	Power	Power Supply Pin for the MST PLL and MPL Interface. 1.74V to 2.0V	
V_{SSA}	1	Ground	Ground Pin for the MPL Interface, and analog circuitry.	
V_{DDcore}	1	Power	Power Supply Pin for the digital core. 1.74V to 2.0V	
V_{SScore}	1	Ground	Ground Pin for the digital core.	
V_{DDIO}	2	Power	Power Supply Pin for the parallel interface I/Os. 1.74V to 3.0V	
V_{SSIO}	2	Ground	Ground Pin for the parallel interface I/Os.	
V_{bulk}	9		Connect to Ground - uArray Package	
DAP	1		Connect to Ground - LLP Package	

Note:
I = Input, O = Output, IO = Input/Output. **Do not float input pins.**

Ordering Information

NSID	Package Type	Package ID
LM2507GR	49L MicroArray, 4.0 X 4.0 X 1.0 mm, 0.5 mm pitch	GRA49A
LM2507SQ	40L LLP, 5.0 X 5.0 X 0.8 mm, 0.4 mm pitch	SQF40A

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Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Supply Voltage (V_{DDA})	−0.3V to +2.2V
Supply Voltage (V_{DD})	−0.3V to +2.2V
Supply Voltage (V_{DDIO})	−0.3V to +3.6V
LVCMOS Input/Output Voltage	−0.3V to (V_{DDIO} +0.3V)
MPL Input/Output Voltage	−0.3V to V_{DDA}
Junction Temperature	+150˚C
Storage Temperature	−65˚C to +150˚C
Lead Temperature Soldering, 40 Seconds	+260˚C
ESD Ratings:	
HBM, 1.5 kΩ, 100 pF	≥±2 kV
EIAJ, 0Ω, 200 pF	≥±200V
Maximum Package Power Dissipation Capacity at 25˚C	
GRA Package	1.8W
Derate GRA Package above 25˚C	15mW/˚C
SQF Package	1.8W
Derate SQF Package above 25˚C	15mW/˚C

Recommended Operating Conditions

	Min	Typ	Max	Units
Supply Voltage				
V_{DDA} to V_{SSA} and V_{DDcore} to V_{SScore}	1.74	1.8	2.0	V
V_{DDIO} to V_{SSIO}	1.74		3.0	V
Clock Frequency	3		20	MHz
Ambient Temperature	−30	25	85	˚C

Electrical Characteristics

Over recommended operating supply and temperature ranges unless otherwise specified. (Notes 2, 3)

Symbol	Parameter	Conditions		Min	Typ	Max	Units
MPL							
I_{OLL}	Logic Low Current (5X I_B)			3.67 I_B	5.0 I_B	6.33 I_B	µA
I_{OMS}	Mid Scale Current (Notes 4, 9)			2.1I_B	3.0 I_B	3.9I_B	µA
I_{OLH}	Logic High Current (1X I_B)			0.7 I_B	1.0 I_B	1.4 I_B	µA
I_B	Current Bias				150		µA
I_{OFF}	MPL Leakage Current	V_{MPL} = 0.8V		−2		+2	µA
LVCMOS (1.74V to 3.0V Operation)							
V_{IH}	Input Voltage High Level			0.7 V_{DDIO}		V_{DDIO}	V
V_{IL}	Input Voltage Low Level			GND		0.3 V_{DDIO}	V
V_{HY}	Input Hysteresis	V_{DDIO} = 1.74V			150		mV
		V_{DDIO} = 3.0V			200		mV
I_{IH}	Input Current High Level	Includes I_{OZ}	Vin = V_{DDIO}	−1	0	+1	µA
I_{IL}	Input Current Low Level		Vin = GND	−1	0	+1	µA
V_{OH}	Output Voltage High Level	I_{OH} = −2 mA		0.75 V_{DDIO}		V_{DDIO}	V
V_{OL}	Output Voltage Low Level	I_{OL} = 2 mA		V_{SSIO}		0.2 V_{DDIO}	V
SUPPLY CURRENT							
I_{DD}	Total Supply Current — Enabled Conditions: MC = 80 MHz, MD = 160 Mbps (Note 5) AAAA/5555	Master	V_{DDIO}		0.02	0.07	mA
			V_{DD}/V_{DDA}		5	11	mA
		Slave	V_{DDIO}		4	10	mA
			V_{DD}/V_{DDA}		6	11	mA

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Electrical Characteristics (Continued)

Over recommended operating supply and temperature ranges unless otherwise specified. (Notes 2, 3)

Symbol	Parameter	Conditions		Min	Typ	Max	Units
SUPPLY CURRENT							
I_{DDZ}	Supply Current—Disable T_A = 25˚C Power Down Modes	MST PD* = L	V_{DDIO}		<1	2	µA
			V_{DD}/V_{DDA}		<1	2.2	µA
		SLV PD* = L	V_{DDIO}		<1	2	µA
			V_{DD}/V_{DDA}		<1	2.2	µA

Switching Characteristics

Over recommended operating supply and temperature ranges unless otherwise specified. (Note 2)

Symbol	Parameter	Conditions		Min	Typ	Max	Units
PARALLEL BUS TIMING See							
t_{SET}	Set Up Time			5			ns
t_{HOLD}	Hold Time			5			ns
t_{RISE}	Rise Time	Edge sensitive outputs only, (Note 6) C_L = 15 pF, *Figure 2*	V_{DDIO} = 1.74V		7	15.5	ns
			V_{DDIO} = 3.0V		3	6.5	ns
t_{FALL}	Fall Time		V_{DDIO} = 1.74V		7	15.5	ns
			V_{DDIO} = 3.0V		2	6	ns
SERIAL BUS TIMING							
t_{DVBC}	Serial Data Valid before Clock (Set Time)	SLV Input *Figure 1*	MC = 80MHz (Note 9)	1.5			ns
t_{DVAC}	Serial Data Valid after Clock (Hold Time)			1.5			ns
POWER UP TIMING							
t_0	MST PLL Lock Counter				4,096		CLK cycles
t_1	MC Pulse Width Low				180		MC cycles
t_2	MC Pulse Width High				180		MC cycles
t_3	MC H-L to Idle State				180		MC cycles
MPL POWER OFF TIMING							
t_{PAZ}	Disable Time to Power Down	(Note 8)				2	ms

Recommended Input Timing Requirements

Over recommended operating supply and temperature ranges unless otherwise specified. (Note 2)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
MASTER REFERENCE CLOCK (CLK)						
f	Clock Frequency		3		20	MHz
t_{CP}	Clock Period		50		333	ns
CLK_{DC}	Clock Duty Cycle		30	50	70	%
t_T	Clock/Data Transition Times (Rise or Fall, 10%–90%)	(Note 7)	2			ns

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Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the device should be operated at these limits. The tables of "Electrical Characteristics" specify conditions for device operation.

Note 2: Typical values are given for V_{DDIO} = 1.8V and V_{DD} = V_{DDA} = 1.8V and T_A = 25˚C.

Note 3: Current into a device pin is defined as positive. Current out of device pins is defined as negative. Voltages are referenced to Ground unless otherwise specified.

Note 4: MPL Current Threshold is set to be $3XI_B$ by the MPL start up Sequence - this is a functional specification only.

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Recommended Input Timing Requirements (Continued)

Note 5: Total Supply Current Conditions: CPU Mode, worse case data pattern, 19.2MHz CLK, DES C_L = 15pF, TYP – V_{DDIO} = V_{DDA} = V_{DDcore} = 1.8V, MAX – V_{DDIO} = 3.0V and V_{DDA} = V_{DDcore} = 2.0V.

Note 6: Applies to WR* and RD* outputs only..

Note 7: Maximum transition time is a function of clock rate and should be less than 30% of the clock period to preserve signal quality.

Note 8: Guaranteed functionally by the I_{DDZ} parameter. See also *Figure 7*.

Note 9: This is a functional parameter and is guaranteed by design or characterization.

Timing Diagrams

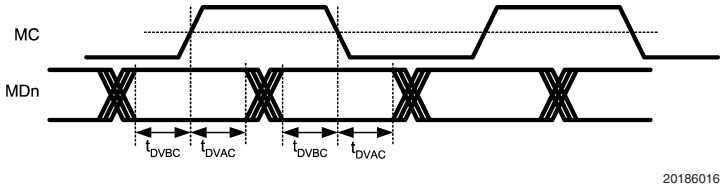

FIGURE 1. Serial Data Valid — SLV Input Set and Hold Time

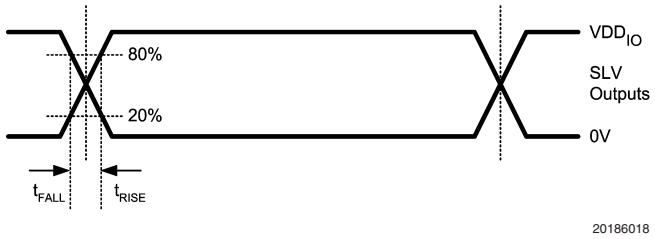

FIGURE 2. SLV Output Rise and Fall Time

Functional Description

BUS OVERVIEW

The LM2507 is a dual link MST/SLV configurable part that supports a 8, 9 or 16-bit CPU (i80 style) interface. The MPL physical layer is purpose-built for an extremely low power and low EMI data transmission while requiring the fewest number of signal lines. No external line components are required, as termination is provided internal to the MPL receiver. A maximum raw throughput of 320 Mbps (raw) is possible with this chipset. When the protocol overhead is taken into account, a maximum data throughput of 240 Mbps is possible. The MPL interface is designed for use with common 50Ω to 100Ω lines using standard materials and connectors. Lines may be microstrip or stripline construction. Total length of the interconnect is expected to be less than 20cm.

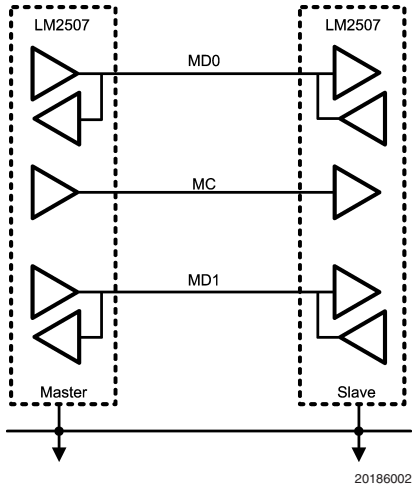

FIGURE 3. MPL Point-to-Point Bus

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SERIAL BUS TIMING

Data valid is relative to both edges for a CPU WRITE as shown in *Figure 4*. Data valid is specified as: Data Valid before Clock, Data Valid after Clock, and Skew between data lines should be less than 500ps.

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Functional Description (Continued)

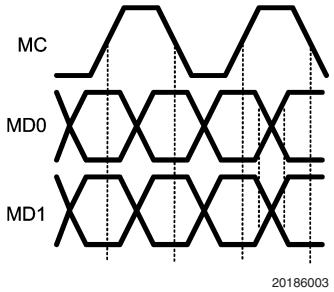

FIGURE 4. Dual Link Timing (WRITE)

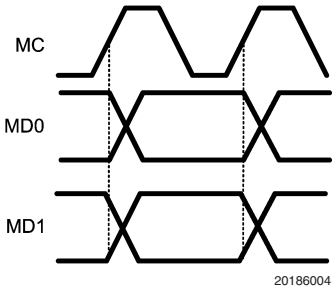

FIGURE 5. Dual Link Timing (READ)

Data is strobed out on the rising edge by the Slave for a CPU READ as shown in *Figure 5*. The Master monitors for the start bit transition (High to Low) and selects the best strobe to sample the incoming data on. This is done to account for the round trip delay of the interconnect and application data rate.

SERIAL BUS PHASES

There are four bus phases on the MPL serial bus. These are determined by the state of the MC and MD lines. The MPL bus phases are shown in *Table 1*.

The LM2507 supports MPL Level 0 Enhanced Protocol with a Class 0 PHY.

TABLE 1. Link Phases

Name		MC State	MDn State	Phase Description	Pre-Phase	Post-Phase
OFF (O)		0	0	Link is Off	A, I or LU	LU
IDLE (I)		A	H	Data is Static (High)	A or LU	A or O
ACTIVE(A)	Data Out WRITE	A	X	Data Out (Write) — includes command, Data Out Phases	LU, A, or I	A, I, or O
	Data In READ	A	X	Data In (Read) — includes command, TA', Data In, and TA" phases	LU, A, or I	A, I, or O
LINK-UP (LU)		H	-	Master initiated Link-Up	O	A, I, or O

Notes on MC/MD Line State:
0 = no current (off)
L = Logic Low — The higher level of current on the MC and MD lines
H = Logic High — The lower level of current on the MC and MD lines
X = Low or High
A = Active Clock

SERIAL BUS START UP TIMING

In the Serial Bus OFF phase, Master transmitters for MD0, MD1 and MC are turned off such that zero current flows over the MPL lines. In addition, both the Master and the Slave are internally held in a low power state. When the PD* input pins are de-asserted (driven High) the Master enables its PLL and waits for enough time to pass for its PLL to lock. After the Master's PLL is locked (t0 = 4,096 CLK Cycles), the Master will perform an MPL start up sequence. The Slave will also power up and await the start up sequence from the Master.

The MPL start up sequence gives the Slave an opportunity to optimize the current sources in its transceiver to maximize noise margins. The Master begins the sequence by driving the MC line logically Low for 180 MC cycles (t1). At this point, the Slave's transceiver samples the MC current flow and adjusts itself to interpret that amount of current as a logical Low. Next the Master drives the MC line logically HIGH for 180 MC cycles (t2). The optimized current configuration is held as long as the MPL remains active. Next, the Master drives both the MC and the MD lines to a logical Low for another 180 MC cycles (t3), after which it begins to toggle the MC line at a rate determined by its PLL setting. The Master will continue to toggle the MC line as long as its PD* pin remains de-asserted (High). At this point the MPL bus may remain in IDLE phase, enter the ACTIVE phase or return to the OFF phase. Active data will occur at the Slave output latency delays (Master + line + Slave) after the data is applied to the Master input. A possible start point is shown by the "C" in *Figure 6*.

In the *Figure 6* example, an IDLE bus phase is shown until point C, after which the bus is active and the High start bit on MD initiates the transfer of information.

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Functional Description (Continued)

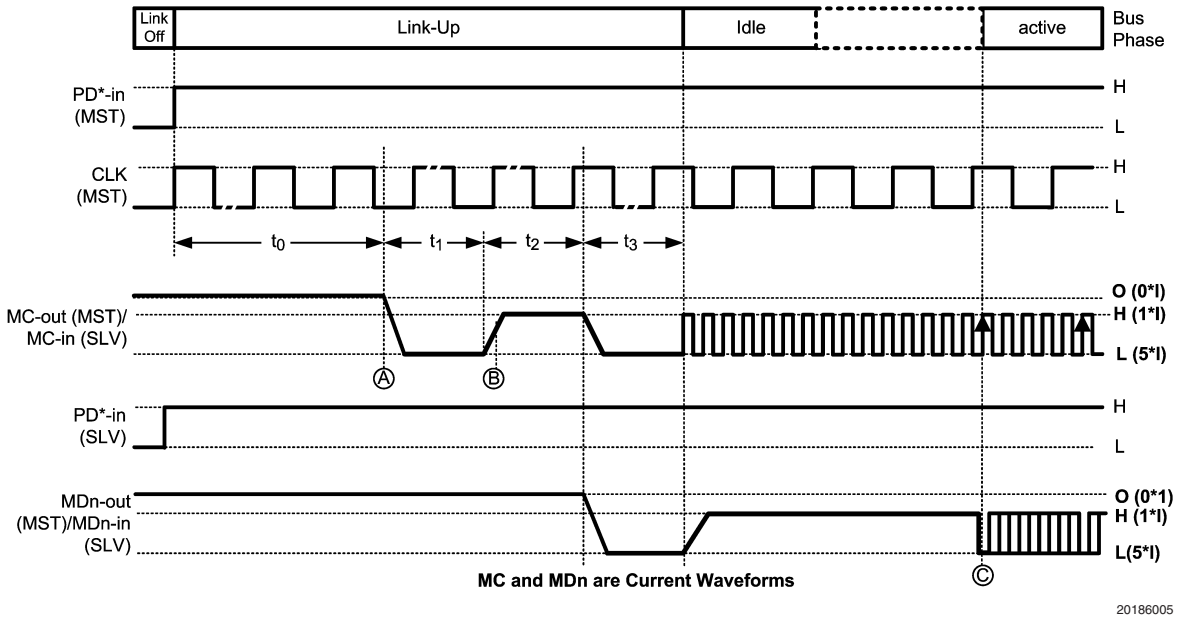

FIGURE 6. Bus Power Up Timing

OFF PHASE

In the OFF phase, both Master and Slave MPL transmitters are turned off with zero current flowing on the MC and MDn lines. *Figure 7* shows the transition of the MPL bus into the OFF phase. If an MPL line is driven to a logical Low (high current) when the OFF phase is entered it may temporarily pass through as a logical High (low current) before reaching the zero line current state.

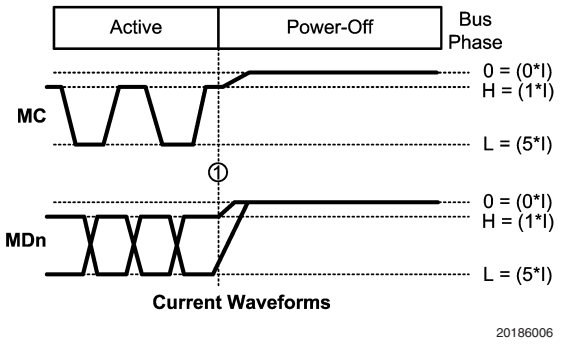

FIGURE 7. Bus Power Down Timing

The link may be powered down by asserting both the Master's and Slave's PD* input pins (Low). This causes the devices to immediately put the link to the OFF Phase and internally enter a low power state. To avoid loss of data the Master's PD* input should only be asserted after the MPL bus has been in the IDLE state for at least 20 MC clock cycles. This gives the Slave enough time to complete any write operations received from the MPL bus.

CPU INTERFACE COMPATIBILITY

The CPU i80 Interface provides compatibility between a CPU Interface host and a small form factor (SFF) Display or other fixed I/O port application.

WRITE TRANSACTION

The WRITE transaction consists of one MC cycle of control information followed by four MC cycles of write data for a 16-bit WRITE. Since WRITE transactions transfer information on both edges of MC it takes five MC cycles to complete a write transaction. The MD0 line carries the Start bit (Low), the A/D (Address/Data) bit and then the data payload of 8 bits (D0-7). The MD1 line carries the R/W* bit (Read/Write*), the CS1/2 bit and then the data payload of 8 bits (D8-15). The data payload is sent least significant bit (LSB) first. The CS1/2 bit denotes which Chipset pin was active. CS1/2 = HIGH designates that CS1* is active (Low). CS1/2 = LOW designates that CS2* is active (Low). CS1* and CS2* LOW is not allowed.

8-bit and 9-bit CPU bus widths may be supported by tieing off unused inputs.

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Functional Description (Continued)

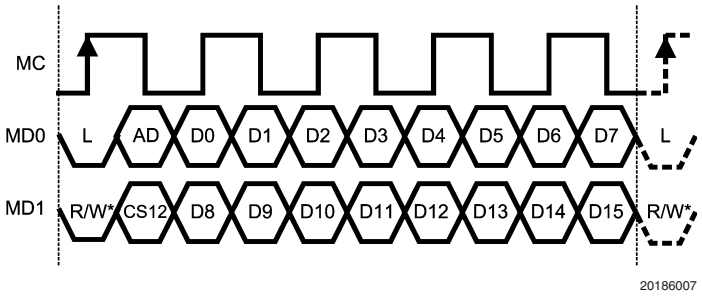

FIGURE 8. 16-bit CPU WRITE Transaction

READ TRANSACTION

The READ transaction is fixed in length. It consists of four sections.

In the first section the Master sends a READ Command to the slave. This command is sent in a single MC cycle (2 edges) and uses a similar format to the 1st cycle of the WRITE transaction. The MD0 line carries the Start bit (Low) and the A/D (Address/Data) bit. The MD1 line carries the R/W* bit (High for reads) and the CS1/2 bit.

The Slave has an optional feature selected by the IDR pin. If IDR is pulled high, as soon as the READ Command is detected by the Slave, it issues two reads to the peripheral device. If IDR is pulled low, the Slave only issues one read. This feature allows a common behavior from the host side regardless of whether the MPL link is used. Since the Master mode device requires a dummy READ (which returns all zeros) to initiate the remote side read, and then another READ after the INTR signal is received, the remote side can be programmed to behave in exactly the same way. Common driver software can be created that would be transparent to the use of the MPL link.

In the second section (TA') the MD lines are turned around, such that the Master becomes the receiver and Slave becomes the transmitter. The Slave must drive the MD lines High by the 14th clock edge. It may then idle the line at the Logic High state or drive the line Low (Start bit) to indicate that read data transmission is starting. This ensures that the MD lines are a stable High state and that the High-to-Low transition of the "Start" bit is seen by the Master.

Figure 9 illustrates a READ_Command and TA' with IDR (Insert Dummy Read) = L. If the IDR = H, then the Bus undetermined state is longer (10 additional MC cycles) to allow for the dummy read cycle on the Slave output to occur.

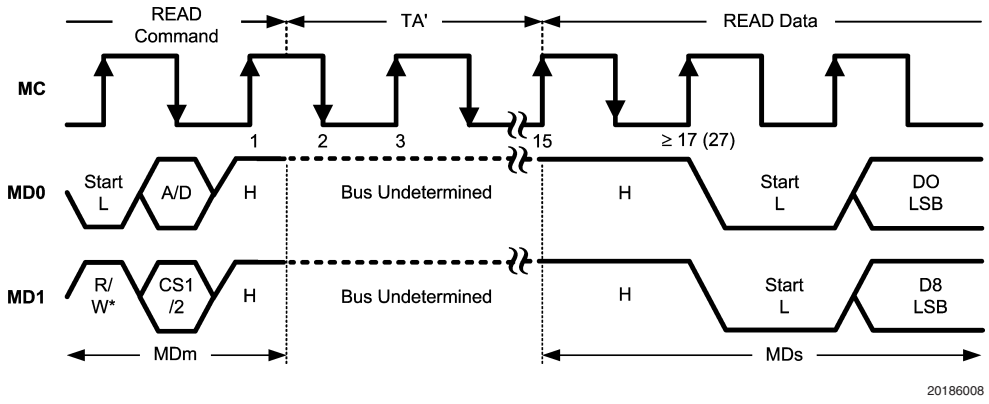

FIGURE 9. READ_Command and TA'

The third section is consists of the transfer of the read data from the Slave to the Master. Note that the READ_Data operates on single-edge clocking (Rising Edge ONLY). Therefore the back channel data signaling rate is ½ of the forward channel (Master-to-Slave direction). When the Slave is ready to transmit data back to the Master it drives the MD lines Low to indicate start of read data, followed by 8 MC cycles of the actual read data payload.

The fourth and final section (TA") occurs after the read data has been transferred from the Slave to the Master. In the fourth section the MD lines are again turned around, such that the Master becomes the transmitter and the Slave becomes the receiver. The Slave drives the MD lines High for 1 bit and then turns off. The MD lines are off momentarily to avoid driver contention. The Master then drives the MD line High for 1 bit time and then idles the bus until the next transaction is sent.

The Master watches the MD line for the READ Start Bit. When this transition (High to Low) is detected it then selects the proper strobe to clock in the data with maximum margin.

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Functional Description (Continued)

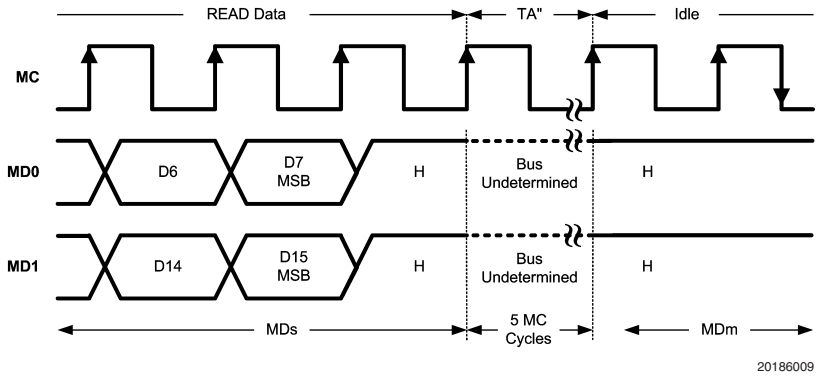

FIGURE 10. READ_Data and TA"

To account for the latency through the MPL link, a dual READ operation is required by the host. The first read returns invalid data (all Low), which the host ignores. Once data has returned to the Master, the INTR signal is asserted to inform the host to initiate a second read operation. During this second read operation the MD line is held in the idle bus phase and valid data is returned through the Master device. After the CS* Low-to-High transition the INTR is de-asserted. The use of the INTR pin is optional. The host may simply wait long enough and then issue the 2nd Read to the Master. In this case the INTR MST output should be leaft as a NC (no connect). READ data will be returned by 36 or 46 MC cycles (depending upon IDR setting). The host just need to wait till after the data is ready and then access it (i.e. 50 or more MC cycles).

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Functional Description (Continued)

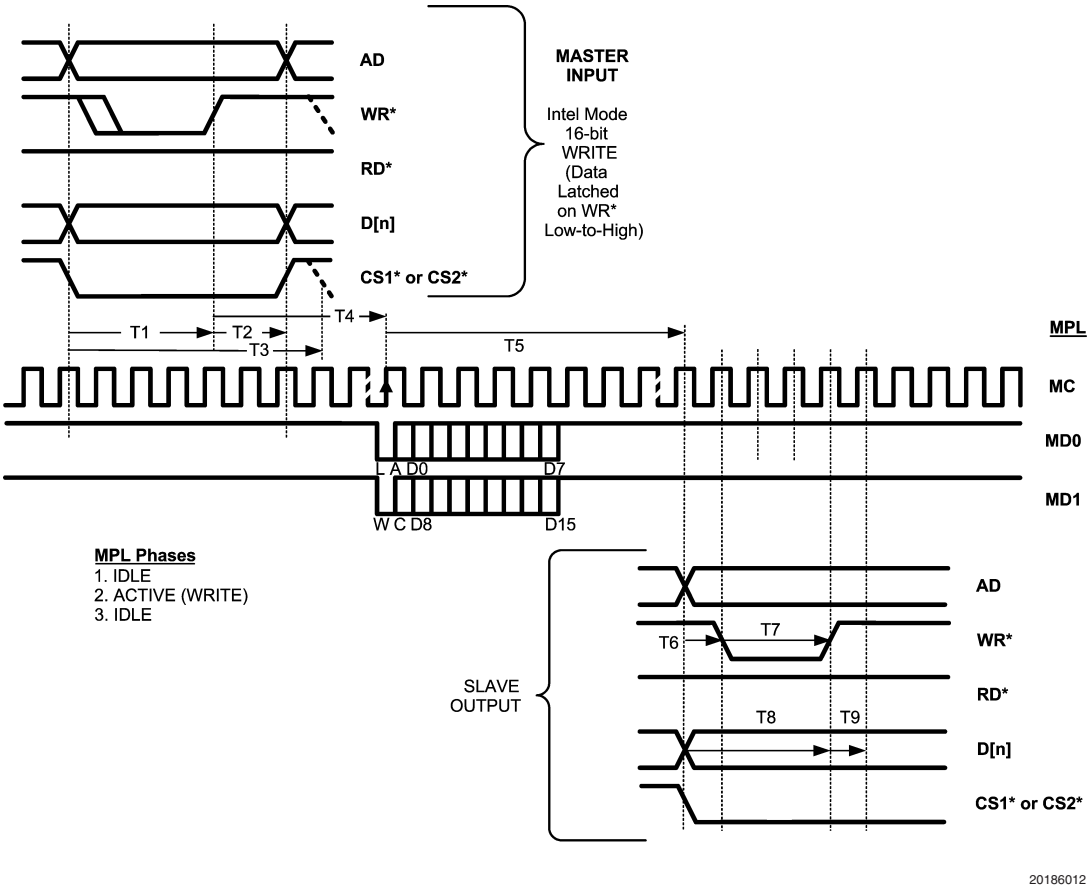

FIGURE 11. WRITE — i80 CPU Interface

TABLE 2. WRITE — i80 CPU Interface Parameters

No.		Parameter	Min	Typ	Max	Units
T1	MasterIN	Data Setup before Write* High	3.5			ns
T2	MasterIN	Data Hold after Write* High	2.5			ns
T3	MasterIN	Write* Cycle Rate	6			MC Cycles
T4	Master	Master Latency		7		MC Cycles
T5	Slave	Slave Latency		8		MC Cycles
T6	SlaveOUT	Data Valid before Write* High-to-Low		1		MC Cycles
T7	SlaveOUT	WR* Pulse Width Low, 16-bit mode		3		MC Cycles
T8	SlaveOUT	Data Valid before Write* Low-to-High		4		MC Cycles
T9	SlaveOUT	Data Valid after Write* Low-to-High		1		MC Cycles

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Functional Description (Continued)

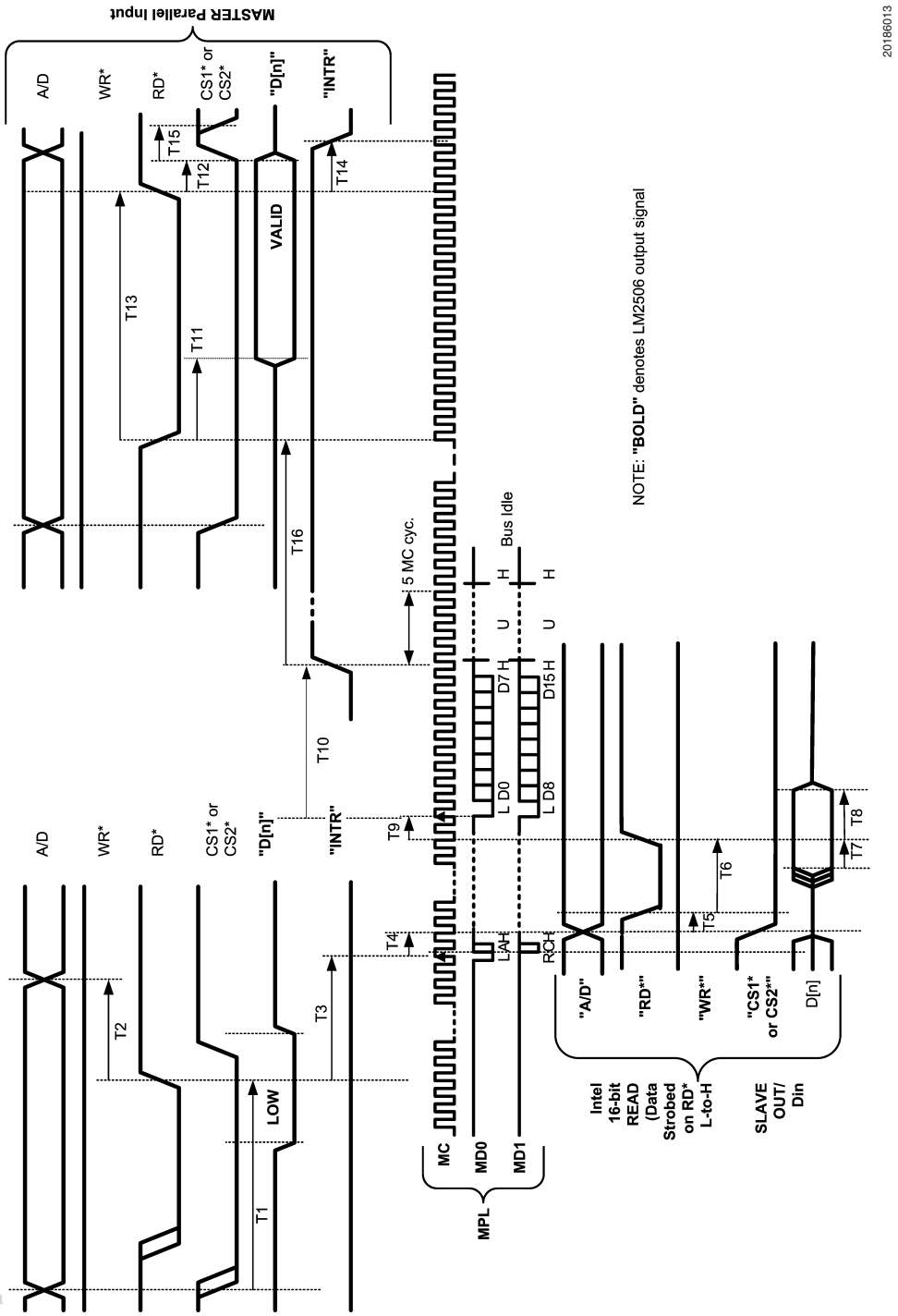

FIGURE 12. READ — i80 CPU Interface

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Functional Description (Continued)

TABLE 3. READ — i80 CPU Interface Parameters

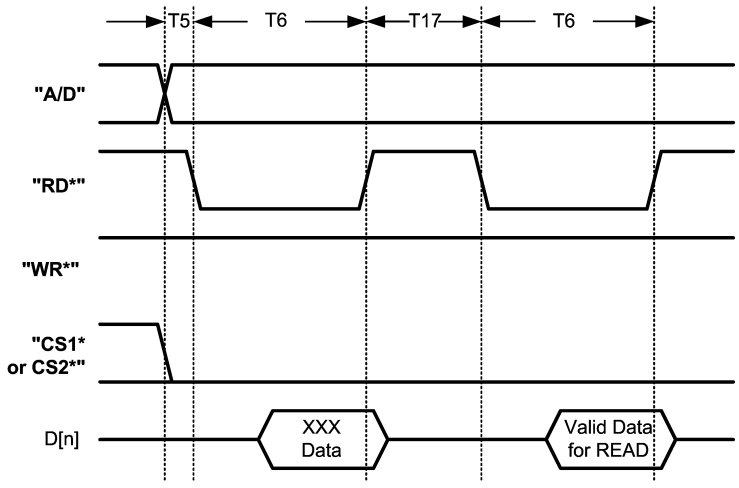
No.		Parameter	Min	Typ	Max	Units
T1	MasterIN	Set Up Time (A/D, RD*) and Data On Time	3.5			ns
T2	MasterIN	Hold Time (A/D, RD*) and Data Off Time	2.5			ns
T3	Master	Master Latency		7		MC Cycles
T4	Slave	Slave Latency		4		MC Cycles
T5	Slave	Read* Delay		1		MC Cycles
T6	Slave	Read Low Pulse Width		6		MC Cycles
T7	Slave	Data Set Up Time	5			ns
T8	Slave	Data Hold Time	5			ns
T9	Slave	Slave Read Latency		4		MC Cycles
T10	Master	MST Read Latency and INTR Delay		14		MC Cycles
T11	Master	Data Delay		13	41	ns
T12	MasterOUT	Data Valid after Strobe	1	7.5		ns
T13	MasterOUT	RD* active pulse width		>50		ns
T14	MasterOUT	INTR De-assert		5		MC Cycles
T15	MasterOUT	Recovery Time, (Note 9)		5		ns
T16	MasterOUT	INTR Response	0			MC Cycles
T17	Slave	IDR Delay, IDR = High, *Figure 13*		4		MC Cycles

SLAVE OUTPUT TIMING

The Slave output recreates the transaction that was sent to the Master. However exact timing of the Slave output is not identical to the Master input. The active pulse (WR* and RD* output pulse) is a function of the MC cycle rate alone. The width applied on the Master input (assuming it meets set and hold requirements), is not regenerated by the Slave output. Also with WRITE transactions the output state is held until the next transaction requires them to be updated. For example after a i80 WRITE to CS1*, the A/D, DATAn, and CS1* output will remain static and hold their last state. CS1* will remain Low until a transaction to CS2* or a PowerDown event. This is acceptable to the target device as normally both an active CS and RD or WR signal is required.

On the display side, the Slave can be configured through the IDR input to issue one or two read transactions to the peripheral. If configured for two read transactions, it will take longer for the INTR signal to be asserted from the Master to account for the time taken for the remote dummy read. Use of this mode allows for consistent behavior from the peripheral regardless of the use of the MPL link (LM2507) or not. See *Figure 13*.

Compatibility of target device's timing requirements should be checked. Check that the active pulse is wide enough for the current settings. If the SLV output is too fast, a slower MC rate should be chosen (use a lower input CLK frequency).



NOTE: **"BOLD"** denotes LM2506 output signals

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FIGURE 13. Slave Output Timing with IDR = H

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Functional Description (Continued)

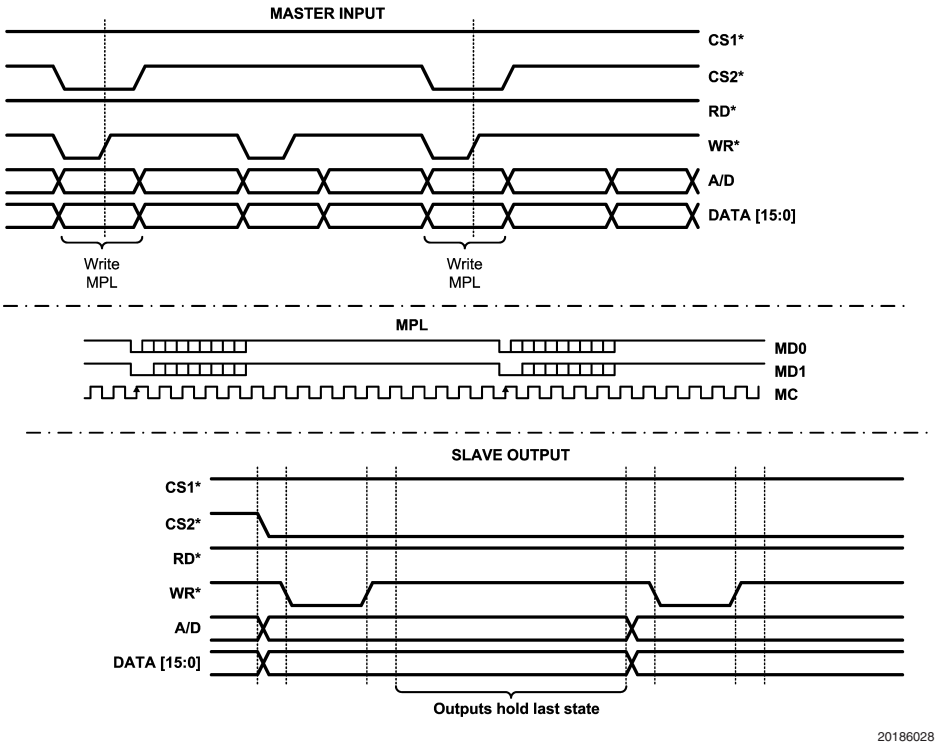

FIGURE 14. Two WRITE Timing – Master IN vs. Slave OUT

LM2507 Features and Operation

POWER SUPPLIES

The V_{DDcore} and V_{DDA} (MPL and PLL) must be connected to the same potential between 1.74V and 2.0V. V_{DDIO} powers the logic interface and may be powered between 1.74 and 3.0V to be compatible with a wide range of host and target devices. **On this device, V_{DDIO} must be powered up before V_{DDcore}/V_{DDA} for proper device configuration/ startup.**

BYPASS RECOMMENDATIONS

Bypass capacitors should be placed near the power supply pins of the device. Use high frequency ceramic (surface mount recommended) 0.1 µF capacitors. A 2.2 to 4.7 µF Tantalum capacitor is recommended near the Master V_{DDA} pin for PLL bypass. A 2.2 to 4.7 µF Tantalum capacitor is recommended near the Slave V_{DDA} pin for MPL bypass. Connect bypass capacitors with wide traces and use dual or larger via to reduce resistance and inductance of the feeds. Utilizing a thin spacing between power and ground planes will provide good high frequency bypass above the frequency range where most typical surface mount capacitors are less effective. To gain the maximum benefit from this, low inductance feed points are important. Also, adjacent signal layers can be filled to create additional capacitance. Minimize loops in the ground returns also for improved signal fidelity and lowest emissions.

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UNUSED/OPEN PINS

Unused inputs must be tied to the proper input level — do not float them. Unused outputs should be left open to minimize power dissipation.

PHASE-LOCKED LOOP

When the LM2507 is configured as a CPU Master, a PLL is enabled to generate the serial link clock. The Phase-locked loop system generates the serial data clock at 4X of the input clock. The MC rate is limited between 12MHz and 80MHz which corresponds to an input CLK of 3 to 20MHz.

MASTER(SER)/SLAVE(DES) SELECTION

The M/S* pin is used to configure the device as either a Master or Slave device. When the M/S* pin is a Logic High, the Master / Serializer configuration is selected. The Driver block is enabled for the MC line, and the MD lines. When the M/S* pin is a Logic Low, the Slave / Deserializer configuration is selected. The Receiver block is enabled for the MC line, and the MD lines.

POWER DOWN/OFF CONFIGURATION / OPTIONS AND CLOCK STOP

Power Up Operation - Upon the application of power to the LM2507, devices configured for Slave activate all outputs. Outputs are held in deasserted states, with all zeros on the data busses until valid data is received from the Master device. If PD* is asserted (Low) prior to the application of power, then the part remains in its power down state.

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LM2507 Features and Operation

(Continued)

On both the Master and the Slave, the PD* pin resets the logic. **The PD* pins should be held low until the power supply has ramped up and is stable and within specifications.**

Power Down and the use of the PD* Input - When the PD* signal is asserted low, the entire chip regardless of mode, powers down. A Low on the PD* input pin will power down the entire device and turn off the line current to MD0, MD1, and MC. In this state the following outputs are driven to:

Master CPU Mode:

INTR = Low

Slave CPU Mode:

DATAn = Low,

A/D = CS1* = CS2* = MF0 = MF1 = High

Multiple configurations for PowerDown are possible with the chipset. These depend on the operating mode and configuration chosen. Two possible applications are shown in *Figure 16*. In (A) both the Master and Slave provide a PD* input pin. This can be connected together as shown or remotely driven (i.e. a GPO signal from another device, assuming same VDDIO level). However for proper MPL start up, the Slave must be powered up at the same time or before the Master device. Do not power up the Master first. In (B) two separate control signals are used. Note that the Master should not be powered up before the Slave.

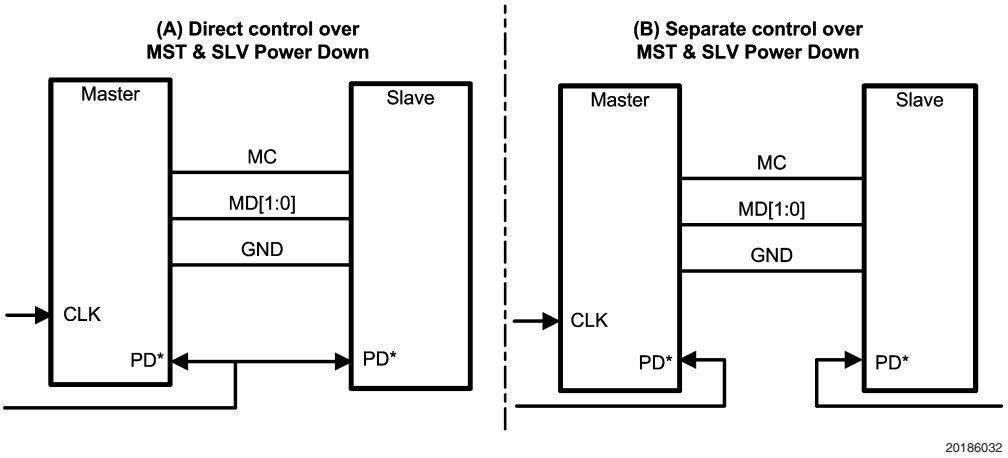

FIGURE 15. Power Down Control Options

Application Information

SYSTEM CONSIDERATIONS

When employing the MPL MST/SLV chipset in place of a parallel bus, a few system considerations must be taken into account. Before sending commands (i.e. initialization commands) to the display, the MST/SLV must be ready to transmit data across the link. The MPL link must be powered up, and the PLL must be locked. Also a review of the Slave output timing should be completed to insure that the timing parameters provided by the Slave output meet the requirements of the LCD driver input. Specifically, pulse width on RD* and WR*, data valid time, and bus cycle rate should be reviewed and checked for inter-operability. Additional details are provided next:

The MPL link should be started up as follows: The chipset should be powered up first, V_{DDIO} must be powered up first, or it may be at the same time as V_{DD}/V_{DDA}. During power up, the PD* inputs should be held Low and released once power is stable and within specification. The Slave PD* may be released first or at the same time as the Master. CLK should be applied prior to releasing Master PD*.

Before data can be sent across the MPL serial link, the link must be ready for transmission. The CLK needs to be applied to the device, and the MST PLL locked. This is controlled by a keep-off counter set for 4096 cycles. After the PLL has lock and the counter expired, an additional 540 MC cycles are required for the start-up of the MPL link. After this, data may now be written to the device.

It takes 5MC Cycles to send a 16-bit CPU Write including the serial overhead. The MC cycle time is calculated based on the PLL Multiplier of 4X and also the input clock frequency. For example, a 19.2MHz input CLK and a 4X PLLCON setting yields a MC frequency of 76.8MHz. Thus it takes 65.1ns to send the word in serial form. To allow some idle time between transmissions (this will force a bit sync per word if the gap is long enough in between), the load rate on the Master input should not be faster than 6 MC cycles, or every 78ns in our example to support a data pipe line. This is sometimes referred to as the bus cycle time (the time between commands).

The Slave output times is also a function of MC cycles. Note that in i80 mode, the width of the WR* pulse low is **three MC cycles** regardless of the pulse width applied to the Master input. System designers need to check compatibility with the display driver to ensure this pulse width meets its requirement. If it is too fast, apply a lower input clock frequency.

The CLK input must be free running and not gapped.

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Application Information (Continued)

MPL SWAP FEATURE

The LM2507 provides a swap function of MPL MD lines depending upon the state of the M/S* pin. This facilitates a straight through MPL interface design eliminating the needs for via and crossovers as shown on *Figure 16*. The parallel bus pins are also swapped to facilitate a flow though orientation of parallel bus signals.

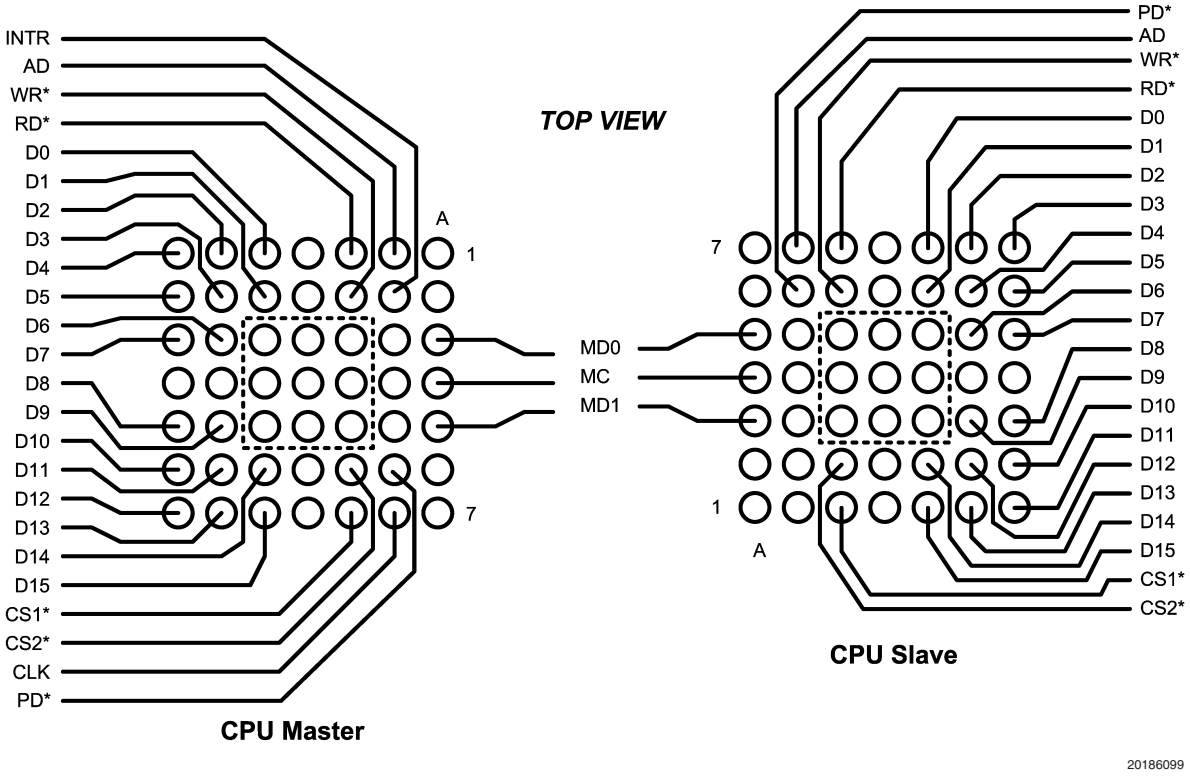

FIGURE 16. MPL Interface Layout and Flow Through Pinout

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Application Information (Continued)

Power and Ground - Bumped Package

Power and ground bump assignments are shown in *Figure 17*. The nine center balls must be connected ground on the PCB. See also, National's Application Note AN-1126, Ball Grid Array, for information on land pattern recommendations and escape routing guidelines.

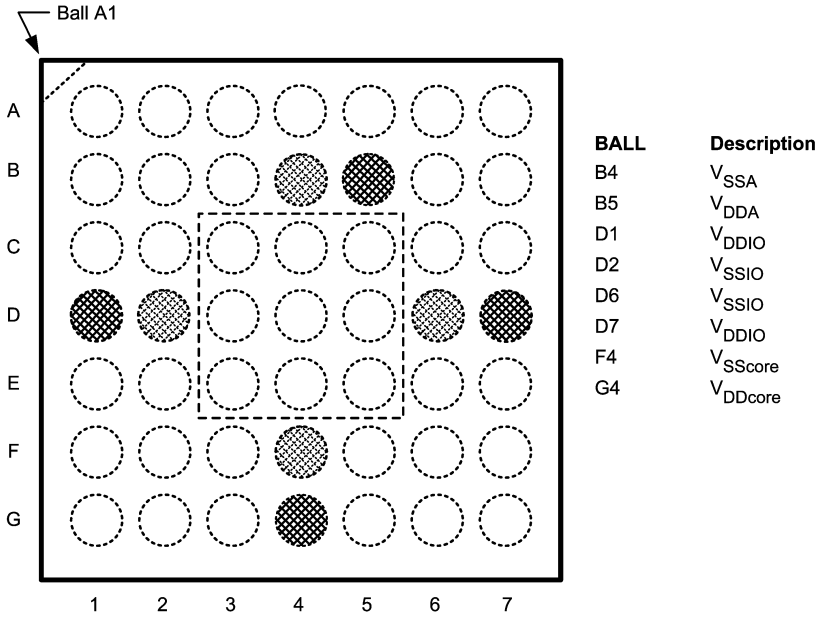

FIGURE 17. LM2507 PWR (V_{DD}) and GND (V_{SS}) Bumps (TOP VIEW)

FLEX CIRCUIT RECOMMENDATIONS

The three MPL lines should generally run together to minimize any trace length differences (skew). For impedance control and also noise isolation (crosstalk), guard ground traces are recommended in between the signals. Commonly a Ground-Signal-Ground (GSGSGSG) layout is used. Locate fast edge rate and large swing signals further away to also minimize any coupling (unwanted crosstalk). In a stacked flex interconnect, crosstalk also needs to be taken into account in the above and below layers (vertical direction). To minimize any coupling locate MPL traces next to a ground layer. Power rails also tend to generate less noise than LVCMOS so they are also good candidates for use as isolation and separation.

The interconnect from the Master to the Slave typically acts like a transmission line. Thus impedance control and ground returns are an important part of system design. Impedance should be in the 50 to 100 Ohm nominal range for the LM2507. Testing has been done with cables ranging from 40 to 110 Ohms without error (BER Testing). To obtain the impedance, adjacent grounds are typically required (1 layer flex), or a ground shield / layer. Total interconnect length is intended to be in the 20cm range, however 30cm is possible at lower data rates. Skew should be less than 500ps to maximize timing margins.

GROUNDING

While the LM2507 employs three separate types of ground pins, these are intended to be connected together to a common ground plane. The separate ground pins help to isolate switching currents from different sections of the integrated circuit (IC). Also required is a nearby signal return (ground) for the MPL signals. These should be provided next to the MPL signals, as that will create the smallest current loop area. The grounds are also useful for noise isolation and impedance control.

PCB RECOMMENDATIONS

General guidelines for the PCB design:

- Floor plan, locate MPL Master near the connector to limit chance of cross talk to high speed serial signals.
- Route serial traces together, minimize the number of layer changes to reduce loading.
- Use ground lines are guards to minimize any noise coupling (guarantees distance).
- Avoid parallel runs with fast edge, large LVCMOS swings.
- Also use a GSGSG pinout in connectors (Board to Board or ZIF).
- Slave device - follow similar guidelines.
- Bypass the device with MLC surface mount devices and thinly separated power and ground planes with low inductance feeds.
- High current returns should have a separate path with a width proportional to the amount of current carried to minimize any resulting IR effects.

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Application Information (Continued)

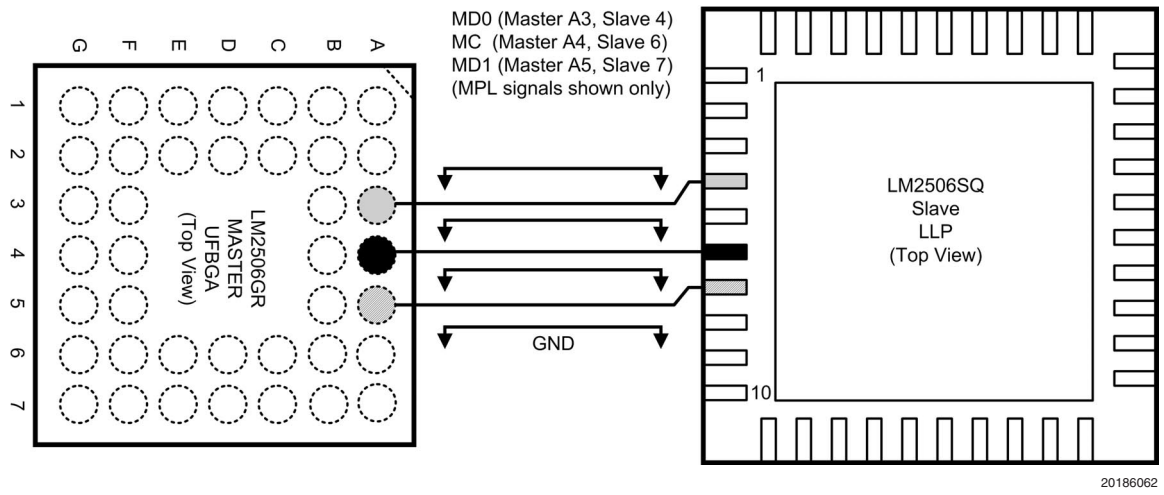

FIGURE 18. MPL Interface Layout – microArray to LLP Package

DISPLAY APPLICATION

The LM2507 chipset is intended for interfacing between a host (processor) and a Display. It supports a 16, 9 or 8-bit i80 CPU style interfaces and can be configured as shown in *Figure 19*. The Display side parallel bus may be connected to one or two displays. Each display has its own chipselect signal. The multidrop bus should be laid out to minimize any resulting stub lengths.

If only one display is required, the unused CS* master input must be tied off (High, disabled). The unused CS* slave output should be left as a no-connect (NC).

If a 8-bit or 9-bit CPU bus width is desired, the unused master inputs must be tied off (connect to Ground). The unused Slave outputs should be left as no-connects.

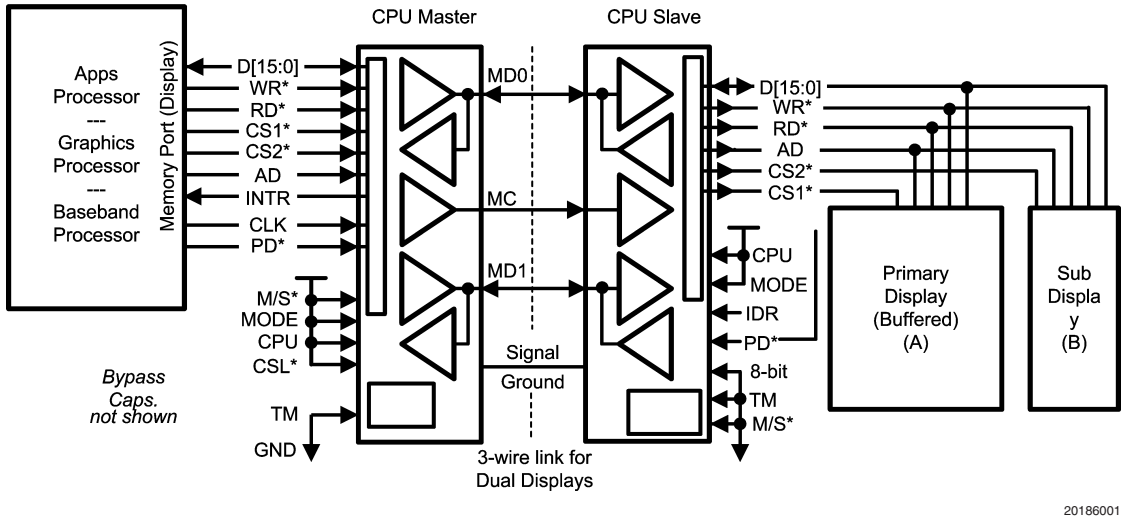

FIGURE 19. CPU Mode Display Interface Application

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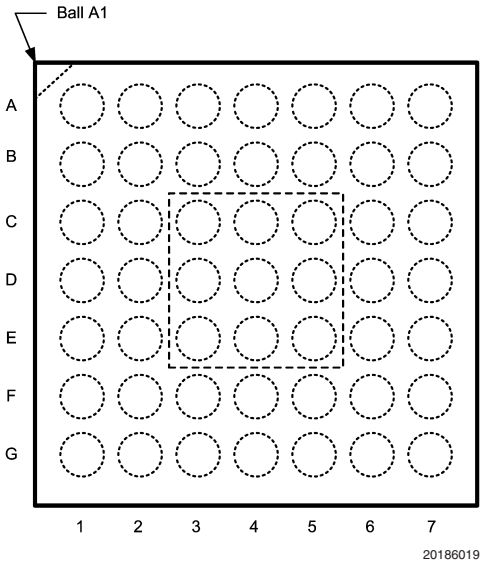
Connection Diagram microArray Package



TOP VIEW
(not to scale)

Master (CPU) Pinout

MST	1	2	3	4	5	6	7
A	TM	CPU	MD0	MC	MD1	CSL*	M/S*
B	AD	INTR	Mode	V_{SSA}	V_{DDA}	PD*	CLK
C	MF0 (RD*)	MF1 (WR*)	V_{bulk}	V_{bulk}	V_{bulk}	CS2*	CS1*
D	V_{DDIO}	V_{SSIO}	V_{bulk}	V_{bulk}	V_{bulk}	V_{SSIO}	V_{DDIO}
E	D0	D1	V_{bulk}	V_{bulk}	V_{bulk}	D14	D15
F	D2	D3	D6	V_{SScore}	D9	D11	D13
G	D4	D5	D7	V_{DDcore}	D8	D10	D12

Slave CPU Pinout

SLV	1	2	3	4	5	6	7
A	TM	CPU	MD1	MC	MD0	IDR	M/S*
B	NC	8-bit	Mode	V_{SSA}	V_{DDA}	PD*	AD
C	CS1*	CS2*	V_{bulk}	V_{bulk}	V_{bulk}	MF1 (WR*)	MF0 (RD*)
D	V_{DDIO}	V_{SSIO}	V_{bulk}	V_{bulk}	V_{bulk}	V_{SSIO}	V_{DDIO}
E	D15	D14	V_{bulk}	V_{bulk}	V_{bulk}	D1	D0
F	D13	D12	D9	V_{SScore}	D6	D4	D2
G	D11	D10	D8	V_{DDcore}	D7	D5	D3

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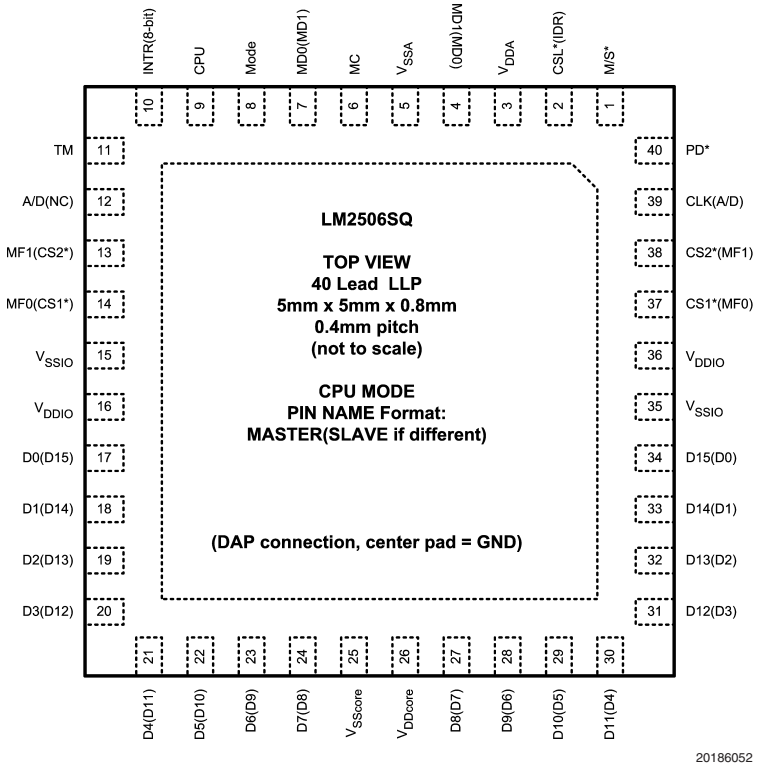
Connection Diagram - LLP Package



TOP VIEW — (not to scale)

TABLE 4. CPU Mode Pad Assignment

Pin #	Master	Slave		Pinl #	Master	Slave
1	M/S*			21	D4	D11
2	CSL*	IDR		22	D5	D10
3	V_{DDA}			23	D6	D9
4	MD1	MD0		24	D7	D8
5	V_{SSA}			25	V_{SScore}	
6	MC			26	V_{DDcore}	
7	MD0	MD1		27	D8	D7
8	Mode			28	D9	D6
9	CPU			29	D10	D5
10	INTR	8-bit		30	D11	D4
11	TM			31	D12	D3
12	A/D	NC		32	D13	D2
13	MF1 (WR*)	CS2*		33	D14	D1
14	MF0 (RD*)	CS1*		34	D15	D0
15	V_{SSIO}			35	V_{SSIO}	
16	V_{DDIO}			36	V_{DDIO}	
17	D0	D15		37	CS1*	MF0 (RD*)
18	D1	D14		38	CS2*	MF1 (WR*)
19	D2	D13		39	CLK	A/D
20	D3	D12		40	PD*	
DAP	GND			DAP	GND	

Note: Pins are different between Master and Slave configurations.

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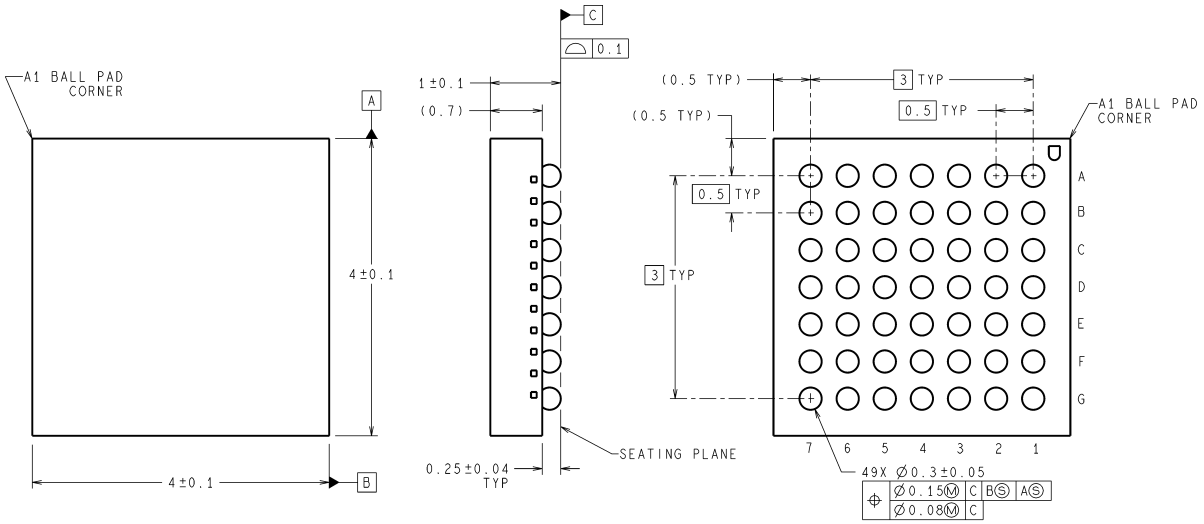
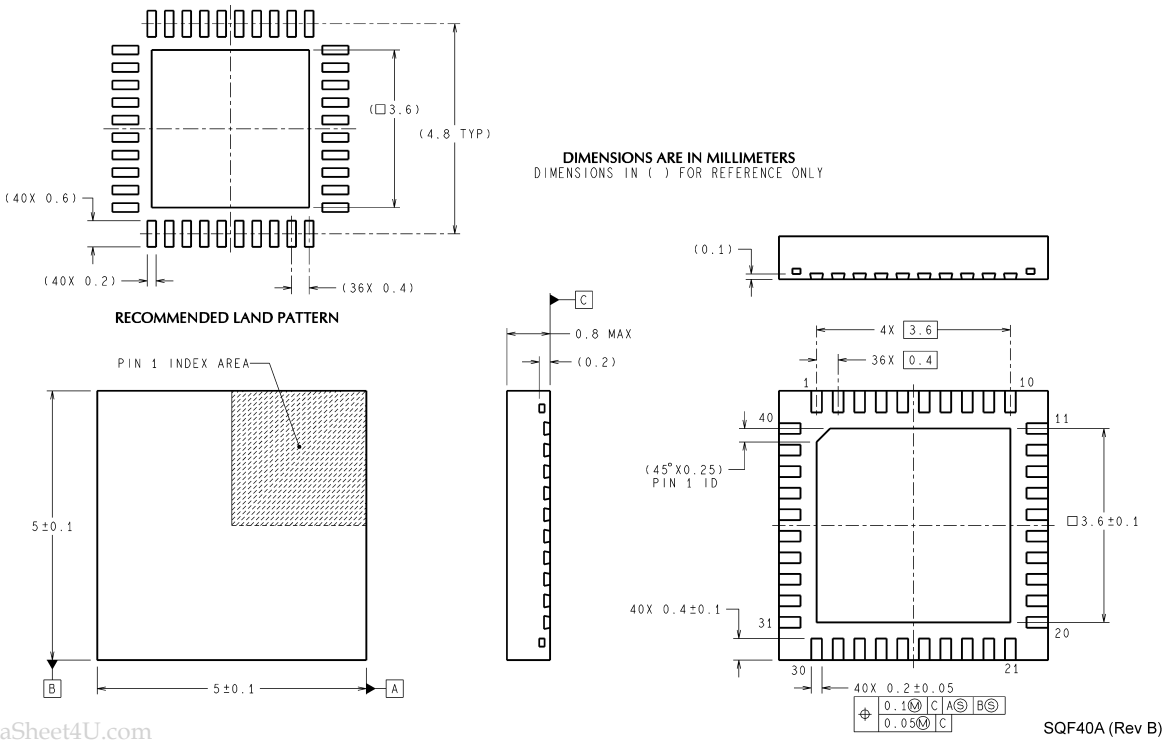
Physical Dimensions inches (millimeters) unless otherwise noted



GRA49A (Rev A)

49L MicroArray, 0.5mm pitch
Order Number LM2507GR
NS Package Number GRA49A



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SQF40A (Rev B)

40L LLP, 0.4mm pitch
Order Number LM2507SQ
NS Package Number SQF40A

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