

LM200

- 240 dot (W) x 64 dot (H) graphic and alpha-numeric display
- Control LSI HD61830 attachment type (see page 76)

MECHANICAL DATA (Nominal dimensions)

Module size	180W x 75H x 15D (max) mm
Effective display area	132W x 39H mm
Number of dots	240W x 64H dot
Dot size	0.48W x 0.48H mm
Pitch	0.53W x 0.53H mm
Weight	about 150g

ABSOLUTE MAXIMUM RATINGS

	min.	max.
Power supply for logic ($V_{DD}-V_{SS}$)	0	7.0V
Power supply for LCD drive ($V_{DD}-V_{EE}$)	0	13.5V
Input voltage (V_i)	V_{SS}	V_{DD}
Operating temperature (T_a)	0	50°C
Storage temperature (T_{stg})	-20	60°C

ELECTRICAL CHARACTERISTICS

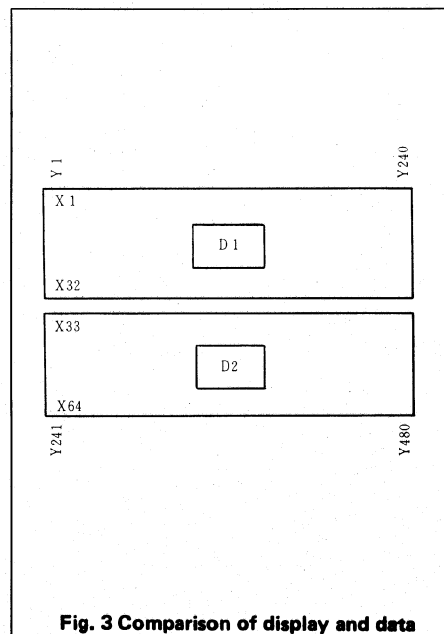
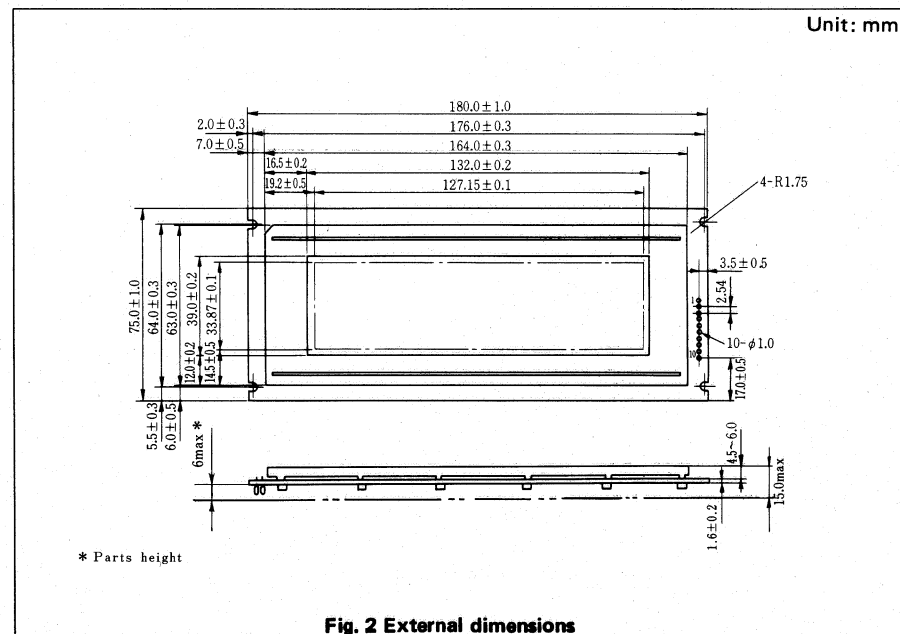
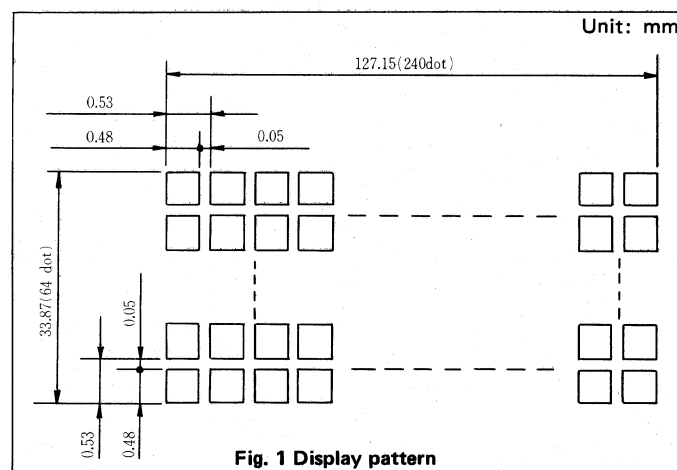
$T_a = 25^\circ\text{C}$, $V_{DD} = 5.0V \pm 0.25V$, $V_{EE} = -5.0V \pm 0.25V$

Input "high" voltage (V_{IH})	$0.7 \times V_{DD} V \text{ min.}$
Input "low" voltage (V_{IL})	$0.3 \times V_{DD} V \text{ max.}$
Clock frequency (f_{CL2})	390 kHz min. 460 kHz typ. 520 kHz max.
Power supply current (I_{DD})	5mA typ. ($D_1, D_2 = GND, f_{CL2} = 460 \text{ kHz}$)
Power supply for LCD drive (Recommended) ($V_O - V_{EE}$)	$D_u = 1/32$ $\begin{array}{ll} \text{at } T_a = 0^\circ\text{C} & \dots\dots\dots 8.0 \text{ V typ.} \\ \text{at } T_a = 25^\circ\text{C} & \dots\dots\dots 7.4 \text{ V typ.} \\ \text{at } T_a = 50^\circ\text{C} & \dots\dots\dots 6.5 \text{ V typ.} \end{array}$

OPTICAL DATA See page 8

INTERNAL PIN CONNECTION

Pin No.	Symbol	Level	Function
1	D1	H/L	Serial row data
2	FLM	H	The FLM signal indicates the beginning of each display cycle.
3	M	H/L	Control signal for a.c. driving
4	CL1	H→L	The CL1 latches the serial data in the shift registers.
5	CL2	H→L	Clock signal for shifting the serial data
6	D2	H/L	Serial row data
7	V _{DD} (+5V)		Power supply for logic circuit
8	V _{SS} (GND)	—	Ground
9	V _{EE} (-5V)	—	Power supply for LC driving
10	V _O	—	Operating voltage for LC driving



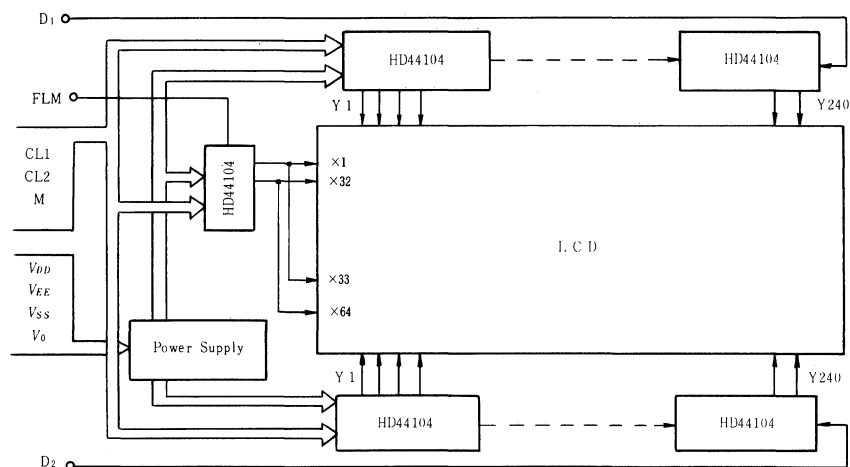


Fig. 4 Block diagram

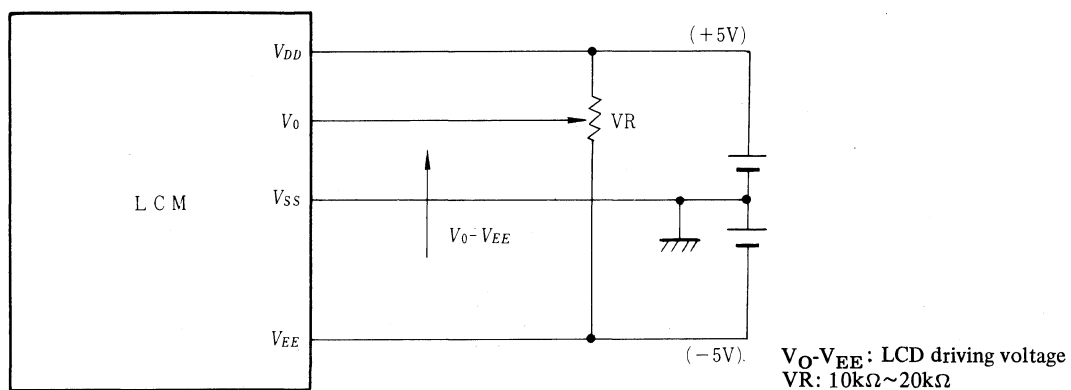


Fig. 5 Power supply

TIMING CHARACTERISTICS

Item	Symbol	min.	typ.	max.	Unit
Clock frequency	f_{CL2}	—	—	520	kHz (Note 1)
Clock pulse width (High level)	t_{CWH}	800	—	—	ns
Clock pulse width (Low level)	t_{CWL}	800	—	—	ns
Clock set up time	t_{CSU}	500	—	—	ns
Data set up time	t_{SU}	300	—	—	ns
FLM set up time	t_{FSU}	300	—	—	ns
M delay time	t_{DM}	-1000	—	+1000	ns (Note 2)
FLM hold time	t_{FH}	0	—	—	ns
Data hold time	t_{DH}	300	—	—	ns

Note 1. Optimum frequency for the highest contrast is different by the type of module.

Note 2. Timing of M signal to CLI may be in the range of ± 1000 ns.

Note 3. In adjusting FLM frequency, avoid setting it around the commercial frequency ($50\text{Hz} \pm 2\text{Hz}$ or $60\text{Hz} \pm 2\text{Hz}$) to prevent LCD flicker.

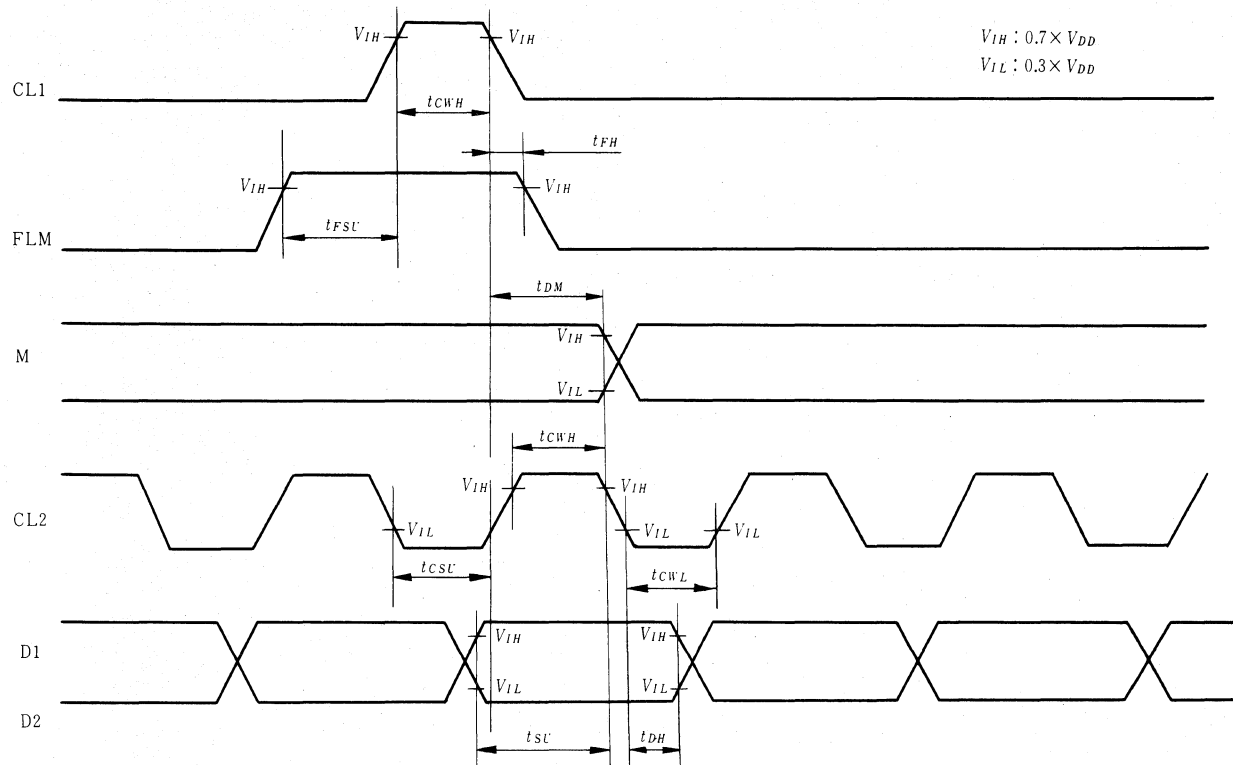


Fig. 6 Interface timing (data write)

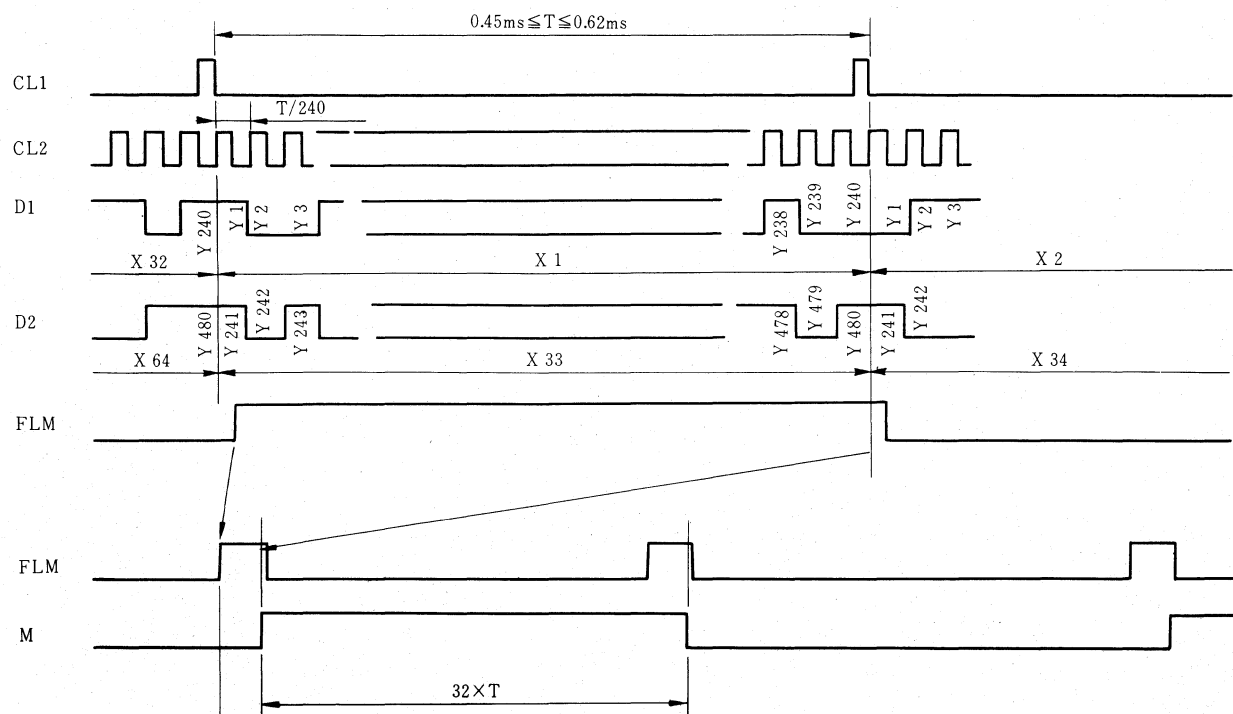


Fig. 7 Interface timing