LM021

- 479 dot (W) x 24 dot (H) graphic and alpha-numeric display
- Control LSI HD61830 attachment type (see page 76)

MECHANICAL DATA (Nominal dimensions)

Module size	290W x 60H x 13D (max) mm
Effective display area	245W x 19H mm
Number of dots	479W x 24H dot
Dot size	0.43W x 0.55H mm
Pitch	0.48W x 0.6H mm
Weight	about 150g

ABSOLUTE MAXIMUM RATINGS

	min.	max.
Power supply for logic ($V_{DD}-V_{SS}$)	0	7.0V
Power supply for LCD drive ($V_{DD}-V_{EE}$)	0	13.5V
Input voltage (V_i)	V_{SS}	V_{DD}V
Operating temperature (Ta)	0	50°C
Storage temperature (Tstg)	−20	60°C

ELECTRICAL CHARACTRISTICS

Ta=25°C, V_{DD}=5.0V±0.25V, V_{EE}=−5.0V±0.25V

Input "high" voltage (V_{iH})	0.7 x V_{DD}V min.
Input "low" voltage (V_{iL})	0.3 x V_{DD}V max.
Clock frequency (f_{CL2})	230 kHz min.
	350 kHz typ.
	460 kHz max.
Power supply current (I_{DD})	4mA typ.
(I_{EE})	2mA typ.

(D_1, D_2=GND, f_{CL2}= 350 kHz)

Power supply for LCD drive (Recommended) (V_O-V_{EE})

Duty = 1/24

at Ta= 0°C	6.0 V typ.
at Ta=25°C	5.4 V typ.
at Ta=50°C	4.4 V typ.

OPTICAL DATA ..... See page 8

INTERNAL PIN CONNECTION

Pin No.	Symbol	Level	Function
1	FLM	H	The FLM signal indicates the beginning of each display cycle.
2	M	H/L	Control signal for a.c. driving.
3	CL1	H→L	The CL1 latches the serial data in the shift registers.
4	D1	H/L	Serial row data
5	D2	H/L	Serial row data
6	CL2	H→L	Clock signal for shifting the serial data
7	V_{DD}(+5V)	–	Power supply for logic circuit
8	V_{SS}(GND)	–	Ground
9	V_{EE}(−5V)	–	Power supply for LC driving
10	V_O	–	Operating voltage for LC driving

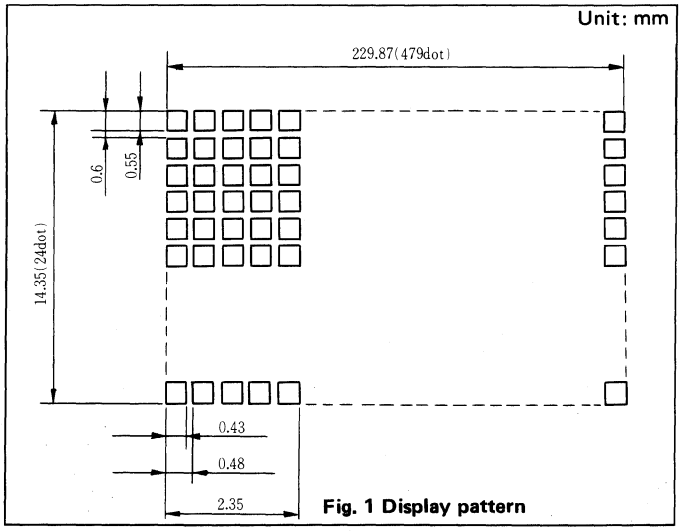


Fig. 1 Display pattern

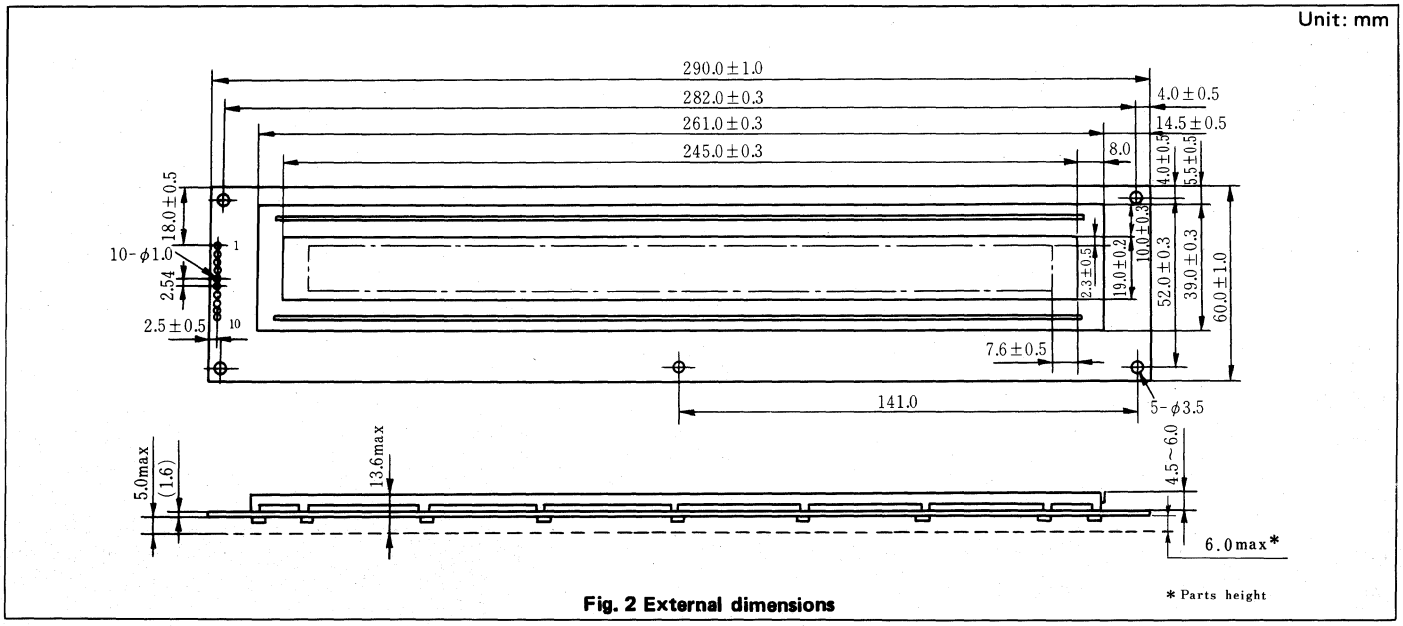
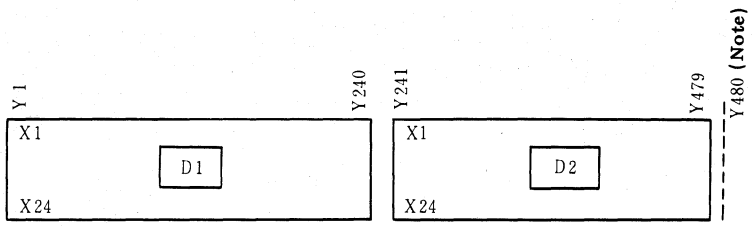


Fig. 2 External dimensions



Note: Y480 is a dummy line.

Fig. 3 Comparison of display and data

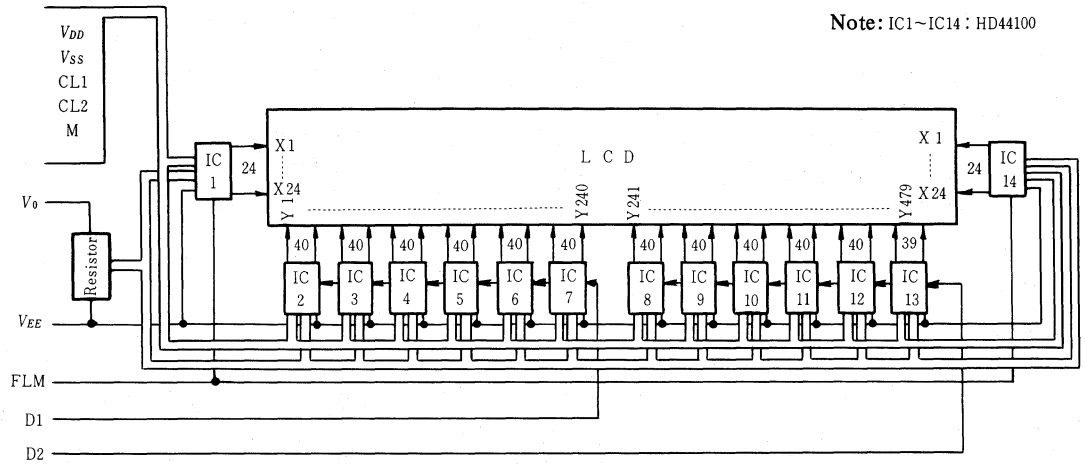
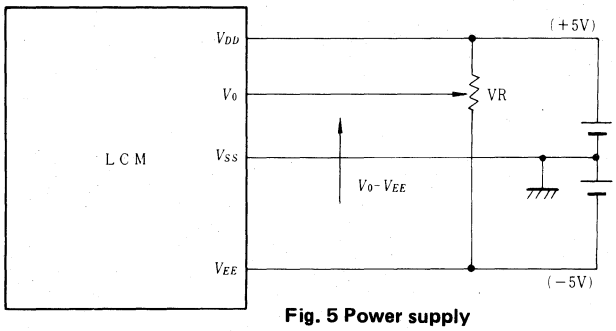


Fig. 4 Block diagram



V_O-V_{EE}: LCD driving voltage
VR: 10kΩ~20kΩ

Fig. 5 Power supply

TIMING CHARACTERISTICS

Item	Symbol	min.	typ.	max.	Unit
Clock frequency	f_{CL2}	–	–	500	kHz (Note 1)
Clock pulse width (High level)	t_{CWH}	800	–	–	ns
Clock pulse width (Low level)	t_{CWL}	800	–	–	ns
Clock set up time	t_{CSU}	500	–	–	ns
Data set up time	t_{SU}	300	–	–	ns
FLM set up time	t_{FSU}	300	–	–	ns
M delay time	t_{DM}	−1000	0	+1000	ns (Note 2)
FLM hold time	t_{FH}	0	–	–	ns
Data hold time	t_{DH}	300	–	–	ns

Note 1. Optimum frequency for the highest contrast is different the type of module.

Note 2. Timing of M signal to CLI may be in the range of ±1000ns.

Note 3. In adjusting FLM frequency, avoid setting it around the commercial frequency (50Hz±2Hz or 60Hz ±2Hz) to prevent LCD flicker.

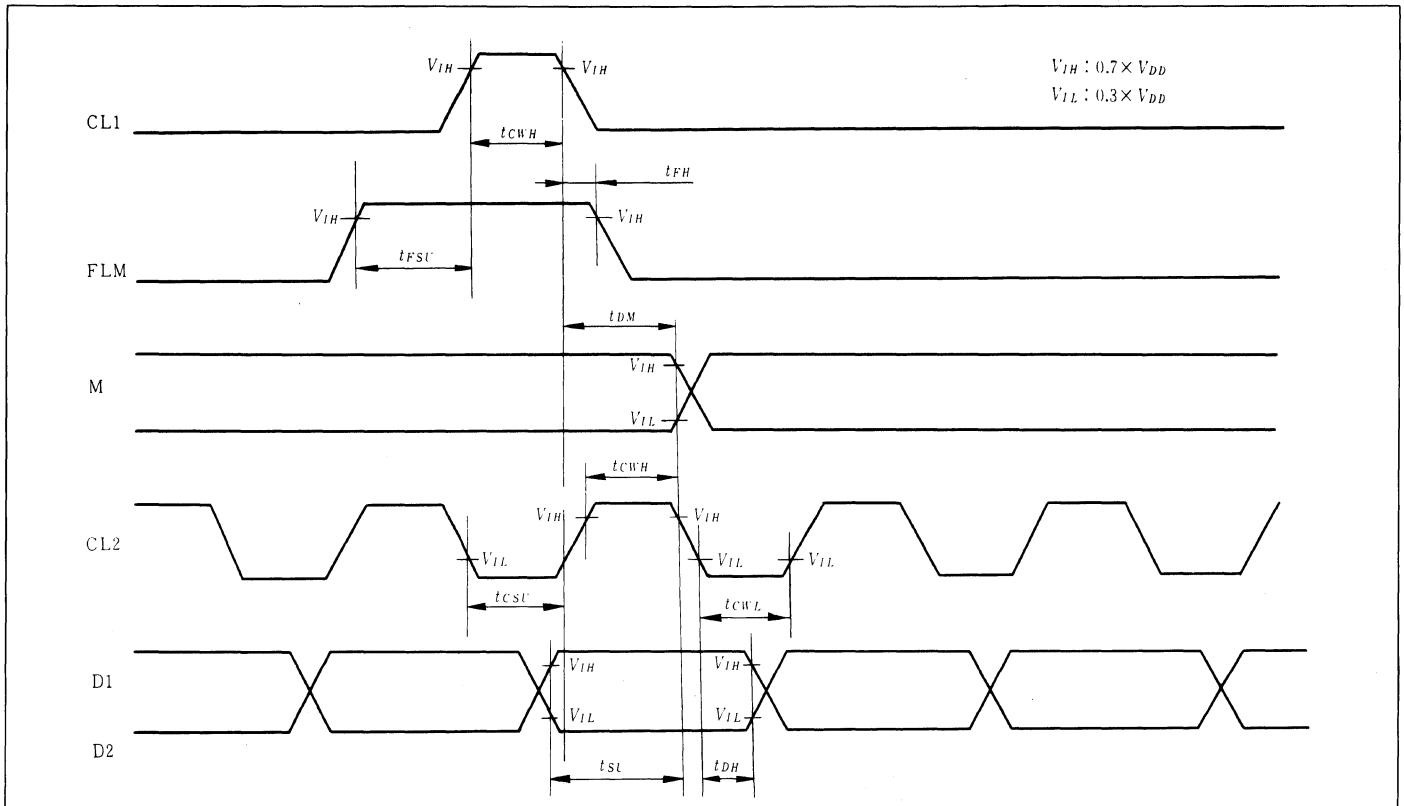


Fig. 6 Interface timing (data write)

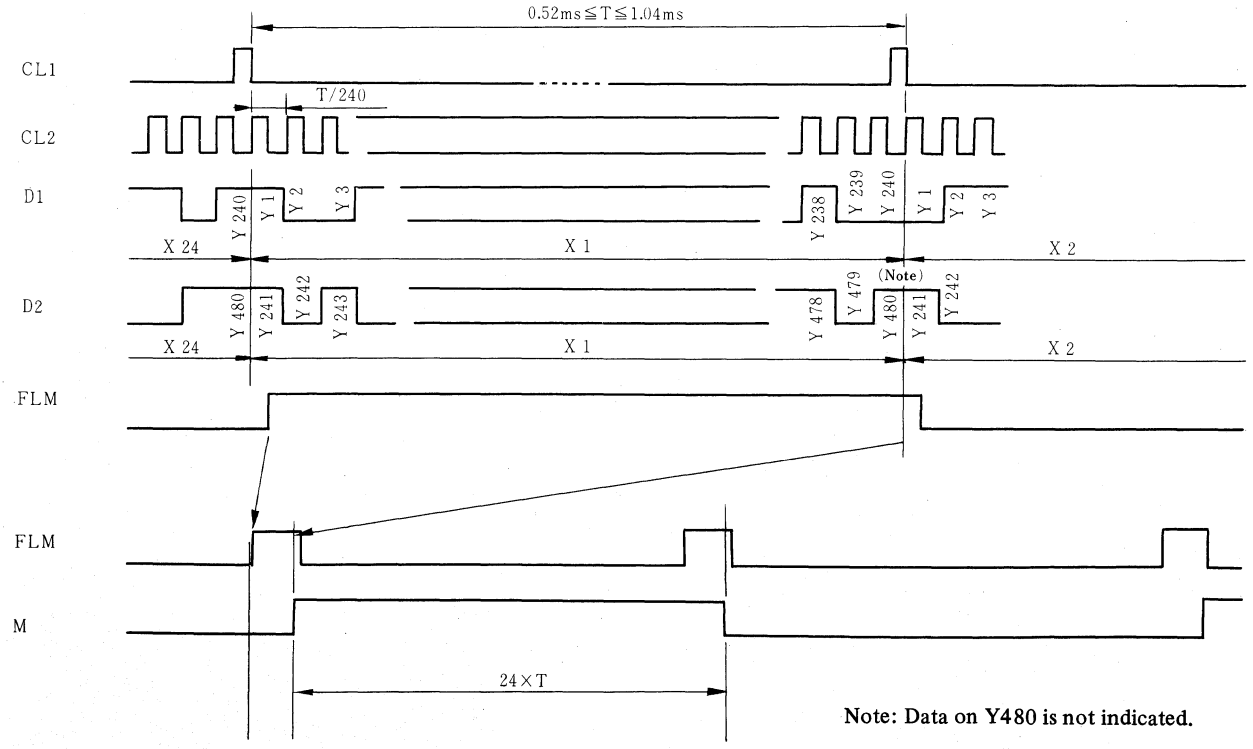


Fig. 7 Interface timing (data read)