LH5P864

CMOS 512K (64K × 8) Pseudo-Static RAM

FEATURES

- 65,536 × 8 bit organization
- Access time: 80 ns (MAX.)
- Cycle time: 140 ns (MIN.)
- Single +5 V power supply
- Power consumption:
  Operating: 440 mW (MAX.)
  Standby (TTL level): 22 mW (MAX.)
  Standby (CMOS level): 2.75 mW (MAX.)
- Operating temperature: 0 to 70°C
- TTL compatible I/O
- 512 refresh cycles/8 ms (MAX.)
- Available for auto-refresh and self-refresh modes
- Package: 32-pin, 525-mil SOP

DESCRIPTION

The LH5P864 is a 512K-bit Pseudo-Static RAM organized as 65,536 × 8 bits. It is fabricated using silicon-gate CMOS process technology. With its built-in oscillator, it is easy to refresh memories without an external clock.

PIN CONNECTIONS

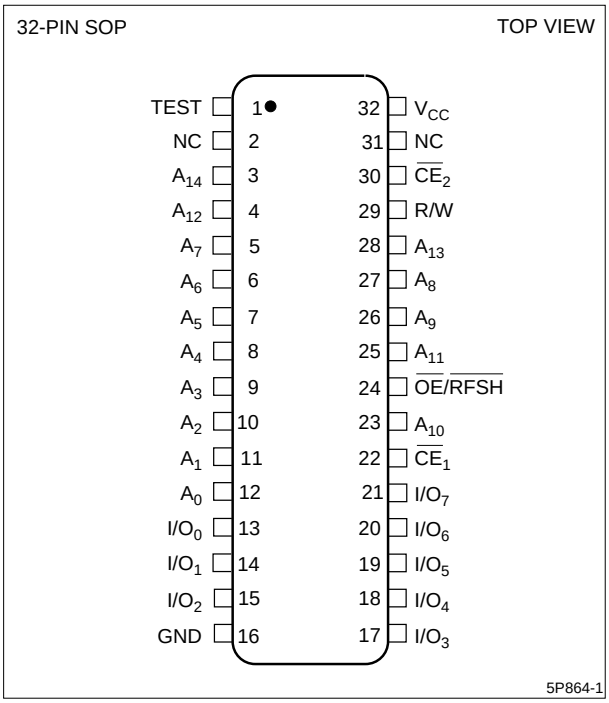


Figure 1. Pin Connections for SOP Package

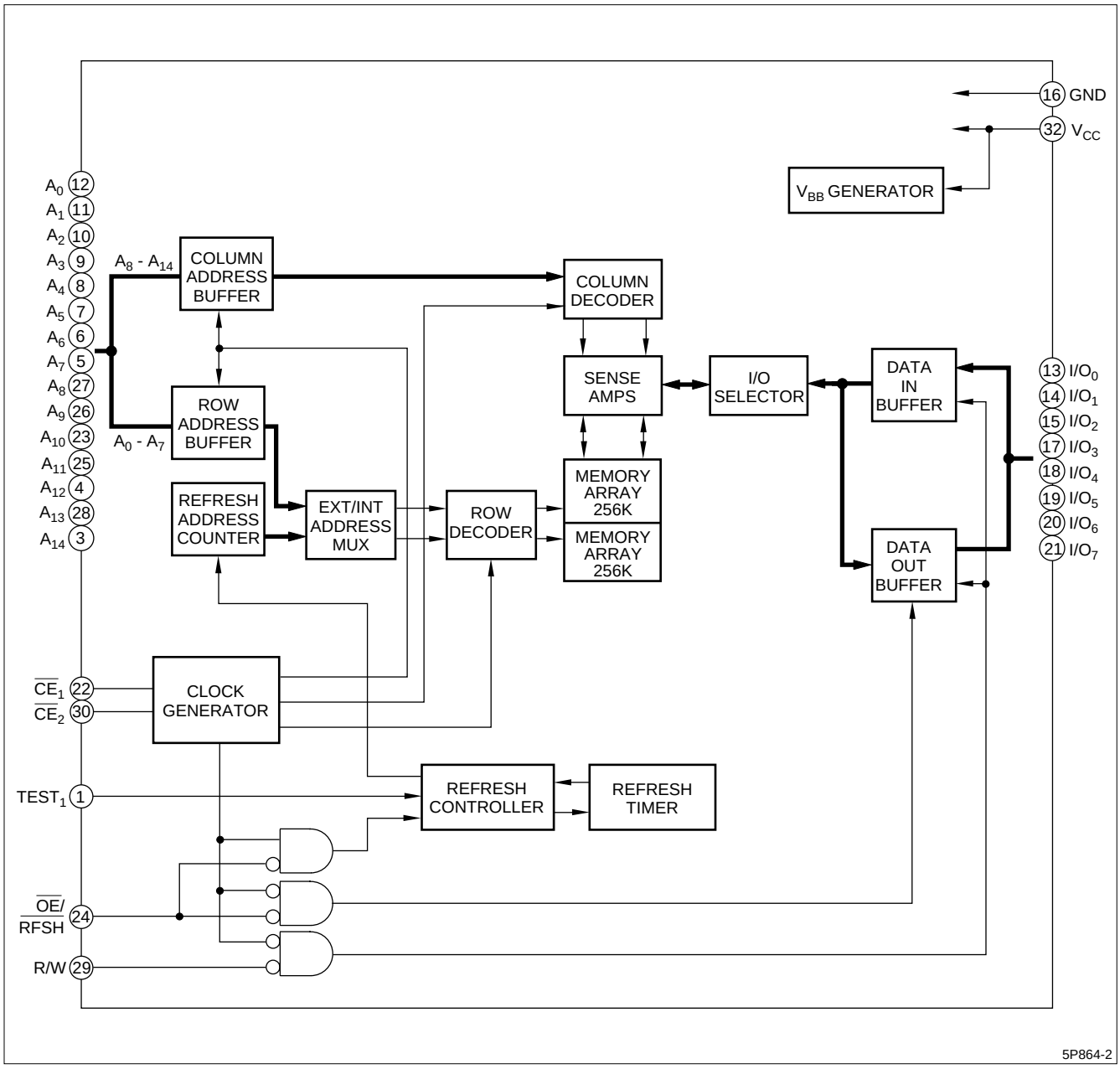


Figure 2. LH5P864 Block Diagram

PIN DESCRIPTION

SIGNAL	PIN NAME
A_0 - A_{14}	Address input
R/W	Read/Write Enable input
$\overline{OE}$/$\overline{RFSH}$	Output Enable input/Refresh input
$\overline{CE_1}$, $\overline{CE_2}$	Chip Enable input
I/O_0 - I/O_7	Data input/output

SIGNAL	PIN NAME
V_{CC}	Power Supply
GND	Ground
Test	Test Input
NC	No Connection

ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	RATING	UNIT	NOTE
Applied voltage on any pin	V_T	-1.0 to +7.0	V	1
Output short circuit current	I_O	50	mA	
Power dissipation	P_D	600	mW	
Operating temperature	Topr	0 to +70	°C	
Storage temperature	Tstg	-65 to +150	°C	

NOTE:
1. The maximum applicable voltage on any pin with respect to GND.

RECOMMENDED OPERATING CONDITIONS (T_A = 0 to +70°C)

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT
Supply voltage	V_{CC}	4.5	5.0	5.5	V
Input voltage	V_{IH}	2.4		V_{CC} + 0.3	V
	V_{IL}	-1.0		0.8	V

CAPACITANCE (T_A = 0 to +70°C, f = 1MHz, V_{CC} = 5.0 V ±10%)

PARAMETER	CONDITIONS	SYMBOL	MIN.	MAX.	UNIT
Input capacitance	A_0 - A_{14}	C_{IN1}		8	pF
	R/W, $\overline{OE}$/RFSH	C_{IN2}		8	pF
	$\overline{CE_1}$, $\overline{CE_2}$	C_{IN3}		8	pF
	$TEST_1$	C_{IN4}		10	pF
Input/Output capacitance	I/O_0 - I/O_7	C_{OUT1}		10	pF

DC CHARACTERISTICS (T_A = 0 to +70°C, V_{CC} = 5.0 V ±10%)

PARAMETER	SYMBOL	CONDITIONS	MIN.	MAX.	UNIT	NOTE
Operating current	I_{CC1}	t_{RC} = t_{RC} (MIN.)		80	mA	1, 2
Standby current	I_{CC2}	TTL input		4.0	mA	1, 3, 5
		CMOS input		0.5	mA	1, 3, 6
Self refresh average current	I_{CC3}	TTL input		4.0	mA	1, 4, 5
		CMOS input		0.5	mA	1, 4, 6
Input leakage current	I_{LI}	0 V ≤ V_{IN} ≤ 6.5 V, 0 V except on test pins	-10	10	µA	
Output leakage current	I_{LO}	0 V ≤ V_{OUT} ≤ V_{CC} + 0.3 V, Outputs in High-Z state	-10	10	µA	
Output HIGH voltage	V_{OH}	I_{OUT} = -1.0 mA	2.4		V	
Output LOW voltage	V_{OL}	I_{OUT} = 4.0 mA		0.4	V	

NOTES:
1. Specified values are with outputs open.
2. I_{CC1} depends on the cycle time.
3. $\overline{CE_1}$ = $\overline{CE_2}$ = V_{IH}, $\overline{OE}$/RFSH = V_{IH}
4. $\overline{CE_1}$ = $\overline{CE_2}$ = V_{IH}, OE/RFSH = V_{IL}
5. $\overline{CE_1}$ = $\overline{CE_2}$ = V_{CC} – 0.2 V, $\overline{OE}$/RFSH = V_{CC} – 0.2 V
6. $\overline{CE_1}$ = $\overline{CE_2}$ = V_{CC} – 0.2 V, $\overline{OE}$/RFSH = 0.2 V

AC CHARACTERISTICS [1,2,3] (T_A = 0 to +70°C, V_{CC} = 5.0 V ±10%)

PARAMETER	SYMBOL	MIN.	MAX.	UNIT	NOTE
Random read, write cycle time	t_{RC}	140		ns	
Read modify write cycle time	t_{RMW}	205		ns	
$\overline{CE}$ pulse width	t_{CE}	80	10,000	ns	
$\overline{CE}$ precharge time	t_P	50		ns	
Address setup time	t_{AS}	0		ns	4
Address hold time	t_{AH}	20		ns	4
Read command setup time	t_{RCS}	0		ns	
Read command hold time	t_{RCH}	0		ns	
$\overline{CE}$ access time	t_{CEA}		80	ns	5
$\overline{OE}$ access time	t_{OEA}		30	ns	5
$\overline{CE}$ to output in Low-Z	t_{CLZ}	20		ns	
$\overline{OE}$ to output in Low-Z	t_{OLZ}	0		ns	
R/W to output in Low-Z	t_{WLZ}	0		ns	
Chip disable to output in High-Z	t_{CHZ}		25	ns	
Output disable to output in High-Z	t_{OHZ}		25	ns	
Write enable to output in High-Z	t_{WHZ}		25	ns	
$\overline{OE}$ setup time	t_{OES}	10		ns	
$\overline{OE}$ hold time	t_{OEH}	10		ns	
$\overline{OE}$ lead time	t_{OEL}	10		ns	
Write command pulse width	t_{WCP}	30		ns	
Write command setup time	t_{WCS}	30		ns	
Write command hold time	t_{WCH}	50		ns	
Data setup time from write	t_{DSW}	30		ns	6
Data setup time from $\overline{CE}$	t_{DSC}	30		ns	6
Data hold time from write	t_{DHW}	0		ns	6
Data hold time from $\overline{CE}$	t_{DHC}	0		ns	6
Transition time (rise and fall)	t_T	3	35	ns	
Refresh time interval	t_{REF}		8	ms	
Auto refresh cycle time	t_{FC}	130		ns	
Refresh delay time from $\overline{CE}$	t_{RFD}	50		ns	
Refresh pulse width (Auto refresh)	t_{FAP}	30	8,000	ns	
Refresh precharge time (Auto refresh)	t_{FP}	30		ns	
$\overline{CE}$ delay time from refresh precharge (Auto refresh)	t_{FCE}	160		ns	
Refresh pulse width (Self refresh)	t_{FAS}	8,000		ns	
$\overline{CE}$ delay time from refresh precharge (Self refresh)	t_{FRS}	160		ns	

NOTES:

1. In order to initialize the circuit, $\overline{CE}_1$, $\overline{CE}_2$ and $\overline{OE}/\overline{RFSH}$ should be kept in V_{IH} for 100 µs after power-up and followed by at least 8 dummy cycles.
2. AC characteristics are measured at t_T = 5 ns.
3. AC characteristics are measured at the following condition (see figure at right).
4. Address is latched at the negative edge of $\overline{CE}_1$ or $\overline{CE}_2$.
5. Measured with a load equivalent to 2TTL + 100 pF.
6. Data is latched at the positive edge of R/W or at the positive edge of $\overline{CE}_1$ or $\overline{CE}_2$.

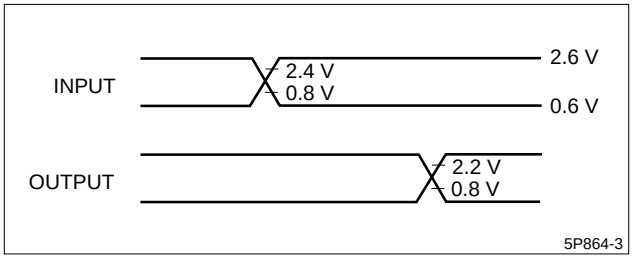


Figure 3. AC Characteristics

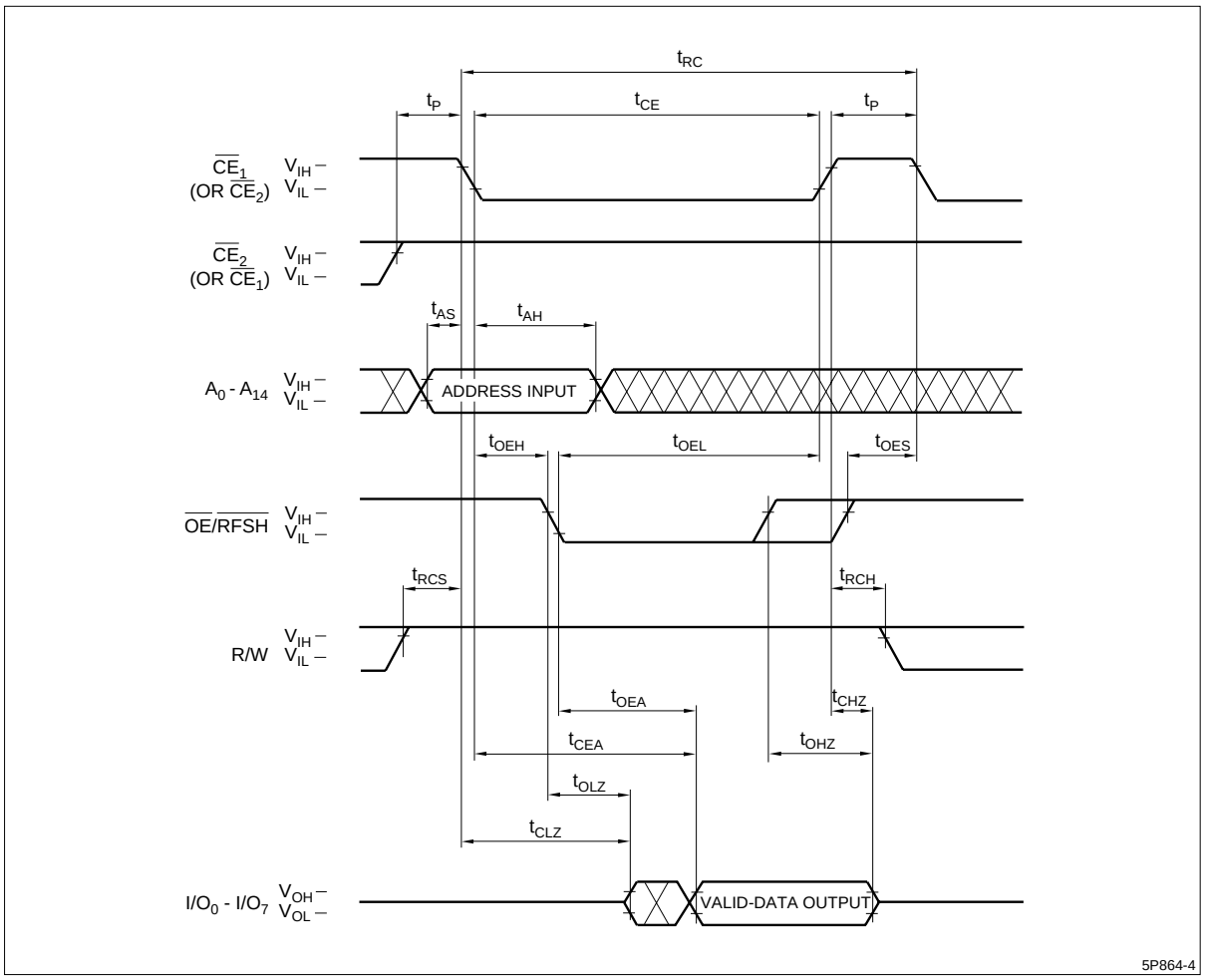


Figure 4. Read Cycle

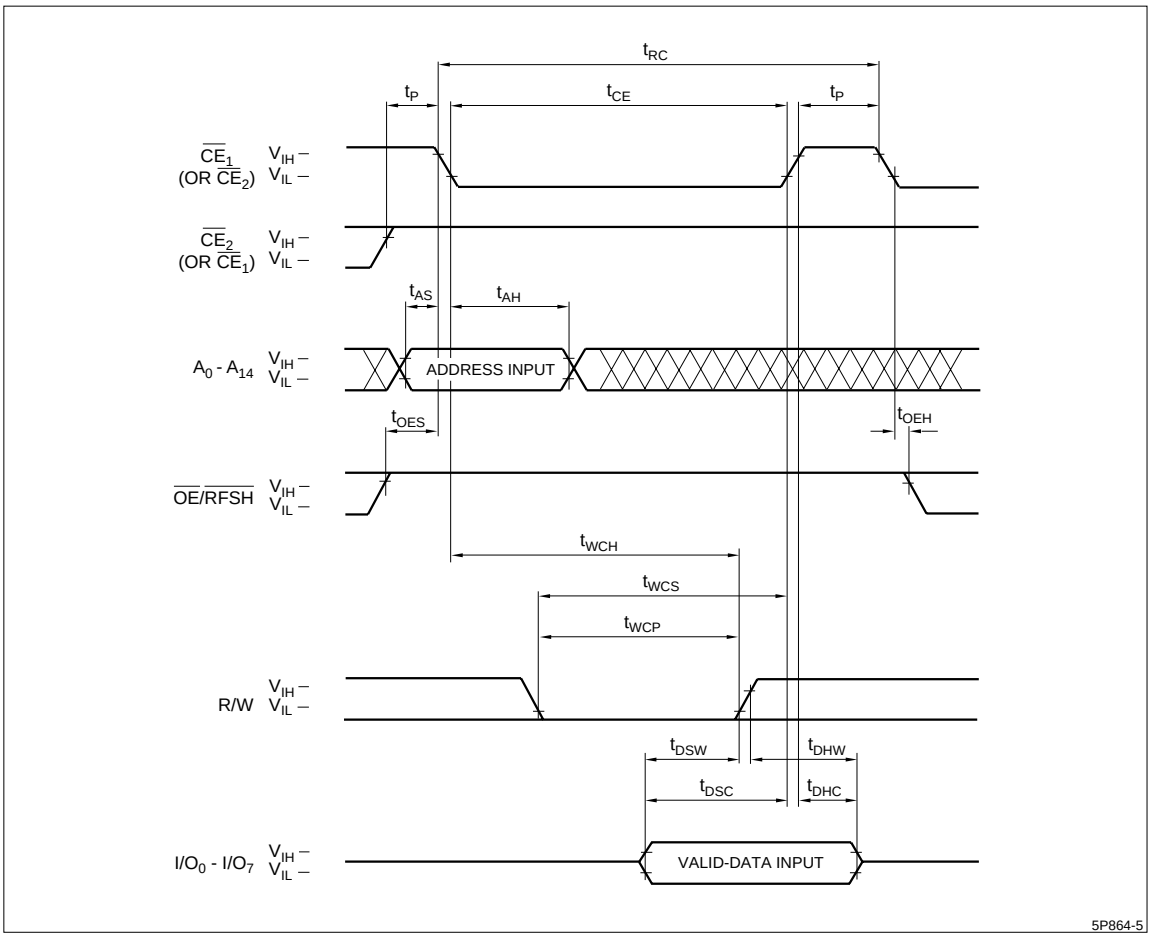


Figure 5. Write Cycle

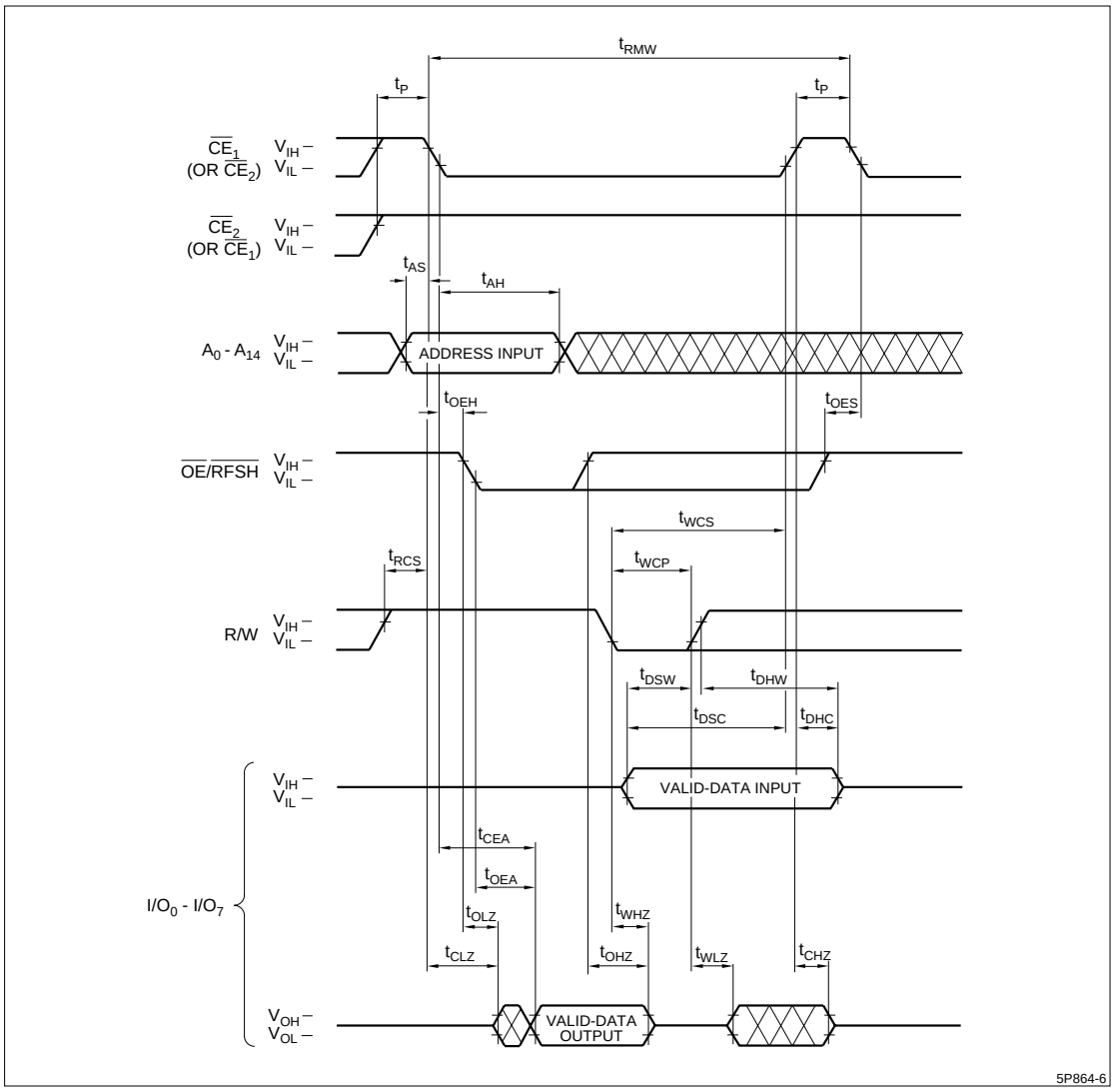


Figure 6. Read-Modify-Write Cycle

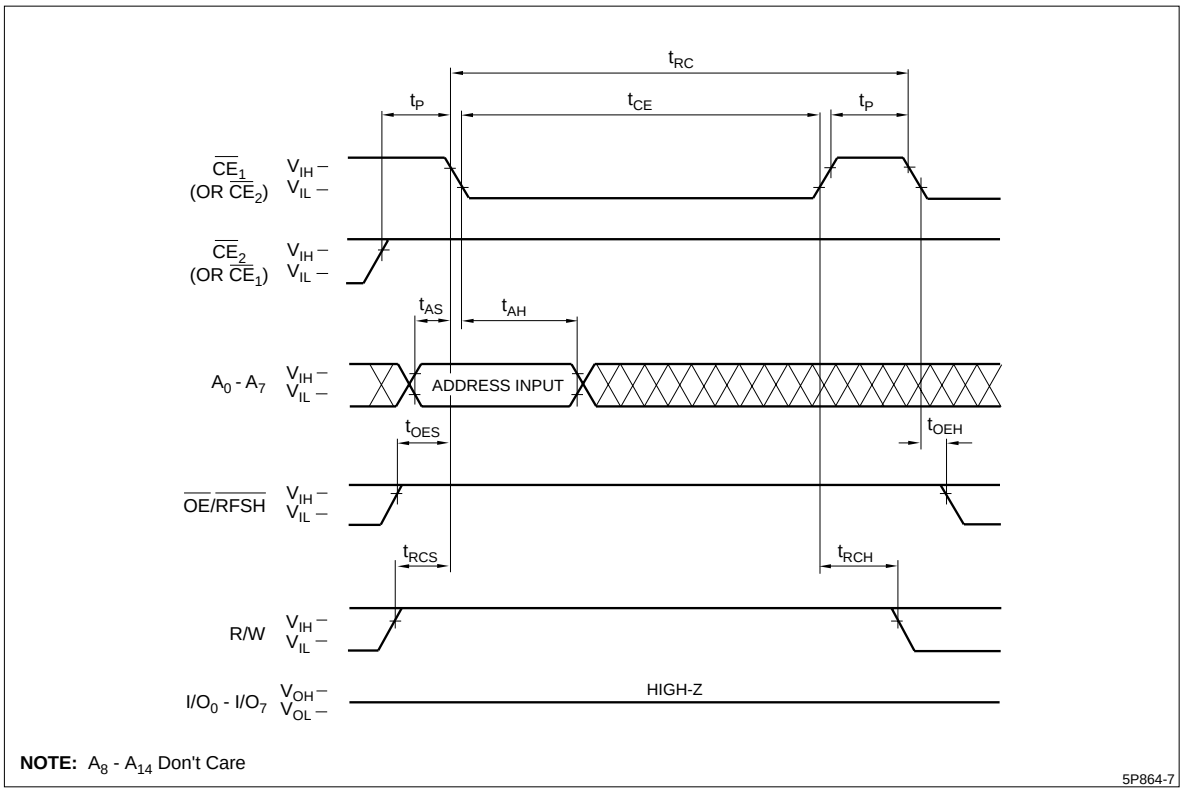


Figure 7. $\overline{CE}$ Only Refresh Cycle

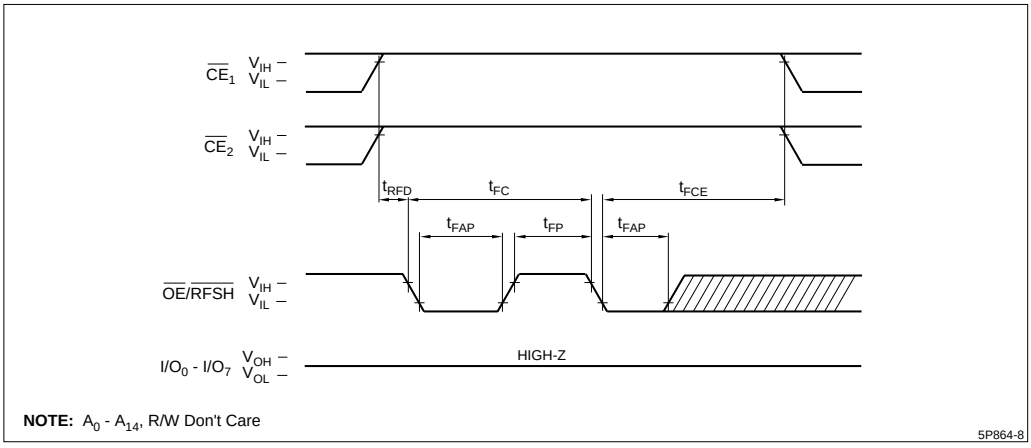


Figure 8. Auto Refresh Cycle

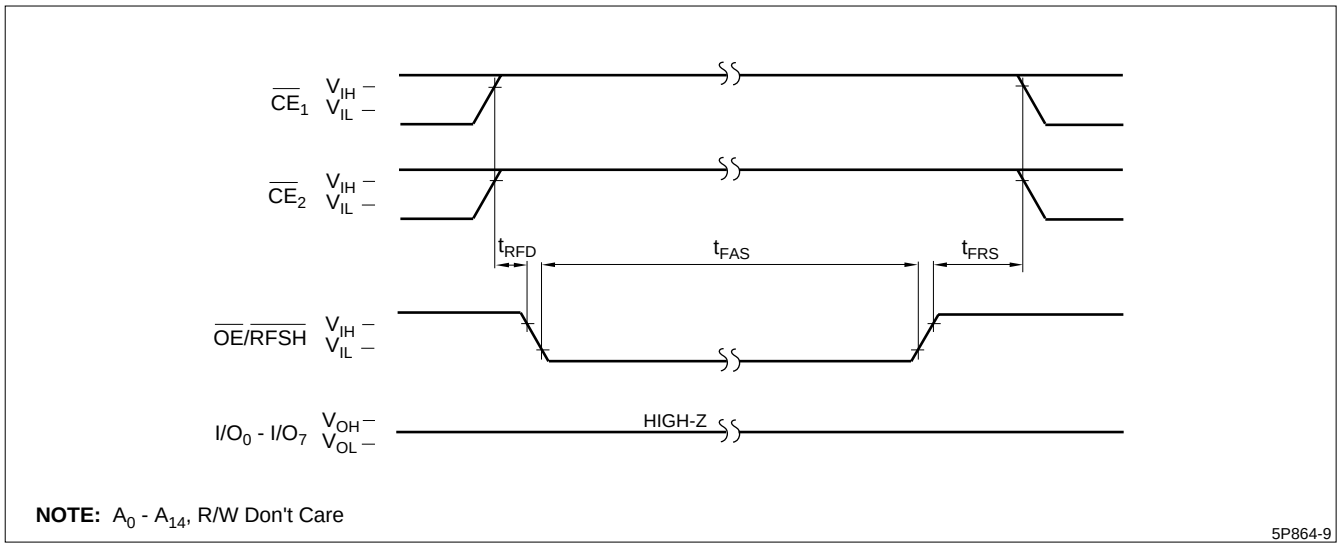
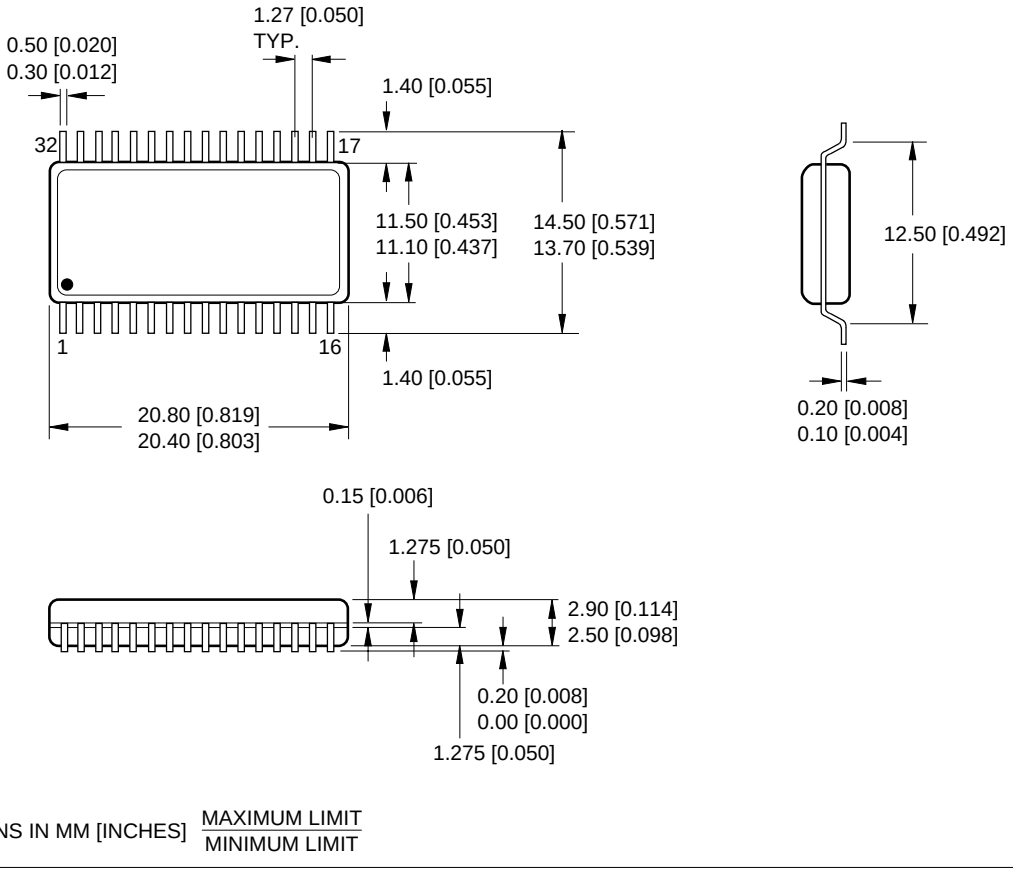


Figure 9. Self Refresh Cycle

PACKAGE DIAGRAM

32SOP (SOP032-P-0525)



32-pin, 525-mil SOP

ORDERING INFORMATION