

LH5P1632

CMOS 512K (32K × 16) Pseudo-Static RAM

FEATURES

- 32,768 × 16 bit organization
- Access time: 80/150 ns (MAX.)
- Cycle time: 140/210 ns (MIN.)
- Single +5 V power supply
- Power consumption (MAX.):
Operating: 467.5/327.5 mW
Standby: 16.5 mW
- TTL compatible I/O
- 256 refresh cycles/4 ms (MAX.)
- Available for auto-refresh mode
- Packages:
40-pin, 600-mil DIP
40-pin, 525-mil SOP

DESCRIPTION

The LH5P1632 is a 512K-bit Pseudo-Static RAM organized as 32,768 × 16 bits. It is fabricated using silicon-gate CMOS process technology.

PIN CONNECTIONS

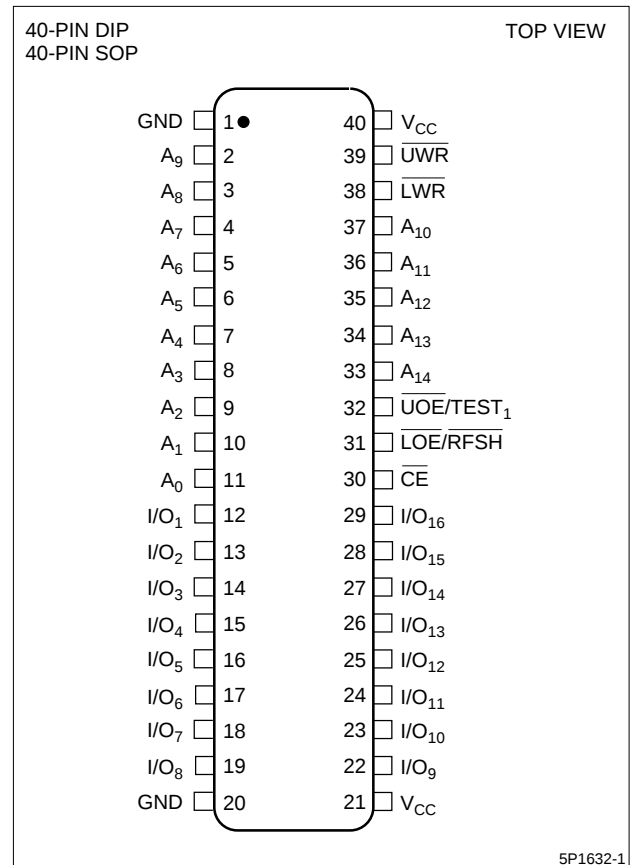


Figure 1. Pin Connections for DIP and SOP Packages

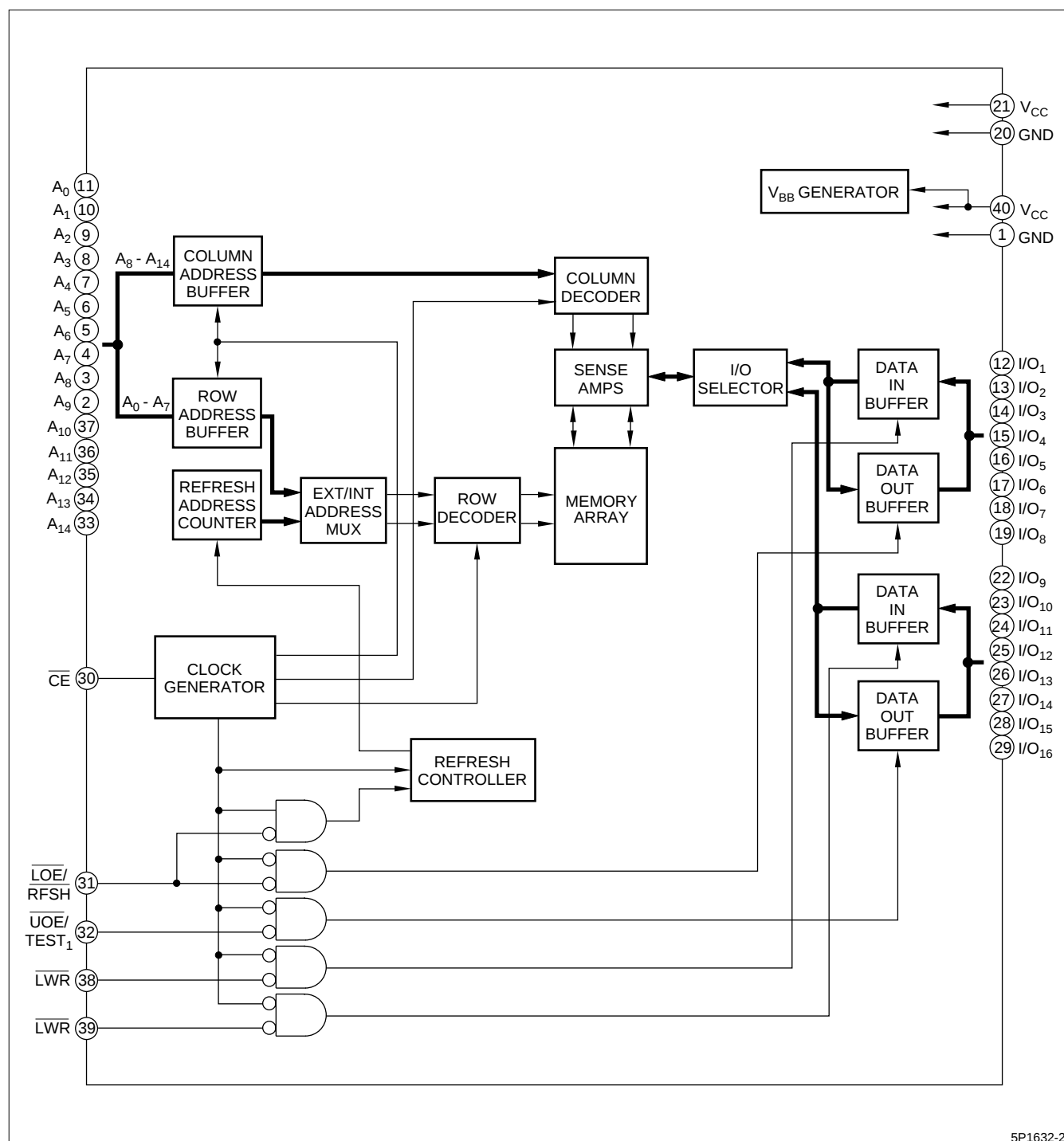


Figure 2. LH5P1632 Block Diagram

PIN DESCRIPTION

SIGNAL	PIN NAME
A ₀ – A ₁₄	Address input
LWR, UWR	Write enable
LOE/RFSH, UOE	Output enable/Refresh input
CE	Chip enable input

SIGNAL	PIN NAME
I/O ₁ – I/O ₁₆	Data input/output
V _{CC}	Power Supply
GND	Ground

ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	RATING	UNIT	NOTE
Applied voltage on all pins	V_T	−1.0 to +7.0	V	1
Output short circuit current	I_O	50	mA	
Power dissipation	P_D	600	mW	
Operating temperature	T_{opr}	0 to +70	°C	
Storage temperature	T_{stg}	−65 to +150	°C	

NOTE:

1. The maximum applicable voltage on any pin with respect to GND.

RECOMMENDED OPERATING CONDITIONS ($T_A = 0$ to +70°C)

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT	NOTE
Supply voltage	V_{CC}	4.5	5.0	5.5	V	
	GND	0	0	0	V	
Input voltage	V_{IH}	2.4		$V_{CC} + 0.3$	V	
	V_{IL}	−0.3		0.8	V	1

NOTE:

1. V_{IL} (MIN.) = −1.0 V when the pulse width is less than 20 ns.

CAPACITANCE ($T_A = 0$ to +70°C, $f = 1$ MHz, $V_{CC} = 5.0$ V $\pm 10\%$)

PARAMETER	CONDITIONS	SYMBOL	MIN.	MAX.	UNIT
Input capacitance	$A_0 - A_{14}$	C_{IN1}		8	pF
	LWR, UWR	C_{IN2}		5	pF
	$\overline{CE}$	C_{IN3}		5	pF
	LOE/RFSH, UOE	C_{IN4}		5	pF
Input/Output capacitance	$I/O_1 - I/O_{16}$	C_{OUT1}		10	pF

DC CHARACTERISTICS ($T_A = 0$ to +70°C, $V_{CC} = 5.0$ V $\pm 10\%$)

PARAMETER	SYMBOL	CONDITIONS	MIN.	MAX.	UNIT	NOTE
Average supply current in normal operation $t_{RC} = t_{RC}$ (MIN)	I_{CC1}	LH5P1632-80		85	mA	1, 2
		LH5P1632-15		65		
Supply current in standby mode	I_{CC2}			3.0	mA	1, 3
Average supply current in CPU internal cycle (LWR = UWR = LOE/RFSH = UOE = V_{IH})	I_{CC3}	LH5P1632-80		85	mA	1, 2
		LH5P1632-15				
Input leakage current	I_{LI}	0 V $\leq V_{IN} \leq 6.5$ V, 0 V except on test pins	−10	10	μ A	
I/O leakage current	I_{LO}	0 V $\leq V_{OUT} \leq V_{CC} + 0.3$ V, Outputs in high-impedance state	−10	10	μ A	
Output HIGH voltage	V_{OH}	$I_{OUT} = -1.0$ mA	2.4		V	
Output LOW voltage	V_{OL}	$I_{OUT} = 4.0$ mA		0.4	V	

NOTES:

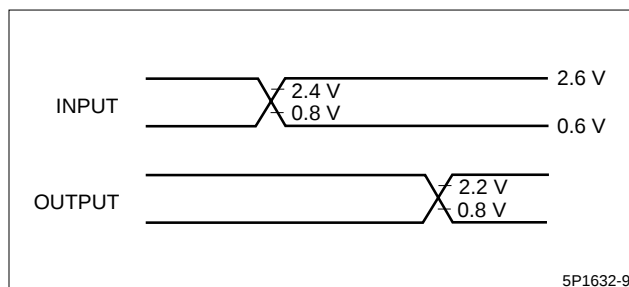
1. Specified values are with outputs open.
2. I_{CC1} and I_{CC3} depend on the cycle time.
3. $\overline{CE}$ = High, LOE/RFSH = High.

AC CHARACTERISTICS ^{1, 2, 3} ($T_A = 0 \text{ to } +70^\circ\text{C}$, $V_{CC} = 5.0 \text{ V} \pm 10\%$)

PARAMETER	SYMBOL	-80 ns		-150 ns		UNIT	NOTE
		MIN.	MAX.	MIN.	MAX.		
READ OR WRITE CYCLE							
Random read, write cycle time	t _{RC}	140		210		ns	
Read modify write cycle time	t _{RMW}	205		280		ns	
CE pulse width	t _{CE}	80	10,000	150	10,000	ns	
CE precharge time	t _p	50		60		ns	
Address setup time	t _{AS}	0		0		ns	4
Address hold time	t _{AH}	20		30		ns	4
Read command setup time	t _{RCS}	0		0		ns	
Read command hold time	t _{RCH}	0		0		ns	
CE access time	t _{CEA}		80		150	ns	5
OE access time	t _{OEA}		30		70	ns	5
CE to output in Low-Z	t _{CLZ}	10		10		ns	
OE to output in Low-Z	t _{OLZ}	0		0		ns	
OE setup time for WR	t _{OSW}	0		0		ns	
Output disable time from CE	t _{CHZ}	0	25	0	35	ns	
Output disable time from OE	t _{OHZ}	0	25	0	35	ns	
Output disable time from WR	t _{WHZ}	0	25	0	35	ns	
OE setup time	t _{OES}	10		10		ns	
OE hold time	t _{OEH}	0		0		ns	
OE lead time	t _{OEL}	10		10		ns	
Write command pulse width	t _{WCP}	60		85		ns	
Write command setup time	t _{WCS}	60		85		ns	
Write command hold time	t _{WCH}	60		85		ns	
Data setup time from WR	t _{DSW}	30		50		ns	
Data setup time from CE	t _{DSC}	30		50		ns	
Data hold time from WR	t _{DHW}	0		0		ns	
Data hold time from CE	t _{DHC}	0		0		ns	
Transition time (rise and fall)	t _T	3	35	3	35	ns	
Refresh time interval	t _{REF}		4		4	ms	
REFRESH CYCLE							
Auto refresh cycle time	t _{FC}	140		190		ns	
Refresh delay time from CE	t _{RFD}	50		60		ns	
Refresh pulse width (Auto Refresh)	t _{FAP}	30	8,000	80	8,000	ns	
Refresh precharge time (Auto Refresh)	t _{FP}	40		30		ns	
CE delay time from Refresh active (Auto Refresh)	t _{FCE}	160		225		ns	

NOTES:

1. In order to initialize the circuit, $\overline{CE}$ and $\overline{OEL}/\overline{RFSH}$ should be kept V_{IH} for 200 μs after power on and followed by at least 8 dummy cycles.
2. AC characteristics shall be tested with $t_T = 5 \text{ ns}$.
3. AC characteristics are measured at the following condition (see figure at right).
4. Address is latched at the negative edge of $\overline{CE}$.
5. Measured with a load equivalent to 2TTL + 100 pF.
6. Data for the lower byte (I/O_1 to I/O_8) is latched at the positive edge of $\overline{LWR}$ or the positive edge of $\overline{CE}$. Data for the upper byte (I/O_9 to I/O_{16}) is latched at the positive edge of $\overline{UWR}$ or the positive edge of $\overline{CE}$.

**Figure 3. AC Characteristics**

TRUTH TABLE

INPUT					OUTPUT		MODE		NOTE
$\overline{CE}$	$\overline{UOE}$	$\overline{LOE/RFSH}$	$\overline{UWR}$	$\overline{LWR}$	$I/O_9 - I/O_{16}$	$I/O_1 - I/O_8$	UPPER BYTE	LOWER BYTE	
H	D	D	D	D	High-Z	High-Z	Standby		
L	L	L	H	H	D_{OUT}	D_{OUT}	Read	Read	
L	H	L	H	H	High-Z	D_{OUT}	CE only refresh	Read	
L	L	H	H	H	D_{OUT}	High-Z	Read	CE only refresh	
L	H	H	H	H	High-Z	High-Z	CE only refresh	CE only refresh	
L	D	D	L	L	D_{IN}	D_{IN}	Write	Write	
L	D	H	L	H	D_{IN}	High-Z	Write	CE only refresh	
L	H	D	H	L	High-Z	D_{IN}	CE only refresh	Write	
L	D	L	L	H	D_{IN}	D_{OUT}	Write	Read	Inhibit
L	L	D	H	L	D_{OUT}	D_{IN}	Read	Write	Inhibit
H	D		D	D	High-Z	High-Z	Auto Refresh		

NOTES:

D = Don't care.

High-Z = High impedance.

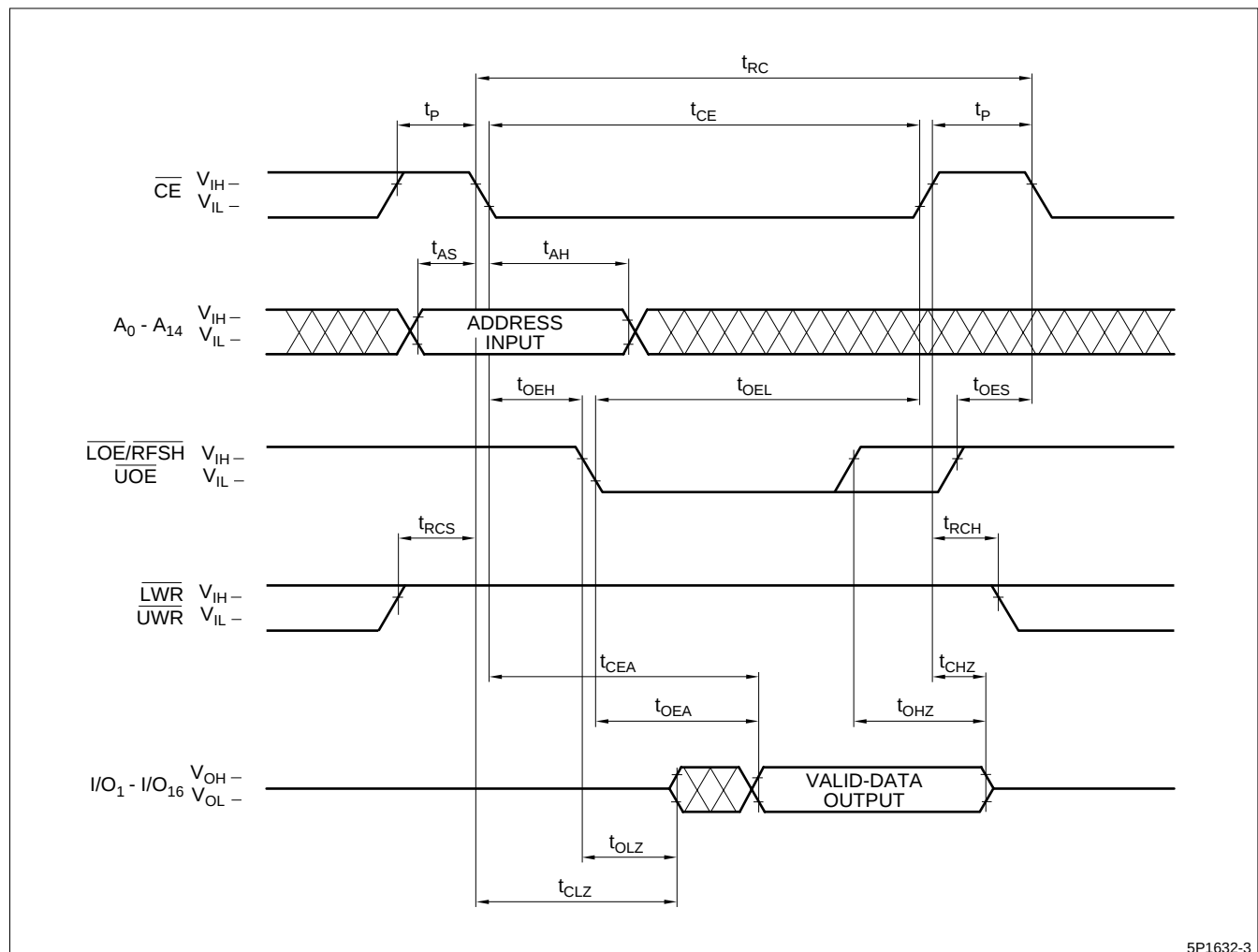


Figure 4. Read Cycle

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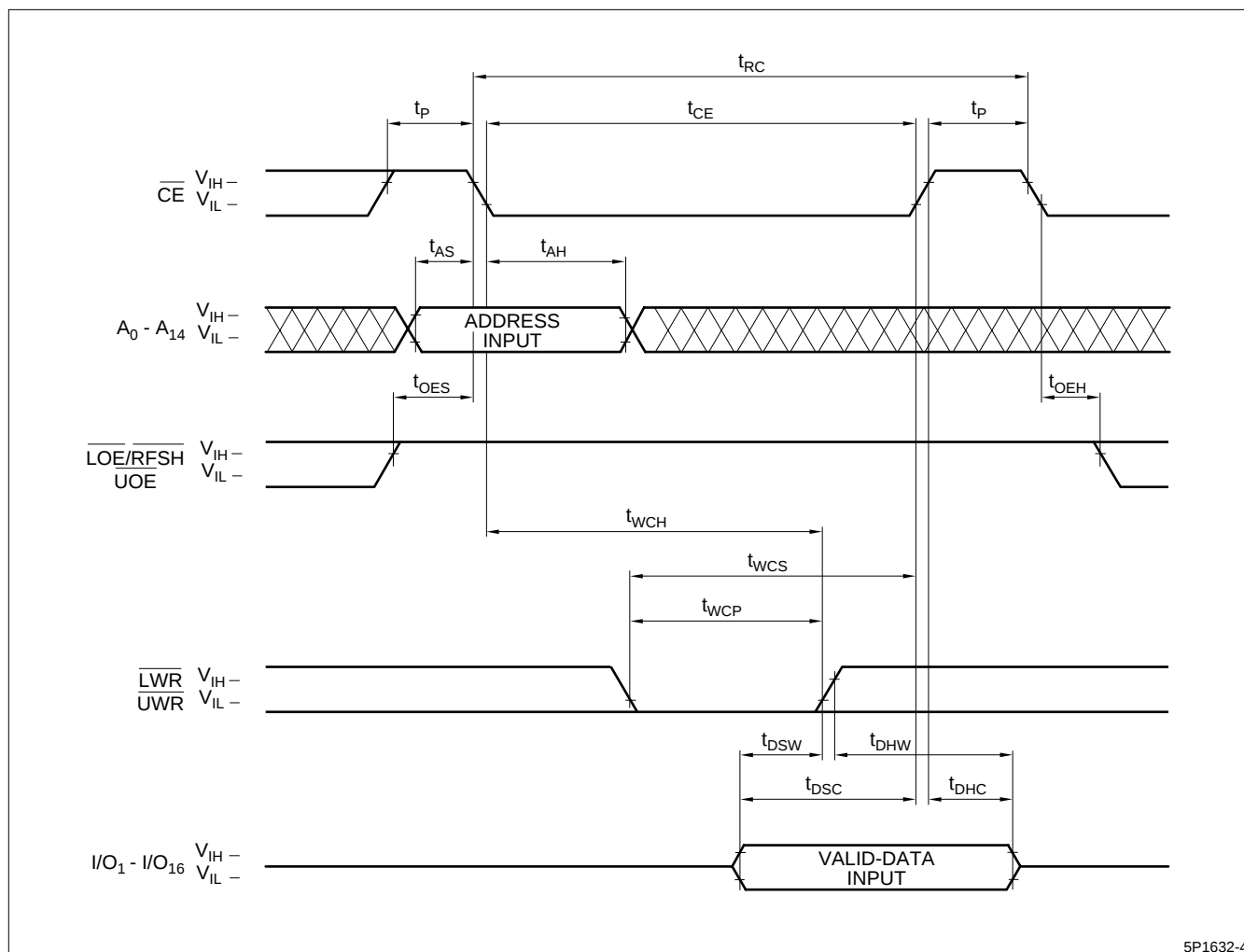
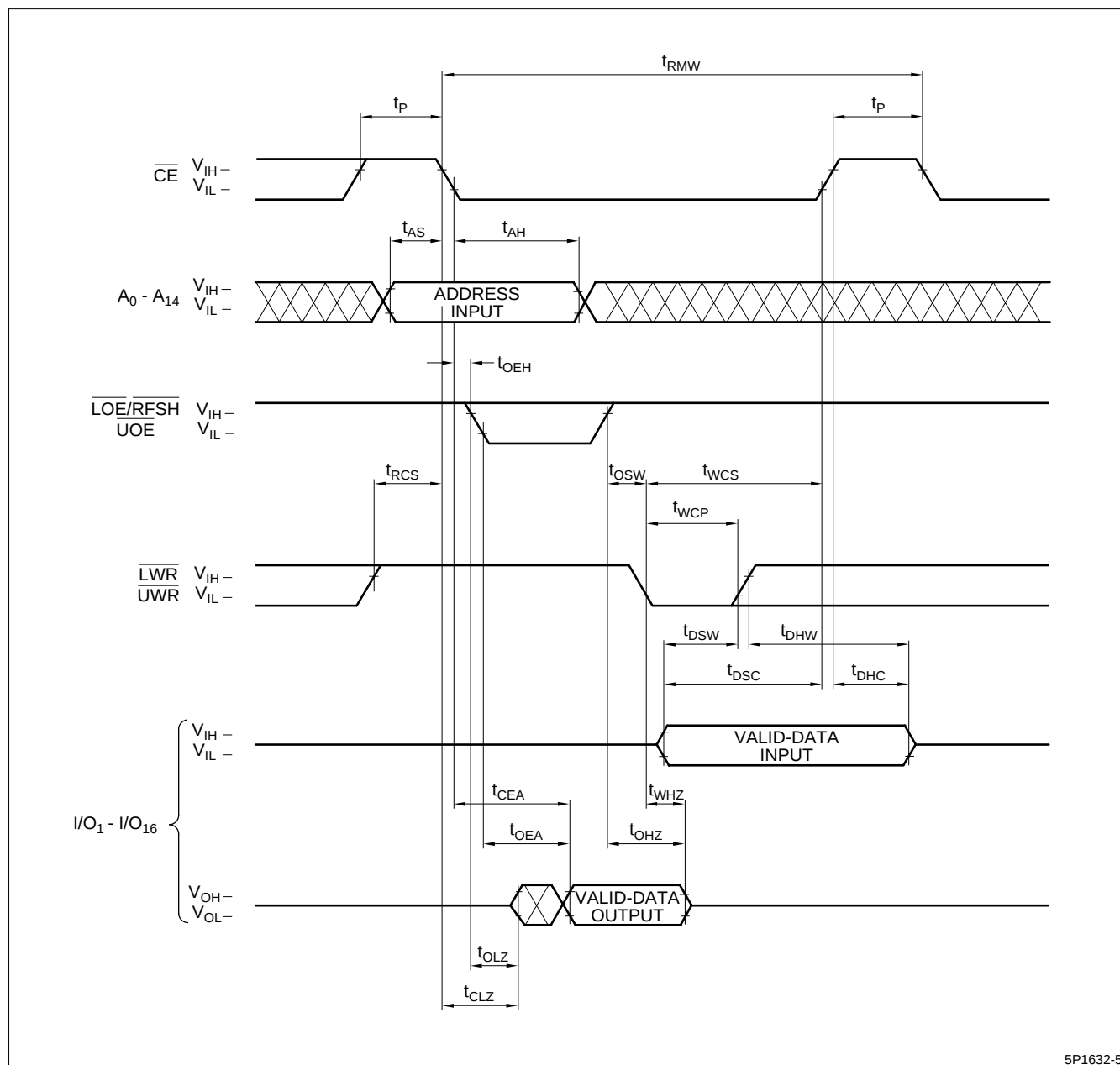


Figure 5. Write Cycle



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Figure 6. Read-Write Cycle

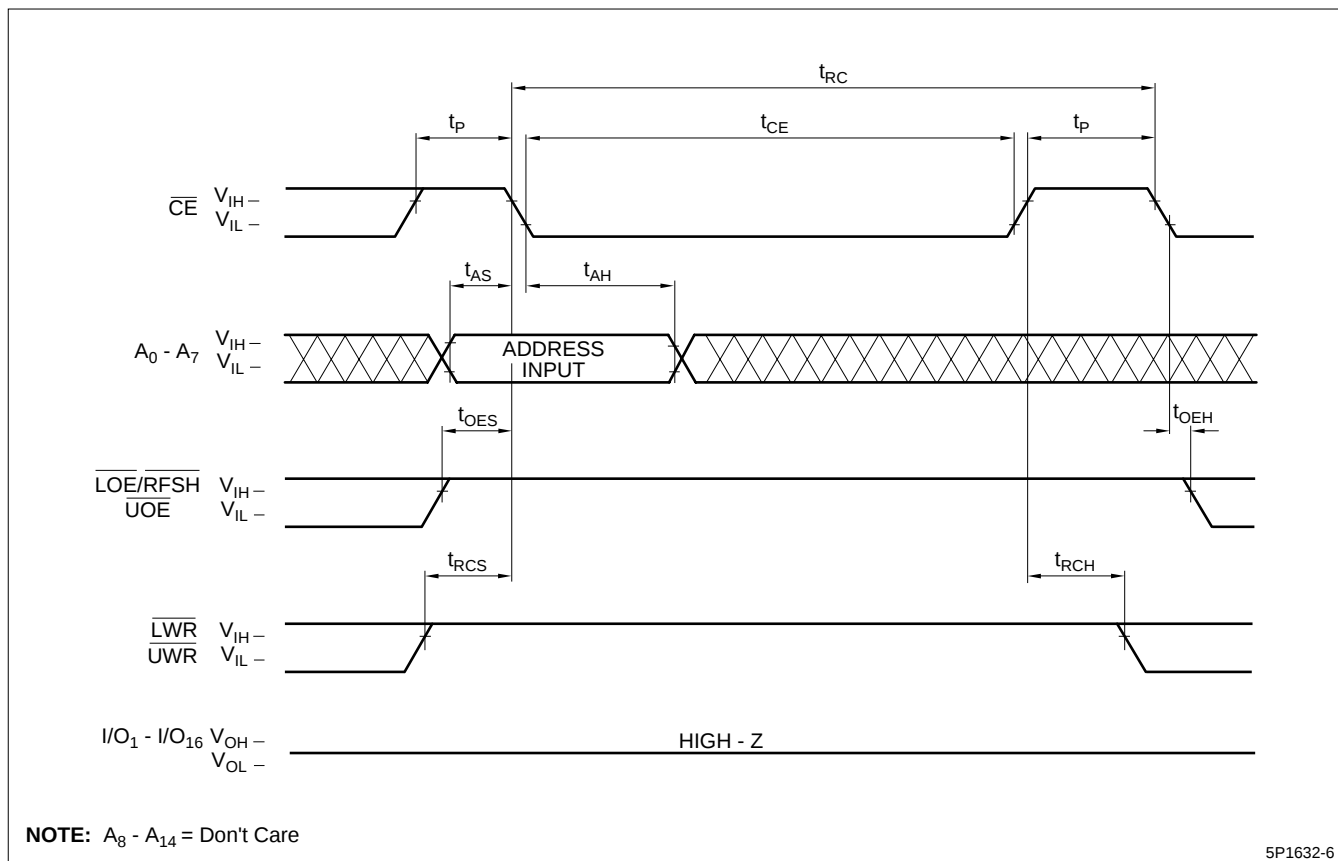


Figure 7. CE Only Refresh Cycle

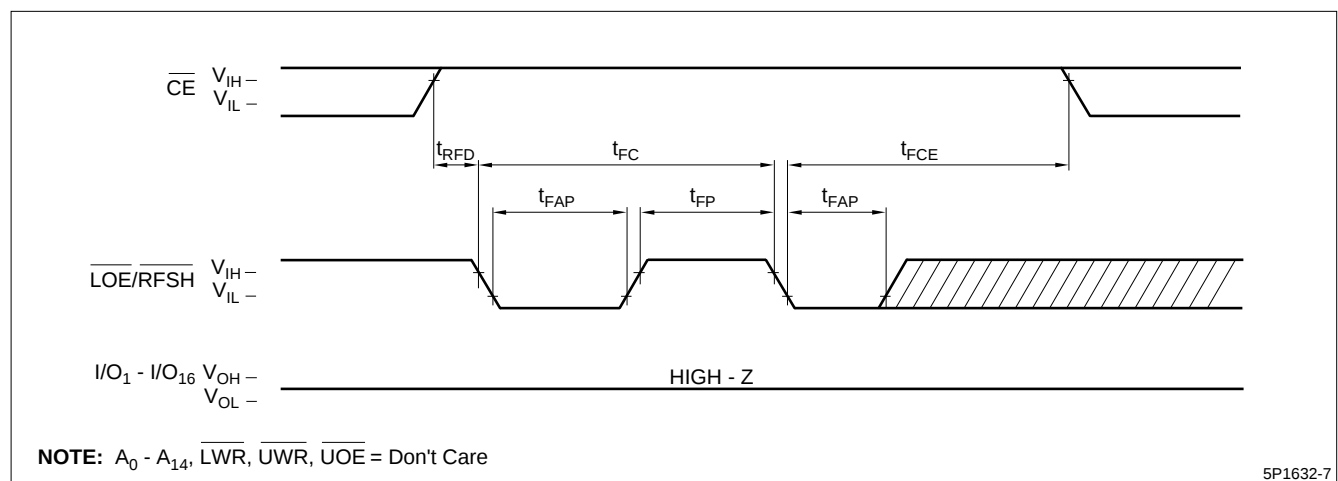
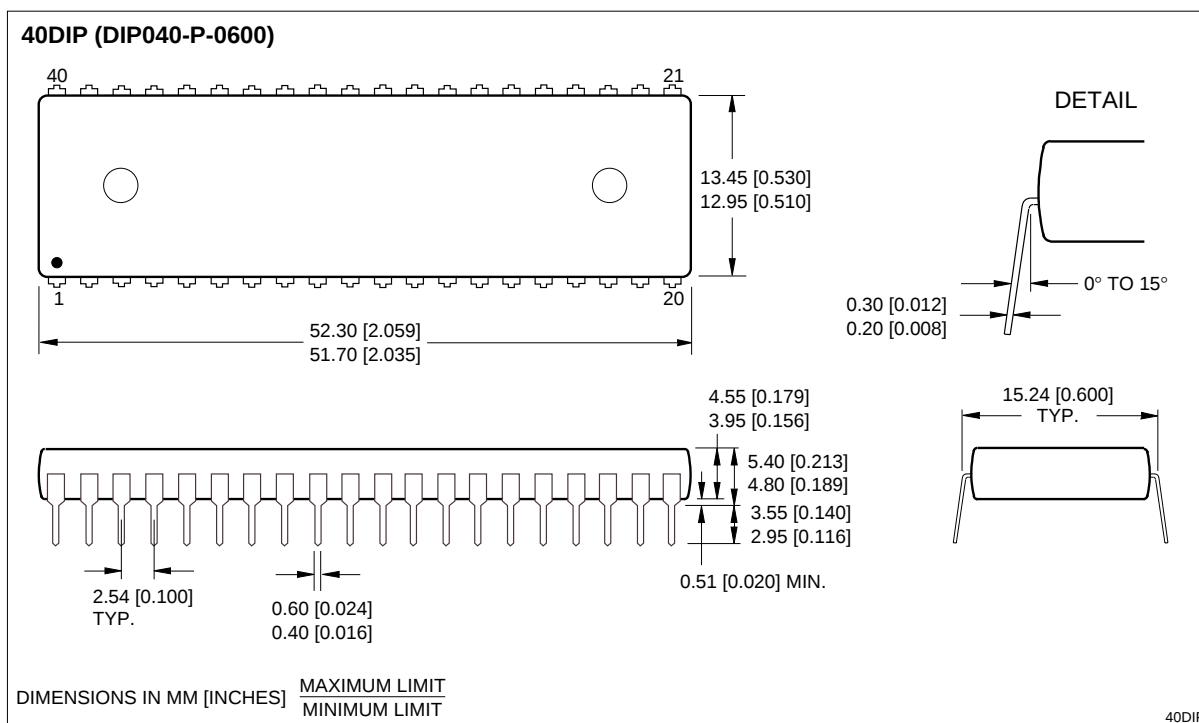
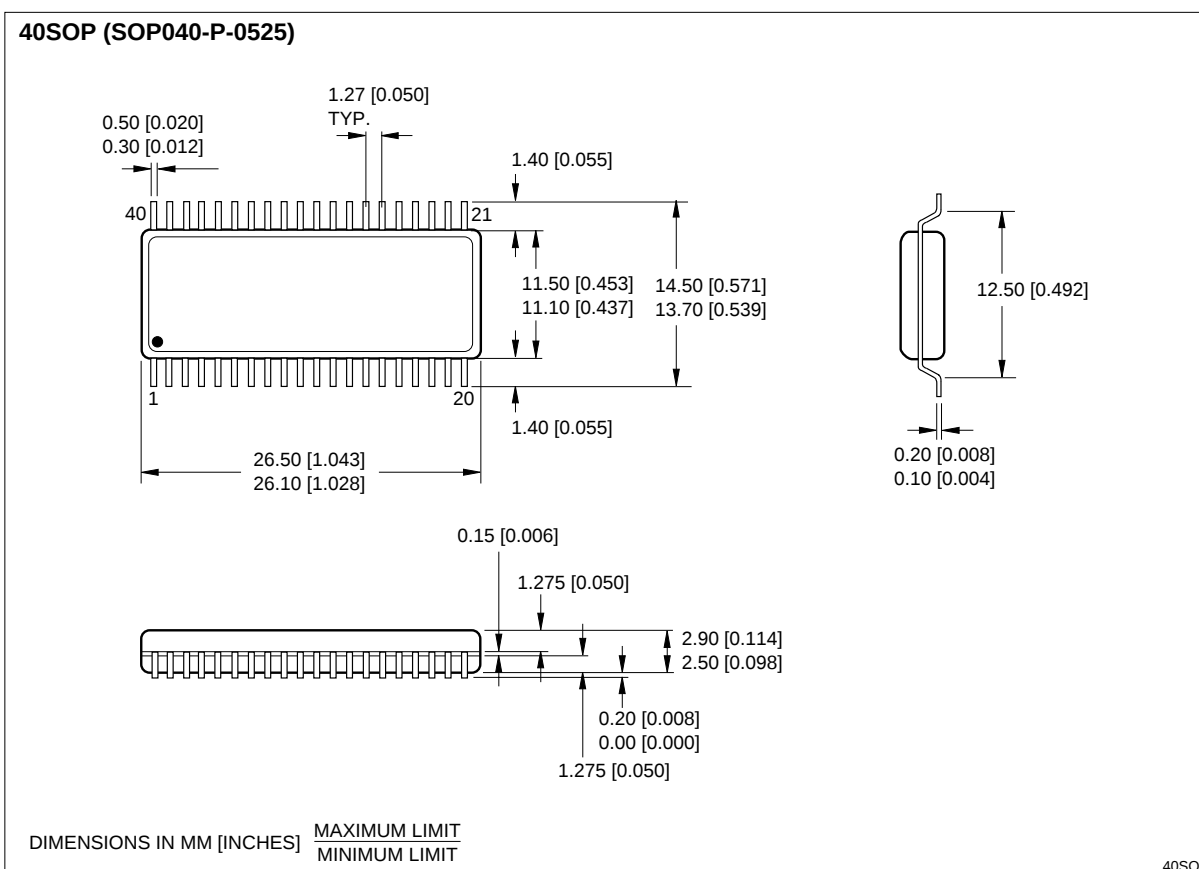


Figure 8. Auto Refresh Cycle

PACKAGE DIAGRAMS



40-pin, 600-mil DIP



40-pin, 525-mil SOP

ORDERING INFORMATION

