Laurel Electronics Co., Ltd.

LCD Module Specification

Model No.: LG1601601-FFDWHUV
LG1601601-LMDWHUV

Table of Contents

RECORD OF REVISION

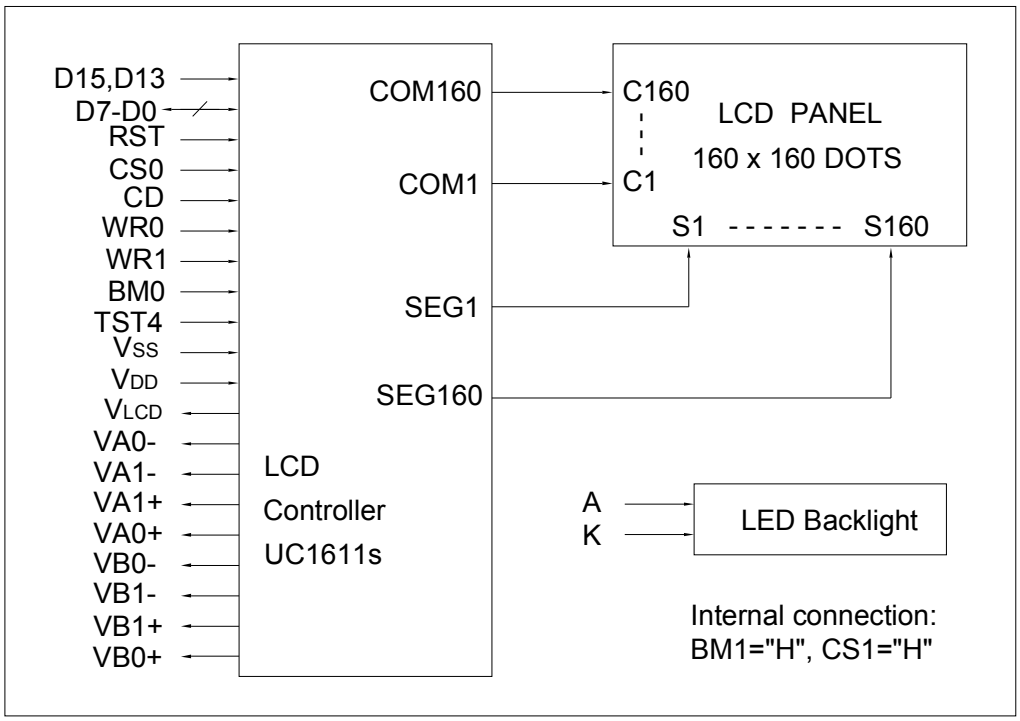
Rev.	Date	Page	Item	Description
0.1	2009/11/28	-	-	New release
0.2	2010/10/26	2	1.1	Remove BMDWH6V and SFDWH6V LCD type
0.3	2011/10/31	16	6	Modify power on Initialization code
0.4	2012/03/22	13	5	Add description of anti-interference capacitors

1. BASIC SPECIFICATIONS

1.1 Features

Item		Specifications	Unit
Display Format		160 x 160	dot
LCD Type	FFDWHUV	FSTN - Positive - Transflective Black characters on white background	-
	LMDWHUV	FSTN - Blue - Negative - Transmissive Pure white characters on blue background	-
Driving Method		1/160 Duty, 1/11 Bias	-
Viewing Direction		12	O'clock
Backlight & Color		LED, white color	-
Outline Dimension (WxHxT)		62.0 x 69.0 x 9.6 (FPC length not included)	mm
Viewing Area (WxH)		55.0 x 55.0	mm
Active Area (WxH)		47.98 x 47.98	mm
Dot Pitch (WxH)		0.30 x 0.30	mm
Dot Size (WxH)		0.28 x 0.28	mm
Weight		33	g
Controller		UC1611s (COG)	-
Interface		4-bit/8-bit parallel, 3/4 wire SPI or I^2C	-
Power Supply (V_{DD})		2.7 to 3.6	V

1.2 Block Diagram



1.3 Terminal Functions (FPC)

<table>
<tr><th>Pin No.</th><th>Symbol</th><th>Level</th><th>Function</th></tr>
<tr><td>1</td><td>VB0+</td><td>-</td><td rowspan="4">LCD Bias Voltages. These voltages are generated internally by UC1611s.
Connect a 4.7uF/6.3V capacitor between VB0+ and VB0–.
Connect a 4.7uF/6.3V capacitor between VB1+ and VB1–.</td></tr>
<tr><td>2</td><td>VB1+</td><td>-</td></tr>
<tr><td>3</td><td>VB1-</td><td>-</td></tr>
<tr><td>4</td><td>VB0-</td><td>-</td></tr>
<tr><td>5</td><td>VA0+</td><td>-</td><td rowspan="4">LCD Bias Voltages. These voltages are generated internally by UC1611s.
Connect a 4.7uF/6.3V capacitor between VA0+ and VA0–.
Connect a 4.7uF/6.3V capacitor between VA1+ and VA1–.</td></tr>
<tr><td>6</td><td>VA1+</td><td>-</td></tr>
<tr><td>7</td><td>VA1-</td><td>-</td></tr>
<tr><td>8</td><td>VA0-</td><td>-</td></tr>
<tr><td>9</td><td>VLCD</td><td>-</td><td>LCD driving voltage. VLCD is generated internally by UC1611s.
Connect a 0.47uF/25V capacitor and a 10MΩ resistor to VSS.</td></tr>
<tr><td>10</td><td>VDD</td><td>2.7 to 3.6V</td><td>Power supply for logic and charge pump</td></tr>
<tr><td>11</td><td>VSS</td><td>0V</td><td>Ground</td></tr>
<tr><td>12</td><td>TST4</td><td>-</td><td>No connection</td></tr>
<tr><td>13</td><td>BM0</td><td>-</td><td>Bus mode selection</td></tr>
<tr><td>14</td><td>WR1</td><td rowspan="2">H/L</td><td rowspan="2">WR[1:0] control the read/write operation of the host interface.
In 8080 mode: WR0 is /WR signal, WR1 is /RD signal.
In 6800 mode: WR0 is R/W signal, WR1 is Enable signal.
In serial modes: These two pins are not used, connect them to VSS.</td></tr>
<tr><td>15</td><td>WR0</td></tr>
<tr><td>16</td><td>CD</td><td>H/L</td><td>Data or instruction selection
L: D0 to D7 are Instruction code H: D0 to D7 are display data
In S9 and I2C mode, CD pin is not used, connect it to VSS.</td></tr>
<tr><td>17</td><td>CS0</td><td>L</td><td>Chip selection signal. Active “L”.</td></tr>
<tr><td>18</td><td>RST</td><td>L</td><td>Reset signal. Active “L”. There is built-in power-on-reset circuit in UC1611s. Connect RST to VDD when it is not used.</td></tr>
<tr><td>19</td><td>D0</td><td rowspan="8">H/L</td><td rowspan="8">Bi-directional bus for parallel host interfaces. In serial modes, connect D0 to SCK, D3 to SDA and D[15,13] to VDD or VSS.
<table>
<tr><th></th><th>BM[1:0]=1x
8-bit parallel</th><th>BM[1:0]=1x
4-bit parallel</th><th>BM[1:0]=1x
S8/S9</th><th>BM[1:0]=11
I2C</th></tr>
<tr><td>D0</td><td>D0</td><td>D0/D4</td><td>SCK</td><td>SCK</td></tr>
<tr><td>D1</td><td>D1</td><td>D1/D5</td><td>–</td><td>–</td></tr>
<tr><td>D2</td><td>D2</td><td>D2/D6</td><td>–</td><td>–</td></tr>
<tr><td>D3</td><td>D3</td><td>D3/D7</td><td>SDA</td><td>SDA</td></tr>
<tr><td>D4</td><td>D4</td><td>–</td><td>–</td><td>–</td></tr>
<tr><td>D5</td><td>D5</td><td>–</td><td>–</td><td>–</td></tr>
<tr><td>D6</td><td>D6</td><td>–</td><td>–</td><td>–</td></tr>
<tr><td>D7</td><td>D7</td><td>–</td><td>1</td><td>1</td></tr>
<tr><td>D13</td><td>0</td><td>1</td><td>0</td><td>1</td></tr>
<tr><td>D15</td><td>0</td><td>0</td><td>1</td><td>1</td></tr>
</table>
Connect unused pins to VDD or VSS.</td></tr>
<tr><td>20</td><td>D1</td></tr>
<tr><td>21</td><td>D2</td></tr>
<tr><td>22</td><td>D3</td></tr>
<tr><td>23</td><td>D4</td></tr>
<tr><td>24</td><td>D5</td></tr>
<tr><td>25</td><td>D6</td></tr>
<tr><td>26</td><td>D7</td></tr>
<tr><td>27</td><td>D13</td><td rowspan="2">H/L</td><td rowspan="2">Bus mode selection. The interface bus mode is determined by BM[1:0] and D[15,13] by the following relationship.
<table>
<tr><th>BM[1:0]</th><th>D15, D13</th><th>Mode</th></tr>
<tr><td>10</td><td>00</td><td>8080/8-bit</td></tr>
<tr><td>11</td><td>00</td><td>6800/8-bit</td></tr>
<tr><td>10</td><td>01</td><td>8080/4-bit</td></tr>
<tr><td>11</td><td>01</td><td>6800/4-bit</td></tr>
<tr><td>10</td><td>10</td><td>4-wire SPI (S8)</td></tr>
<tr><td>11</td><td>10</td><td>3-wire SPI (S9)</td></tr>
<tr><td>11</td><td>11</td><td>2-wire SPI (I2C)</td></tr>
</table></td></tr>
<tr><td>28</td><td>D15</td></tr>
</table>

Note: BM1 and CS1 are fixed to “H” on ITO glass.

2. ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Min.	Max.	Unit
Supply Voltage (Logic & Charge Pump)	VDD	-0.3	4.0	V
LCD Generated Voltage	VLCD	-0.3	19.8	V
Input Voltage	VIN	-0.4	VDD+0.5	V
Operating Temperature	Topr	-20	+70	°C
Storage Temperature	Tstg	-30	+80	°C

3. ELECTRICAL CHARACTERISTICS

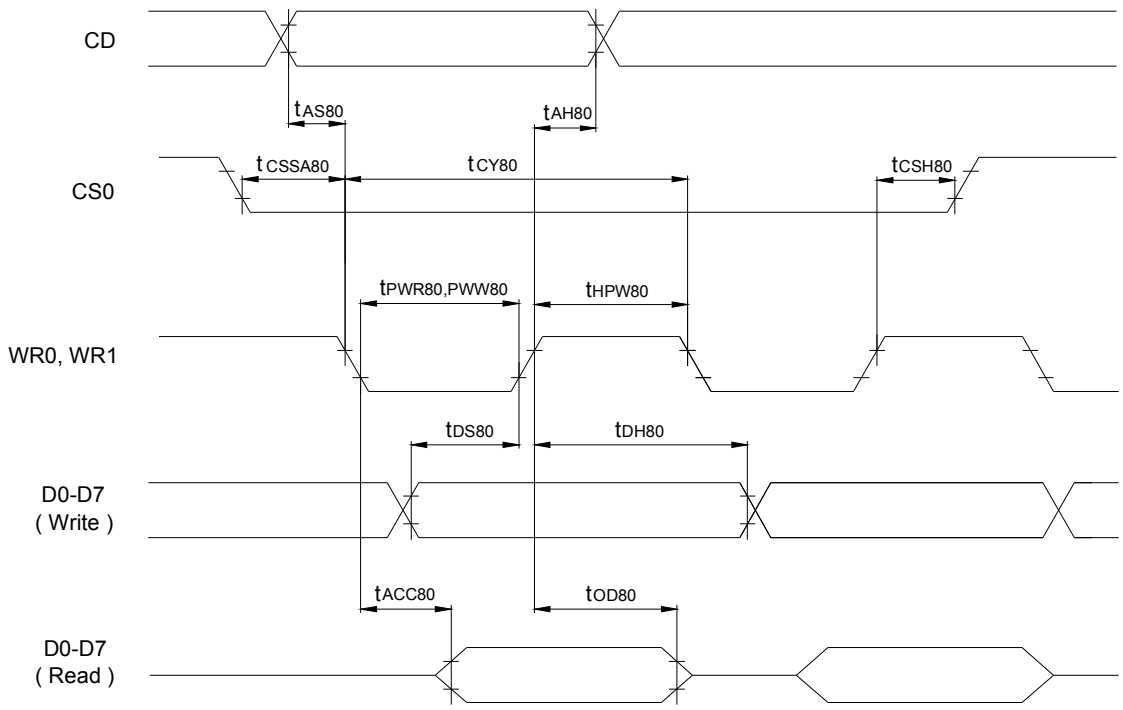
3.1 DC Characteristics (Ta=25°C)

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Supply Voltage (Logic & Charge Pump)	VDD		2.7	3.3	3.6	V
Charge Pump Output Voltage	VLCD		-	16.8	17.5	V
Input Low Voltage	VIL		0	-	0.2VDD	V
Input High Voltage	VIH		0.8VDD	-	VDD	V
Output Low Voltage	VOL		0	-	0.2VDD	V
Output High Voltage	VOH		0.8VDD	-	VDD	V
Supply Current (B/W mode)	IDD	VDD=3.3V VLCD=16.8V	-	1.0	1.5	mA
Supply Current (4/8-shade mode)			-	1.5	2.0	mA

3.2 Parallel Bus Timing Characteristics (8080 Series MPU, VDD=2.7V to 3.6V, Ta=25°C)

Description	Signal	Symbol	Condition	Min.	Max.	Unit
Address setup time Address hold time	CD	t_{AS80} t_{AH80}		0 0	-	ns
System cycle time 8 bits bus (read) (write) 4 bits bus (read) (write)	WR0, WR1	t_{CY80}		 180 160 130 100	-	
Low pulse width 8 bits bus (read) (write) 4 bits bus (read) (write)	WR0, WR1	t_{PWR80} t_{PWW80}		 75 65 50 35	-	
High pulse width 8 bits bus (read) (write) 4 bits bus (read) (write)	WR0, WR1	t_{HPW80}		 75 65 50 35	-	
Data setup time Data hold time	D0 to D7	t_{DS80} t_{DH80}		30 0	-	
Read access time Output disable time	D0 to D7	t_{ACC80} t_{OD80}	CL=100pF	- 30	60 -	
Chip select setup time Chip select hold time	CS0	t_{CSSA80} t_{CSH80}		0 0	-	

Note: The rising time and the falling time are stipulated to be equal to or less than 15ns.

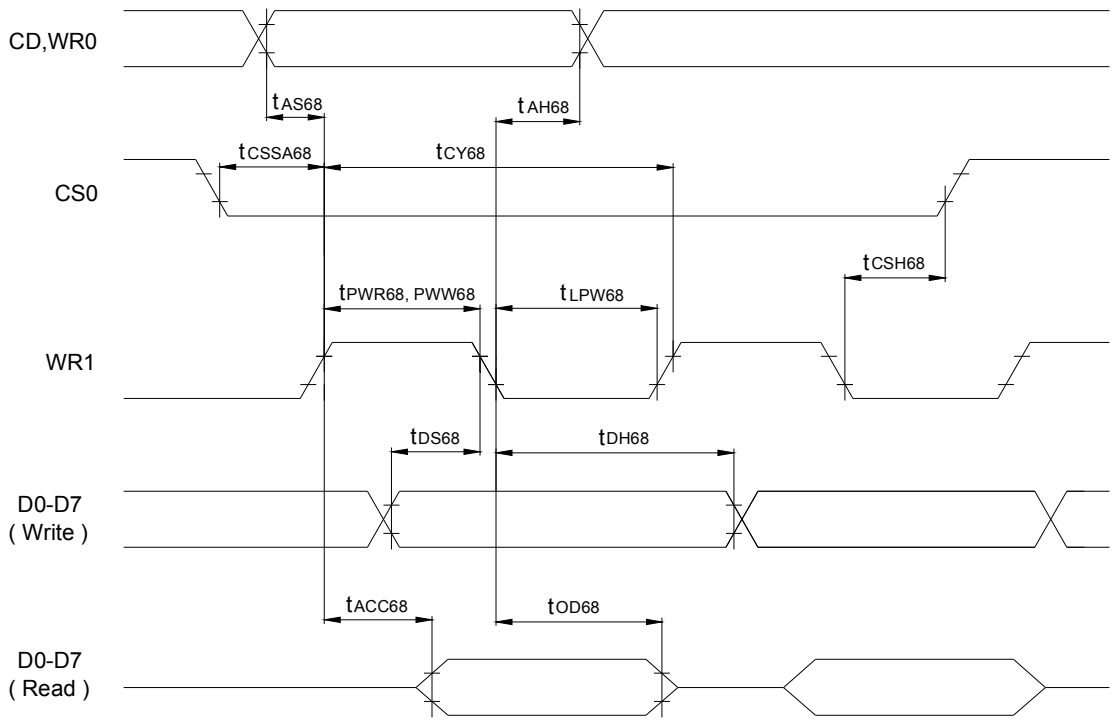


Parallel Bus Timing Characteristics (for 8080 MPU)

3.3 Parallel Bus Timing Characteristics (6800 Series MPU, VDD=2.7V to 3.6V, Ta=25°C)

Description	Signal	Symbol	Condition	Min.	Max.	Unit
Address setup time Address hold time	CD, WR0	t_{AS68} t_{AH68}		0 0	-	ns
System cycle time 8 bits bus (read) (write) 4 bits bus (read) (write)	WR1	t_{CY68}		 180 160 130 100	-	
Pulse width 8 bits (read) 4 bits	WR1	t_{PWR68}		75 50	-	
Pulse width 8 bits (write) 4 bits	WR1	t_{PWW68}		65 35	-	
Low pulse width 8 bits bus (read) (write) 4 bits bus (read) (write)	WR1	t_{LPW68}		 75 65 50 35	-	
Data setup time Data hold time	D0 to D7	t_{DS68} t_{DH68}		30 0	-	
Read access time Output disable time	D0 to D7	t_{ACC68} t_{OD68}	CL=100pF	- 30	60 -	
Chip select setup time Chip select hold time	CS0	t_{CSSA68} t_{CSH68}		0 0	-	

Note: The rising time and the falling time are stipulated to be equal to or less than 15ns.

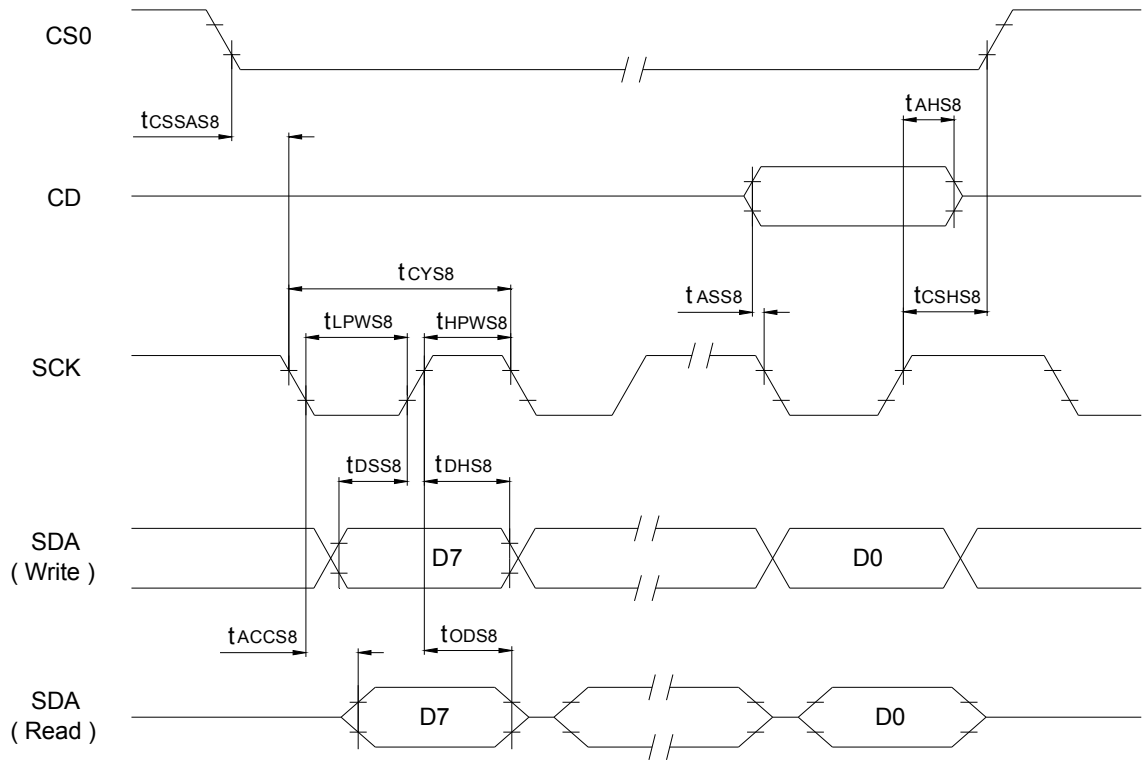


Parallel Bus Timing Characteristics (for 6800 MPU)

3.4 Serial Bus Timing Characteristics (for S8, VDD=2.7V to 3.6V, Ta=25°C)

Description	Signal	Symbol	Condition	Min.	Max.	Unit
Address setup time	CD	t_{ASS8}		0	-	ns
Address hold time		t_{AHS8}		0	-	
System cycle time (read) (write)	SCK	t_{CYS8}		150 51	-	
Low pulse width (read) (write)		t_{LPWS8}		60 18	-	
High pulse width (read) (write)		t_{HPWS8}		60 18	-	
Read access time Output disable time	SDA	t_{ACCS8} t_{ODS8}		- 15	50 -	
Data setup time Data hold time	SDA	t_{DSS8} t_{DHS8}		15 0	-	
Chip select setup time Chip select hold time	CS0	t_{CSSAS8} t_{CSHS8}		0 0	-	

Note: The rising time and the falling time are stipulated to be equal to or less than 15ns.

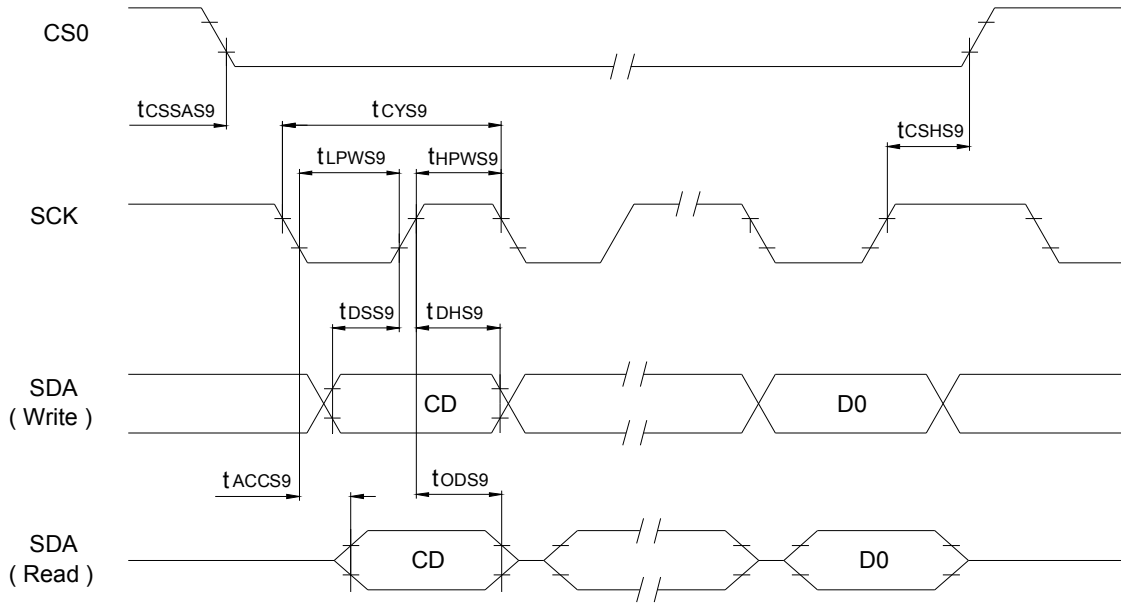


Serial Bus Timing Characteristics (for S8)

3.5 Serial Bus Timing Characteristics (for S9, VDD=2.7V to 3.6V, Ta=25°C)

Description	Signal	Symbol	Condition	Min.	Max.	Unit
System cycle time (read) (write)	SCK	t_{CYS9}		150 51	-	
Low pulse width (read) (write)		t_{LPWS9}		60 18	-	
High pulse width (read) (write)		t_{HPWS9}		60 18	-	
Read access time Output disable time	SDA	t_{ACCS9} t_{ODS9}		-- 15	50 -	
Data setup time Data hold time	SDA	t_{DSS9} t_{DHS9}		15 0	-	
Chip select setup time Chip select hold time	CS0	t_{CSSAS9} t_{CSHS9}		0 0	-	

Note: The rising time and the falling time are stipulated to be equal to or less than 15ns.

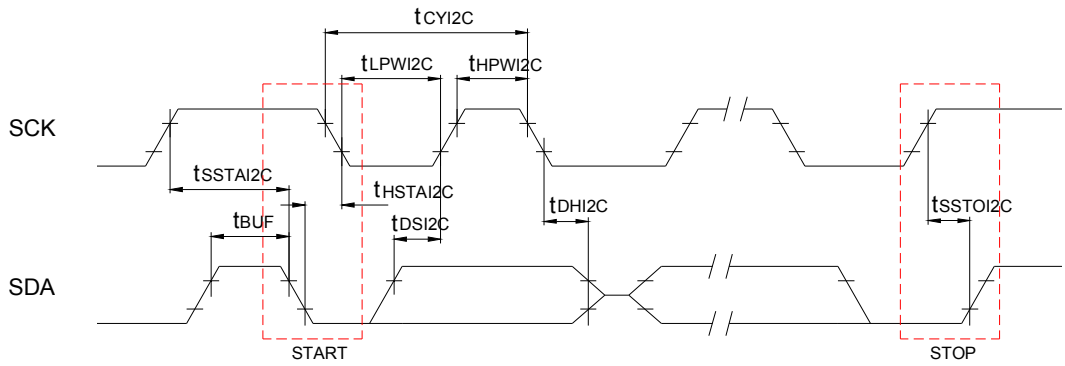


Serial Bus Timing Characteristics (for S9)

3.6 Serial Bus Timing Characteristics (for I^2C, VDD=2.7V to 3.6V, Ta=25°C)

Description	Signal	Symbol	Condition	Min.	Max.	Unit
SCK cycle time (read) (write)	SCK	t_{CYI2C}	$t_r + t_f$ ≤100ns	610 306	-	
Low pulse width (read) (write)		t_{LPWI2C}		290 138	-	
High pulse width (read) (write)		t_{HPWI2C}		290 138	-	
Data setup time Data hold time START setup time START hold time STOP setup time	SCK	t_{DSI2C} t_{DHI2C} $t_{SSTAI2C}$ $t_{HSTAI2C}$ $t_{SSTOI2C}$		33 11 28 50 28	-	
Bus free time between STOP and START condition	SDA	t_{BUF}		165	-	

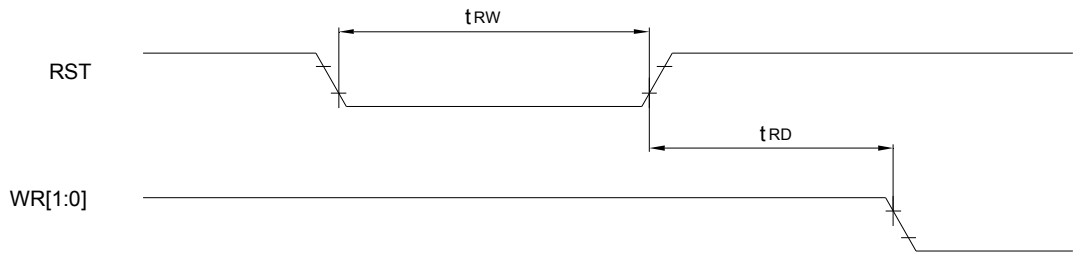
Note: The rising time and the falling time are stipulated to be equal to or less than 15ns.



Serial Bus Timing Characteristics (for I^2C)

3.7 Reset Characteristics (VDD=2.7V to 3.6V, Ta=25°C)

Description	Signal	Symbol	Condition	Min.	Max.	Unit
Reset low pulse width	RST	t_{RW}		3	-	us
Reset to WR pulse delay	RST, WR	t_{RD}		10	-	ms

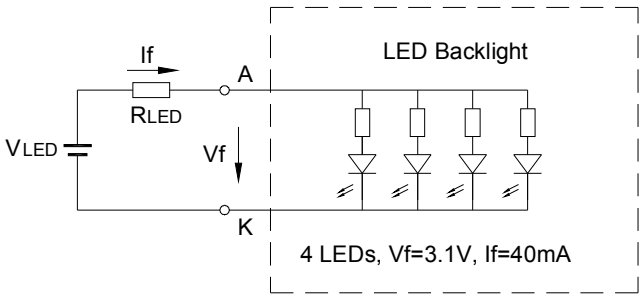


Reset Characteristics

3.8 LED Backlight Characteristics (Ta=25°C)

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Forward Voltage	Vf		2.9	3.1	3.3	V
Forward Current	If	Vf=3.1V	-	40	-	mA
Color	White					

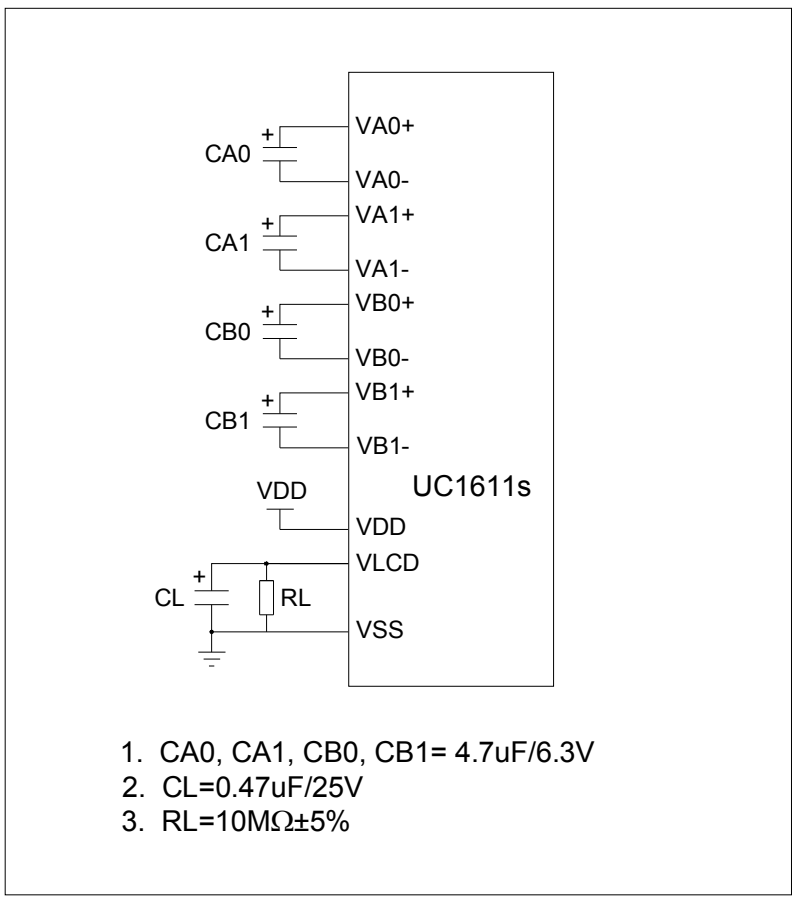
* RLED is the current limiting resistor for LED backlight. RLED=(VLED-3.1V)/40mA



Recommended vaule for RLED

VLED	RLED
5.0V	47Ω ±1%,1/4W
3.3V	5.1Ω ±1%,1/10W
3.0V	0Ω ,1/10W

3.9 Power Supply for Logic and LCD Driving (VDD=2.7V to 3.6V)



1. CA0, CA1, CB0, CB1= 4.7uF/6.3V
2. CL=0.47uF/25V
3. RL=10MΩ±5%

4. DISPLAY CONTROL COMMANDS

The following is a list of host commands supported by UC1611s.

C/D: 0: Control, 1: Data
W/R: 0: Write Cycle, 1: Read Cycle
Useful Data bits
– Don't Care

	Command	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0	Action	Default
1	Write Data Byte	1	0	#	#	#	#	#	#	#	#	Write 1 byte	N/A
2	Read Data Byte	1	1	#	#	#	#	#	#	#	#	Read 1 byte	N/A
3	Get Status	0	1	Ver	MX	MY	WA	DE	WS	MD	MS	Get Status	N/A
				ID[1:0]		PMO[5:0]							
				Product Code				0	0	0	EF		
4	Set Column Address LSB	0	0	0	0	0	0	#	#	#	#	Set CA[3:0]	0
	Set Column Address MSB	0	0	0	0	0	1	#	#	#	#	Set CA[7:4]	0
5	Temp. Compensation	0	0	0	0	1	0	0	1	#	#	Set TC[1:0]	00b:-0.05 %/°C
6	Set Panel Loading	0	0	0	0	1	0	1	0	#	#	Set PC[1:0]	11b: 33-55nF
7	Set Pump Control	0	0	0	0	1	0	1	1	#	#	Set PC[3:2]	11b
8	Set Adv. Program Control (double-byte command)	0	0	0	0	1	1	0	0	R	R	Set APC[R] [7:0] R=0 to 3	N/A
				#	#	#	#	#	#	#	#		
9	Set Scroll Line LSB	0	0	0	1	0	0	#	#	#	#	Set SL[3:0]	0
	Set Scroll Line MSB			0	1	0	1	#	#	#	#	Set SL[7:4]	0
10	Set Page Address LSB	0	0	0	1	1	0	#	#	#	#	Set PA[3:0]	0
	Set Page Address MSB			0	1	1	1	0	#	#	#	Set PA[6:4]	0
11	Set Potentiometer (double-byte command)	0	0	1	0	0	0	0	0	0	1	Set PM[7:0]	PM=EAH
				#	#	#	#	#	#	#	#		
12	Set Isolation Clock Front	0	0	1	0	0	0	0	0	1	0	Set ISOF[3:0]	1H
				0	0	0	1	0	0	1	1		
				-	-	-	-	#	#	#	#		
13	Set Isolation Clock Back	0	0	1	0	0	0	0	0	1	0	Set ISOB[3:0]	0H
				0	0	0	1	0	1	0	0		
				-	-	-	-	#	#	#	#		
14	Set Partial Display Control	0	0	1	0	0	0	0	1	#	#	Set LC[9:8]	00b: Disable
15	Set RAM Address Control	0	0	1	0	0	0	1	#	#	#	Set AC[2:0]	001b
16	Set Fixed Lines	0	0	1	0	0	1	#	#	#	#	Set FL[3:0]	0
17	Set Line Rate	0	0	1	0	1	0	0	0	#	#	Set LC[5:4]	10b: 28klps
18	Set All-Pixel-ON	0	0	1	0	1	0	0	1	0	#	Set DC[1]	0
19	Set Inverse Display	0	0	1	0	1	0	0	1	1	#	Set DC[0]	0
20	Set Display Enable	0	0	1	0	1	0	1	#	#	#	Set DC[4:2]	110b
21	Set LCD Mapping Control (double-byte command)	0	0	1	1	0	0	0	0	0	0	Set LC[3:0]	0
				0	0	0	0	#	#	#	#		
22	Set N-line Inversion (double byte command)	0	0	1	1	0	0	1	0	0	0	Set NIV[6:0]	00H
				-	#	#	#	#	#	#	#		

Command Table (continued)

	Command	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0	Action		Default
23	Set Display Pattern	0	0	1	1	0	1	0	#	#	#	Set DC[7:5]		000b
24	System Reset	0	0	1	1	1	0	0	0	1	0	System Reset		N/A
25	NOP	0	0	1	1	1	0	0	0	1	1	No operation		N/A
26	Set test control (double-byte command)	0	0	1	1	1	0	0	1	TT		For testing only. Do not use		N/A
		0	0	#	#	#	#	#	#	#	#			
27	Set LCD Bias Ratio	0	0	1	1	1	0	1	0	#	#	Set BR[1:0]		10b: 11
28	Set COM End	0	0	1	1	1	1	0	0	0	1	Set CEN[7:0]		159
		0	0	#	#	#	#	#	#	#	#			
29	Set Partial Display Start	0	0	1	1	1	1	0	0	1	0	Set DST[7:0]		0
		0	0	#	#	#	#	#	#	#	#			
30	Set Partial Display End	0	0	1	1	1	1	0	0	1	1	Set DEN[7:0]		159
		0	0	#	#	#	#	#	#	#	#			
31	Set Window Program Starting Column Address	0	0	1	1	1	1	0	1	0	0	Sharedwith MTP Commands	Set WPC0	0
				#	#	#	#	#	#	#	#			
32	Set Window Program Starting Page Address	0	0	1	1	1	1	0	1	0	1		Set WPP0	0
				-	#	#	#	#	#	#	#			
33	Set Window Program Ending Column Address	0	0	1	1	1	1	0	1	1	0		Set WPC1	255
				#	#	#	#	#	#	#	#			
34	Set Window Program Ending Page Address	0	0	1	1	1	1	0	1	1	1		Set WPP1	79
				-	#	#	#	#	#	#	#			
35	Set Window Program Mode	0	0	1	1	1	1	1	0	0	#	Set AC[3]		0: Inside
36	Set MTP Operation Control	0	0	1	0	1	1	1	0	0	0	Set MTPC[5:0]		10H
				-	-	#	#	#	#	#	#			
37	Set MTP Write Mask	0	0	1	0	1	1	1	0	0	1	Set MTPM[5:0]		0
				-	-	#	#	#	#	#	#			
38	Set V_{MTP1} Potentiometer	0	0	1	1	1	1	0	1	0	0	Shared with Window Program Commands	Set MTP1	N/A
				#	#	#	#	#	#	#	#			
39	Set V_{MTP2} Potentiometer	0	0	1	1	1	1	0	1	0	1		Set MTP2	N/A
				#	#	#	#	#	#	#	#			
40	Set MTP Write Timer	0	0	1	1	1	1	0	1	1	0		Set MTP3	N/A
				#	#	#	#	#	#	#	#			
41	Set MTP Read Timer	0	0	1	1	1	1	0	1	1	1		Set MTP4	N/A
				#	#	#	#	#	#	#	#			
Serial Read Command (Enable in S8 or S9 Bus Modes Only)														
42	Get Status	0	0	1	1	1	1	1	1	1	0	Get Status till Chip Disable		N/A
		-	1	Ver	MX	MY	WA	DE	WS	MD	MS			
				ID[1:0]		PMO[5:0]								
				Product Code				0	0	0	EF			

Note: Please refer to UC1611s datasheet for details.

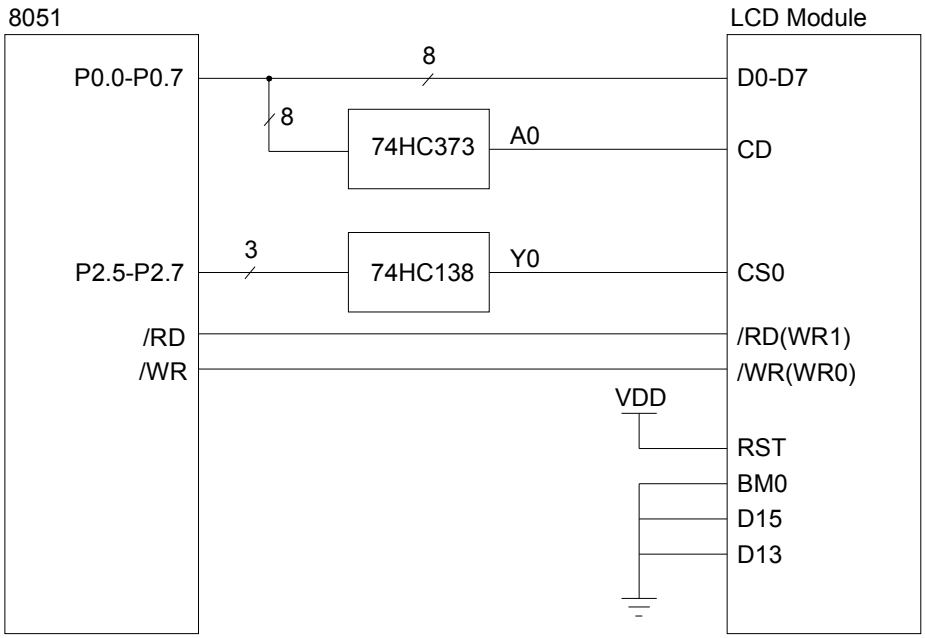
5. CONNECTION WITH MPU

UC1611s supports two parallel bus protocols, 8080 or 6800 (in either 8-bit or 4-bit bus width), and three serial bus protocols (4-wire, 3-wire and 2-wire). Designers can either use parallel bus to achieve high data transfer rate, or use serial bus to save the I/O terminals. The interface bus mode is determined by BM0 and D[15,13] by the following relationship.

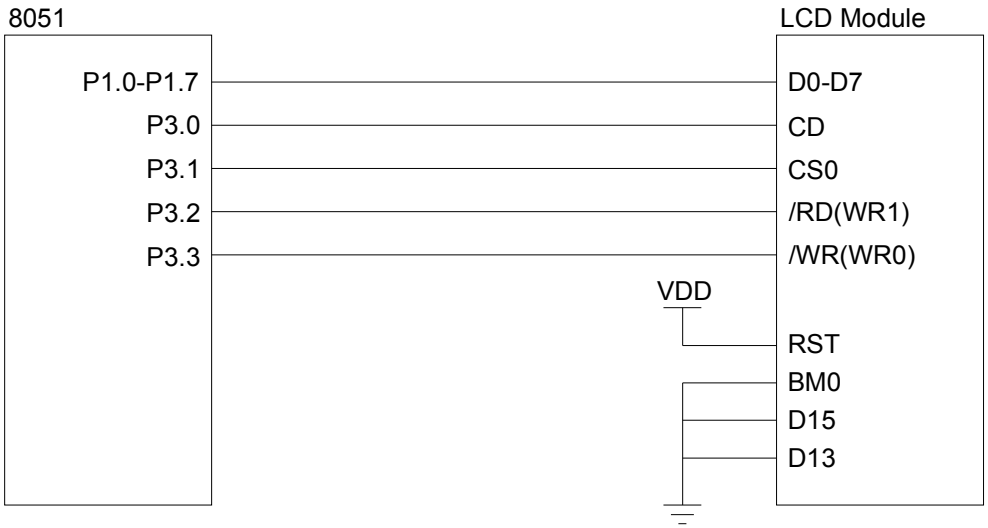
Bus type		8080		6800		S8	S9	I^2C
Width		8-bit	4-bit	8-bit	4-bit	4-wire	3-wire	2-wire
Access		Read/Write						
Control & Data Pins	BM0	0	0	1	1	0	1	1
	D[15,13]	00	01	00	01	10	10	11
	CS0	Chip Select						A2
	CD	Control / Data					–	
	WR0	/WR		R/W		0		
	WR1	/RD		EN		0		
	D[7:4]	Data	–	Data	–	–		
	D[3:0]	Data	Data	Data	Data	D3=SDA, D0=SCK		

Note: 1. BM1 and CS1 is fixed to “H” on ITO glass.
2. Connect unused control pins and data bus pins to VDD or VSS.

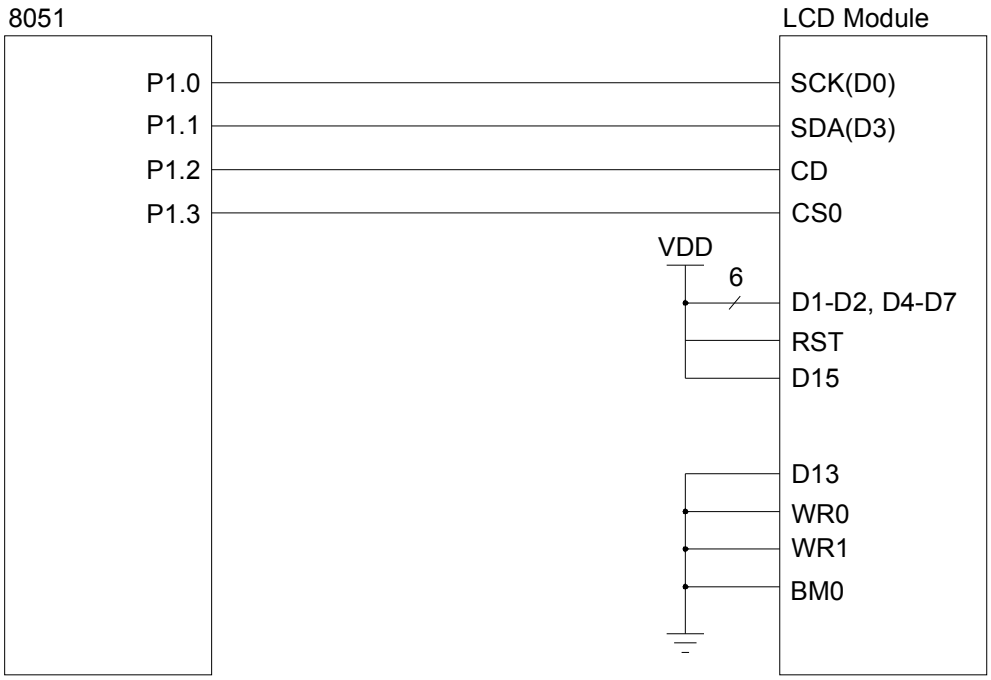
In order to reduce the transmission interference between MCU and lcm, it is suggested that 100pF capacitors should be added between GND and CD, CS0, /WR, /RD signals.



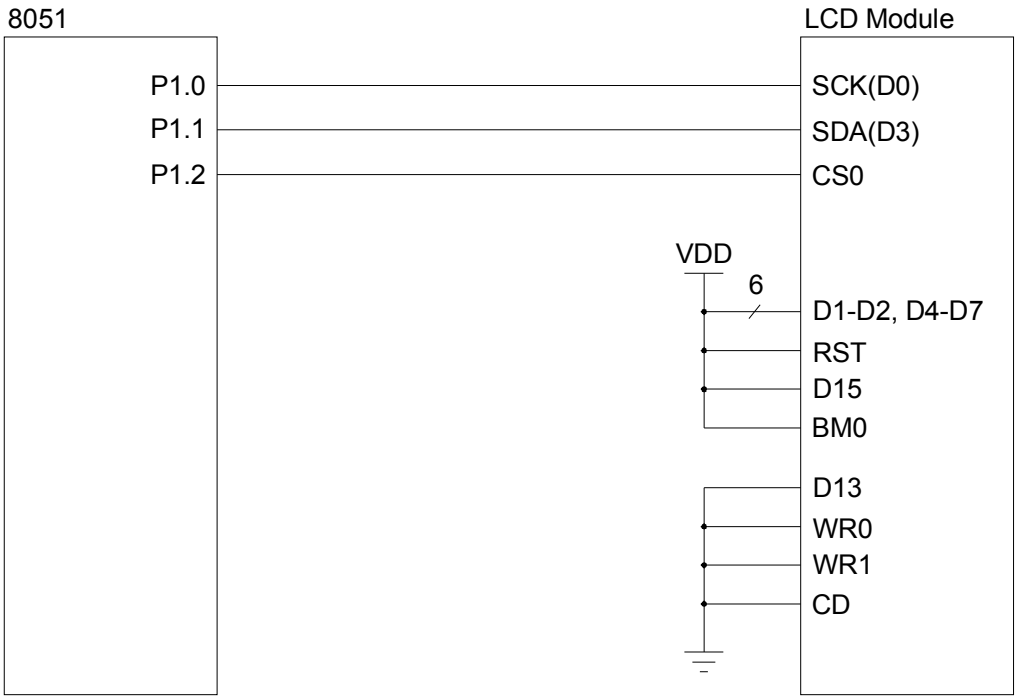
a. 8080 8-bit parallel interface



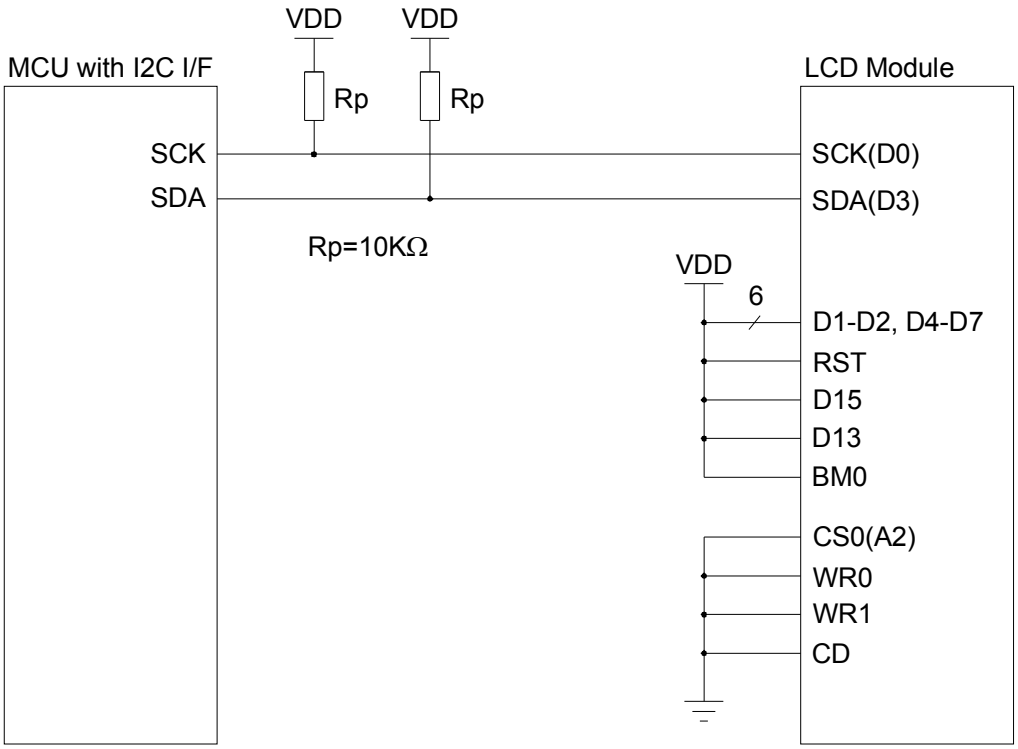
b. 8080 8-bit parallel interface



c. 4-wire SPI (S8) interface



d. 3-wire SPI (S9) interface



e. 2-wire SPI (I2C) interface

6. INITIALIZATION AND POWER OFF

6.1 Power on Initialization Sequence

No.	Command	Operation
1	Power on	Power on
2	Automatic Power-On-Reset or System Reset by RST terminal	There is built-in Power-On-Reset circuit in UC1611s. System Reset will be activated automatically after VDD is stabilized. Delay 150ms, and then start the following initialization commands. Connect RST to VDD when it is not used.
3	Set Temperature Compensation: 24H	TC[1:0]=10b: -0.05%/°C **Note 1**
4	Set Panel Loading: 2BH	PC[1:0]=11b: 33nF < LCD < 55NF
5	Set Pump Control: 2FH	PC[3:2]=11b: Internal VLCD
6	Set LCD Mapping Control: C0H, 04H	MY=1b: COM Reverse MX=0b: SEG Normal MSF=0b: MSB first
7	Set N-Line Inversion: C8H, 08H	NIV[5:0]=01000b: 8 lines inversion NIV[6]=0b: non-XOR
8	Set LCD Bias Ratio: EAH	BR[1:0]=10b: 1/11 bias
9	Set Potentiometer: 81H, DCH	PM[7:0]=11011100b: “11011100b ” is a reference value, modify this value to get the best display contrast. Because of the manufacturing dispersion of LCD modules, potentiometer (PM[7:0]) value may need be changed to match the driving voltage (VLCD) for different lot of LCD modules.
10	Set Display Enable: A9H	DC[4:3]=00b: B/W mode; DC2=1b: Display on
11	Set Display Pattern: D1H	DC[7:6]=00b: Pattern0; DC5=1b: 1 bit for 1 pixel
12	End of initialization	
13	Write display data	

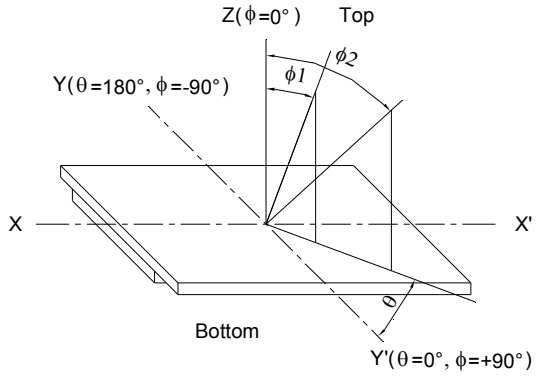
Note 1: To get best contrast ratio, we suggest using different temperature compensation coefficient for different temperature range. For -20°C to +40°C, 0.00%/°C is recommended; For +40°C to +70°C, -0.15%/°C is recommended. Users should put the temperature sensor as close as possible to the lcd panel. If temperature testing circuit is not available, we suggest using -0.05%/°C to get a balanced contrast ratio for temperature range of -20°C to +70°C.

6.2 Power off Sequence

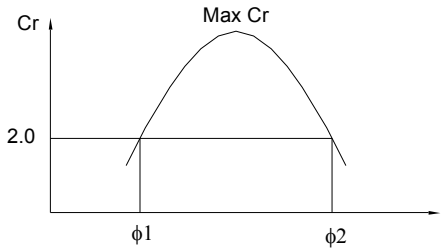
No.	Command	Description
1	Optional status	Normal operation
2	System Reset: E2H	Reset system, delay 2 ms.
3	Power off	Power off

7. ELECTRO-OPTICAL CHARACTERISTICS (Ta=25°C)

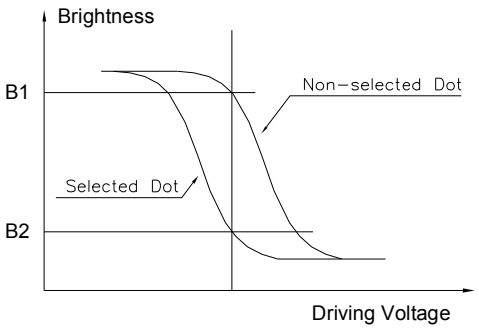
Item	Symbol	Condition	Min.	Typ.	Max.	Unit	Note
View Angle	Φ2-Φ1	Cr≥2 , θ=0°	-	60	-	Deg	Note1, Note2
Contrast Ratio	Cr	Φ=0°,θ=0°	3	-	-	-	Note3
Response Time	tr (rise)	Φ=0°,θ=0°	-	200	-	ms	Note4
	tf (fall)	Φ=0°,θ=0°	-	250	-	ms	



Note1: Definition of viewing angle ϕ, θ

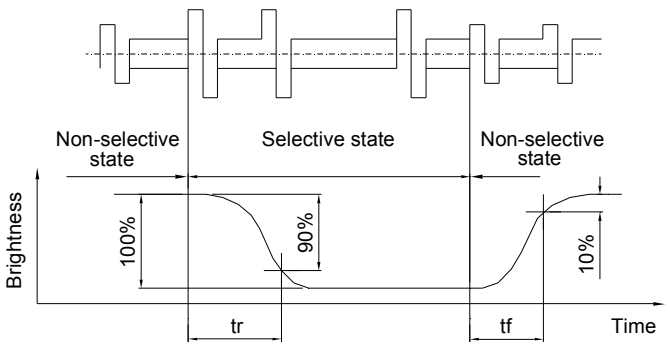


Note2: Definition of viewing angle range ϕ1, ϕ2



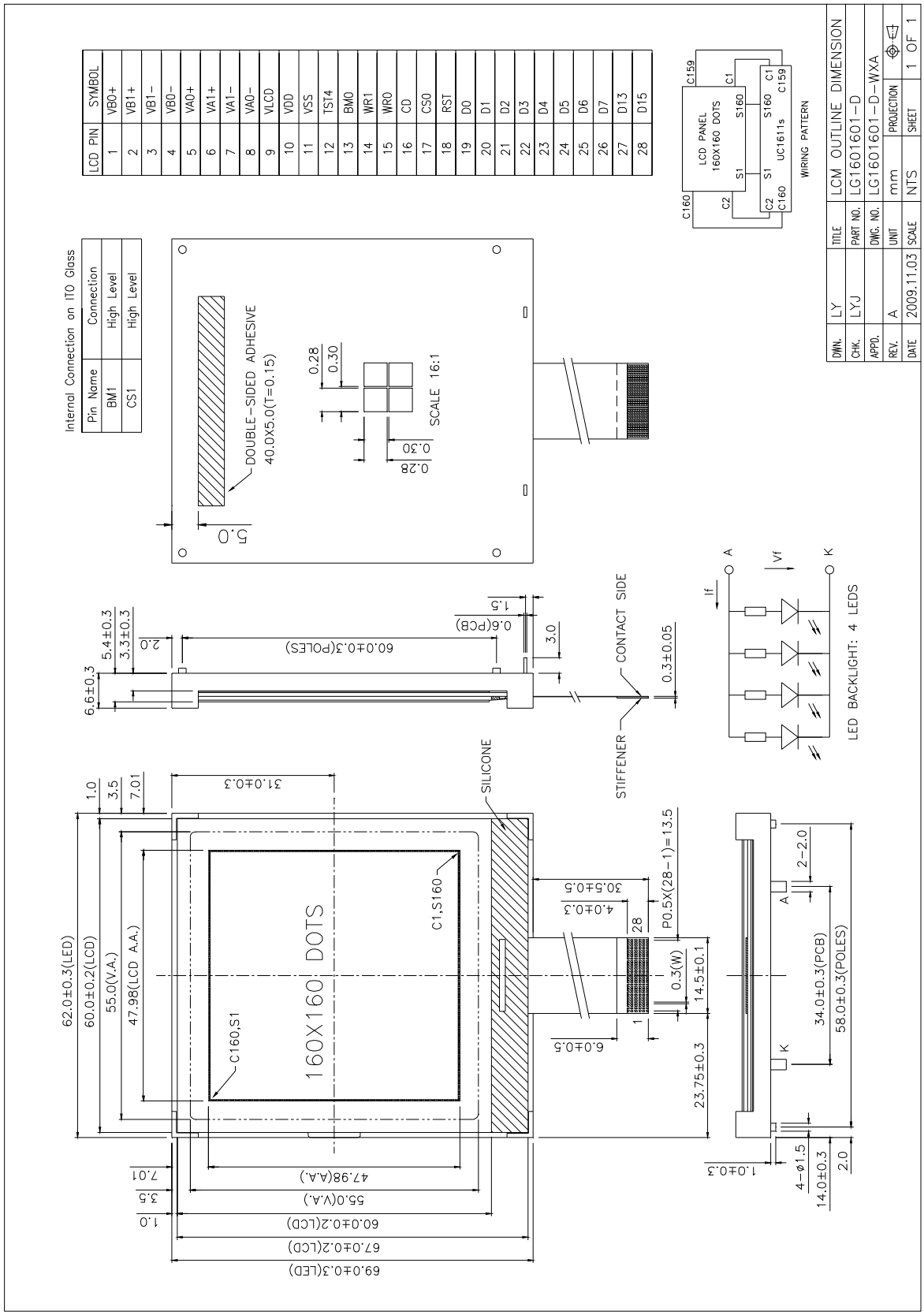
$$\text{Contrast Ratio} = \frac{\text{Brightness of non-selected dot (B1)}}{\text{Brightness of selected dot (B2)}}$$

Note3: Definition of contrast ratio (positive type)



Note3: Definition of response time

8. DIMENSIONAL OUTLINE



9. LCD MODULE NUMBERING SYSTEM

L	G	160	160	1	-	F	F	D	W	H	U	V	-	XXXXX
(1)	(2)	(3)	(4)	(5)		(6)	(7)	(8)	(9)	(10)	(11)	(12)		(13)

(1) Brand

(2) Module type

C - Character module

G - Graphic module

(3) Display format

Character module : Number of characters per line, two digits XX

Graphic module : Number of columns, three digits XXX

(4) Display format

Character module : Number of lines, one digit X

Graphic module : Number of rows, two or three digits XX or XXX

(5) Development number : One or two digits X or XX

(6) LCD mode

T - TN Positive, Gray **N** - TN Negative, Blue

S - STN Positive, Yellow green **G** - STN Positive, Gray

B - STN Negative, Blue **F** - FSTN Positive, White

K - FSTN Negative, Black **L** - FSTN Negative, Blue

Q - FFSTN Negative, Black

(7) Polarizer mode

R - Reflective **F** - Transflective **M** - Transmissive

(8) Backlight type

N - Without backlight **L** - Array LED **D** - Edge light LED **E** - EL **C** - CCFL

(9) Backlight color

Y - Yellow green **B** - Blue **W** - White **G** - Green

A - Amber **R** - Red **M** - Multi color **Nil** - Without backlight

(10) Operating temperature range

S - Standard temperature (0 to +50 ^{o}C) **H** - Extended temperature (-20 to +70 ^{o}C)

(11) Viewing direction

3 - 3:00 **6** - 6:00 **9** - 9:00 **U** - 12:00

(12) DC-DC Converter

N or Nil - Without DC-DC converter **V** - Built in DC-DC converter

(13) Version code

Nil or 0 to ZZZZZ - Version code

10. PRECAUTIONS FOR USE OF LCD MODULE

10.1 Handing Precautions

1) The display panel is made of glass. Do not subject it to a mechanical shock by dropping it from a high place, etc.
2) If the display panel is damaged and the liquid crystal substance inside it leaks out, be sure not to get any in your mouth. If the substance comes into contact with your skin or clothes, promptly wash it off using soap and water.
3) Do not apply excessive force on the surface of display or the adjoining areas of LCD module since this may cause the color tone to vary.
4) The polarizer covering the display surface of the LCD module is soft and easily scratched. Handle this polarizer carefully.
5) If the display surface of LCD module becomes contaminated, blow on the surface and gently wipe it with a soft dry cloth. If it is heavily contaminated, moisten cloth with one of the following solvents.
   · Isopropyl alcohol
   · Ethyl alcohol
   Solvents other than those mentioned above may damage the polarizer.
   Especially, do not use the following:
   · Water
   · Ketone
   · Aromatic Solvents
6) When mounting the LCD module make sure that it is free of twisting, warping, and distortion. Distortion has great influence upon display quality. Also keep the stiffness enough regarding the outer case.
7) Be sure to avoid any solvent such as flux for soldering never stick to Heat-Seal. Such solvent on Heat-Seal may cause connection problem of heat-Seal and TAB.
8) Do not forcibly pull or bend the TAB I/O terminals.
9) Do not attempt to disassemble or process the LCD module.
10) NC terminal should be open. Do not connect anything.
11) If the logic circuit power is off, do not apply the input signals.
12) To prevent destruction of the elements by static electricity, be careful to maintain an optimum work environment.
   · Be sure to ground the body when handling the LCD module.
   · Tools required for assembly, such as soldering irons, must be properly grounded.
   · To reduce the amount of static electricity generated, do not conduct assembly and other work under dry conditions.
   · The LCD module is coated with a film to protect the display surface. Exercise care when peeling off this protective film since static electricity may be generated.

10.2 Storage Precautions

1) When storing the LCD module, avoid exposure to direct sunlight or to the light of fluorescent lamps and high temperature/high humidity. Whenever possible, the LCD module should be stored in the same conditions in which they were shipped from our company.

2) Exercise care to minimize corrosion of the electrodes. Corrosion of the electrodes is accelerated by water droplets or a current flow in a high humidity environment.

10.3 Design Precautions

1) The absolute maximum ratings represent the rated value beyond which LCD module can not exceed. When the LCD modules are used in excess of this rated value, their operating characteristics may be adversely affected.
2) To prevent the occurrence of erroneous operation caused by noise, attention must be paid to satisfy VIL, VIH specification values, including taking the precaution of using signal cables that are short.
3) The liquid crystal display exhibits temperature dependency characteristics. Since recognition of the display becomes difficult when the LCD is used outside its designated operating temperature range, be sure to use the LCD within this range. Also, keep in mind that the LCD driving voltage levels necessary for clear displays will vary according to temperature.
4) Sufficiently notice the mutual noise interference occurred by peripheral devices.
5) To cope with EMI, take measures basically on outputting side.
6) If DC is impressed on the liquid crystal display panel, display definition is rapidly deteriorated by the electrochemical reaction that occurs inside the liquid crystal display panel. To eliminate the opportunity of DC impressing, be sure to maintain the AC characteristics of the input signals sent to the LCD Module.

10.4 Others

1) Liquid crystals solidify under low temperatures (below the storage temperature range) leading to defective orientation or the generation of air bubbles (black or white). Air bubbles may also be generated if the LCD module is subjected to a strong shock at a low temperature.
2) If the LCD modules have been operating for a long time showing the same display patterns, the display patterns may remain on the screen as ghost images and a slight contrast irregularity may also appear. A normal operating status can be regained by suspending use for some time. It should be noted that this phenomenon does not adversely affect performance reliability.
3) To minimize the performance degradation of the LCD modules resulting from destruction caused by static electricity, etc., exercise care to avoid touching the following sections when handling the module:
   · Terminal electrode sections.
   · Part of pattern wiring on TAB, etc.