

Bias Resistor Transistor

NPN Silicon Surface Mount Transistor with Monolithic Bias Resistor Network

LDTC144GWT1G

● Applications

Inverter, Interface, Driver

● Features

- 1) Built-in bias resistors enable the configuration of an inverter circuit without connecting external input resistors (see equivalent circuit).
- 2) The bias resistors consist of thin-film resistors with complete isolation to allow positive biasing of the input. They also have the advantage of almost completely eliminating parasitic effects.
- 3) Only the on/off conditions need to be set for operation, making the device design easy.

- We declare that the material of product compliance with RoHS requirements.

● Absolute maximum ratings (Ta=25°C)

Parameter		Symbol	Limits	Unit
Collector-base voltage		V_{CBO}	50	V
Collector-emitter voltage		V_{CEO}	50	V
Emitter-base voltage		V_{EBO}	5	V
Collector current		I_C	100	mA
Collector Power dissipation	DTC144GE	P_c	150	mW
	DTC144GUA / DTC144GKA		200	
	DTC144GSA		300	
Junction temperature		T_j	150	°C
Storage temperature		T_{stg}	-55 to +150	°C

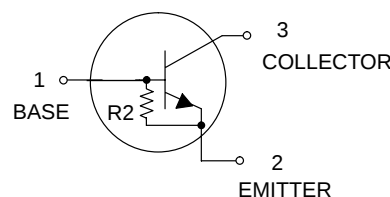
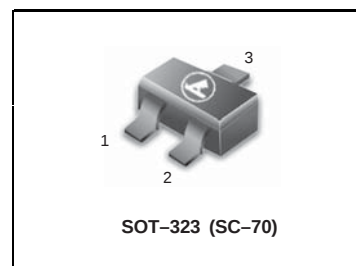
DEVICE MARKING AND RESISTOR VALUES

Device	Marking	R1 (K)	R2 (K)	Shipping
LDTC144GWT1G	L1	—	47	3000/Tape & Reel
LDTC144GWT3G	L1	—	47	10000/Tape & Reel

● Electrical characteristics (Ta=25°C)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
Collector-base breakdown voltage	BV_{CBO}	50	—	—	V	$I_C=50\mu A$
Collector-emitter breakdown voltage	BV_{CEO}	50	—	—	V	$I_C=1mA$
Emitter-base breakdown voltage	BV_{EBO}	5	—	—	V	$I_E=160\mu A$
Collector cutoff current	I_{CBO}	—	—	0.5	μA	$V_{CB}=50V$
Emitter cutoff current	I_{EBO}	65	—	130	μA	$V_{EB}=4V$
Collector-emitter saturation voltage	$V_{CE(sat)}$	—	—	0.3	V	$I_C=10mA$, $I_B=0.5mA$
DC current transfer ratio	h_{FE}	68	—	—	—	$I_C=5mA$, $V_{CE}=5V$
Emitter-base resistance	R	32.9	47	61.1	k Ω	—
Transition frequency	f_T	—	250	—	MHz	$V_{CE}=10V$, $I_E=-5mA$, $f=100MHz$ *

* Transition frequency of the device.



LDTTC144GWT1G

●Electrical characteristic curves

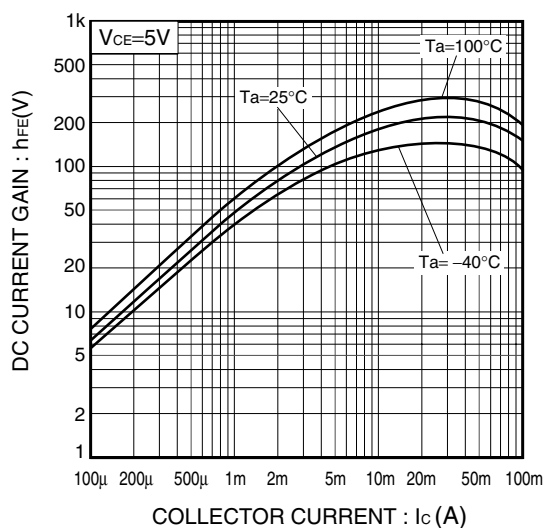


Fig.1 DC current gain
vs. Collector current

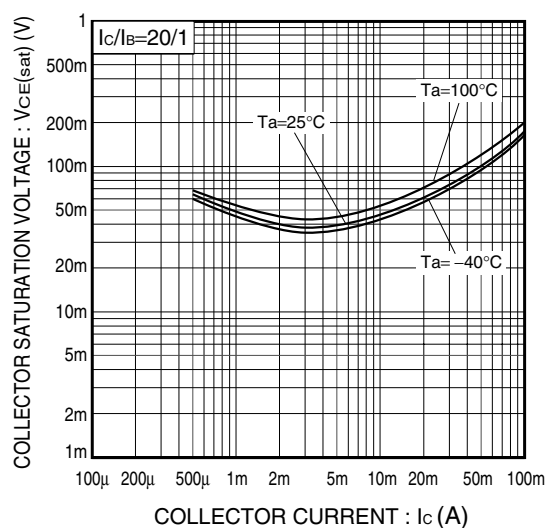
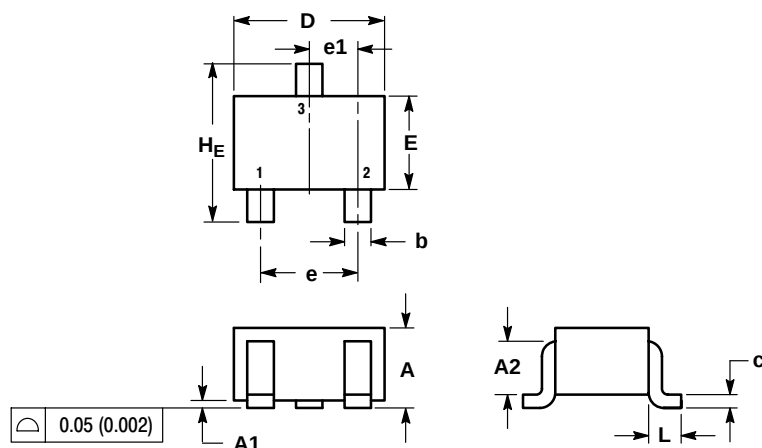


Fig.2 Collector-Emitter saturation voltage
vs. Collector current

LDTC144GWT1G

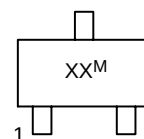
SC-70 (SOT-323)



- NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
 2. CONTROLLING DIMENSION: INCH.

DIM	MILLIMETERS			INCHES		
	MIN	NOM	MAX	MIN	NOM	MAX
A	0.80	0.90	1.00	0.032	0.035	0.040
A1	0.00	0.05	0.10	0.000	0.002	0.004
A2	0.7 REF			0.028 REF		
b	0.30	0.35	0.40	0.012	0.014	0.016
c	0.10	0.18	0.25	0.004	0.007	0.010
D	1.80	2.10	2.20	0.071	0.083	0.087
E	1.15	1.24	1.35	0.045	0.049	0.053
e	1.20	1.30	1.40	0.047	0.051	0.055
e1	0.65 BSC			0.026 BSC		
L	0.425 REF			0.017 REF		
HE	2.00	2.10	2.40	0.079	0.083	0.095

GENERIC MARKING DIAGRAM



- XX = Specific Device Code
M = Date Code
▪ = Pb-Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "▪", may or may not be present.

SOLDERING FOOTPRINT*

