Green-Mode PWM Controller with BNO and OTP Protections

Rev. 00

General Description

The LD7539 is built-in with several functions, protection and EMI-improved solution in a tiny package. It takes less components counts or circuit space, especially ideal for those total solutions of low cost.

The implemented functions include low startup current, green-mode power-saving operation, leading-edge blanking of the current sensing and internal slope compensation. It also features more protections like BNO (Brownout), OTP (Over Temperature Protection), OLP (Over Load Protection) and OVP (Over Voltage Protection) to prevent circuit damage occurred under abnormal conditions.

Furthermore, the Frequency Swapping function is to reduce the noise level and thus helps the power circuit designers to easily deal with the EMI filter design by spending minimum amount of component cost and developing time.

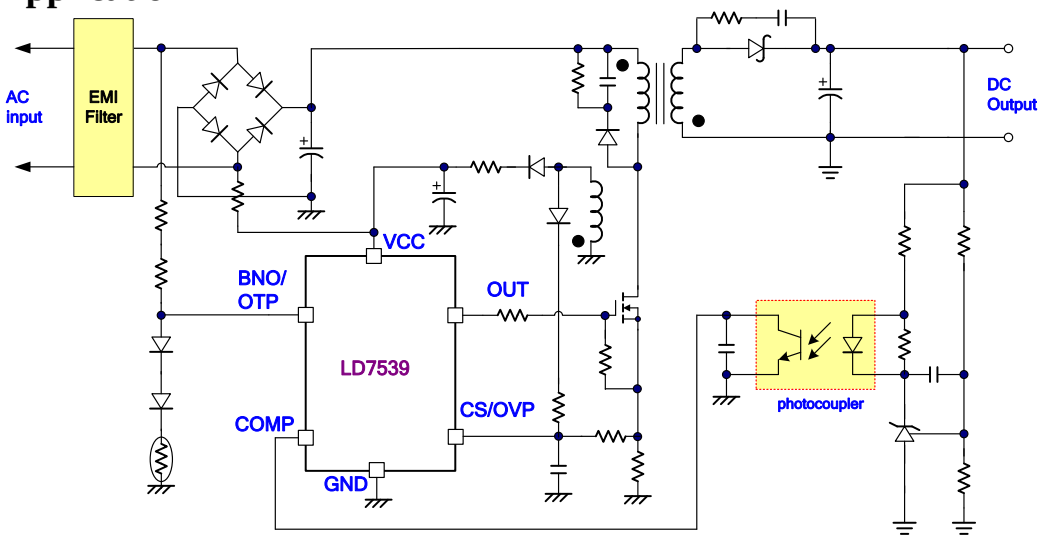
Features

- High-Voltage CMOS Process with Excellent ESD protection
- Very Low Startup Current (<14μA)
- Green Mode Control
- UVLO (Under Voltage Lockout)
- LEB (Leading-Edge Blanking) on CS Pin
- Internal Frequency Swapping
- Internal Slope Compensation
- AC Input BNO (Brownout) Protection
- OVP (Over Voltage Protection) on Vcc Pin
- Adjustable OVP (Over Voltage Protection) on CS Pin
- Adjustable OCP (Over Current Protection) on CS Pin
- OTP (Over Temperature Protection) through a NTC
- OLP (Over Load Protection)
- 250/-500mA Driving Capability

Applications

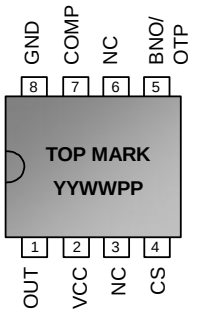
- Switching AC/DC Adaptor and Battery Charger
- Open Frame Switching Power Supply

Typical Application

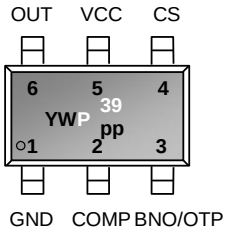


Pin Configuration

DIP-8 (TOP VIEW)



SOT-26 (TOP VIEW)



YY, Y : Year code (D: 2004, E: 2005…..)
WW, W : Week code
PP : Production code
P39 : LD7539

Ordering Information

Part number	Package	Top Mark	Shipping
LD7539 GL	SOT-26	YWP/39	3000 /tape & reel
LD7539 GN	DIP-8	LD7539 GN	3600 /tube /Carton

The LD7539 is ROHS compliant/ Green Packaged.

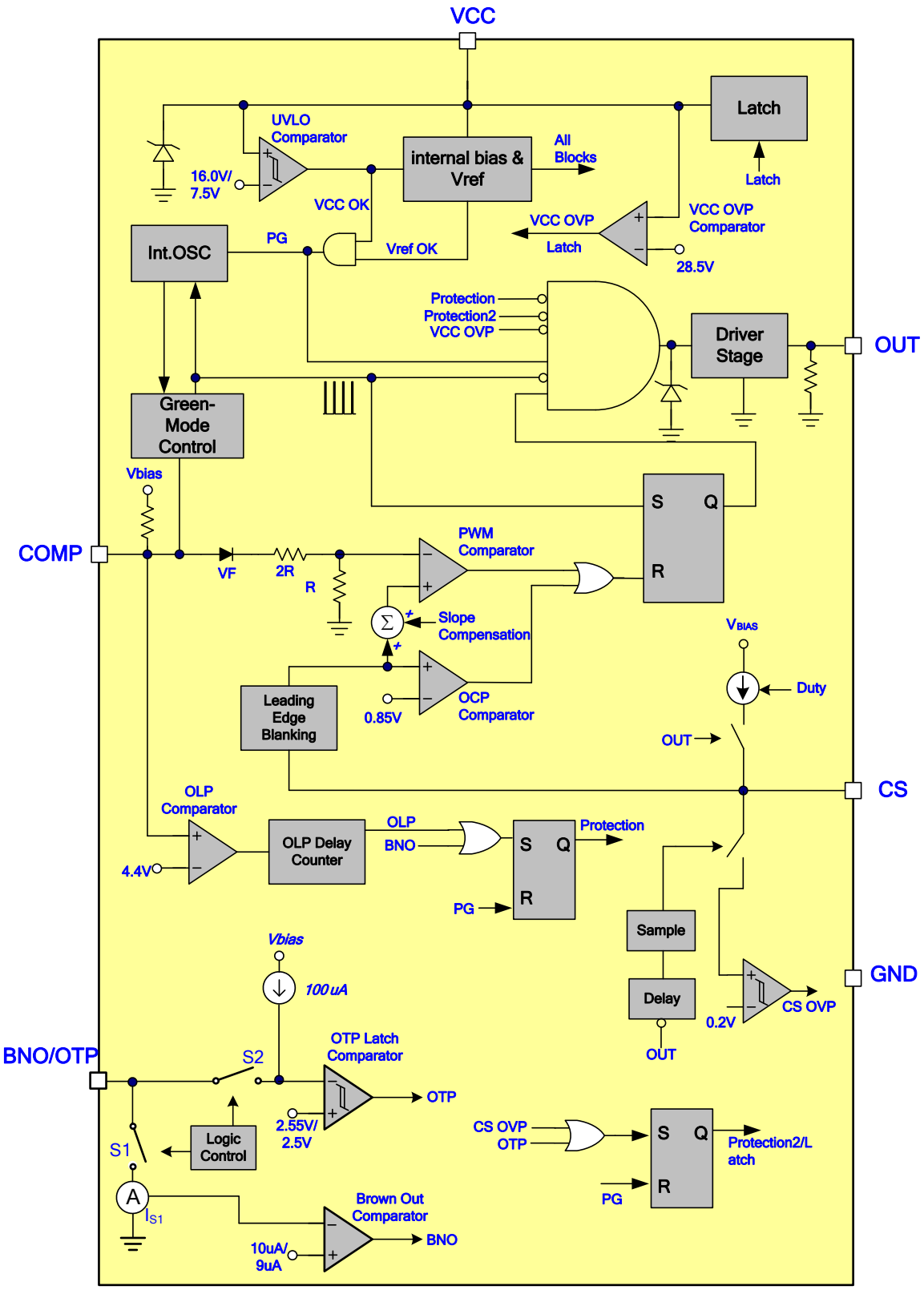
Protection Mode

Switching Freq.	VCC OVP	CS OVP	OLP	OTP Pin
65kHz	Latch	Latch	Auto recovery	Latch

Pin Descriptions

PIN SOT-26	PIN DIP-8	NAME	FUNCTION
1	8	GND	Ground
2	7	COMP	Voltage feedback pin (same as the COMP pin in UC384X). Connect a photo-coupler to close the control loop and achieve the regulation.
3	5	BNO/OTP	This pin is connected to the AC line input via two resistors to achieve brownout function. This pin also can achieve the OTP latching function by connecting an external NTC thermal resistor between this pin and GND pin.
4	4	CS/OVP	Current sense pin, connect it to sense the MOSFET current. This pin is also connected to an auxiliary winding of the PWM transformer through a resistor and a diode for output over-voltage protection.
5	2	VCC	Supply voltage pin
6	1	OUT	Gate drive output to drive the external MOSFET

Block Diagram



Absolute Maximum Ratings

Supply Voltage VCC	-0.3V ~30V
COMP, BNO/OTP, CS	-0.3V ~6V
OUT	-0.3V ~Vcc+0.3V
Maximum Junction Temperature	150°C
Storage Temperature Range	-65°C to 150°C
Package Thermal Resistance (SOT-26, θ_{JA})	250°C/W
Package Thermal Resistance (DIP-8, θ_{JA})	100°C/W
Power Dissipation (SOT-26, at Ambient Temperature = 85°C)	160mW
Power Dissipation (DIP-8, at Ambient Temperature = 85°C)	400mW
Lead temperature (Soldering, 10sec)	260°C
ESD Voltage Protection, Human Body Model	2.5 KV
ESD Voltage Protection, Machine Model	250 V

Caution:

Stress exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stress above Recommended Operating Conditions may affect device reliability.

Recommended Operating Conditions

Item	Min.	Max.	Unit
Operating Ambient Temperature	-40	85	°C
Operating Junction Temperature	-40	125	°C
Supply VCC Voltage	8.5	26.5	V
VCC Capacitor	3.3	10	μF
Start-up resistor Value (AC Side, Half Wave)	400K	1.8M	Ω
Comp Pin Capacitor	1	100	nF
CS Pin Capacitor Value	47	390	pF

Note:

1. It's essential to connect VCC pin with a SMD ceramic capacitor (0.1μF~0.47μF) to filter out the undesired switching noise for stable operation. This capacitor should be placed close to IC pin as possible
2. Connecting a capacitor to COMP pin is also essential to filter out the undesired switching noise for stable operation.
3. The small signal components should be placed to IC pin as possible.

Electrical Characteristics

(T_A = +25°C unless otherwise stated, V_{CC}=15.0V)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Supply Voltage (Vcc Pin)					
Startup Current	VCC < UVLO (ON)		9	14	μA
Operating Current (with 1nF load on OUT pin)	V_{COMP}=0V	0.5	0.58	0.66	mA
	V_{COMP}=3V		1.85		mA
	OLP Tripped/ Auto		0.45		mA
	BNO Tripped/ Auto		0.45		mA
	OVP, CS OVP Tripped/ Latch		0.95		mA
	OTP Pin Tripped/Latch		0.95		mA
Holding Current	Vcc=6V (latched)	370	430	490	μA
UVLO (off)		7.0	7.5	8.0	V
UVLO (on)		15	16	17	V
BNO Enable VCC Level		12	13	14	V
VCC OVP Level		27.5	28.5	29.5	V
VCC OVP pin de-bounce time	*		8		cycle
Voltage Feedback (Comp Pin)					
Short Circuit Current	V_{COMP}=0V	0.105	0.125	0.145	mA
Open Loop Voltage	COMP pin open	4.75	5	5.25	V
Green Mode Threshold VCOMP	*		2.4		V
Zero Duty Threshold VCOMP			1.4		V
Zero Duty Hysteresis			100		mV
Current Sensing (CS/OVP pin)					
Maximum Input Voltage, V_{CS_OFF}		0.837	0.85	0.863	V
Max. OCP Compensation Current, I_{OCP}		234	240	246	μA
Leading Edge Blanking Time, LEB		170	230	290	ns
Internal Slope Compensation	0% to D_{MAX}. (Linearly increase)*		300		mV
Input impedance		1			MΩ
Delay to Output	*			100	ns
Soft Start Duration	*		6.5		ms
Over Voltage Protection (CS/OVP pin)					
OVP Trip Current Level		0.182	0.2	0.218	V
De-bounce Cycle	*		8		Cycle

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Oscillator for Switching Frequency					
Frequency, FREQ		63	65	67	kHz
Green Mode Frequency, FREQG		21.5	25	28	kHz
Swapping Frequency	V_{COMP}>3V		± 4.0		kHz
Temp. Stability	(-20°C ~85°C)*	0	5		%
Voltage Stability	(VCC=11V-25V)*	0	1		%
Gate Drive Output (OUT Pin)					
Output Low Level	VCC=15V, Io=20mA			1	V
Output High Level	VCC=15V, Io=20mA	8		15	V
Output High Clamp Level	V_{CC}=20V		15		V
Rising Time	Load Capacitance=1000pF		150	250	ns
Falling Time	Load Capacitance=1000pF		50	100	ns
Max. Duty		71	75	79	%
OLP (Over Load Protection)					
OLP Trip Level		4.2	4.4	4.6	V
OLP Delay Time at start-up	OLP+ Soft Start*		71.5		ms
OLP Delay Time after start-up		55	65	75	ms
BNO Pin Protection (BNO/OTP Pin) Auto Recovery					
BNO IN Trip Level		9.2	10	10.8	μA
BNO Out Trip Level		8.28	9	9.72	μA
BNO IN De-bounce Time	V_{COMP} >3V		250		μs
BNO Out De-bounce Time	V_{COMP} >3V	63	70	77	ms
OTP Pin Latch Protection (BNO/OTP Pin)					
OTP Pin Source Current		93	100	107	μA
OTP Turn-On Trip Level		2.50	2.55	2.60	V
OTP Turn-Off Trip Level		2.45	2.5	2.55	V
OTP pin de-bounce time	V_{COMP} >3V	400	500	600	μs
OTP detect time	*		2		ms

*: Guaranteed by design.

Typical Performance Characteristics

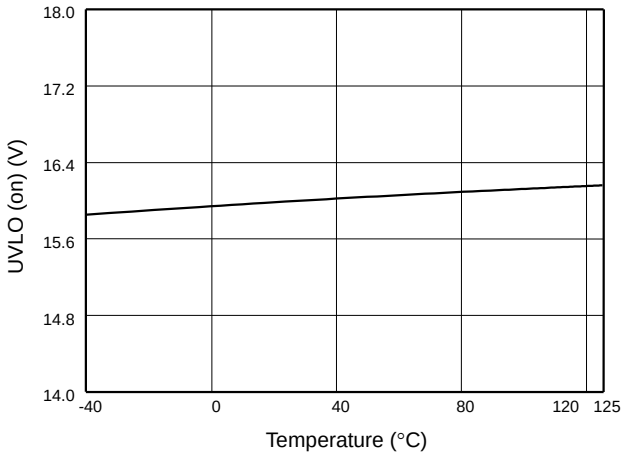


Fig. 1 UVLO (on) vs. Temperature

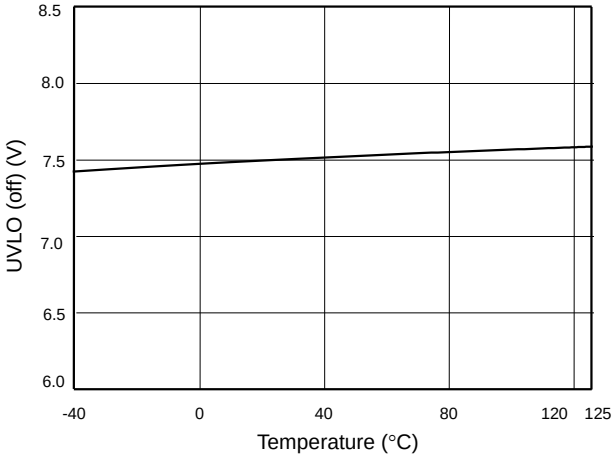


Fig. 2 UVLO (off) vs. Temperature

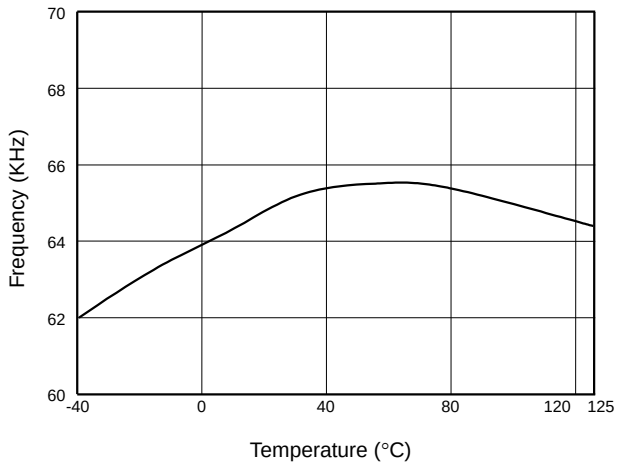


Fig. 3 Frequency vs. Temperature

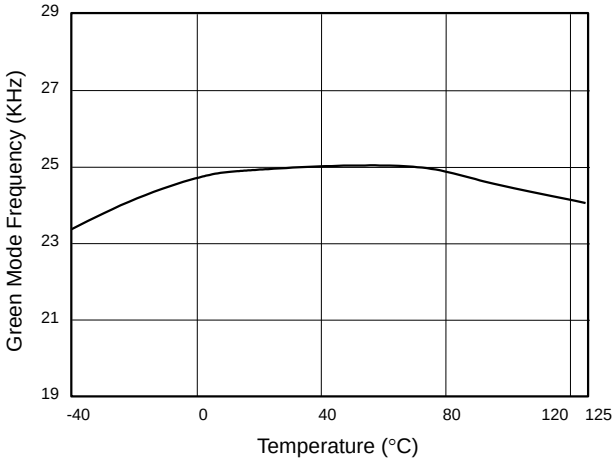


Fig. 4 Green Mode Frequency vs. Temperature

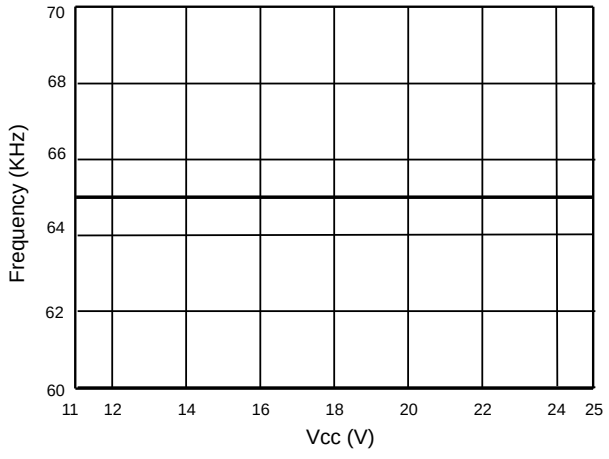


Fig. 5 Frequency vs. Vcc

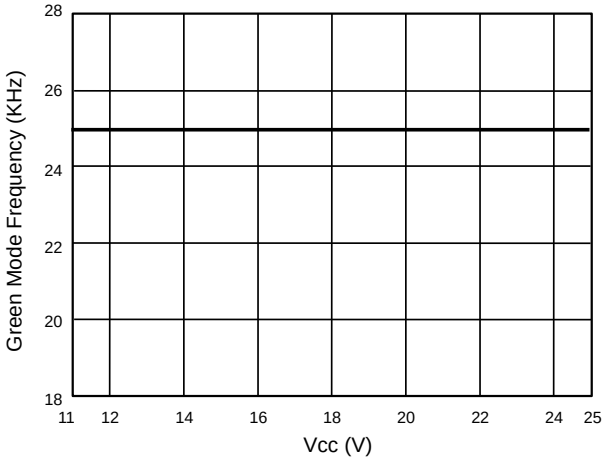


Fig. 6 Green Mode Frequency vs. Vcc

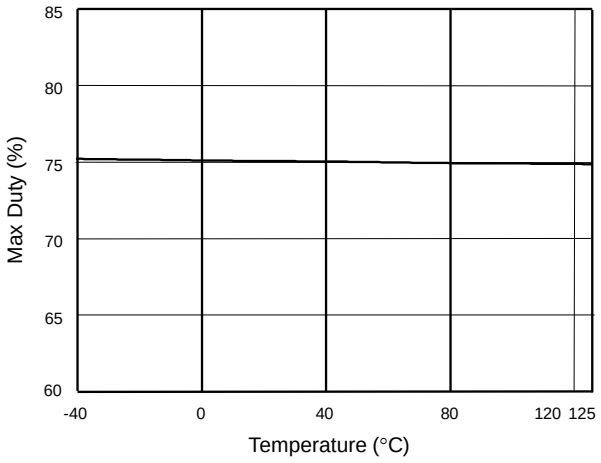


Fig. 7 Max Duty vs. Temperature

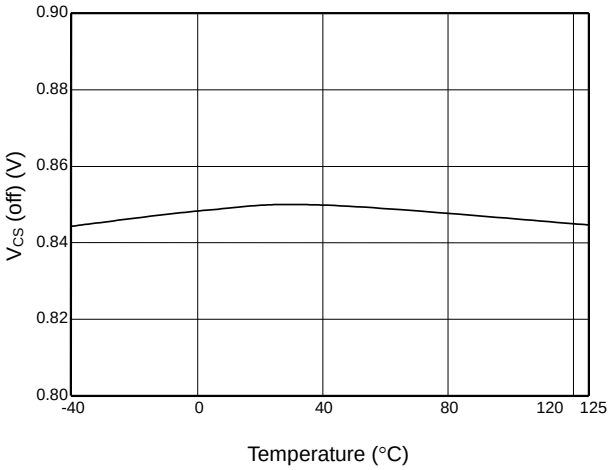


Fig. 8 V_{CS} (off) vs. Temperature

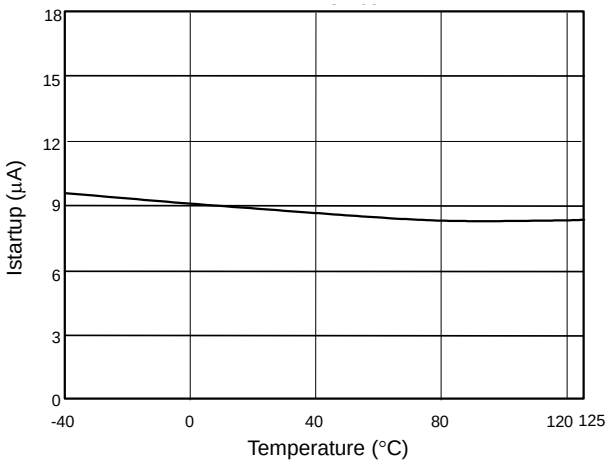


Fig. 9 Startup Current (Istartup) vs. Temperature

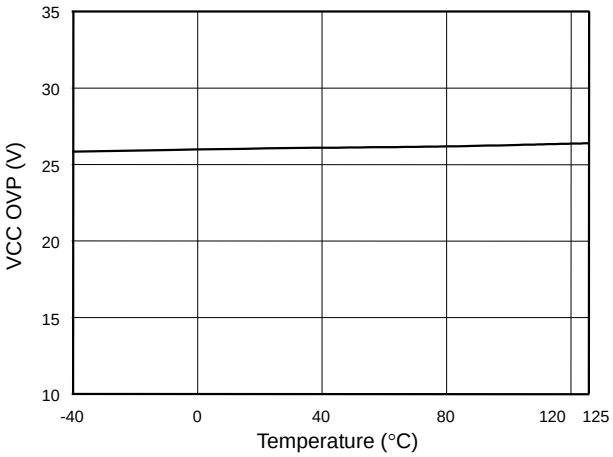


Fig. 10 VCC OVP vs. Temperature

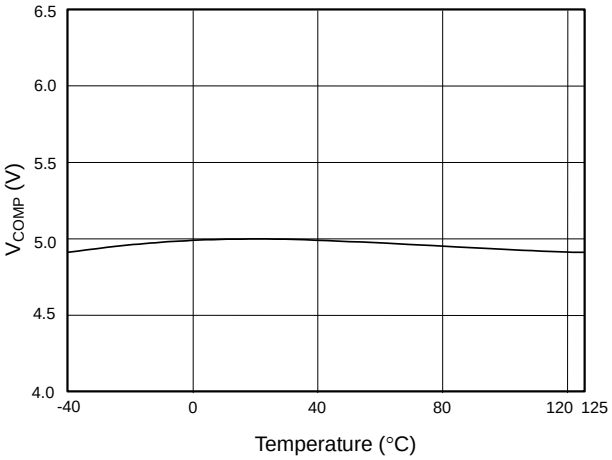


Fig. 11 V_{COMP} open loop voltage vs. Temperature

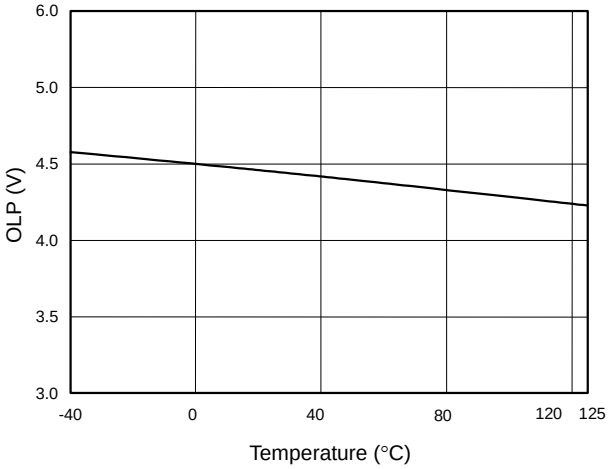


Fig. 12 OLP-Trip Level vs. Temperature

Application Information

Operation Overview

The LD7539 meets the green-power requirement and is intended for the use in those modern switching power suppliers and adaptors which demand higher power efficiency and power-saving. It integrates more functions to reduce the external components counts and the size. Its major features are described as below.

Under Voltage Lockout (UVLO)

An UVLO comparator is implemented in it to detect the voltage on the VCC pin. It would assure the supply voltage enough to turn on the LD7539 PWM controller and further to drive the power MOSFET. As shown in Fig. 13, a hysteresis is built in to prevent the shutdown from the voltage dip during startup.

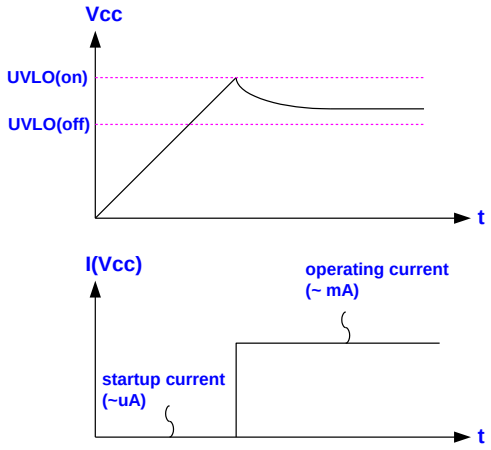


Fig. 13

Startup Current and Startup Circuit

The typical startup circuit to generate V_{CC} of the LD7539 is shown in Fig. 14. During the startup transient, the V_{CC} is below UVLO threshold. Before it has sufficient voltage to develop OUT pulse to drive the power MOSFET, R1 will provide the startup current to charge the capacitor C1. Once V_{CC} obtains enough voltage to turn on the LD7539 and further to deliver the gate drive signal, it will enable the auxiliary winding of the transformer to provide supply current. Lower startup current requirement on the PWM controller will help to increase the value of R1 and then reduce the power consumption on R1. By using CMOS process and the special circuit design, the maximum startup current for LD7539 is only 14μA.

If a higher resistance value of the R1 is chosen, it will take usually more time to start up. To carefully select the value of R1 and C1 will optimize the power consumption and startup time.

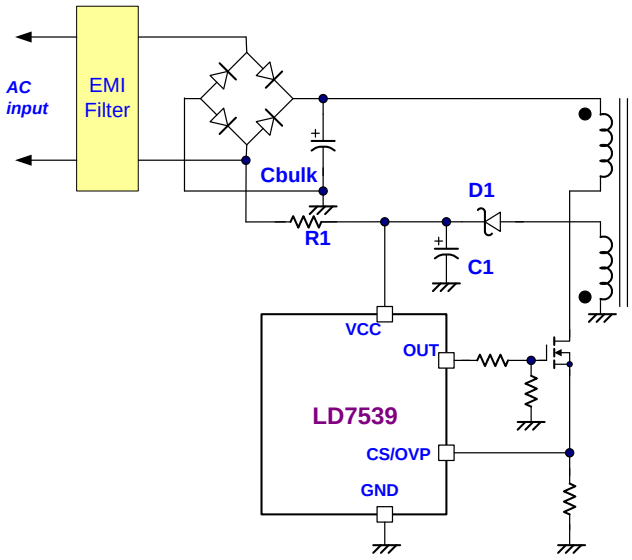


Fig. 14

Current Sensing and Leading-edge Blanking

The typical current mode of PWM controller feedbacks both current signal and voltage signal to close the control loop and achieve regulation. As shown in Fig. 15, the LD7539 detects the primary MOSFET current from the CS pin, which is not only for the peak current mode control but also for the pulse-by-pulse current limit. The maximum voltage threshold of the current sensing pin is set at 0.85V. From above, the MOSFET peak current can be obtained from below.

$$I_{PEAK(MAX)} = \frac{0.85V}{R_S}$$

A leading-edge blanking (LEB) time is included in the input of CS pin to prevent the false-trigger from the current spike.

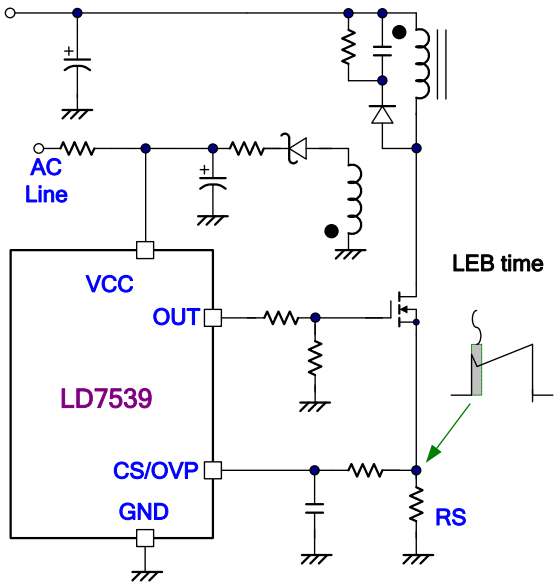


Fig. 15

Output Stage and Maximum Duty-Cycle

An output stage of a CMOS buffer, with typical 250/-500mA driving capability, is incorporated to drive a power MOSFET directly. And the maximum duty-cycle of LD7539 is limited to 75% to avoid the transformer saturation.

Voltage Feedback Loop

The voltage feedback signal is provided from the TL431 at the secondary side through the photo-coupler to the COMP pin of the LD7539. Similar to UC3842, the LD7539 would carry a diode voltage offset at the stage to feed the voltage divider at the ratio of RA and RB, that is,

$$V_{-(PWM_{COMPARATOR})} = \frac{R}{R+2R} \times (V_{COMP} - V_F)$$

A pull-high resistor is embedded internally and can be eliminated externally.

Oscillator and Switching Frequency

The LD7539 is implemented with Frequency Swapping function which helps the power supply designers both to optimize EMI performance and lower system cost. The switching frequency substantially centers at 65KHz, and swap between a range of ±4KHz.

Green-Mode Operation

By using the green-mode control, the switching frequency can be reduced under the light load condition. This feature helps to improve the efficiency at light load. The green-mode control is Leadtrend Technology's own property. Fig. 16 shows the characteristics of the switching frequency vs. the comp pin voltage (V_{COMP})

On/Off Control

The LD7539 will be turned off if COMP pin is pulled below 1.4V. The output of the LD7539 will be disabled immediately under such condition. The off-mode will not be released until the pull-low signal is removed.

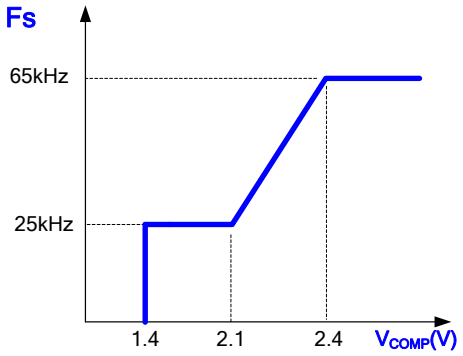


Fig. 16

Internal Slope Compensation

In the conventional applications, the problem of the stability is a critical issue for current mode controlling, when it operates over 50% duty-cycle. As UC384X, It takes slope compensation from injecting the ramp signal of the RT/CT pin through a coupling capacitor. It therefore requires no extra design for the LD7539 since it has integrated it already.

Brownout and OTP Protection

LD7539 is implemented with BNO and OTP protection in one pin. As shown in Fig. 17. It detects BNO signal during

positive cycle of AC input voltage and OTP signal during negative cycle, working with an unfiltered AC input (Line or Neutral). During the positive cycle, S1 will turn on and BNO comparator will sense the input voltage S1. Then, BNO/OTP pin voltage will drop to 0.3V, less than the forward conducted voltage of D1, D2. Meanwhile, there's no more current flowing through NTC to affect BNO function. However, the D1 and D2 will leak a little at high temperature. So, the BNO level will be affected. It's suggested to choose low leakage current type of D1 and D2 (EX: BAS116WS) to increase BNO accuracy. While S1's current stays at low level (<BNO out trip level) for more than a de-bounce time, the BNO comparator will turn off the controller and VCC will hiccup between UVLO-ON and UVLO-OFF until the S1's current draws back above BNO in trip level. The brownout protection is auto recovery.

During negative cycle, the S1 current will sink to 2μA and S1 is disabled, leaving S2 enabled to detect OTP function. After 2ms of OTP detecting time, the OTP function will be disabled and BNO function enabled. When S2 is on, a constant current (I_{OTP}) flows through NTC resistor and produces voltage over BNO/OTP pin. If the BNO/OTP pin voltage is lower than OTP turn-off trip level and lasts for a de-bounce time, latch mode is activated and stops PWM switching. There are two conditions required to restart it successfully. First, cool down the circuit so that NTC resistance will increase and raise BNO/OTP pin voltage up above OTP turn-on trip level. Then, remove the AC power cord and restart AC power-on recycling.

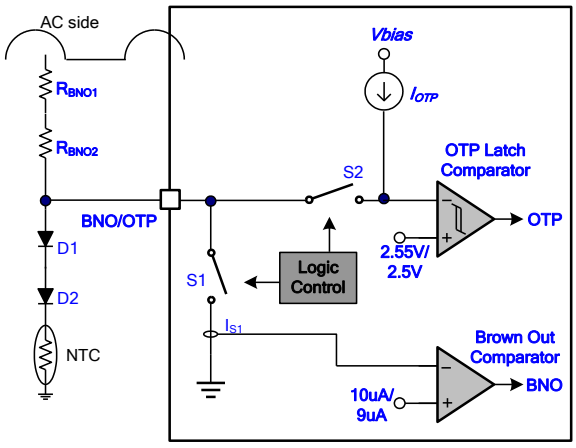


Fig. 17

Adjustable Over Current Compensation (CS/OVP Pin)

In general, the power converter can deliver more current with high input voltage than low input voltage. To compensate this, an offset voltage is added to the CS signal by an internal current source (I_{OCP}) and an external resistor (R_{OCP}) in series between the sense resistor (Rs) and the CS/OVP pin, as shown in Fig. 18. Different values of resistors in series with the CS pin may adjust the amount of compensation. The value of I_{OCP} depends on the duty cycle of OUT pin. The equation of I_{OCP} is decreased as:

$$I_{OCP} = \begin{cases} (0.625 - Duty) \cdot 480uA & (0.125 < Duty < 0.625) \\ 0uA & (Duty \geq 0.625) \\ 240uA & (Duty \leq 0.125) \end{cases}$$

At light load, this offset is in same level of magnitude as the current sense signal, it shall be canceled. Therefore the compensation current will be fully added once the COMP voltage is above 2.9V.

R_{OCP}:470Ω~1.2kΩ; C_{OCP}:47pF~390pF

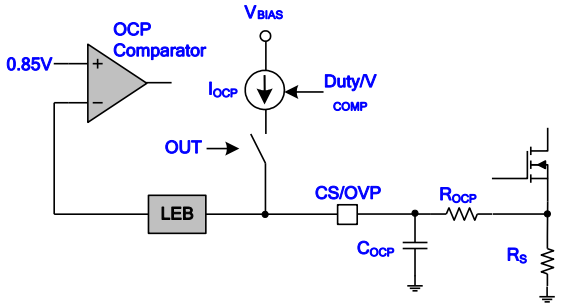


Fig. 18

Output Over Voltage Protection (CS/OVP Pin) - Latch mode

An output overvoltage protection is implemented in the LD7539, as shown in Fig. 19 and 20. The auxiliary winding voltage is reflected to secondary winding and therefore the flat voltage on the CS/OVP pin is proportional to the output voltage. By sensing the auxiliary voltage via the divided resistors, LD7539 can sample this flat voltage level after some delay time to perform output over-voltage protection. This delay time is used to ignore the voltage ringing from leakage inductance of PWM transformer. The sampling voltage level is compared with internal threshold voltage 0.2V. If the sampling voltage exceeds the OVP trip level, an internal counter starts counting subsequent OVP events. The counter has been added to prevent incorrect OVP detection which might occur during ESD or lightning events. However, if typically 8 cycles of subsequent OVP events are detected, the OVP circuit switches the power MOSFET off. As the protection is latched, the converter restarts only after the internal latch is reset.

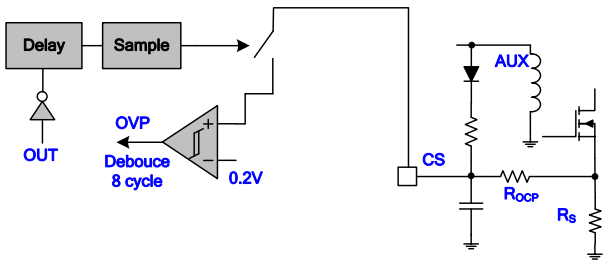


Fig. 19

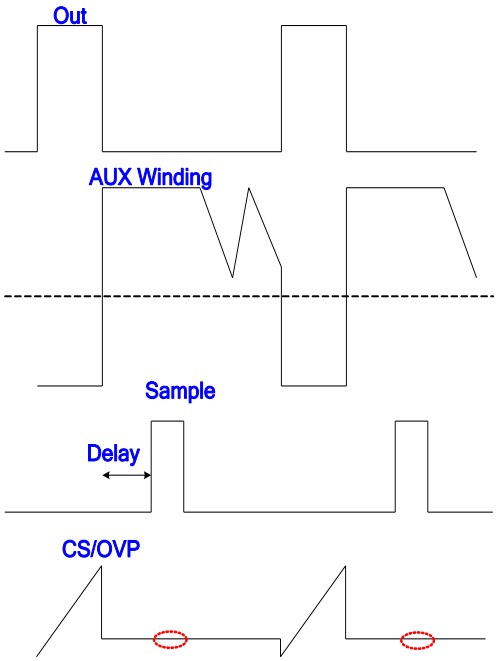


Fig. 20

Over Load Protection (OLP) - Auto Recovery

To protect the circuit from damage due to over-load condition and short or open-loop condition, the LD7539 is built in with smart OLP function. It also features auto recovery; see Fig. 21 for the waveform. In case of fault condition, the feedback system will force the voltage loop toward the saturation and then pull the voltage high on COMP pin (VCOMP). When the V_{COMP} ramps up to the OLP threshold and continues over OLP delay time, the protection will be activated and then turn off the gate output to stop the switching of power circuit.

With the protection mechanism, the average input power will be minimized to remain the component temperature and stress within the safe operating area.

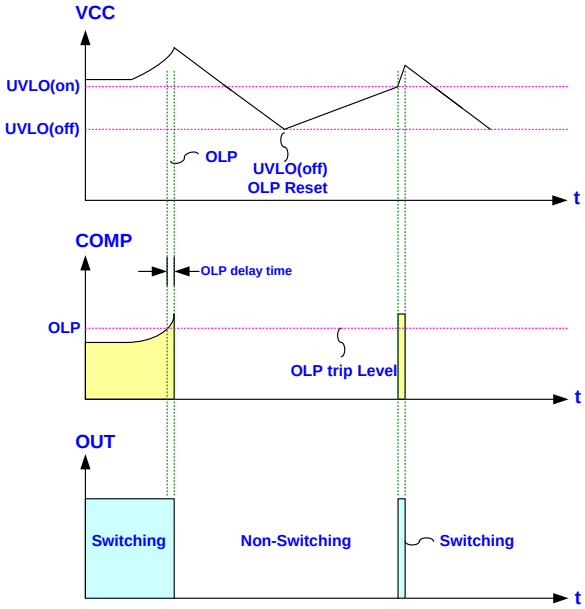


Fig. 21

OVP (Over Voltage Protection) on Vcc - Latch mode

LD7539 features Vcc OVP in latch mode. As soon as the voltage over the Vcc pin rises above OVP threshold, the output gate drive circuit will be shutdown simultaneous to latch off the power MOSFET. On the contrast, if the voltage on Vcc pin drops below OVP threshold and starts AC-recycling again, it will soon resume to normal operation. Fig. 22 shows its operation.

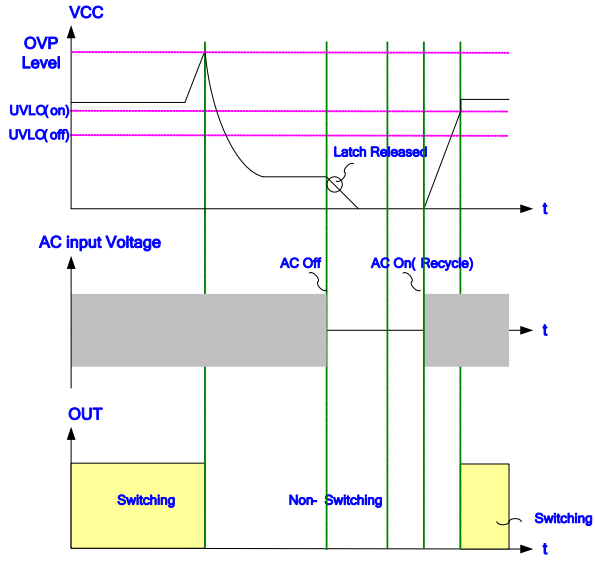


Fig. 22

MOSFET Characteristic

The MOSFET is divided into three operation regions, ohmic region, saturation region, and the cut-off region, shown as Fig. 23. For switching power supply applications, it shall operate in ohmic and cut-off region. Never reach the region of saturation; it would cause damage for acting beyond the maximum safety operating area. It's necessary to check the characteristic of MOSFET. Fig. 24 shows a totem pole architecture for the circuit of OUT. The output high level of OUT is at around VCC-1.5V. Refer to on-region characteristics of the MOSFET, check the saturation current of $VGS_{H(MIN)}$ to make sure the saturation current is high enough to activate MOSFET to operate in ohmic region. In order not to decrease the voltage across VG, it's recommended not to connect a forward diode between the gate of the MOSFET and OUT pin, for example like Fig 25.

In addition, pulling VCC level high can keep VGSH in high level, for example:

1. Increase N_X value to pull VCC level high.
2. Increase VCC capacitance to improve VCC's performance to drop at startup transient, shown as Fig 26.

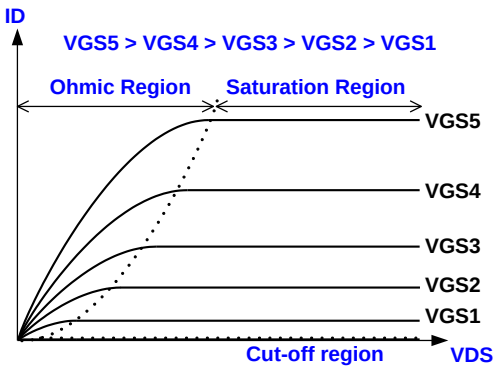


Fig. 23

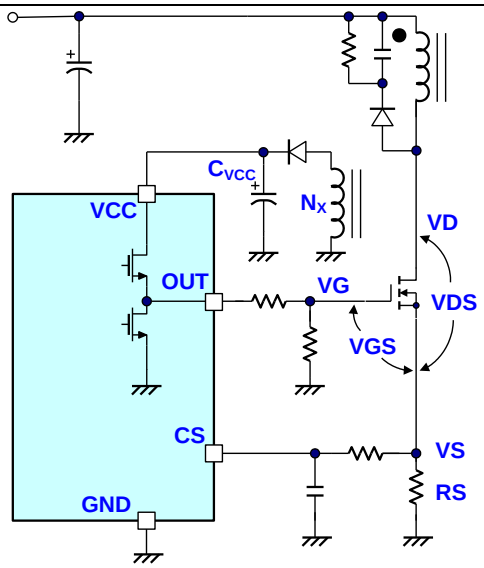


Fig. 24

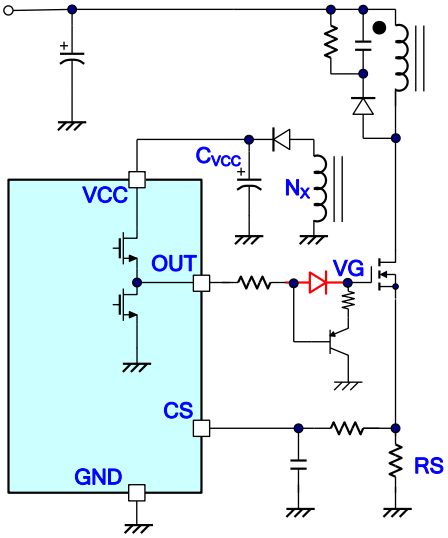


Fig. 25

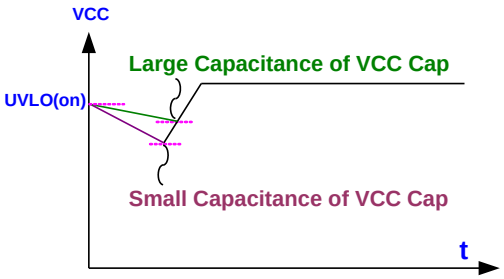
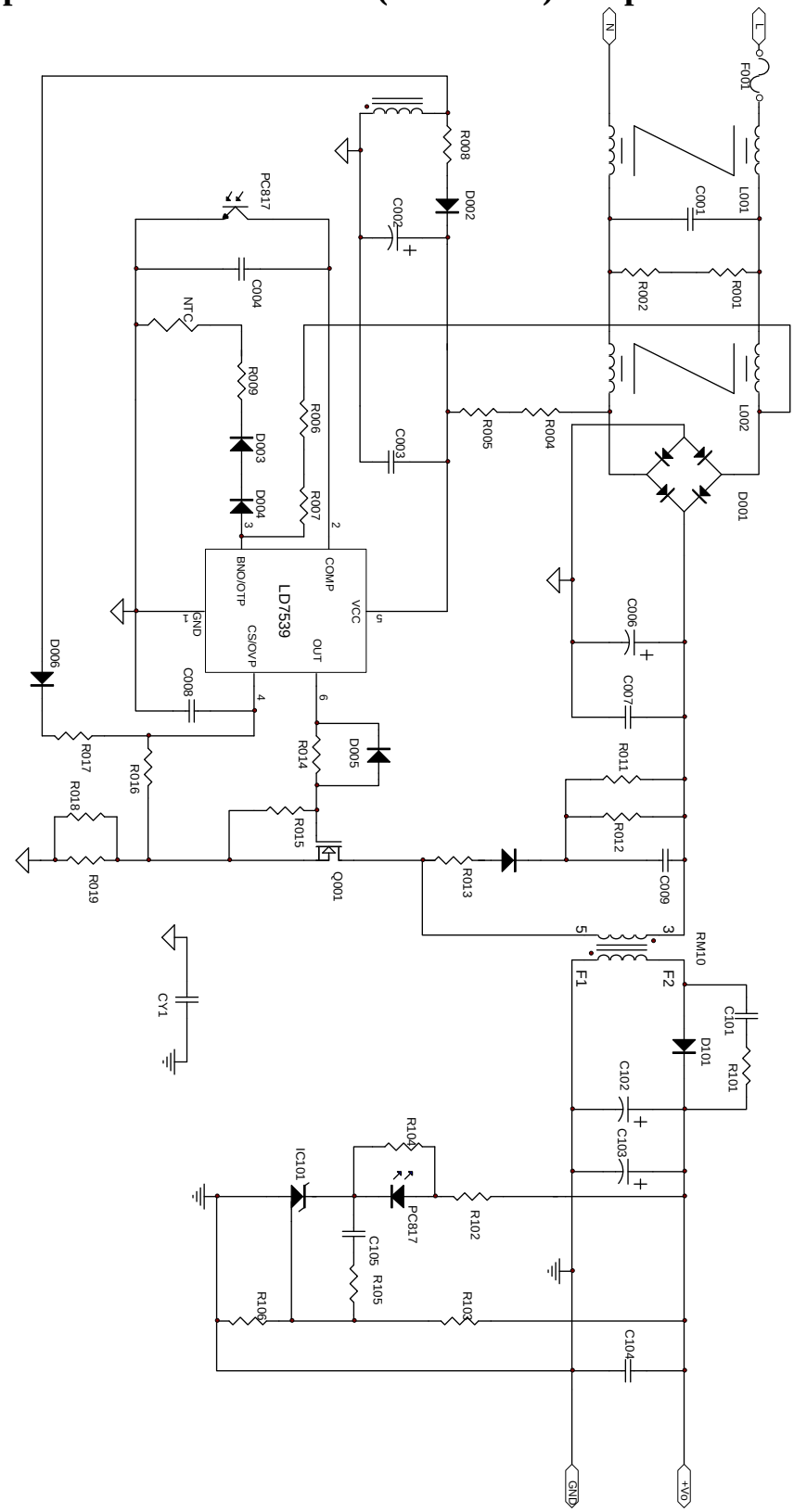


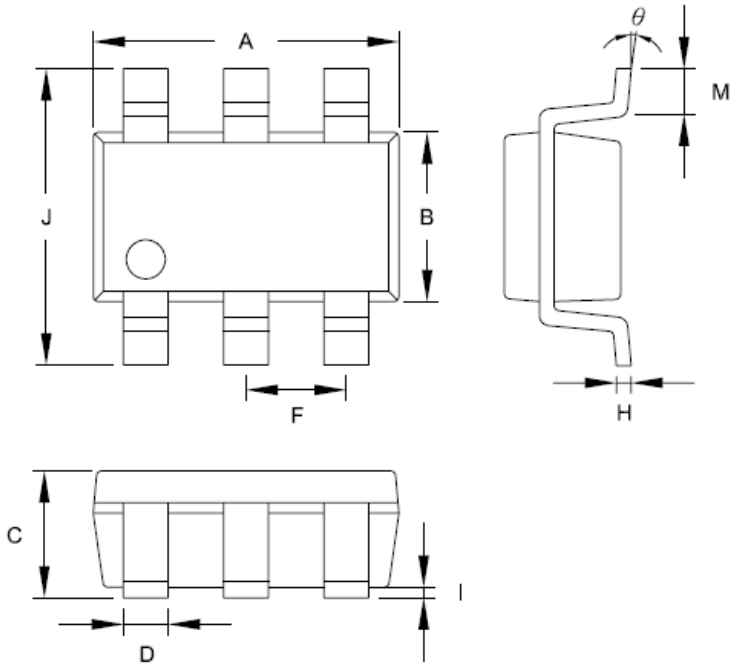
Fig. 26

Reference Application Circuit --- 65W (19V/3.42A) Adapter



Package Information

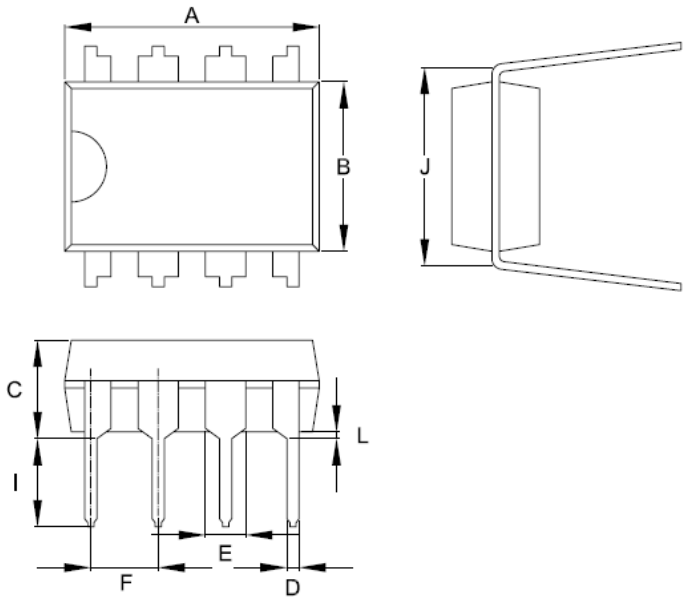
SOT-26



Symbol	Dimension in Millimeters		Dimensions in Inches	
	Min	Max	Min	Max
A	2.692	3.099	0.106	0.122
B	1.397	1.803	0.055	0.071
C	-------	1.450	-------	0.057
D	0.300	0.500	0.012	0.020
F	0.95 TYP		0.037 TYP	
H	0.080	0.254	0.003	0.010
I	0.050	0.150	0.002	0.006
J	2.600	3.000	0.102	0.118
M	0.300	0.600	0.012	0.024
θ	0°	10°	0°	10°

Package Information

DIP-8



Symbol	Dimension in Millimeters		Dimensions in Inches	
	Min	Max	Min	Max
A	9.017	10.160	0.355	0.400
B	6.096	7.112	0.240	0.280
C	-----	5.334	------	0.210
D	0.356	0.584	0.014	0.023
E	1.143	1.778	0.045	0.070
F	2.337	2.743	0.092	0.108
I	2.921	3.556	0.115	0.140
J	7.366	8.255	0.29	0.325
L	0.381	------	0.015	--------

Important Notice

Leadtrend Technology Corp. reserves the right to make changes or corrections to its products at any time without notice. Customers should verify the datasheets are current and complete before placing order.

Revision History

Rev.	Date	Change Notice
00	12/24/2012	Original Specification