Design Specification

OLED Display Controller
And
Driver IC

LD7138

Version 1.0
2012/05/10

LDT Inc. Mplaza 3F, 538, Dujeong-dong, Seobuk-gu, Cheonan, Chungnam, 331-958, Korea
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◎ Revision History

REV.	Contents	Date
1.0	The First Version.	2012.04.16

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1. FEATURES

Power Supply
VCC_C = 8 ~ 18V
VDD = 1.65 ~ 3.3V

Display Area
Max. 128(RGB) x 128 (Pixel) for 65K Color

Graphics RAM
Dot matrix : 128 **x** 16 Bit **x** 128 **=** 262,144 Bit

Column Driver
Max 128(RGB) Outputs
65K Color
Maximum Output Current = 255uA (1uA Step), Maximum Peak Current = 1008uA (16 Step)
Next Pin to Pin Current Deviation ±2.0% (Iout = 100uA)
Current Deviation at 1Chip Max-Min ±4.0% (Iout = 100uA)
Average Current Deviation against absolute level ±6.0% (Iout = 100uA)

Row Driver
Max. 128 Outputs
Variable duty ratio (1 to 128)
ON resistance typical 25ohm (Max. 40ohm)

CPU Interface
8bit Write and Read
Address A0 is used to select command and parameter (data)
Selectable 68/80 series parallel bus or serial interface
Parallel I/F : write cycle 10MHz
read cycle 2MHz
Serial I/F : serial clock 10MHz when write mode,
serial clock 2MHz when read mode

Advanced Display Features
Adjustable Frame Frequency (60Hz ~ 120Hz).
Internal Regulator for Row Driver.
Oscillator & Reference resistor is internal.

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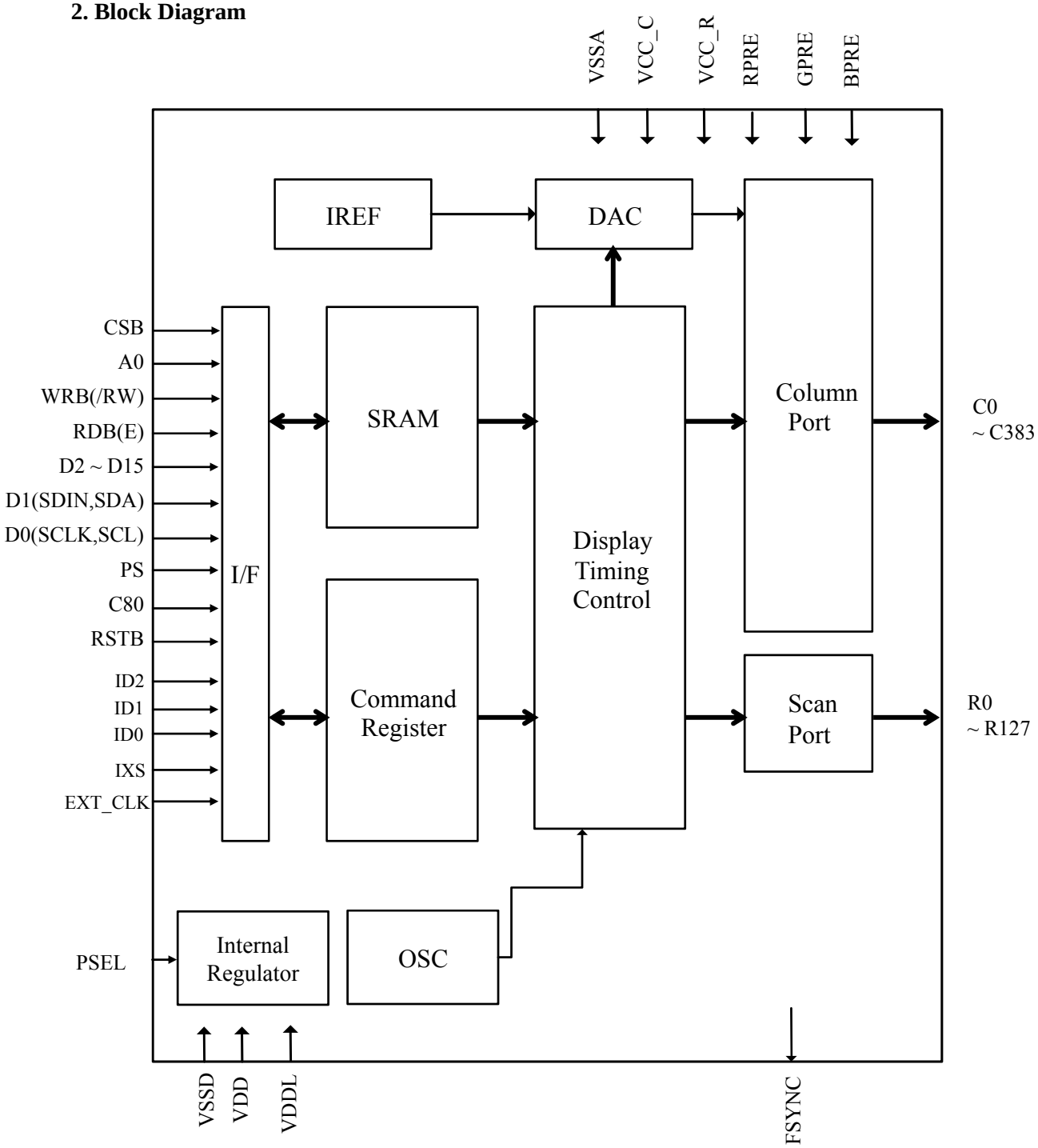
2. Block Diagram



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3. PIN DESCRIPTION

3. 1. Pin Description

PIN NAME	TYPE	I/O	Function
VDD	Power	-	Interface Power & Analog Power
VDDL			Internal Logic Power. Refer to application guide. Capacitor is connected between VDDL and VSSD.
VSSA			Analog (Driver) GND
VSSD			Logic GND
VCC_C	Power	-	Column Driver Power
VCC_R			This pin is the power output pin of internal row power regulator. A 4.7uF capacitor is recommended to connect between V_{CC_R} and GND. If internal row power regulator is disabled, It must be connected to the external high voltage source.
RPRE			Column Driver Pre-Charge Power for Red
GPRE			Column Driver Pre-Charge Power for Green
BPRE			Column Driver Pre-Charge Power for Blue
PSEL		I	This pin enable/disable internal logic power regulator. When this pin is tied with VDD pin, it is the internal logic power regulator enabled.

PIN NAME	TYPE	I/O	Function
D15 ~ D0	Host Interface Pins	I/O	These are 16-bit bi-directional data bus to be connected to the microprocessor's data bus. When I2C interface mode is selected, D1 will be the I2C data input (SDA) and D0 will be the I2C bus clock input (SCL), and D2 ~ D15 should be tied VDD or VSS. When serial interface mode is selected, D1 will be the serial data input (SDIN), D0 wil l be the serial clock input (SCLK), and D2 ~ D15 should be tied VDD or VSS or floating.
ID2/ID0		I	These pins configure I2C interface address. Using these pins. I2C Address can be selected.
WRB/ RW		I	Write (Active Low) for 80 Series, H : Read, L : Write for 68 Series
RDB/ E		I	Read (Active Low) for 80 Series, Read or Write Enable for 68 Series
A0		I	Address (L: command, H: Parameter)
RSTB		I	Reset (Active Low)
CSB		I	Chip Select (Active Low)
C80		I	H: 68CPU L: 80CPU
PS		I	H: Parallel L: Serial
IXS		I	H : I2C is selected, L : I2C is not selected
EXT_CLK	Clock Input Pin	I	External Clock Input Pin
FSYNC	Other	O	Frame Signal & Oscillator Clock output

*. Interface Mode Table

Interface Mode	PS	IXS
Parallel	1	X
Serial SPI	0	0
Serial I2C	0	1

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PIN NAME	TYPE	I/O	Function
R0 ~ R127	OLED Driver Pins	O	OLED Dot Matrix Row Output
C0 ~ C383			OLED Dot Matrix Column Output

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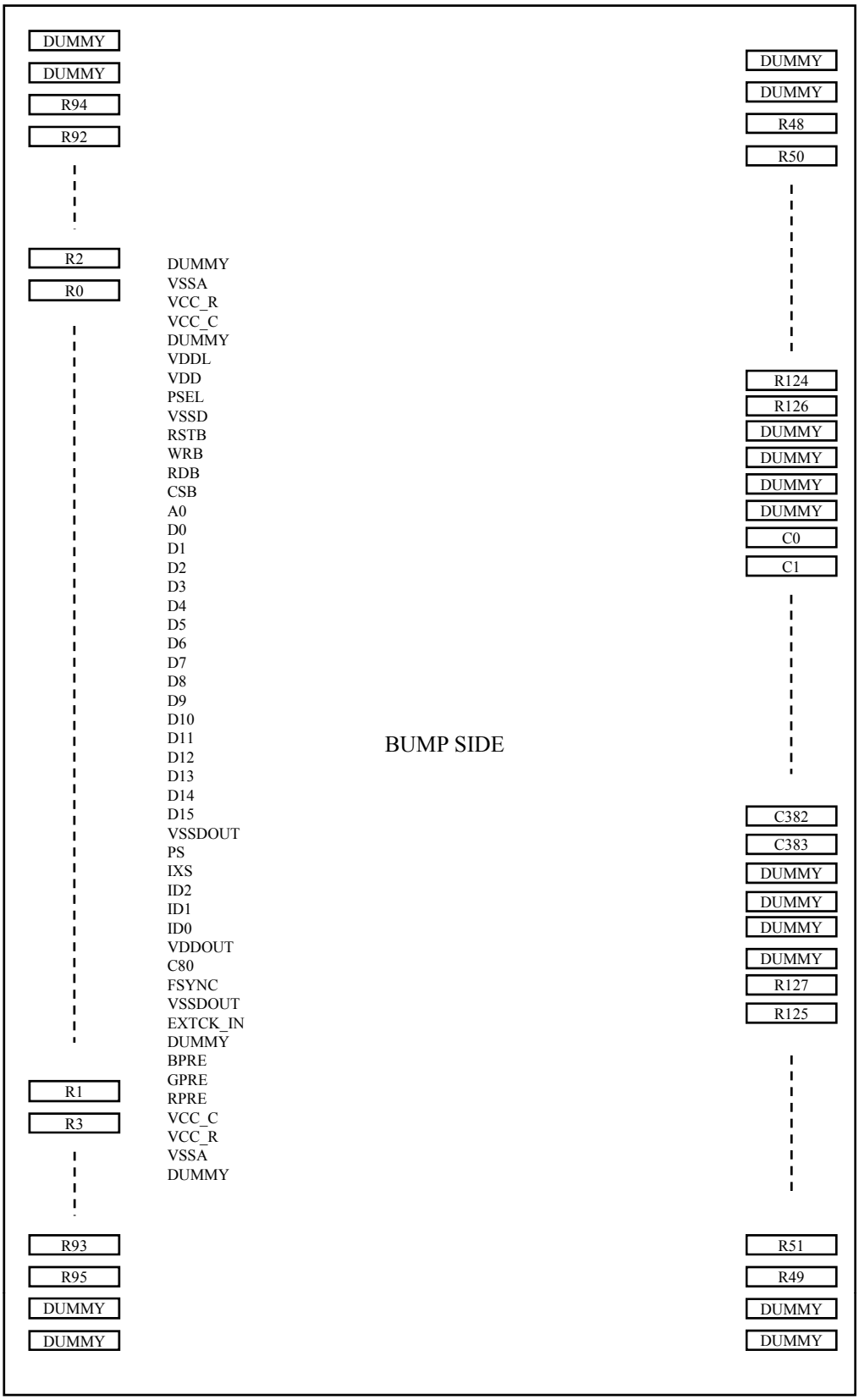
3. 2. Pad Layout



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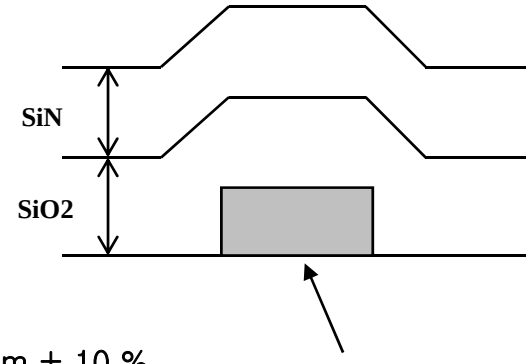
3. 2. 1 Bump Specification

Feature

- Bump Height = 12um ± 3um
- Bump Area = 1200um^2 (Min.) except dummy pad
- Bump Height Tolerant (All the Lot) : Typ. Value ± 3um
- Bump Height Tolerant (1 Wafer) : Typ. Value ± 2um
- Bump Height Tolerant (1 Chip) : R (Max. – Min.) within 2um
- Bump Hardness 60 ± 20HV
- Bump Gap = 15um (Typ) ± 2um (Min. 11um)
- Bump Dimple ≤ 1.5um

3. 2. 2 Passivation Thickness



SiN : 1300nm ± 10 %
SiO2 : 300nm ± 10 %

3. 2. 3 Thickness of the Chip

- 350um ± 20um

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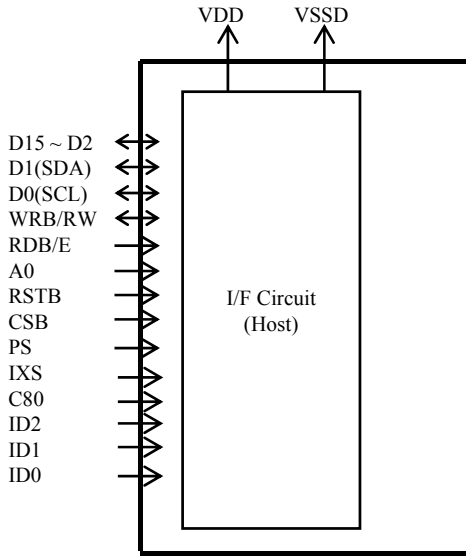
4. Host Interface Block Diagram

4.1. Block Diagram



4.2. Format

- 16bit Data Bus

<table>
<tr><td colspan="2">Command</td></tr>
<tr><td>Write the Address</td><td>Write the Parameter</td></tr>
<tr><td rowspan="2">1st
15 0
Command</td><td>2nd
15 0
Parameter</td></tr>
<tr><td>Write the Graphic Data</td></tr>
<tr><td></td><td>2nd
15 0
Parameter
2Byte = 1 Pixels (RGB)</td></tr>
</table>

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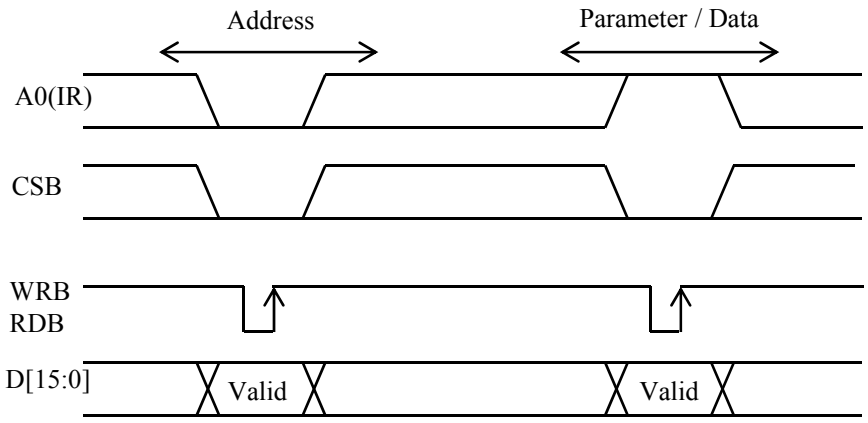
4.3. Timing

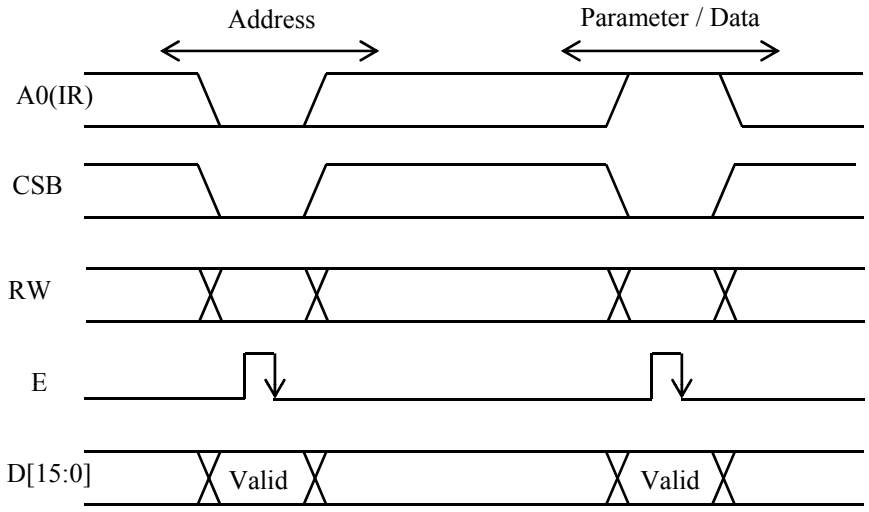
- Parallel Interface (80 Series CPU)

Function	CSB	WRB	RDB	A0(IR)	D[15:0]
Write Command	L	↑	H	L	Command
Write Parameter or Data	L	↑	H	H	Parameter or Data
Read Parameter or Data	L	H	↑	H	Parameter or Data



- Parallel Interface (68 Series CPU)

Function	CSB	RW	E	A0(IR)	D[15:0]
Write Command	L	L	↓	L	Command
Write Parameter or Data	L	L	↓	H	Parameter or Data
Read Parameter or Data	L	H	↓	H	Parameter or Data



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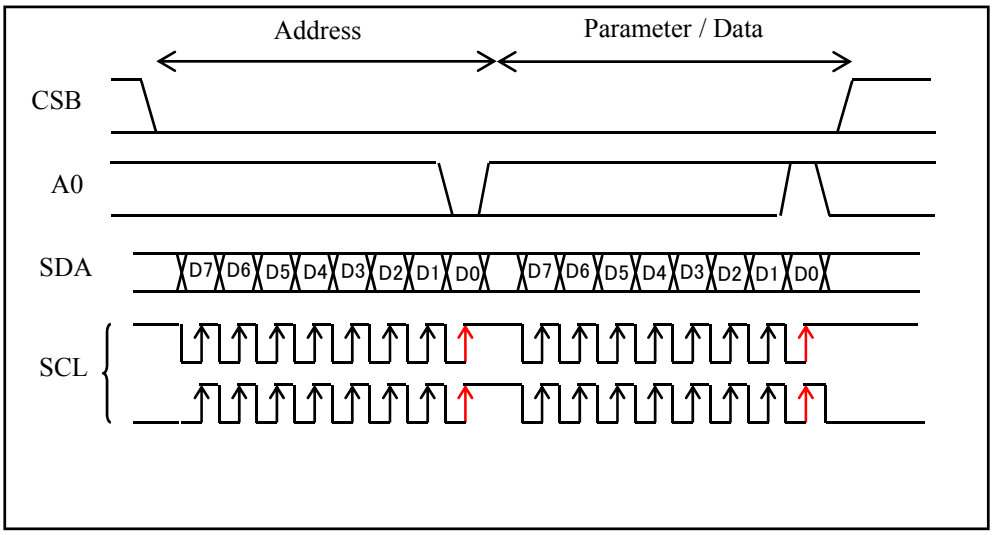
- Serial Interface

This IC's IF can be connected to SPI IF.
The high level of CSB signal clears the internal buffer of SDA and SCL Counter .
The 8th SCL fixes the address or data (parameter) according to A0 status.

Write Timing



◇ Notice

- All command inputs have a priority over previous commands.
- To select Parallel/Serial Interface use PS Input. (H: Parallel L: Serial)
- Serial clock (SCL) works in the unit of 8 clocks.

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- I2C Interface

The bidirectional I2C bus consists of the serial clock (SCL) and serial data (SDA) lines. Both lines must be connected to a positive supply through a pull-up resistor when connected to the output stages of a device. Data transfer may be initiated only when the bus is not busy.

I2C communication with this device is initiated by a master sending a Start condition, a high-to-low transition on the SDA input/output while the SCL input is high (see Figure 1). After the Start condition, the device address byte is sent, most significant bit (MSB) first, including the data direction bit (R/W).

After receiving the valid address byte, this device responds with an acknowledge (ACK), a low on the SDA input/output during the high of the ACK-related clock pulse.

On the I2C bus, only one data bit is transferred during each clock pulse. The data on the SDA line must remain stable during the high pulse of the clock period, as changes in the data line at this time are interpreted as control commands (Start or Stop) (see Figure 2).

A Stop condition, a low-to-high transition on the SDA input/output while the SCL input is high, is sent by the master (see Figure 1).

Any number of data bytes can be transferred from the transmitter to receiver between the Start and the Stop conditions. Each byte of eight bits is followed by one ACK bit. The transmitter must release the SDA line before the receiver can send an ACK bit. The device that acknowledges must pull down the SDA line during the ACK clock pulse so that the SDA line is stable low during the high pulse of the ACK-related clock period (see Figure 3). When a slave receiver is addressed, it must generate an ACK after each byte is received. Similarly,
the master must generate an ACK after each byte that it receives from the slave transmitter. Setup and hold times must be met to ensure proper operation.

A master receiver will signal an end of data to the slave transmitter by not generating an acknowledge (NACK) after the last byte has been clocked out of the slave. This is done by the master receiver by holding the SDA line high. In this event, the transmitter must release the data line to enable the master to generate a Stop condition.

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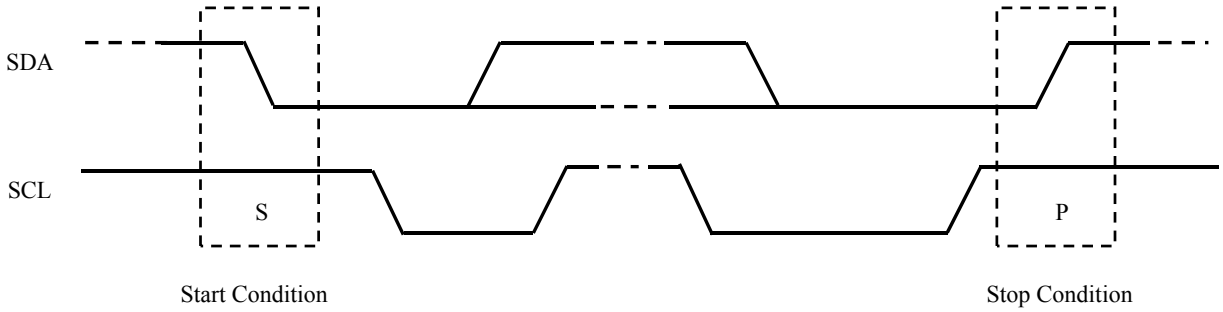

Figure 1. Definition of Start and Stop Conditions

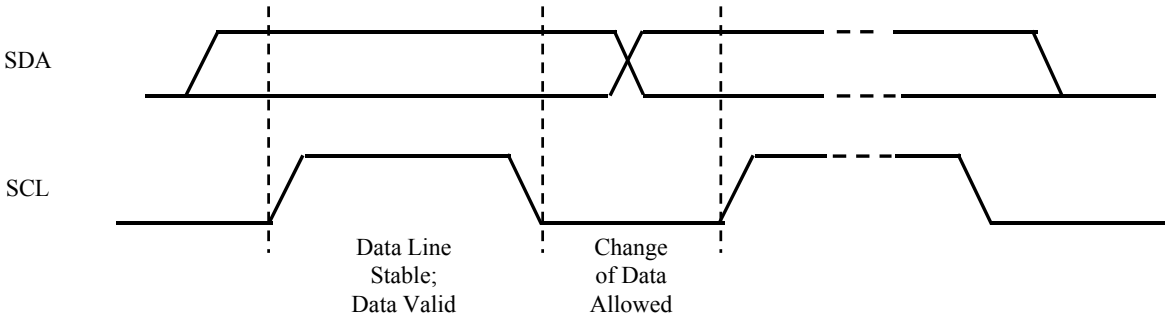

Figure 2. Bit Transfer

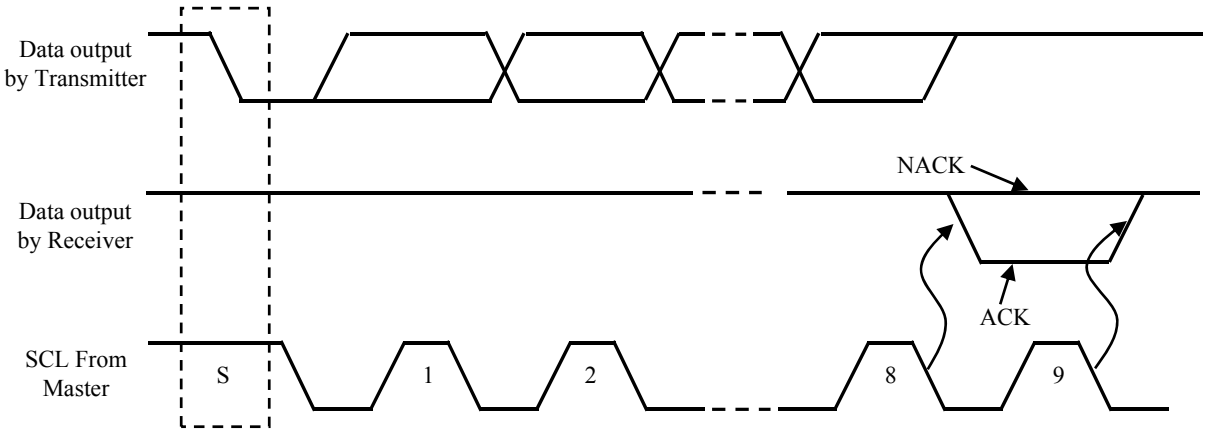

Figure 3. Acknowledgement on I2C Bus

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- I2C Device ID Address

Following a START condition, the bus master must output the address of the slave it is accessing. The address is shown in Figure 4. To conserve power, no internal pull-up resistors are incorporated on the hardware selectable address pins and they must be pulled HIGH or LOW.

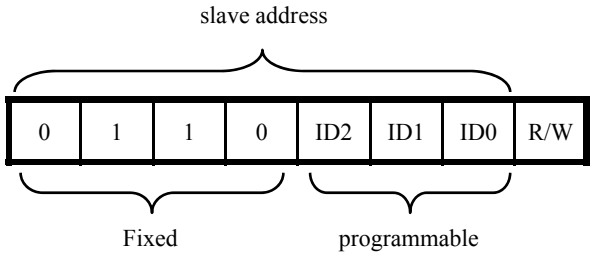

Figure 4. Device ID Address

The last bit of the address byte defines the operation to be performed. When set to logic 1 a read is selected, while a logic 0 selects a write operation.

MSB bit is first transfered.

- I2C Bus Transactions

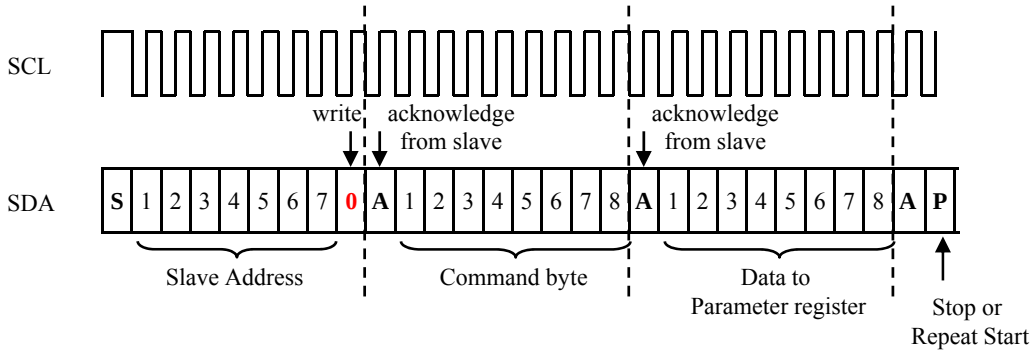

Figure 5. Write Single Parameter Command

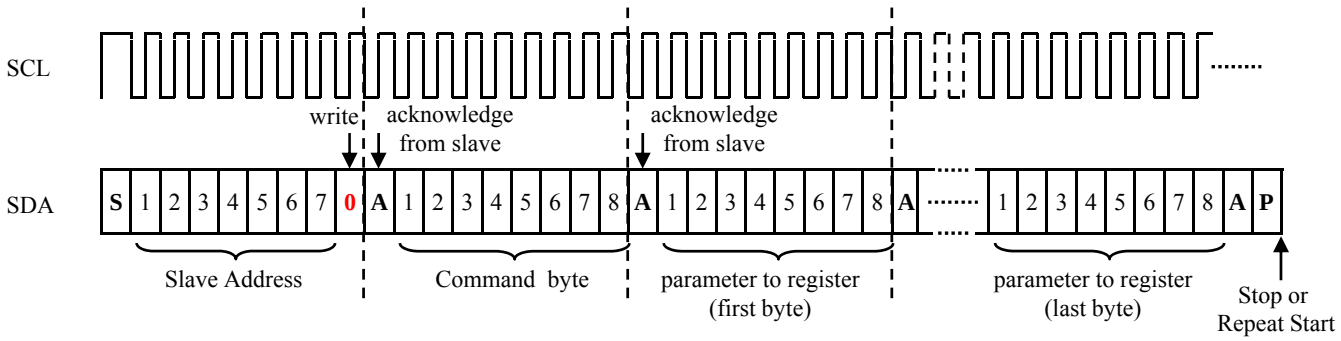

Figure 6. Write Multi Parameter Command

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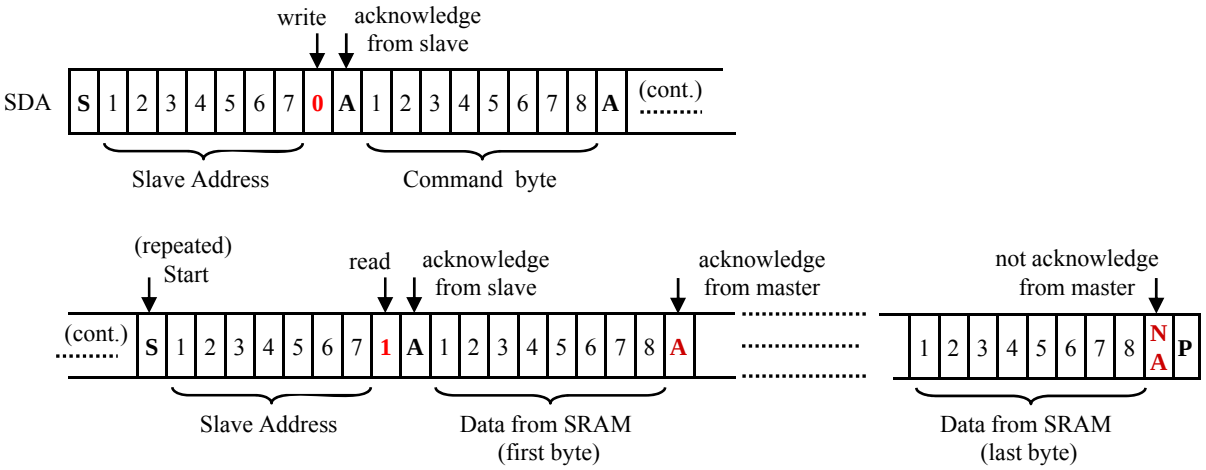

Figure 7. Read From SRAM

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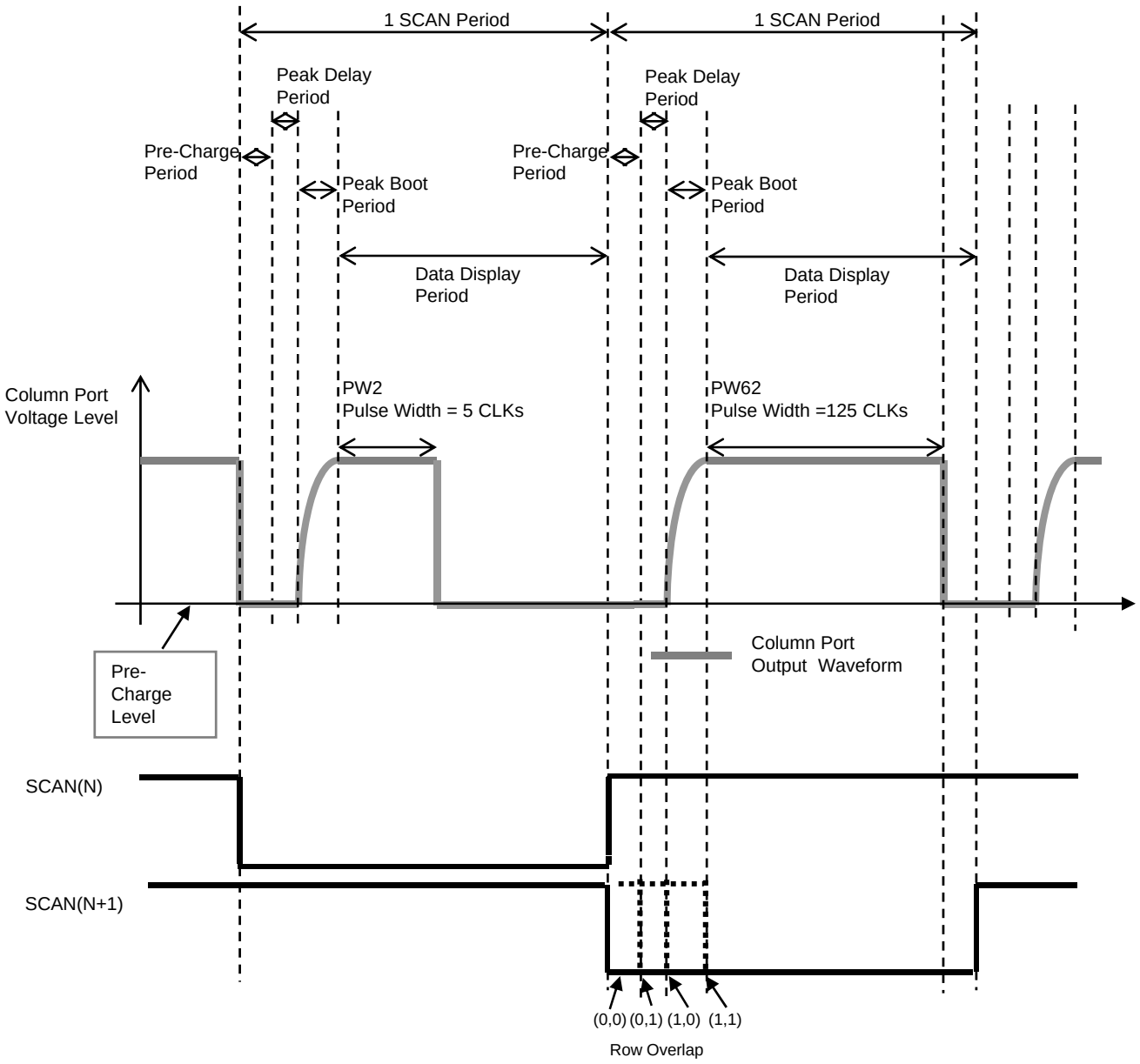
4.4. Column / Scan Driver Output Wave Form



Related Command

1. PreC_Width
2. PeakDelay
3. PeakWidth(RGB)
4. Dot Data Current(RGB)
5. Dot Peak Current(RGB)
6. Row Overlap

Gray Scale (Pulse Width)	Unit (DCLK)
PW0	0
PW1	3
PW2	5
⋮	⋮
PW62	125
PW63	127

Gamma Correction Table

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5. Command Register

5.1. Command Register List & Map

Address	Register Name	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	Default
01h	SOFTRES	-	-	-	-	-	-	-	-	-
02h	DDISPON/OFF	-	-	-	-	-	-	-	D0	00h
03h	DSTBYON/OFF	-	-	-	-	-	-	-	D0	01h
04h	DFRAME	-	-	-	-	M	F2	F1	F0	02h
05h	WriteDirection	-	-	-	-	D3	D2	D1	D0	00h
06h	ScanDirection	-	-	-	-	-	-	-	D0	00h
07h	DispSize	-	-	-	-	-	FX6	FX5	FX4	00h
		-	-	-	-	FX3	FX2	FX1	FX0	00h
		-	-	-	-	-	TX6	TX5	TX4	07h
		-	-	-	-	TX3	TX2	TX1	TX0	0Fh
		-	-	-	-	-	FY6	FY5	FY4	00h
		-	-	-	-	FY3	FY2	FY1	FY0	00h
		-	-	-	-	-	TY6	TY5	TY4	07h
		-	-	-	-	TY3	TY2	TY1	TY0	0Fh
08h	IF_BUS_SEL	-	-	-	-	-	-	D1	I0	00h
09h	Data_Masking	-	-	-	RV	-	R	G	B	07h
0Ah	MBoxSize	-	-	-	-	-	XS6	XS5	XS4	00h
		-	-	-	-	XS3	XS2	XS1	XS0	00h
		-	-	-	-	-	XE6	XE5	XE4	07h
		-	-	-	-	XE3	XE2	XE1	XE0	0Fh
		-	-	-	-	-	YS6	YS5	YS4	00h
		-	-	-	-	YS3	YS2	YS1	YS0	00h
		-	-	-	-	-	YE6	YE5	YE4	07h
		-	-	-	-	YE3	YE2	YE1	YE0	0Fh
0Bh	DISPStart	-	-	-	-	-	DX6	DX5	DX4	00h
		-	-	-	-	DX3	DX2	DX1	DX0	00h
		-	-	-	-	-	DY6	DY5	DY4	00h
		-	-	-	-	DY3	DY2	DY1	DY0	00h

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5.1. Command Register List & Map

Address	Register Name	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	Default
0Ch	DataWrite/Read	D7	D6	D5	D4	D3	D2	D1	D0	-
0Dh	READREG	D7	D6	D5	D4	D3	D2	D1	D0	-
0Eh	DotCurrent	-	-	-	-	IR7	IR6	IR5	IR4	00h
		-	-	-	-	IR3	IR2	IR1	IR0	00h
		-	-	-	-	IG7	IG6	IG5	IG4	00h
		-	-	-	-	IG3	IG2	IG1	IG0	00h
		-	-	-	-	IB7	IB6	IB5	IB4	00h
		-	-	-	-	IB3	IB2	IB1	IB0	00h
0Fh	PeakCurrent	-	-	PR5	PR4	PR3	PR2	PR1	PR0	00h
		-	-	PG5	PG4	PG3	PG2	PG1	PG0	00h
		-	-	PB5	PB4	PB3	PB2	PB1	PB0	00h
10h	SCLK	-	-	-	-	SCLK3	SCLK2	SCLK1	SCLK0	01h
1Ch	PreC_Width	-	-	D5	D4	D3	D2	D1	D0	08h
1Dh	PeakWidth	-	-	D5	D4	D3	D2	D1	D0	05h
		-	-	D5	D4	D3	D2	D1	D0	05h
		-	-	D5	D4	D3	D2	D1	D0	05h
1Eh	PeakDelay	-	-	-		D3	D2	D1	D0	05h
1Fh	Row_Scan	-	-	D5	D4	D3	-	D1	D0	00h
30h	VCC_R_SEL	-	-	-	EN	-	D2	D1	D0	04h
34h	RGB_MODE	-	-	-	-	-	-	-	D0	00h
3Ah	Gamma_Tune	-	-	-	-	I3	I2	I1	I0	00h
3Bh	Gamma_Init	-	-	-	-	-	-	-	-	-
3Eh	TEST	-	-	-	-	-	-	D1	D0	00h

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5.2. Description of Command Register

5.2.1. Normal Display Command

(1) Software Reset (0x01h)

Instruction	W/R	A0	D7	D6	D5	D4	D3	D2	D1	D0	Default
SOFTRES	W	L	0	0	0	0	0	0	0	1	

◆ All registers are initialized with default value without altering the graphic RAM.
◆ All Dot display are turned OFF.
◆ The OSC. is stopped.

(2) Set Dot Matrix Display ON/OFF (0x02h)

Instruction	W/R	A0	D7	D6	D5	D4	D3	D2	D1	D0	Default
DDISP ON/OFF	W	L	0	0	0	0	0	0	1	0	
PARAMETER	W	H	-	-	-	-	-	-	-	P0	00h

◆ P0 = 0: indicates the dot matrix display turns OFF (Default).
◆ P0 = 1: indicates the dot matrix Display turns ON.

※NOTE

Display OFF means

- All Column Output go to pre-charge level.
- All Row Output go to the ground level
- Stop Data transfer from memory to Dot Matrix Driver.

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(3) Set Dot Matrix Display Stand-by ON/OFF (0x03h)

Instruction	W/R	A0	D7	D6	D5	D4	D3	D2	D1	D0	Default
DSTBYON/OFF	W	L	0	0	0	0	0	0	1	1	
PARAMETER	W	H	-	-	-	-	-	-	-	P0	01h

◆ P0 = 0 : Indicates the dot oscillator is starting. And it does not make the dot matrix display turn ON.
◆ P0 = 1 : Indicates the dot oscillator is stopping. And it make the dot matrix display OFF.
※NOTE
After software or hardware reset command is executed, it makes dot matrix display stand-by ON.

(4) Set OSC Control (0x04h)

Instruction	W/R	A0	D7	D6	D5	D4	D3	D2	D1	D0	Default
DFRAME	W	L	0	0	0	0	0	1	0	0	
PARAMETER	W	H	-	-	-	-	M0	F2	F1	F0	02h

◆ Parameter Definition

F2	F1	F0	Frame Frequency *1)
0	0	0	60Hz
0	0	1	75Hz
0	1	0	90Hz(Default) *2)
0	1	1	105Hz
1	0	0	120Hz

◆ OSC mode selection
M0 = 0 Internal RC Oscillation mode
= 1 External Clock mode

*1) Conditions
Pre-Charge_Width(Pcw) = 8
Peak-Pulse_Width(Ppw) = 5
Peak_Pulse_Delay(Pdw) = 5
Scan Nember(Scan_N) = 128
*2) Osc_Frequency(Fosc) = 3.4 MHz

Frame Frequency(Hz) = 1 / [(1/Fosc)*(Pcw+Ppw+Pdw+129) * Scan_N]

(5) Set Graphic RAM Writing Direction (0x05h)

Instruction	W/R	A0	D7	D6	D5	D4	D3	D2	D1	D0	Default
Write Direction	W	L	0	0	0	0	0	1	0	1	
PARAMETER	W	H	-	-	-	-	D3	D2	D1	D0	00h

◆ D3=0: indicates the Graphic RAM is accessed by order of RGB.
◆ D3=1: indicates the Graphic RAM is accessed by order of BGR

Refer to Page. 39 (Memory Map)

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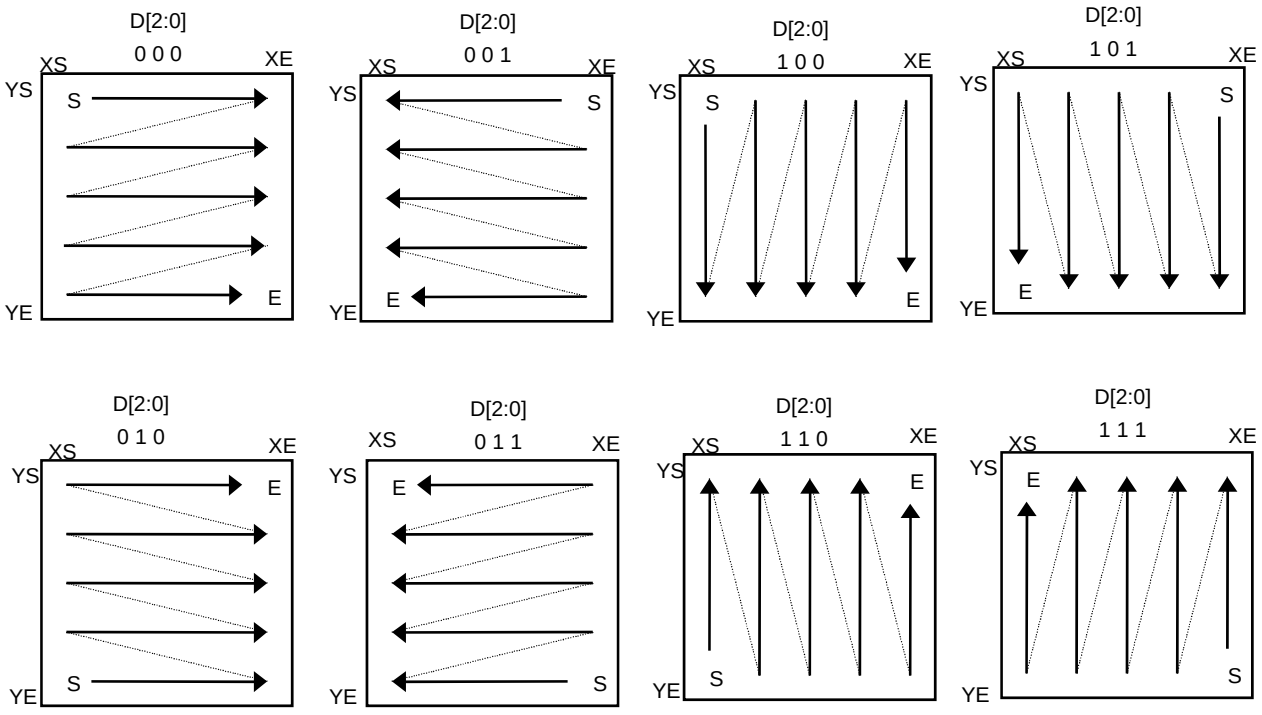


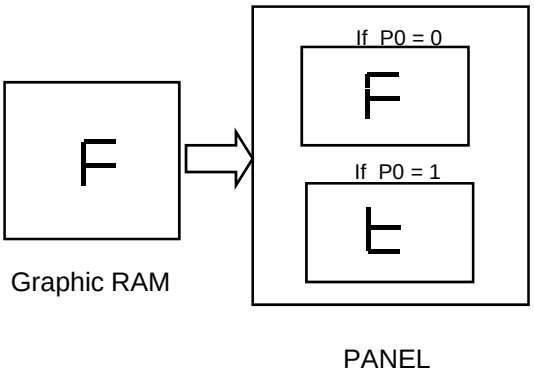
(6) Set Row Scan Direction (0x06h)

Instruction	W/R	A0	D7	D6	D5	D4	D3	D2	D1	D0	Default
ScanDirection	W	L	0	0	0	0	0	1	1	0	
PARAMETER	W	H	-	-	-	-	-	-	-	P0	00h

◆ P0 = 0: indicates row address is scanning from min. to max.

◆ P0 = 1: indicates row address is scanning from max. to min.

For example is as bellows;



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(7) Set Display Size (0x07h)

Instruction	W/R	A0	D7	D6	D5	D4	D3	D2	D1	D0	Default
DispSize	W	L	0	0	0	0	0	1	1	1	
1st Xstart 1	W	H	-	-	-	-	-	FX6	FX5	FX4	00h
2nd Xstart 2	W	H	-	-	-	-	FX3	FX2	FX1	FX0	00h
3rd Xend 1	W	H	-	-	-	-	-	TX6	TX5	TX4	07h
4th Xend 2	W	H	-	-	-	-	TX3	TX2	TX1	TX0	0Fh
5th Ystart 1	W	H	-	-	-	-		FY6	FY5	FY4	00h
6th Ystart 2	W	H	-	-	-	-	FY3	FY2	FY1	FY0	00h
7th Yend 1	W	H	-	-	-	-	-	TY6	TY5	TY4	07h
8th Yend 2	W	H	-	-	-	-	TY3	TY2	TY1	TY0	0Fh

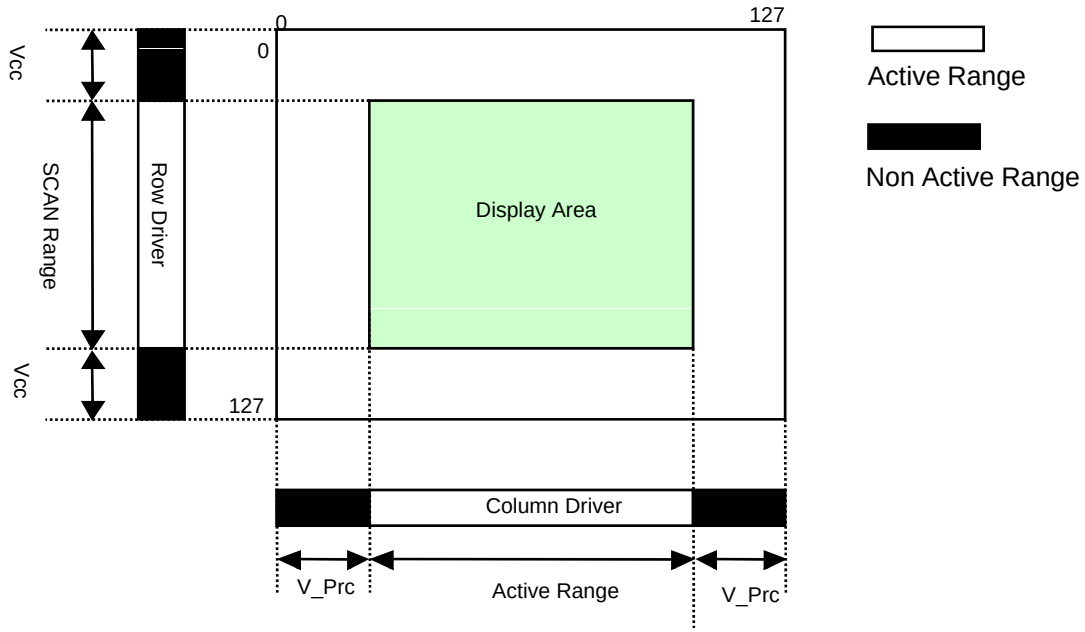
◆ Setting Row and Column Outputs Range (= Active area).

◆ From FX to TX ：The range of active Column Outputs setting. (Range : 00h up to 7Fh)
Setting Value = Pixel number –1
”Xend＜Xstart” is inhibited.

◆ From FY to TY ：The range of active Row Outputs setting. (Range：00h up to 7Fh)
Setting Value = Pixel number –1
”Yend＜Ystart” is inhibited.

※NOTE

1. The outputs that are out of setting range go to Pre_charge voltage for Column and VCC for Row.
2. Line scan frequency is same under any display size. Frame frequency is changed by DispSize command.



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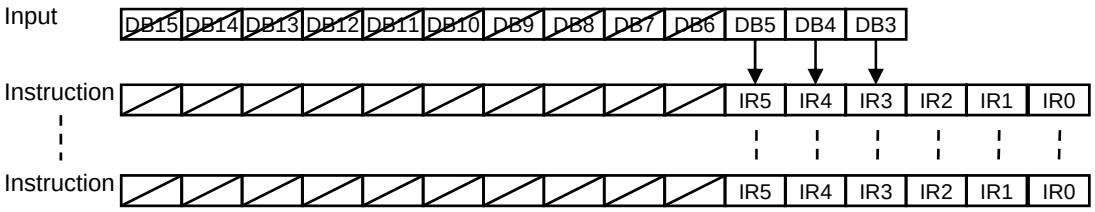
(8) Set Interface Bus Type (0x08h)

Instruction	W/R	A0	D7	D6	D5	D4	D3	D2	D1	D0	Default
I/F Bus Sel	W	L	0	0	0	0	1	0	0	0	
Parameter	W	H	-	-	-	-	-	-	P1	P0	00h

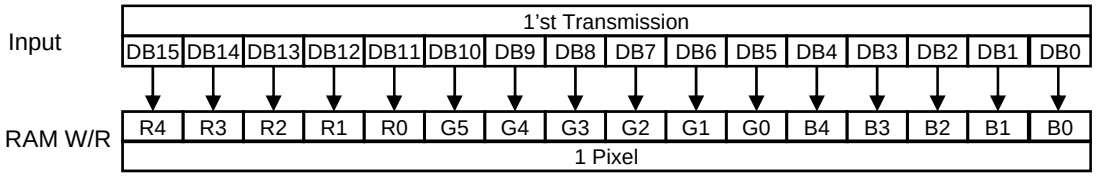
P1	P0	Description
0	0	6Bit I/F Bus
0	1	8Bit I/F Bus
1	1	16Bit I/F Bus

When Serial I/F and I2C,
Interface Bus Type is must be 6BIT or 8BIT I/F Bus.

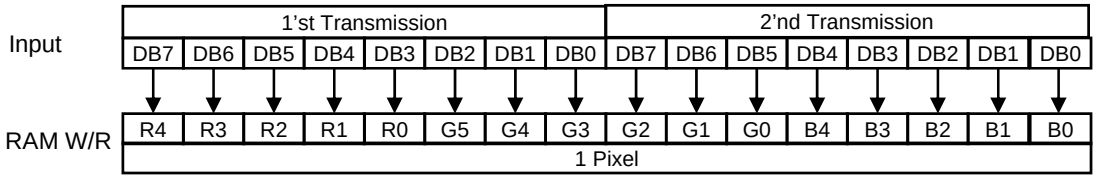
Instruction



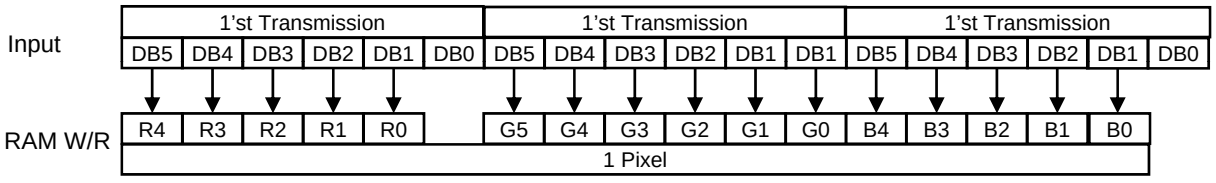
16-Bit I/F(65K color)



8-Bit I/F(65K color)



6-Bit I/F(65K color)



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(9) Set Masking Data (0x09h)

Instruction	W/R	A0	D7	D6	D5	D4	D3	D2	D1	D0	Default
Data_Masking	W	L	0	0	0	0	1	0	0	1	
PARAMETER	W	H	-	-	-	RV	-	R	G	B	07h

When RV ="1", Output Data = (Data XOR "FFFFh") AND Pallet (R,G,B).

◆ When RV ="0", Data AND Pallet(R,G,B) ⇒ Output Data

◆ For example, If pallet is (0,1,1) then R data is 00h and G&B is Display Data.

(10) Set Read/Write Box Data (0x0Ah)

Instruction	W/R	A0	D7	D6	D5	D4	D3	D2	D1	D0	Default
MBOXSize	W	L	0	0	0	0	1	0	1	0	
1st Xstart 1	W	H	-	-	-	-	-	XS6	XS5	XS4	00h
2nd Xstart 2	W	H	-	-	-	-	XE3	XE2	XE1	XE0	00h
3rd Xend 1	W	H	-	-	-	-	-	XE6	XE5	XE4	07h
4th Xend 2	W	H	-	-	-	-	XE3	XE2	XE1	XE0	0Fh
5th Ystart 1	W	H	-	-	-	-	-	YS6	YS5	YS4	00h
6th Ystart 2	W	H	-	-	-	-	YS3	YS2	YS1	YS0	00h
7th Yend 1	W	H	-	-	-	-	-	YE6	YE5	YE4	07h
8th Yend 2	W	H	-	-	-	-	YE3	YE2	YE1	YE0	0Fh

XS6-XS0 ：X axis Reading/Writing Start Point (Range: 00h ~ 7Fh)

◆ XE6-XE0 ：X axis Reading/Writing End Point (Range: 00h ~ 7Fh)

"XE < XS" is inhibited.

◆ YS6-YS0 ： Y axis Reading/Writing Start Point (Range: 00h~7Fh)

◆ YE6-YE0 ： Y axis Reading/Writing Start Point (Range: 00h~7Fh)

"YE<YS" is inhibited.

◆ After this command executes, writing address is set like under table.

Writing Direction Mode	X address	Y address
00	XS	YS
01	XE	YS
10	XS	YE
11	XE	YE

※NOTE : Refer to the Writing Direction Set Command.

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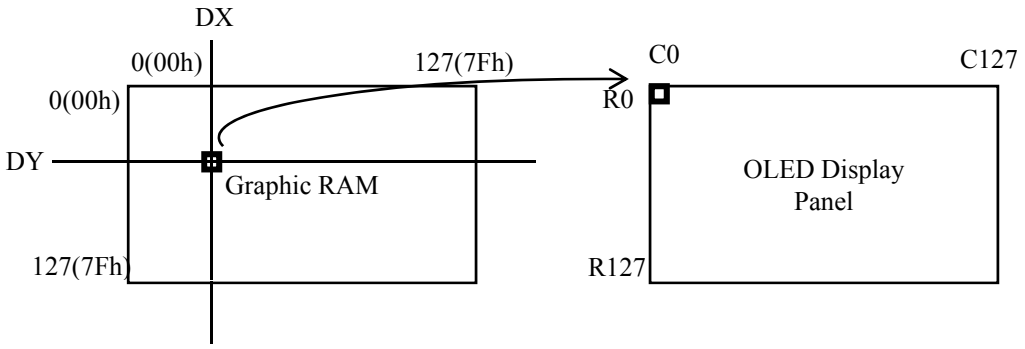
(11) Set Display Start Address (0x0Bh)

Instruction	W/R	A0	D7	D6	D5	D4	D3	D2	D1	D0	Default
DISPStart	W	L	0	0	0	0	1	0	1	1	
1st Parameter	W	H	-	-	-	-	-	DX6	DX5	DX4	00h
2nd Parameter	W	H	-	-	-	-	DX3	DX2	DX1	DX0	00h
3rd Parameter	W	H	-	-	-	-	-	DY6	DY5	DY4	00h
4th Parameter	W	H	-	-	-	-	DY3	DY2	DY1	DY0	00h

◆ This command shift the memory reading address.
◆ DX6-DX0 ：X axis Reading Start address. (Range: 00h ~ 7Fh)
◆ DY6-DY0 ：Y axis Reading Start address (Range：00h ~ 7Fh)



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(12) Read/Write Dot matrix Display Data (0x0Ch)

Instruction	W/R	A0	D7	D6	D5	D4	D3	D2	D1	D0
DataWrite/Read	W	L	0	0	0	0	1	1	0	0

Parameter Mode	W/R	A0	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
16 Bit Write/Read	W/R	H	R4	R3	R2	R1	R0	G5	G4	G3	G2	G1	G0	B4	B3	B2	B1	B0

Parameter Mode	W/R	A0	D7	D6	D5	D4	D3	D2	D1	D0
8 Bit Write/ Read	W	H	R4	R3	R2	R1	R0	G5	G4	G3
8 Bit Write/ Read	W	H	G2	G1	G0	B4	B3	B2	B1	B0

Parameter Mode	W/R	A0	D7	D6	D5	D4	D3	D2	D1	D0
6Bit Write/ Read	W/R	H	-	-	R4	R3	R2	R1	R0	-
6Bit Write/ Read	W/R	H	-	-	G5	G4	G3	G2	G1	G0
6Bit Write/ Read	W/R	H	-	-	B4	B3	B2	B1	B0	-

- ◆ This command can't write data in the out of reading / writing-box.
- ◆ Address is auto increment acceding to WriteDirection setting direction.
- ◆ When memory address increment/decrement is reached at the end of reading /writing-box memory write finish.
- ◆ If you read / write again, re-inter "Data Write/Read" command.

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◆ Data Write Sequence

Seq.	RW	A0	16Bit DATA BUS	8 Bit DATA BUS	6 Bit DATA BUS
1	W	L	Data Write/ Read command	Data Write/ Read command	Data Write / Read command
2	W	H	Write 1st Parameter	Write 1st Upper Parameter.	Write 1st Upper Parameter.
3	W	H	Write 2nd Parameter	Write 1st Lower Parameter.	Write 1st Middle Parameter.
4	W	H	:	:	Write 1st Lower Parameter.
:	:	:	:	:	:
N+1	W	H	Write nth Parameter	:	:
:	:	:		:	:
2N	W	H		Write nth Upper Parameter.	:
2N+1	W	H		Write nth Lower Parameter.	:
:	:	:			:
3N-1	W	H		.	Write nth Upper Parameter.
3N	W	H			Write nth Middle Parameter.
3N+1	W	H			Write nth Lower Parameter.

◆ Data Read Sequence

Seq.	RW	A0	16 Bit Mode DATA BUS	8 Bit Mode DATA BUS	6 Bit Mode DATA BUS
1	W	L	DataWrite/ Read command	Data Write/ Read command	Data Write/ Read command
2	R	H	Dummy	Dummy	Dummy
3	R	H	Read 1st Parameter	Dummy	Dummy
4	R	H	Read 2nd Parameter	Read 1st Upper Parameter.	Dummy
5	R	H		Read 1st Lower Parameter.	Read 1st Upper Parameter.
6	R	H			Read 1st Middle Parameter.
7	R	H	:	:	Read 1st Lower Parameter.
:	:	:	:	:	:
N+2	R	H	Read nth Parameter	:	:
:	:	:		:	:
2N+2	R	H		Read nth Upper Parameter.	:
2N+3	R	H		Read nth Lower Parameter.	:
:	:	:		:	:
3N+2	R	H			Read nth Upper Parameter.
3N+3	R	H			Read nth Middle Parameter.
3N+4	R	H			Read nth Lower Parameter.

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(13) Read Register Status (0x0Dh)

Instruction	W/R	A0	D7	D6	D5	D4	D3	D2	D1	D0	Default
READREG	W	L	0	0	0	0	1	1	0	1	
Parameter	R	H	-	-	D5	D4	D3	D2	D1	D0	
:	R	H	-	-	:	:	:	:	:	:	
Parameter	R	H	-	-	D5	D4	D3	D2	D1	D0	

◆ Read out specific internal register

Order	Register
1	DDISP_ON/OFF, DSTBY_ON/OFF
2	DispSize XS<6:4>
3	DispSize XS<3:0>
4	DispSize XE<6:4>
5	DispSize XE<3:0>
6	DispSize YS<6:4>
7	DispSize YS<3:0>
8	DispSize YE<6:4>
9	DispSize YE<3:0>
10	Row Overlap<1:0>

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(14) Set Dot Matrix Current Level (0x0Eh)

Instruction	W/R	A0	D7	D6	D5	D4	D3	D2	D1	D0	Default
DotCurrent	W	L	0	0	0	0	1	1	1	0	
1st Parameter	W	H	-	-	-	-	IR7	IR6	IR5	IR4	00h
2nd Parameter	W	H	-	-	-	-	IR3	IR2	IR1	IR0	00h
3rd Parameter	W	H	-	-	-	-	IG7	IG6	IG5	IG4	00h
4th Parameter	W	H	-	-	-	-	IG3	IG2	IG1	IG0	00h
5th Parameter	W	H	-	-	-	-	IB7	IB6	IB5	IB4	00h
6th Parameter	W	H	-	-	-	-	IB3	IB2	IB1	IB0	00h

◆ Parameter Definition (1.0uA Step)

I[7:0]	Output Current [Iref]
00h	0.0 uA
01h	1.0 uA
:	:
FEh	254.0 uA
FFh	255.0 uA

(15) Set Dot Matrix Peak Current Level (0x0Fh)

Instruction	W/R	A0	D7	D6	D5	D4	D3	D2	D1	D0	Default
PeakCurrent	W	L	0	0	0	0	1	1	1	1	
1st Parameter	W	H	-	-	PR5	PR4	PR3	PR2	PR1	PR0	00h
2nd Parameter	W	H	-	-	PG5	PG4	PG3	PG2	PG1	PG0	00h
3rd Parameter	W	H	-	-	PB5	PB4	PB3	PB2	PB1	PB0	00h

◆ Parameter Definition (16uA Step)

I[7:0]	Output Current [Iref]
00h	0.0 uA
01h	16.0 uA
:	:
3Eh	992.0 uA
3Fh	1008.0 uA

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(16) Set Pre-Charge Width (0x1Ch)

Instruction	W/R	A0	D7	D6	D5	D4	D3	D2	D1	D0	Default
PreC_Width	W	L	0	0	0	1	1	1	0	0	
1st Parameter	W	H	-	-	T5	T4	T3	T2	T1	T0	08h

◆ Parameter Definition (DCLK Unit)

T[5:0]	Pre-Charge Pulse Width
01h	1
:	
08h	8 (Default)
:	
3Eh	62
3Fh	63

◆ Parameter Range : 01h ~ 3Fh

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(17) Set Peak Pulse Width (0x1Dh)

Instruction	W/R	A0	D7	D6	D5	D4	D3	D2	D1	D0	Default
PeakWidth	W	L	0	0	0	1	1	1	0	1	
1st Parameter	W	H	-	-	W5	W4	W3	W2	W1	W0	05h (for Red)
2nd Parameter	W	H	-	-	W5	W4	W3	W2	W1	W0	05h (for Green)
3rd Parameter	W	H	-	-	W5	W4	W3	W2	W1	W0	05h (for Blue)

◆ Parameter Definition (DCLK Unit)

W[5:0]	Peak Pulse Width
00h	0
01h	1
:	:
05h	5 (Default)
:	:
3Eh	62
3Fh	63

(18) Set Peak Pulse Delay (0x1Eh)

Instruction	W/R	A0	D7	D6	D5	D4	D3	D2	D1	D0	Default
PeakDelay	W	L	0	0	0	1	1	1	1	0	
Parameter	W	H	-	-	-	-	W3	W2	W1	W0	05h

◆ Parameter Definition (DCLK Unit)

W[3:0]	Peak Pulse Width
00h	0
01h	1
:	:
05h	5 (Default)
:	:
0Eh	14
0Fh	15

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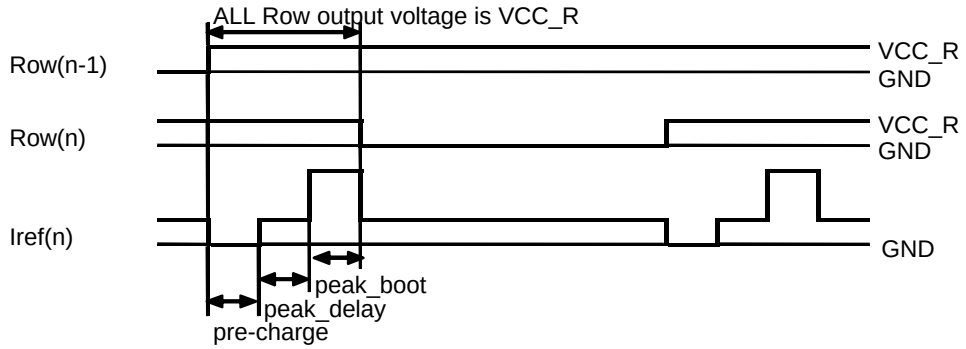
(19) Set Row Scan Operation (0x1Fh)

Instruction	W/R	A0	D7	D6	D5	D4	D3	D2	D1	D0	Default
Row_Scan	W	L	0	0	0	1	1	1	1	1	
Parameter	W	H	-	-	D5	D4	D3	-	D1	D0	00h



◆ Row Output VCC_R timing setting table

D5	D4	All Row VCC_R Time
0	0	None (Default)
0	1	Pre-Charge Timing
1	0	Pre-Charge + Peak Delay Timing
1	1	Pre-Charge + Peak Delay + Max(RGB)Peak boot Timing

◆ Parameter Definition

D3=0 Normal Scan.

D3=1 All Row are in GND.

◆ Row Scan Sequence

D1,D0	Row Scan Mode
00	Mode 1 : alternate scan mode. (Default)
01	Mode 2 : sequential scan mode.
10	Mode 3 : simultaneous scan mode. (half period)

D1,D0	DispDirection	Case of 96 Line Scan
00	0	R0,R1,R2 ….. R126,R127,R0,R1
	1	R127,R126,R93 ….. R1,R0,R127,R126
01	0	R0,R2,R4 ….. R126,R1,R3, ….. R127R0
	1	R127,R125,R91 ….. R1,R126,R124 ….. R0,R127
10	0	R0,R2 ….. R126,R0,R2 ….. R1,R3 ….. R127,R1,R3 …..
	1	R127,R125 ….. R1,R127,R125 ….. R126,R124 ….. R0,R126,R124 …..

◆ In Mode 3, Maximum Row number is 64 line at Display Size setting.

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(20) Set Internal Regulator for Row Scan (0x30h)

Instruction	W/R	A0	D7	D6	D5	D4	D3	D2	D1	D0	Default
VCC_R_SEL	W	L	0	0	1	1	0	0	0	0	
Parameter	W	H	-	-	-	EN	-	D2	D1	D0	04h

◆ EN = “1” => Internal scan regulator enable

◆ EN = “0” => Internal scan regulator disable
* VCC_R pin must be connected to the external voltage source or VCC_C.

When DSTBON/OFF = "1", Internal scan regulator is disable regardless of EN = "1" or EN = "0".

D[2:0]	VCC_R
000	VCC_C × 0.85
001	VCC_C × 0.80
010	VCC_C × 0.75
011	VCC_C × 0.70
100	VCC_C × 0.65

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(21) Set Gamma Correction Table (0x3Ah)

INSTRUCTION	WR	A0	D7	D6	D5	D4	D3	D2	D1	D0	Default	
Gamma Tune	W	L			3		A					
R_PW0	W	H			-	-	-	I6	I5	I4	00h	
	W	H			-	-	I3	I2	I1	I0	00h	
R_PW1	W	H			-	-	-	I6	I5	I4	00h	
	W	H			-	-	I3	I2	I1	I0	04h	
⋮							⋮					64 Parameters
R_PW30	W	H			-	-	-	I6	I5	I4	07h	
	W	H			-	-	I3	I2	I1	I0	08h	
R_PW31	W	H			-	-	-	I6	I5	I4	07h	
	W	H			-	-	I3	I2	I1	I0	0Fh	
G_PW0	W	H			-	-	-	I6	I5	I4	00h	
	W	H			-	-	I3	I2	I1	I0	00h	
G_PW1	W	H			-	-	-	I6	I5	I4	00h	
	W	H			-	-	I3	I2	I1	I0	02h	
⋮							⋮					128 Parameters
G_PW62	W	H			-	-	-	I6	I5	I4	07h	
	W	H			-	-	I3	I2	I1	I0	0Ch	
G_PW63	W	H			-	-	-	I6	I5	I4	07h	
	W	H			-	-	I3	I2	I1	I0	0Fh	
B_PW0	W	H			-	-	-	I6	I5	I4	00h	
	W	H			-	-	I3	I2	I1	I0	00h	
B_PW1	W	H			-	-	-	I6	I5	I4	00h	
	W	H			-	-	I3	I2	I1	I0	04h	
⋮							⋮					64 Parameters
B_PW30	W	H			-	-	-	I6	I5	I4	07h	
	W	H			-	-	I3	I2	I1	I0	08h	
B_PW31	W	H			-	-	-	I6	I5	I4	07h	
	W	H			-	-	I3	I2	I1	I0	0Fh	

(22) Set Gamma Correction Table Initialize (0x3Bh)

Instruction	W/R	A0	D7	D6	D5	D4	D3	D2	D1	D0	Default
Gamma_initial	W	L	0	0	1	1	1	0	1	1	

- This command initialize the Gamma Table to the linear scale.
  Linear Scale : 00h, 02h, 04h, 08h, ..., 7Ah, 7Ch, 7Fh (Green)
  Linear Scale : 00h, 04h, 08h, 0Ch, ..., 74h, 78h, 7Fh (Red, Blue)

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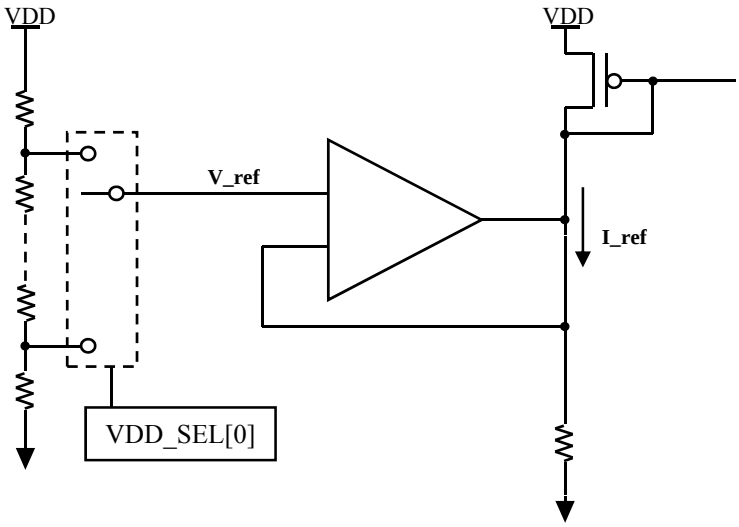
(23) Set VDD Selection (0x3Ch)

Instruction	W/R	A0	D7	D6	D5	D4	D3	D2	D1	D0	Default
VDD_SEL	W	L	0	0	1	1	1	1	0	0	
Parameter	W	H	-	-	-	-	-	-	-	D0	0h

◆ VDD = 2.8V, [D0=0] → Default
◆ VDD = 1.8V, [D0=1]

◆ This command maintains V_ref level constant regardless of various VDD level.



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(24) Set TEST (0x3Eh)

Instruction	W/R	A0	D7	D6	D5	D4	D3	D2	D1	D0	Default
TEST	W	L	0	0	1	1	1	1	1	0	
Parameter	W	H	-	-	-	-	-	-	D1	D0	0h

◆ D[1:0] = 00 : FSYNC outputs VSS (Low).
D[1:0] = 01 : FSYNC outputs frame sync signal.
D[1:0] = 10 : FSYNC outputs oscillator clock.
D[1:0] = 11 : FSYNC outputs SCLK.

(25) Set RGB_MODE Selection (0x34h)

Instruction	W/R	A0	D7	D6	D5	D4	D3	D2	D1	D0	Default
RGB_MODE	W	L	0	0	1	1	0	1	0	0	
Parameter	W	H	-	-	-	-	-	-	-	D0	0h

◆ D[0] = 0 : RGB MODE (default).
D[0] = 1 : GRAY MODE

In GRAY MODE,
R, G, B Paremeter is same value setting at DotCurrent(0Eh), PeakCurrent(0Fh), PeakWidth(1Dh)

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(26) Set System clock division-ratio (0x10h)

Instruction	W/R	A0	D7	D6	D5	D4	D3	D2	D1	D0	Default
SCLK	W	L	0	0	0	1	0	0	0	0	
Parameter	W	H	-	-	-	-	SCLK3	SCLK2	SCLK1	SCLK0	01h

◆ SCLK[3:0] : Selection of clock dividing ratio (for Display Control)

1111 = not used
1110 = 1/1024
1101 = 1/512
1100 = 1/256
1011 = 1/128
1010 = 1/64
1001 = 1/32
1000 = 1/24
0111 = 1/16
0110 = 1/12
0101 = 1/8
0100 = 1/6
0011 = 1/4
0010 = 1/3
0001 = 1/2 Through (Master Clock Frequency)
0000 = nor used

This Register is to set the system clock (SCLK) dividing ratio of the pre-scalar. The Maximum dividing ratio of master clock is 1024 and it is possible to let the clock go through without dividing.

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6. Functional Description

6.1. Memory Map

Memory (65K Color Mode)

MSB		LSB
<15:11>	<10:5>	<4:0>
Red	Green	Blue

1 Address = 1 Pixels

(Default)

Display (65K Color Mode)

1 Pixels

C0	C1	C2
Red	Green	Blue

WriteDirection = 00h

Memory (65K Color Mode)

MSB		LSB
<15:11>	<10:5>	<4:0>
Red	Green	Blue

1 Address = 1 Pixels

Display (65K Color Mode)

1 Pixels

C0	C1	C2
Blue	Green	Red

WriteDirection = 08h

Memory (65K Color Mode)

<15:11>	<10:5>	<4:0>
Red	Green	Blue

1 Address = 1 Pixels

(Default)

Display (65K Color Mode)

1 Pixels

C0	C1	C2
Red	Green	Blue

Column
Memory X Address

Row Memory Y Address	00h	01h	02h	...	7Eh	7Fh
00h	(00,00)	(01,00)	(02,00)	...	(7E,00)	(7F,00)
01h	(00,01)	(01,01)	(02,01)	...	(7E,01)	(7F,01)
...						
7Eh	(00,7E)	(01,7E)	(02,7E)	...	(7E,7E)	(7F,7E)
7Fh	(00,7F)	(01,7F)	(02,7F)	...	(7E,7F)	(7F,7F)

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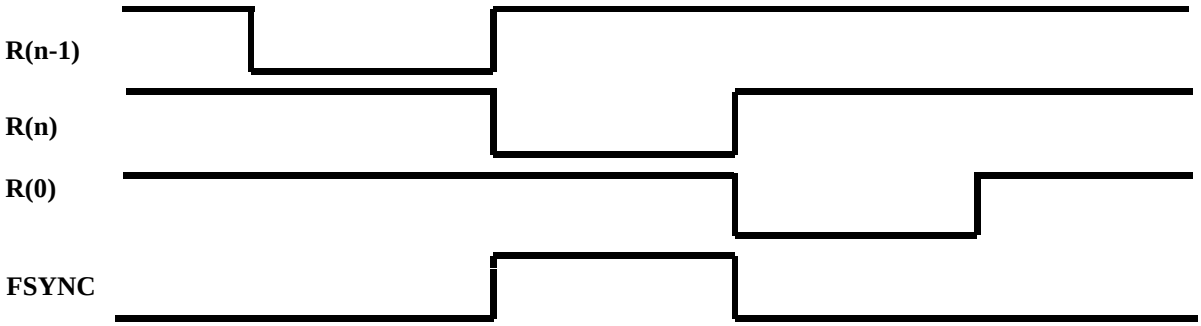
6.2. The Command List synchronized to FSYNC.

These listed commands are synchronized to FSYNC.

Address	Register Name
02h	DDISPOFF
06h	ScanDirection
09h	DataMasking
0Bh	DispStart
0Eh	DotCurrent
3Dh	DMODE



FSYNC is activated by TEST Command (3Eh=01h).

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7. Software Reset

Software Reset (SOFTRES(01h)) has auto-clear-function (within 200ns).
In the Software Reset condition, this IC's function is as follows:

- Display OFF
- Clock Oscillation Halt
- Register Writing is impossible (IF operation halt)
- Internal register (Except the Graphic Data) value is initialized.

8. Hardware Reset (RSTB)

This pad ignores the pulse shorter than 30ns.
In the Hardware Reset condition, this IC's function is as follows:

- Display OFF
- Clock Oscillation Halt
- Register Writing is impossible (IF operation halt)
- Internal register (Except the Graphic Data) value is initialized.

9. Software Sleep

Software Sleep function (DSTBYON/OFF (03h)) makes this IC shift to sleep condition. In the Software Sleep Condition, all display functions are halted and a clock oscillation is suspended, and power consumption is going to the lowest. The default value of this register is "H" (active condition).
All of the internal state in the software sleep and the contents of the data memory are held.

In the Software Sleep condition, this IC's function is as follows:

- Display OFF
- Clock Oscillation Halt
- It is possible to write the Data Memory and the Register.

* After Software Sleep, the register of DDISPON/OFF(02h) is cleared.

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10. Electrical Characteristics

10.1. Absolute Maximum Ratings

10.1.1. Controller Driver Section

(Ta = 25 ± 2 ℃, VSSA=VSSD=0V)

Parameter	Symbol	Conditions	Specification		Unit
			MIN	MAX	
Maximum Supply Voltage	VDD	VDD - VSSD	-0.3	+3.6	V
	VDDL	VDDL - VSSD	-0.3	+2.4	V
	VCC_C	VCC_C - VSSA	-0.3	+20	V
	R/G/BPRE	PRE - VSSA	-0.3	+7	V
	VCC_R	VCC_R - VSSA	-0.3	+20	V
Protection Voltage	VDDIN	All Terminals	-0.3	VDD +0.3	V
Protection Current	Ii	All Terminals		-15	mA
Peak Output Current	Io	All Terminals		+15	mA
Operating Ambient Temp.	TOPR		-40	+85	℃
Retention Ambient Temp.	TSTG		-55	+125	℃

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10.2. Allowance Operating Range

10.2.1. Controller Driver Section

(Ta = 25℃, VSSA=VSSD=0V)

Parameter	Symbol	Conditions	Specification			Unit
			MIN	TYP	MAX	
Maximum Supply Voltage	VDD	VDD - VSSD		2.8	3.3	V
	VDDL	VDDL - VSSD		1.8	2.0	V
	VCC_C	VAH - VSSA	8		18	V
	R/G/BPRE	PRE - VSSA	0		6	V
	VCC_R	VCC_R – VSSA	2.0		18	V
	VSSD(A)			0		V
Input Voltage High	VIH	Logic Input Terminals	0.8*VDD		VDD	V
Input Voltage Low	VIL	Logic Input Terminals	VSS		0.2*VDD	V
Output Voltage (High)	VOH	Logic Output Terminals VDD=3V (Iout = -200uA)	0.9 *VDD		VDD	V
Output Voltage (Low)	VOL	Logic Output Terminals VDD=3V (Iout = 200uA)	VSS		0.1*VDD	V
Input Leakage Current (High)	IIH	Logic Input Terminals	-1.0		+1.0	uA
Input Leakage Current (Low)	IIL	Logic Input Terminals	-1.0		+1.0	uA

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10.2.2. Controller Driver Section

(Ta = 25℃, VSSA=VSSD=0V, VDD=2.8V, VCC_C=VCC_R=18V, R/G/BPRE=0V)

Parameter	Symbol	Conditions	Related Pins	Specification			Unit
				MIN	TYP	MAX	
Output Current Pin to Pin Evenness	Cptp1	Iout = 100uA VDS = **5V**	C0 ~ C287	-2.0		+2.0	%
Output Current Chip In Evenness	Ccin1	Iout = 100uA VDS = **5V**	C0 ~ C287	-4.0		+4.0	%
Output Current Chip to Chip Evenness	Cctc1	Iout = 100uA VDS = **5V**	C0 ~ C287	-6.0		+6.0	%
Peak Current Pin to Pin Evenness	Cptp2	Iout = 512uA VDS = **8V**	C0 ~ C287	-2.0		+2.0	%
Peak Current Chip In Evenness	Ccin2	Iout = 512uA VDS = **8V**	C0 ~ C287	-4.0		+4.0	%
Peak Current Chip to Chip Evenness	Cctc2	Iout = 512uA VDS = **8V**	C0 ~ C287	-6.0		+6.0	%
COUT - PRE On Resistance	RALon1	VCC_C=16V, PRE=0V VDS = 1V	C0 ~ C287		300	500	Ω
ROUT - VSSA On Resistance	Rkn	VCC_C=16V, VCC_R=16V, ILOAD=50mA	R0 ~ R95		25	40	Ω
ROUT - VKH On Resistance	Rkp	VCC_C=16V, VCC_R=16V, VDS=1V	R0 ~ R95		1.0	1.3	kΩ
Stand-By Current	IDD1	PSEL=VDD	VDD			30	uA
Stand-By Current	ICC1		VCC_C VCC_R			5.0	uA
Operating Current	IDD2		VDD		1	2	mA
Operating Current	ICC2		VCC_C VCC_R		2	5	mA

[Note]
I_{avg} : $\sum(I_k - I_{k+1}) / 384$: (k = 1 ~ 384)
Cptp : $(I_k - I_{k+1}) / I_{avg}$: (k = 1 ~ 384)
Ccin : $(I_{max} - I_{min}) / I_{avg}$
Cctc : $(I_{avg} - I_{ref}(SPEC)) / I_{ref}(SPEC)$
Operating Current : Iout=100uA, All Data On, Frame Frequency = 120Hz, VCC_C=VCC_R=16V, VDD=2.8V, All Column & Scan Open, Display Full Size, Others default

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(Ta = 25℃, VSSA=VSSD=0V, VDD=2.8V, VCC_C=VCC_R=18V, R/G/BPRE=0V)

Symbol	Parameter	Conditions	MIN	TYP	MAX	UNIT
V_{OL}	Low Logic Output Level (open-drain) at 3mA sink current at **SDA, SCL (I²C)**	V_{DD} > 2V	0.0	—	0.4	V
		V_{DD} < 2V	0.0	—	0.2*V_{DD}	
I_{OL}	Low-Level output Current (I²C)	VOL = 0.4V	3	-	-	mA
		VOL = 0.6V	6	—	-	

10.3. AC Characteristics

10.3.1. Clock Timing

(Ta = 25℃, VSSA=VSSD=0V, VDD=2.8V, VCC_C=VCC_R=18V, R/G/BPRE=0V)

Parameter	Symbol	Conditions	Specification			Unit
			MIN	TYP	MAX	
Internal Oscillation Frequency	T_{CR2}	Ta = 25 ℃, VDD=2.8V	3.0	3.36	3.7	MHz

OSC. Frequency is based on frame frequency 90Hz. (04h/02h)

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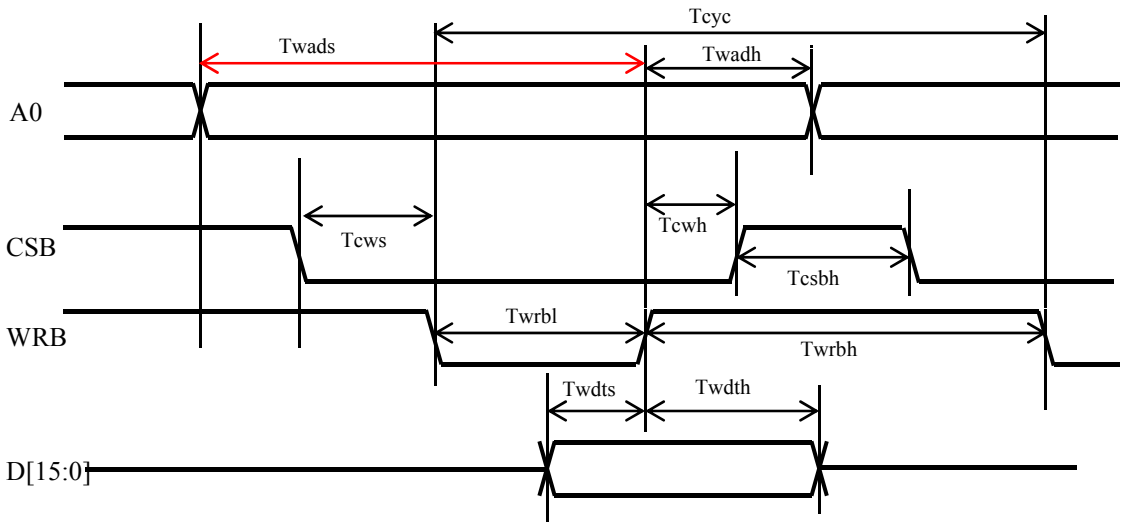
10.3.2. Host Interface Characteristics

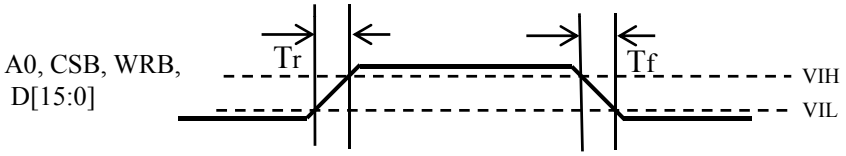
10.3.2.1. Parallel Interface

Writing Timing for 80Series CPU

(Ta = 25℃, VSSA=VSSD=0V, VDD=2.8V, VCC_C=VCC_R=18V, R/G/BPRE=0V, CL=100pF)

Parameter	Symbol	Related Pins	Specification		Unit
			MIN	MAX	
Write Cycle Time	Tcyc	WRB	100	-	ns
Address Setup Time	Twads	A0	50		ns
Address Hold Time	Twadh	A0	20		ns
Select Setup Time	Tcws	CSB	10		ns
Select Hold Time	Tcwh	CSB	20		ns
Write Low Pulse Width	Twrbl	WRB	30		ns
Write High Pulse Width	Twrbh	WRB	40		ns
Select High Pulse Width	Tcsbh	CSB	10		ns
Data Setup Time	Twdts	D15 ~ D0	10		ns
Data Hold Time	Twdth	D15 ~ D0	30		ns
Rising Time	Tr	A0, CSB, WRB, D15 ~ D0	-	30	ns
Falling Time	Tf	A0, CSB, WRB, D15 ~ D0	-	30	ns





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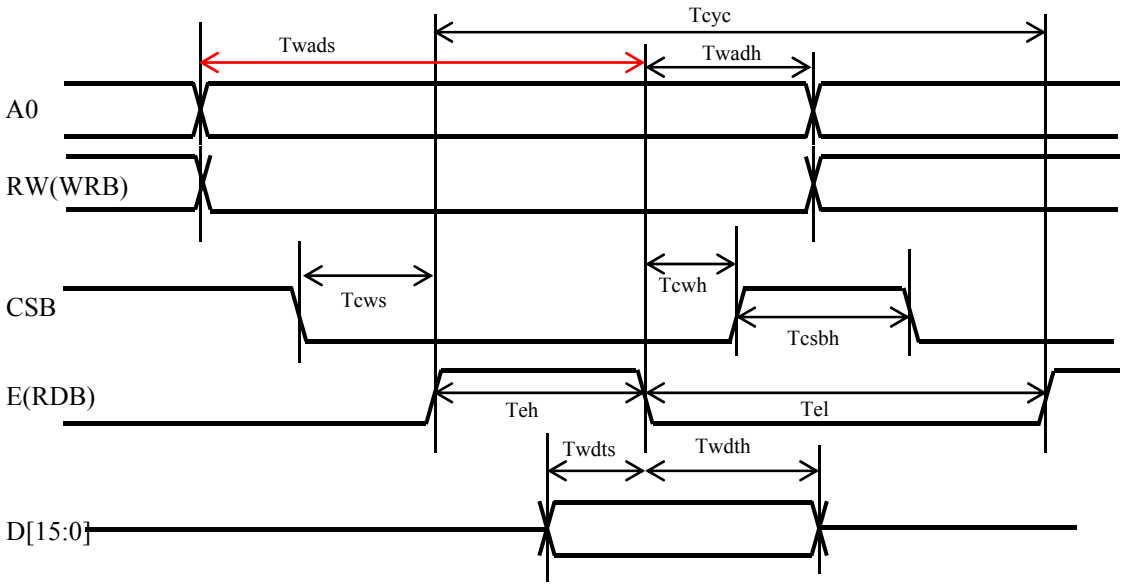
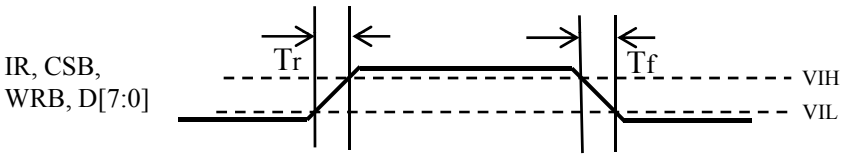
Writing Timing for 68 Series CPU

(Ta = 25℃, VSSA=VSSD=0V, VDD=2.8V, VCC_C=VCC_R=18V, R/G/BPRE=0V, CL=100pF)

Parameter	Symbol	Related Pins	Specification		Unit
			MIN	MAX	
Write Cycle Time	Tcyc	E	100	-	ns
Address Setup Time	Twads	A0, RW	50		ns
Address Hold Time	Twadh	A0, RW	20		ns
Select Setup Time	Tcws	CSB	10		ns
Select Hold Time	Tcwh	CSB	20		ns
Write Low Pulse Width	Tel	E	40		ns
Write High Pulse Width	Teh	E	30		ns
Select High Pulse Width	Tcsbh	CSB	10		ns
Data Setup Time	Twdts	D15 ~ D0	10		ns
Data Hold Time	Twdth	D15 ~ D0	30		ns
Rising Time	Tr	A0, CSB, RW, E, D15 ~ D0	-	30	ns
Falling Time	Tf	A0, CSB, RW, E, D15 ~ D0	-	30	ns





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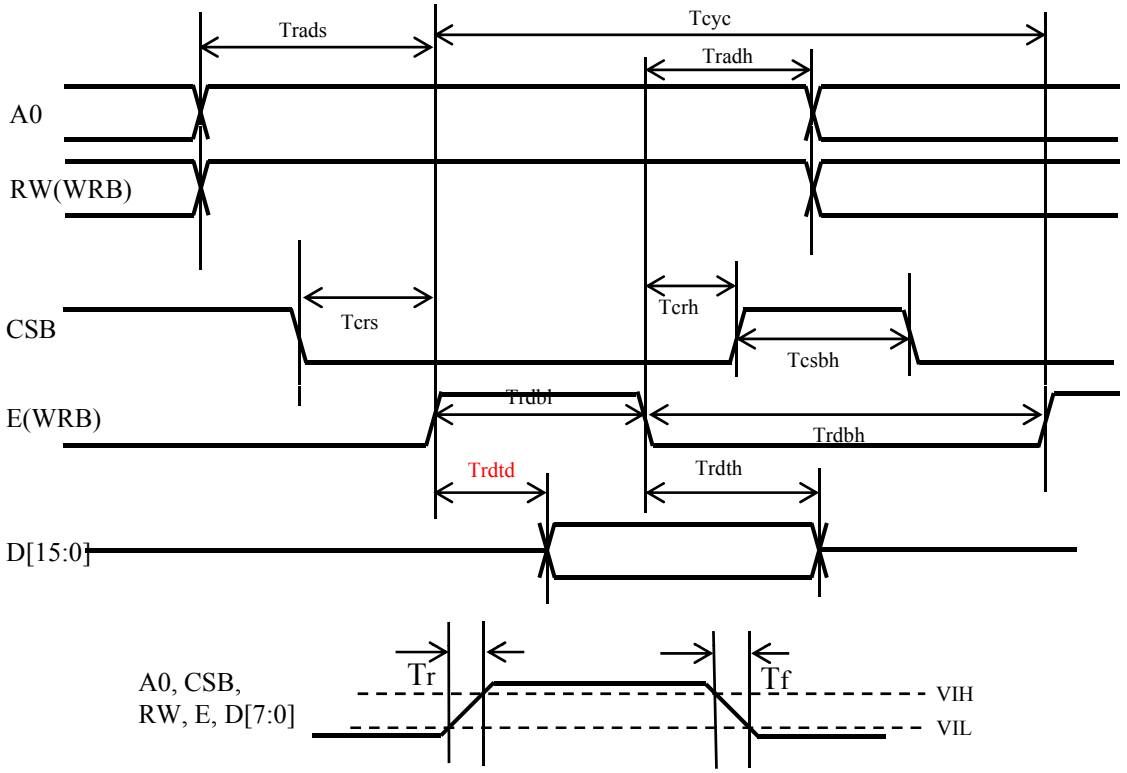
Reading Timing for 68 Series CPU

(Ta = 25℃, VSSA=VSSD=0V, VDD=2.8V, VCC_C=VCC_R=18V, R/G/BPRE=0V, CL=100pF)

Parameter	Symbol	Related Pins	Specification		Unit
			MIN	MAX	
Read Cycle Time	Tcyc	E	500	-	ns
Address Setup Time	Trads	A0, RW	50		ns
Address Hold Time	Tradh	A0, RW	20		ns
Select Setup Time	Tcrs	CSB	10		ns
Select Hold Time	Tcrh	CSB	20		ns
Read Low Pulse Width	Tel	E	200		ns
Read High Pulse Width	Teh	E	200		ns
Select High Pulse Width	Tcsbh	CSB	10		ns
Data Delay Time	Trdtd	D15 ~ D0	-	150	ns
Data Hold Time	Trdth	D15 ~ D0	20		ns
Rising Time	Tr	A0, CSB, RW, E, D15 ~ D0	-	30	ns
Falling Time	Tf	A0, CSB, RW, E, D15 ~ D0	-	30	ns



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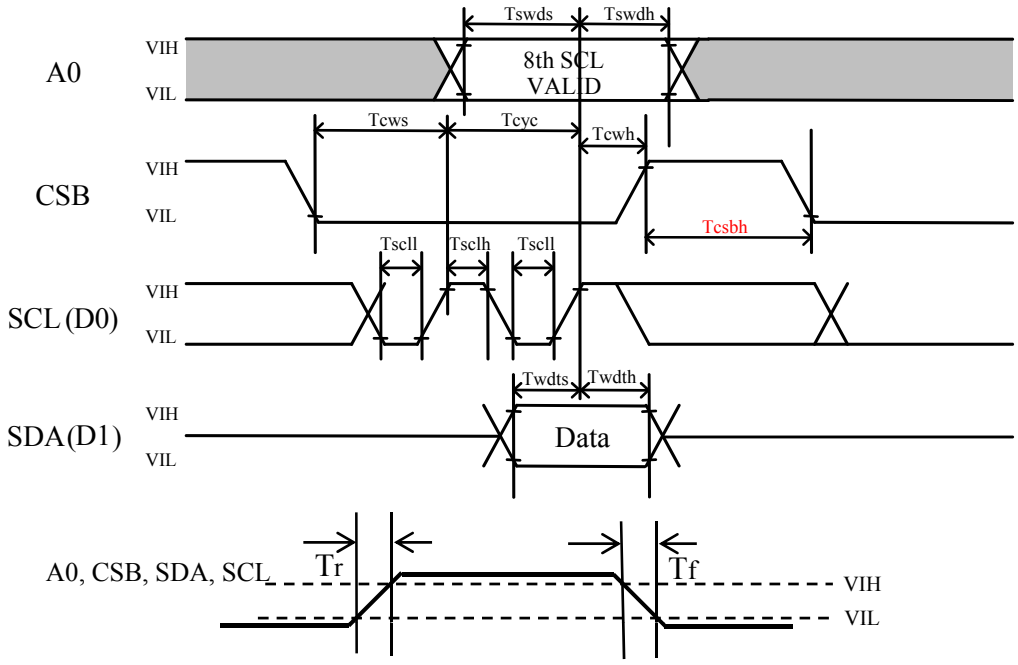
10.3.2.2. Serial Interface

Writing Timing

(Ta = 25℃, VSSA=VSSD=0V, VDD=2.8V, VCC_C=VCC_R=18V, R/G/BPRE=0V, CL=100pF)

Parameter	Symbol	Related Pins	Specification		Unit
			MIN	MAX	
Write Cycle Time	Tcyc	SCL(D0)	100	-	ns
Address Setup Time	Tswds	A0	65		ns
Address Hold Time	Tswdh	A0	35		ns
Select Setup Time	Tcws	CSB	65		ns
Select Hold Time	Tcwh	CSB	35		ns
SCL Low Pulse Width	Tscll	SCL(D0)	45		ns
Write High Pulse Width	Tsclh	SCL(D0)	45		ns
Select High Pulse Width	Tcsbh	CSB	30		ns
Data Setup Time	Twdts	SDA(D1)	20		ns
Data Hold Time	Twdth	SDA(D1)	30		ns
Rising Time	Tr	A0, CSB, SDA, SCL	-	30	ns
Falling Time	Tf	A0, CSB, SDA, SCL	-	30	ns



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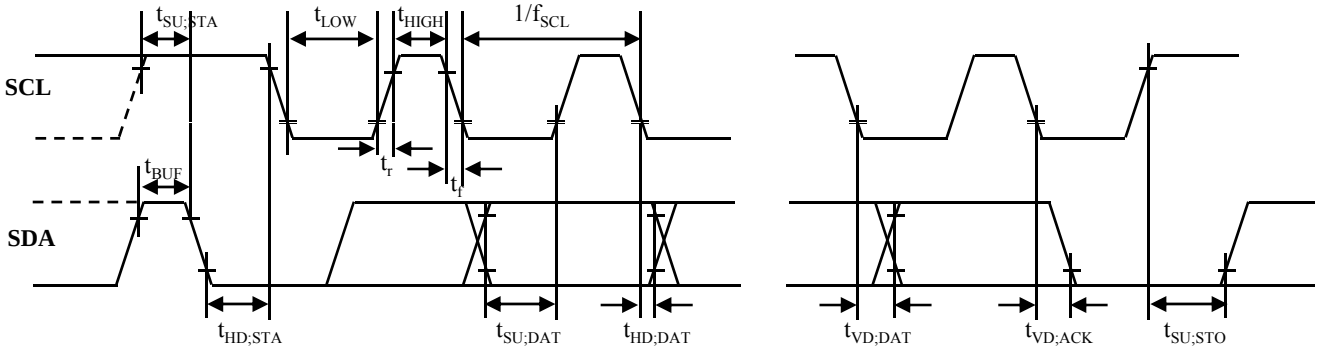
10.3.2.3. I2C Interface

Writing Timing

(Ta = 25℃, VSSA=VSSD=0V, VDD=2.8V, VCC_C=VCC_R=18V, R/G/BPRE=0V, CL=100pF)

Symbol	Parameter	Standard mode		Fast mode		Unit
		MIN	MAX	MIN	MAX	
f_{scl}	SCL clock frequency	0	100	0	400	kHz
t_{BUF}	bus free time between a STOP and START condition	4.7	-	1.3	-	us
$t_{HD;STA}$	hold time (repeated) START condition	4.0	-	0.6	-	us
$t_{SU;STA}$	set-up time form a repeated START condition	4.7	-	0.6	-	us
$t_{SU;STO}$	set-up time for STOP condition	4.0	-	0.6	-	us
$t_{SU;DAT}$	data set-up time	250	-	100	-	ns
$t_{HD;DTA}$	data hold time	0	-	0	-	ns
$t_{VD;ACK}$	data valid acknowledge time	0.3	3.45	0.1	0.9	us
$t_{VD;DAT}$	data valid time	300	-	50	-	ns
t_{LOW}	LOW period of the SCL clock	4.7	-	1.3	-	us
t_{HIGH}	HIGH period of the SCL clock	4.0	-	0.6	-	us
t_f	fall time of both SDA and SCL signals	-	300	-	300	ns
t_r	rise time of both SDA and SCL signals	-	1000	-	300	ns
t_{SP}	pulse width of spikes that must be suppressed by the input filter	0	50	0	50	ns



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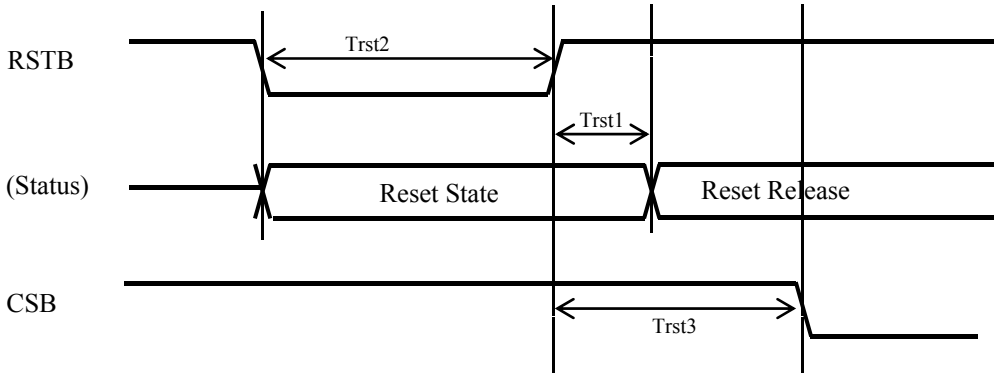
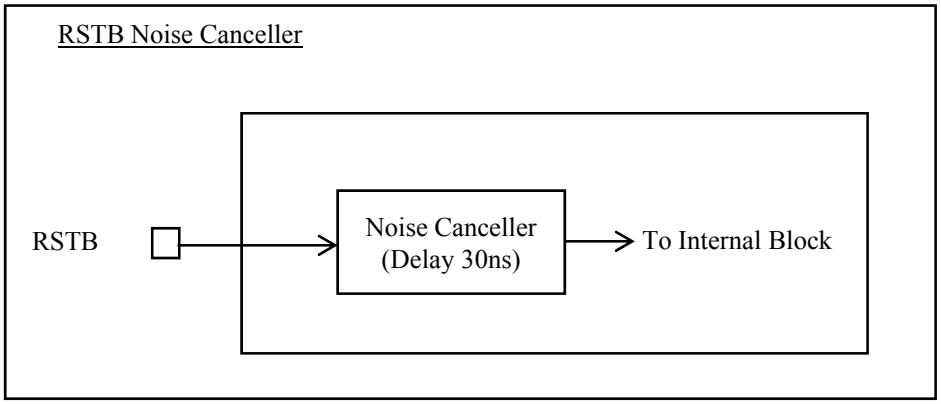
10.3.2.4. Reset Timing

(Ta = 25℃, VSSA=VSSD=0V, VDD=2.8V, VCC_C=VCC_R=18V, R/G/BPRE=0V, CL=100pF)

Parameter	Symbol	Related Pins	Specification		Unit
			MIN	MAX	
The completion Time of Reset	Trst1	RSTB	30 (Typ.)		ns
Reset Low Pulse Width	Trst2	RSTB	1000		ns
RSTB non-overlap to CSB	Trst3	RSTB, CSB	100		ns

* RSTB pad ignores typically the pulse width less than 30ns.





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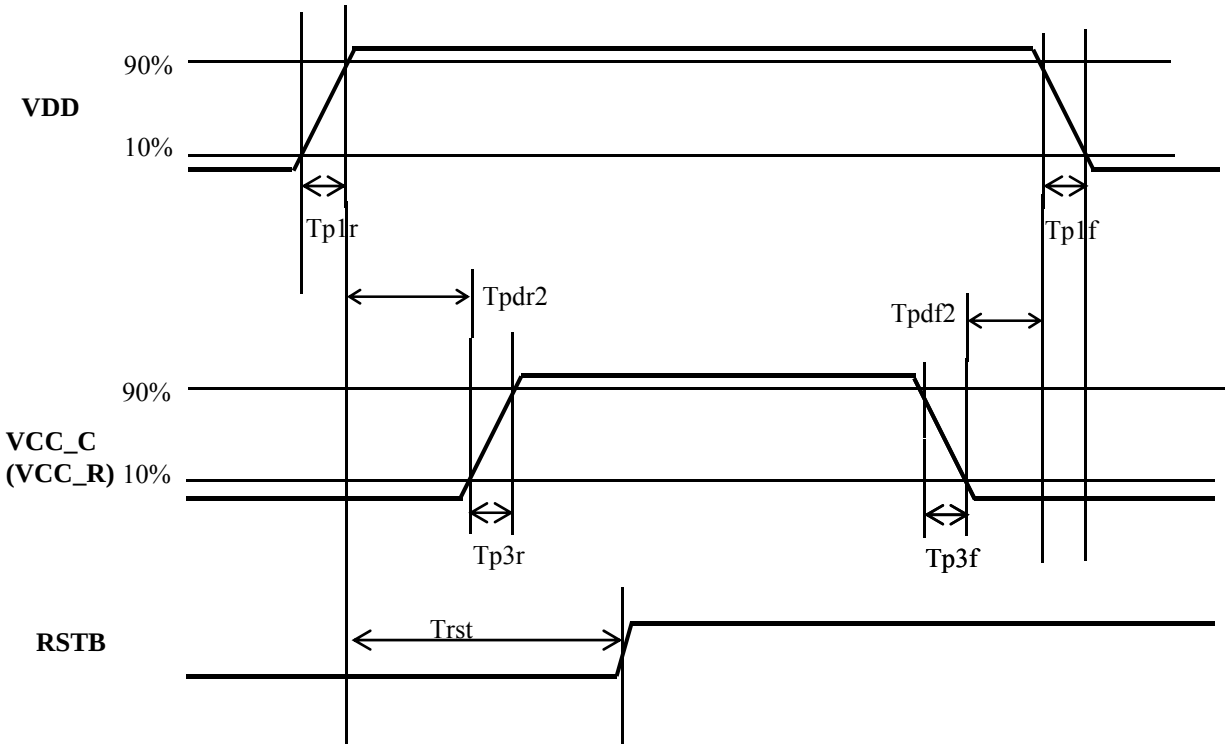
10.4. Power Sequence

PSEL = VDD, C_{VDDL} = 2uF



(Ta = 25℃, VSSA=VSSD=0V, VDD=2.8V, VCC_C=VCC_R=18V, R/G/BPRE=0V, CL=100pF)

Parameter	Symbol	Related Pins	Specification			Unit
			MIN	TYP	MAX	
VDD On Slope VDD Off Slope	Tp1r Tp1f	VDD	0.2	1	5	ms/V
VCC_C(VCC_R) On Slope VCC_C(VCC_R) Off Slope	Tp3r Tp3f	VCC_C(VCC_R)	0.2	1	5	ms/V
From VDD to VCC_C(VCC_R) Delay	Tpdr2	VDD, VCC_C(VCC_R)	2	-	-	ms
From VCC_C(VCC_R) to VDD Delay	Tpdf2	VDD, VCC_C(VCC_R)	2	-	-	ms
From VDD to H/W Reset Release	Trst	VDD, RSTB	30	-	-	ms

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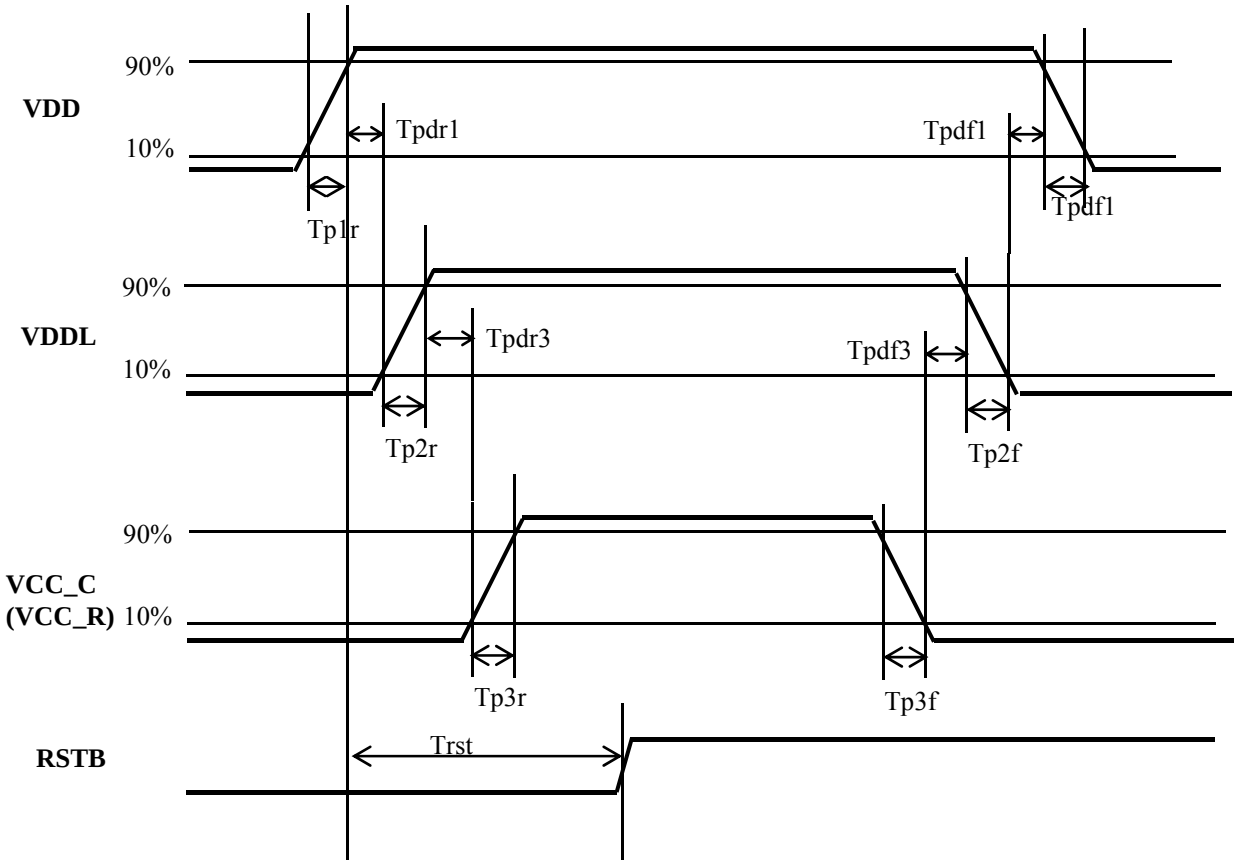
10.4. Power Sequence (‘CONT) PSEL = VSS



(Ta = 25℃, VSSA=VSSD=0V, VDD=2.8V, VCC_C=VCC_R=18V, R/G/BPRE=0V, CL=100pF)

Parameter	Symbol	Related Pins	Specification			Unit
			MIN	TYP	MAX	
VDDL On Slope VDDL Off Slope	Tp2r Tp2f	VDDL	0.2	1	5	ms/V
From VDD to VDDL Delay	Tpdr1	VDD, VDDL	1	-	-	ms
From VDDL to VDD Delay	Tpdf1	VDD, VDDL	1	-	-	ms
From VDDL to VCC_C(VCC_R) Delay	Tpdr3	VDDL, VCC_C(VCC_R)	1	-	-	ms
From VCC_C(VCC_R) to VDDL Delay	Tpdf3	VDDL, VCC_C(VCC_R)	1	-	-	ms
From VDD to H/W Reset Release	Trst	VDD, RSTB	30	-	-	ms

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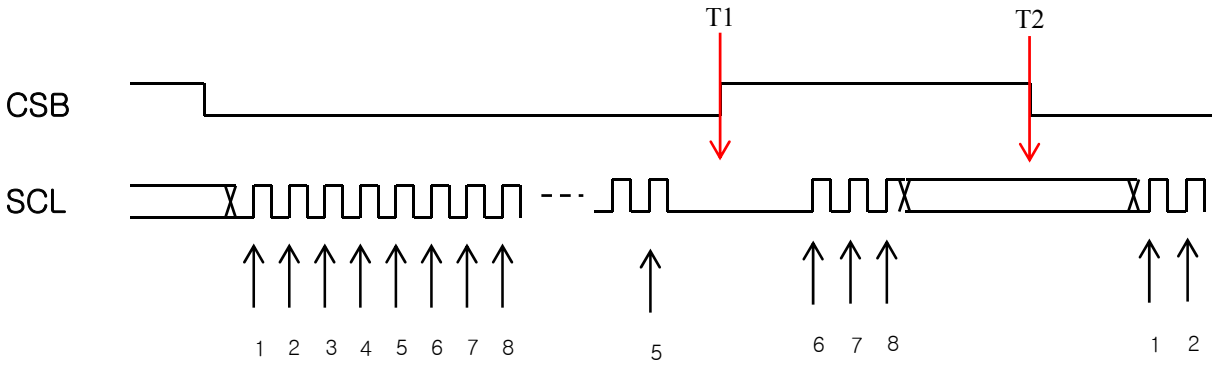
11. Application Guide

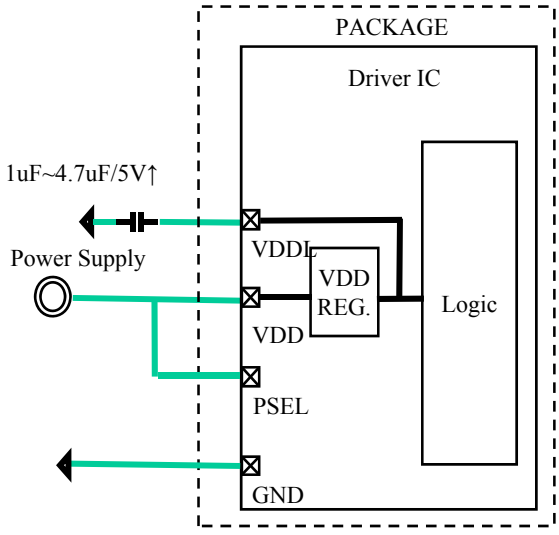
11.1 Serial I/F User Guide

The condition of serial I/F initialization is that CSB should go from “Low” to “High” .

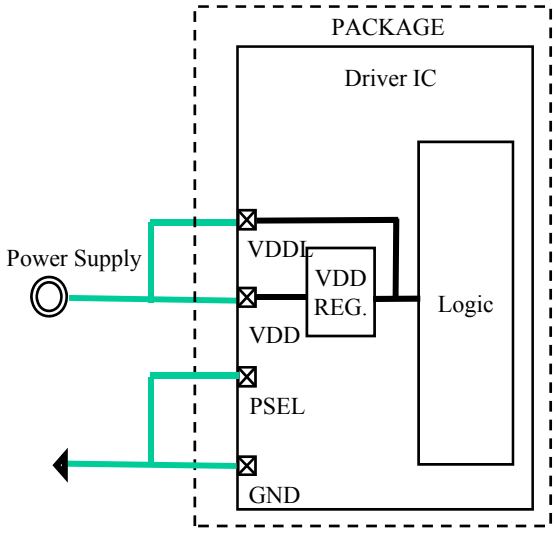


Note1. At T1, Serial Shift Register and Serial Clock Counter are initialized.
Note2. From T1 to T2, inputted SCL is ignored.

11.2. Internal Regulator for Logic Power



VDD=3.3V ~ 2V
VDD Reg. ON



VDD=1.9V ~ 1.65V
VDD Reg. OFF

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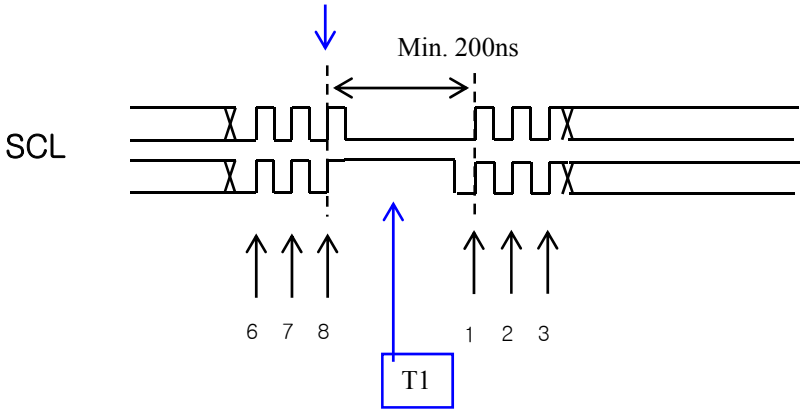
11.3 User Guide using Software Reset command.

14.3.1 Serial I/F

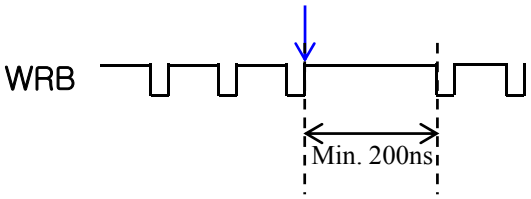
Software Reset is issued.



In the case of Software Reset Command
Minimum 200ns is necessary from 8th SCL up-edge to next 1st SCL up-edge.
Even though CSB is set to High at the T1 timing, minimum 200ns is needed.

14.3.2 Parallel I/F (80 Mode)

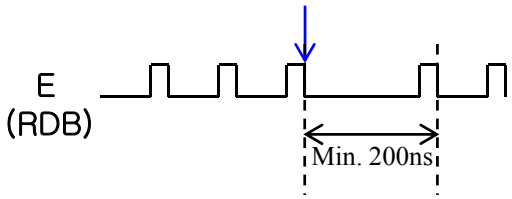
Software Reset is issued.



In the case of Software Reset Command
Minimum 200ns is necessary from WRB up-edge to next WRB up-edge.

14.3.3 Parallel I/F (68 Mode)

Software Reset is issued.



In the case of Software Reset Command
Minimum 200ns is necessary from E down-edge to next E down-edge.

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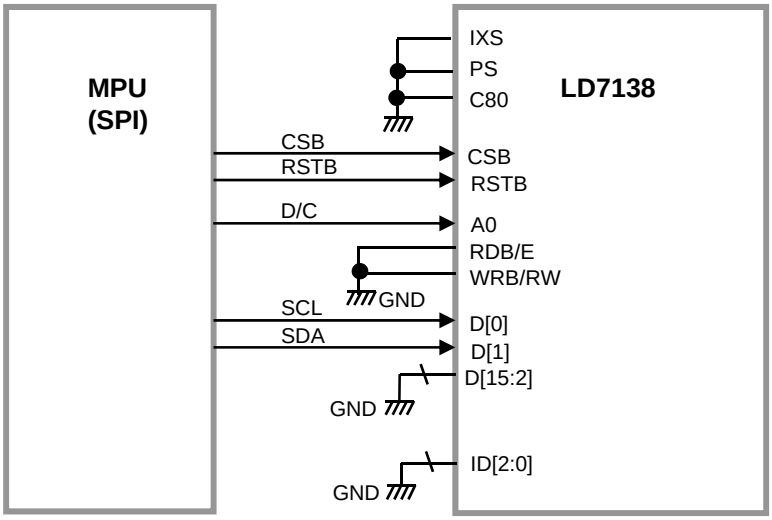
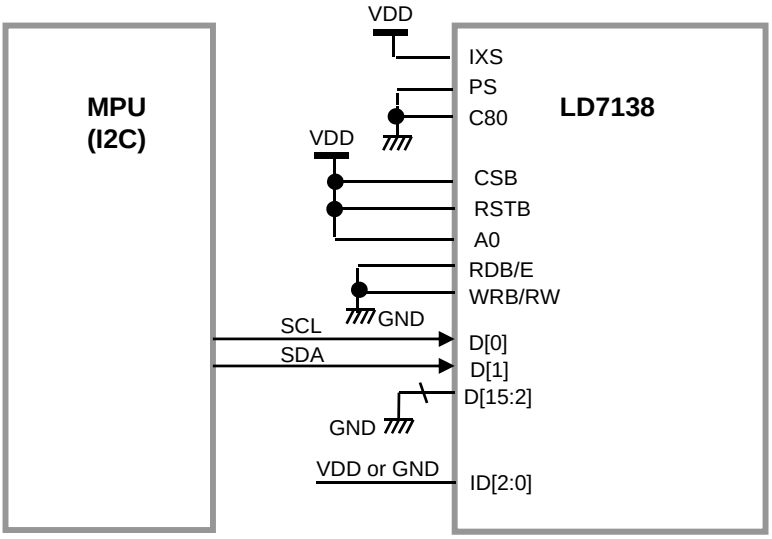
11.4 User Guide for Interface.

14.4.1 Serial I/F



14.4.2 I2C I/F



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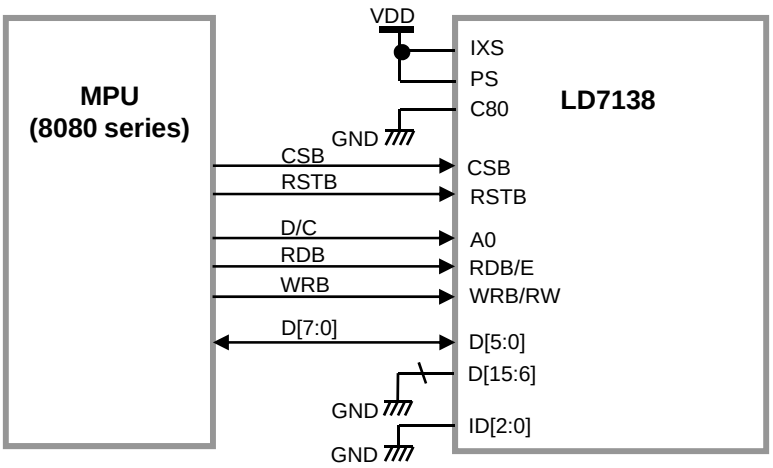
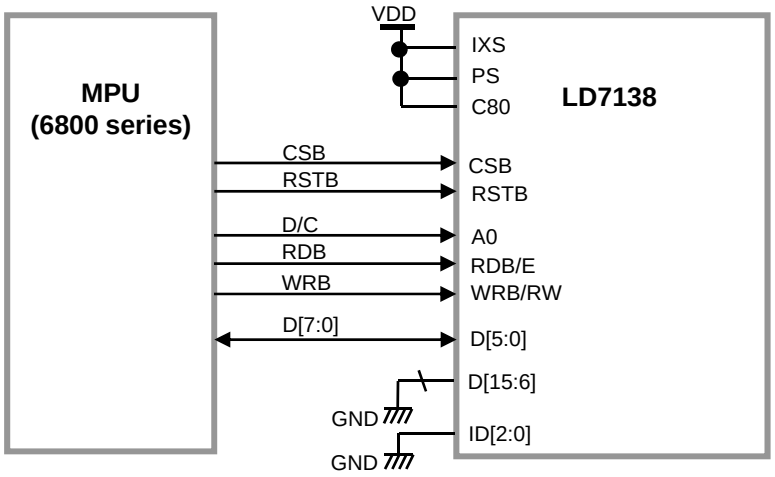
14.4.2 8080-series MPU Interface with 6bit Bus



14.4.3 6800-series MPU Interface with 6bit Bus



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