

SANYO Semiconductors DATA SHEET



CMOSIC LC87F6D64A — FROM 64K byte, RAM 2048 byte on-chip 8-bit 1-chip Microcontroller

Overview

The SANYO LC87F6D64A is 8-bit microcomputer with the following on-chip functional blocks:

- CPU: operable at a minimum bus cycle time of 100ns
- 64K-byte flash ROM (re-writeable on board/On-chip debugger)
- On-chip RAM: 2048 byte
- VFD automatic display controller/driver
- 16-bit timer/counter (can be divided into two 8-bit timers)
- two 8-bit timer with prescaler
- timer for use as date/time clock
- Day-Minute-Second Counter (DMSC)
- System clock divider function
- Synchronous serial I/O port (with automatic block transmit /receive function)
- Asynchronous/synchronous serial I/O port
- Remote control receive function
- 8-channel×8-bit AD converter
- 14-source 10-vectored interrupt system
- All of the above functions are fabricated on a single chip.

Features

■Flash ROM

- Single 5V power supply, writeable on-board.
- Block erase in 128 byte units
- 65536 × 8 bits

■RAM

• 2048×9 bits

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■Minimum Bus Cycle Time

- 100ns (10MHz) V_{DD}=3.0 to 5.5V
- 150ns (4MHz) V_{DD}=2.5 to 5.5V Note: The bus cycle time indicates ROM read time.
- ■Minimum Instruction Cycle Time (tCYC)
 - 300ns (10MHz) V_{DD}=3.0 to 5.5V
 - 750ns (4MHz) VDD=2.5 to 5.5V

Ports

• Input/output ports

1 1 1	
Data direction programmable for each bit individually:	10 (P1n, P7n)
Data direction programmable in nibble units:	8 (P0n)
(When N-channel open drain output is selected, data can	n be input in bit units.)
• VFD output ports	
Large current outputs for digits:	9 (S0/T0 to S8/T8)

Large current outputs for digits:	9(50/10 to 58/18)
Large current outputs for digits/segments:	7 (S9/T9 to S15/T15)
Digit/segment outputs:	8 (S16 to S23)
Segment outputs:	30 (S24 to S53)
• Oscillator pins:	2 (CF1/XT1, CF2/XT2)
• Reset pin:	$1 (\overline{\text{RES}})$
• Power supply:	$4 (V_{SS}1, V_{DD}1 \text{ to } V_{DD}3)$
• VFD power supply:	1 (VP)

■VFD Automatic Display Controller

- Programmable segment/digit output pattern Output can be switched between digit/segment waveform output (pins 9 to 23 can be used for output of digit waveforms). parallel-drive available for large current VFD.
- 16-step dimmer function available

■Timers

• Timer 0: 16-bit timer/counter with capture register

Mode 0: 2 channel 8-bit timer with programmable 8-bit prescaler and 8-bit capture register Mode 1: 8-bit timer with 8-bit programmable prescaler and 8-bit capture register

- + 8-bit counter with 8-bit capture register
- Mode 2: 16-bit timer with 8-bit programmable prescaler and 16-bit capture register
- Mode 3: 16-bit counter with 16-bit capture register
- Timer 4: 8-bit timer with 6-bit prescaler
- Timer 5: 8-bit timer with 6-bit prescaler
- Base Timer
 - 1) The clock signal can be selected from any of the following.
 - Sub-clock (32.768kHz crystal oscillator), system clock, and prescaler output from timer 0 2) Interrupts can be selected to occur at one of five different times.
- Day and time counter

1) Using with a base timer, it can be used as 65000 day + minute + second counter.

■SIO

- SIO 0: 8-bit synchronous serial interface
 - 1) LSB first /MSB first function available
 - 2) Internal 8-bit baud-rate generator (maximum transmit clock period 4/3 tCYC)
 - 3) Consecutive automatic data communication
 - (1 to 256 bits (communication available for each bit) (stop and reopening available for each byte))
- SIO 1: 8-bit asynchronous/synchronous serial interface
 - Mode 0: Synchronous 8-bit serial IO (2-wire or 3-wire, transmit clock 2 to 512 tCYC)
 - Mode 1: Asynchronous serial IO (half duplex, 8 data bits, 1 stop bit, baud rate 8 to 2048 tCYC)
 - Mode 2: Bus mode 1 (start bit, 8 data bits, transmit clock 2 to 512 tCYC)
 - Mode 3: Bus mode 2 (start detection, 8 data bits, stop detection)

\blacksquareAD Converter: 8 bits \times 8 channels

Remote Control Receiver Circuit (sharing pins with P70/INT0/RMIN)

- Noise rejection function
- (Units of noise rejection filter: about 120µs, when selecting a 32.768kHz crystal oscillator as a clock.)
- Supporting reception formats with a guide-pulse of half-clock/clock/none.
- Determines a end of reception by detecting a no-signal periods (No carrier). (Supports same reception format with a different bit length.)
- X'tal HOLD mode release function

■Watchdog Timer

- The watching timer period is set using an external RC.
- Watchdog timer can produce interrupt, system reset.

■Clock Output Function

- 1) Able to output selected oscillation clock 1/1, 1/2, 1/4, 1/8, 1/16, 1/32, or 1/64 as system clock.
- 2) Able to output oscillation clock of sub clock.

■Interrupts: 14 sources, 10 vector interrupts

- Three priority (low, high and highest) multiple interrupts are supported. During interrupt handling, an equal or lower priority interrupt request is refused.
- If interrupt requests to two or more vector addresses occur at once, the higher priority interrupt takes precedence. In the case of equal priority levels, the vector with the lowest address takes precedence.

No.	Vector	Selectable Level	Interrupt Signal
1	00003H	X or L	INTO
2	0000BH	X or L	INT1
3	00013H	H or L	INT2/T0L/remote control receiver
4	0001BH	H or L	INT3/Base timer 0/1
5	00023H	H or L	тон
6	0002BH	H or L	
7	00033H	H or L	SIO0
8	0003BH	H or L	SIO1
9	00043H	H or L	ADC
10	0004BH	H or L	Port0/T4/T5

• Priority Level: X>H>L

• For equal priority levels, vector with lowest address takes precedence.

Subroutine Stack Levels: 1024 levels maximum (Stack is located in RAM.)

■High-speed Multiplication/Division Instructions

- 16 bits \times 8 bits (5 tCYC execution time)
- 24 bits \times 16 bits (12 tCYC execution time)
- 16 bits ÷ 8 bits (8 tCYC execution time)
- 24 bits ÷ 16 bits (12 tCYC execution time)

■Oscillation Circuits

- On-chip RC oscillation circuit for system clock use.
- On-chip CF oscillation circuit* for system clock use. (Rf built in)
- On-chip Crystal oscillation circuit* low speed system clock use. (Rf built in)
- Frequency variable RC oscillation circuit (internal) for system clock.
 - 1) Adjustable in $\pm 4\%$ (typ) step from a selected center frequency.
- 2) Measures oscillation clock using a input signal from XT1 as a reference.
- * The CF oscillation terminal and the crystal oscillation terminal cannot be used at the same time because of commonness.

System Clock Divider Function

- Able to reduce current consumption Available minimum instruction cycle time: 300ns, 600ns, 1.2µs, 2.4µs, 4.8µs, 9.6µs, 19.2µs, 38.4µs, 76.8µs. (Using 10MHz main clock)
- ■Standby Function
 - HALT mode

HALT mode is used to reduce power consumption. Program execution is stopped. Peripheral circuits still operate but VFD display and some serial transfer operations stop.

- 1) Oscillation circuits are not stopped automatically.
- 2) Release occurs on system reset or by interrupt.
- HOLD mode

HOLD mode is used to reduce power consumption. Both program execution and peripheral circuits are stopped. 1) The CF, RC, X'tal and frequency variable RC oscillators automatically stop operation.

- 2) Release occurs on any of the following conditions.
 - (1) input to the reset pin goes "Low"
 - (2) a specified level is input to at least one of INT0, INT1, INT2
 - (3) an interrupt condition arises at port 0
- X'tal HOLD mode.

X'tal HOLD mode is used to reduce power consumption. Program execution is stopped.

- All peripheral circuits except the base-timer are stopped.
- 1) The CF, RC, frequency variable RC oscillation circuits stop automatically.
- 2) Crystal oscillator is maintained in its state at HOLD mode inception.
- 3) Release occurs on any of the following conditions.
 - (1) input to the reset pin goes "Low"
 - (2) Setting at least one of the INT0, INT1 and INT2 pins to the specified level
 - (3) Having an interrupt source established at port 0
 - (4) Having an interrupt source established in the base timer circuit
 - (5) Having an interrupt source established in the remote control receiver circuit

■On-chip Debugger

• Supports software debugging with the IC mounted on the target board.

■Package Form

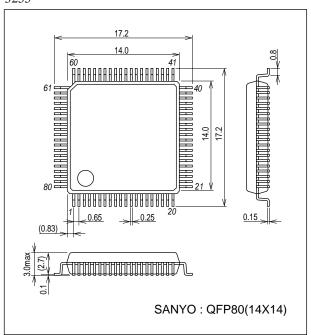
• QFP80(14×14): Lead-free type

■Development Tools

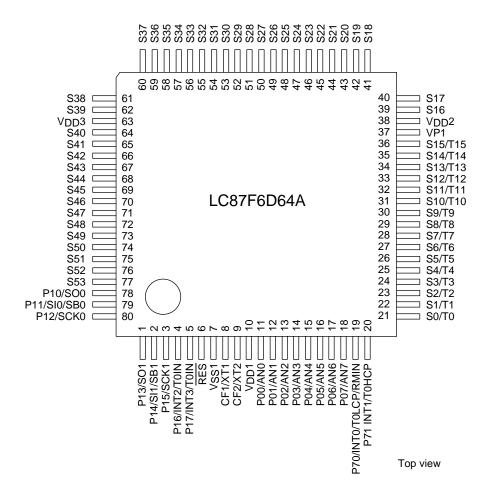
• On-chip debugger: TCB87- type-B + LC87F6D64A

Package Dimensions

unit : mm (typ) 3255

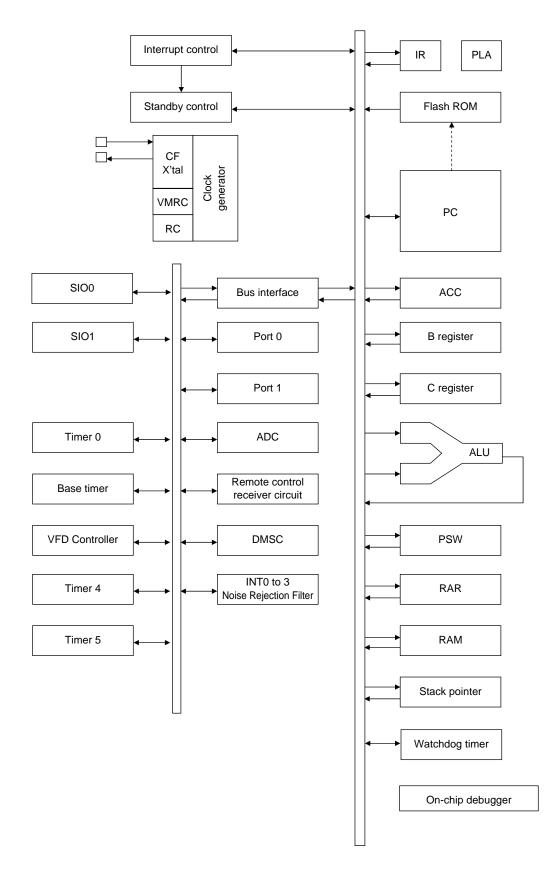


Pin Assignment



SANYO: QFP80(14×14) "Lead-free Type"

System Block Diagram



Pin Description

Pin name	I/O				Function				Option
V _{SS} 1	-	Power supp	ly (-)						No
V _{DD} 1 V _{DD} 2	-	Power supp	ly (+)						No
V _{DD} 3 VP	-	VFD Power	supply (-)						No
PORT0	I/O	8bit input/ou							Yes
P00 to P07	1/0	-		able in nibble	units				165
F 00 10 F 07					in nibble units				
		Input for HC	LD release						
		Input for por	rt 0 interrupt						
		Other functi							
					ected from sub	-			
PORT1	I/O	On-chip dec Sbit input/ou		BGP0 to DBG	SP2 (P05 to P07)			Yes
	1/0	-		able for each b	hit				165
P10 to P17				n be specified					
		Other pin fu	-						
		P10: SIO0	data output						
			-	s input/output					
			clock input/ou	Itput					
		P13: SIO1	•	innut/output					
			clock input/ous	s input/output					
		P16: INT2		nput					
			Buzzer output	1					
		The following	types of inter	rupt detection	are possible:			_	
			Rising	Falling	Rising/ Falling	H level	L level		
		INT2	enable	enable	enable	disable	disable		
		INT3	enable	enable	enable	disable	disable		
PORT7		 2bit input/or 	utput port						
P70 to P71		-		ecified for each	n bit				
		Use of pull-	up resistor ca	n be specified	for each bit				
		 Other functi 							
			•	•	ner 0L capture i	•			
		-	-		control receiver	-			
			•	rupt detection	ner 0H capture i are possible:	input			
			Rising	Falling	Rising/ Falling	H level	L level		
		INT0	enable	enable	disable	enable	enable		
		INT1	enable	enable	disable	enable	enable	1	
S0/T0 to S8/T8	0	Large curre	nt output for \	/FD display co	ontroller digit (ca	n be used for	segment)	1	No
S9/T9 to S15/T15	0	-			ontroller segmen		9,		No
S16 to S53	0	-		ontroller segm	-				No
RES		Reset termina		on cogn					No
CF1/XT1	1	<ceramic osc<="" td=""><td></td><td>d></td><td></td><td></td><td></td><td></td><td>No</td></ceramic>		d>					No
		 Input termin 							
		< crystal osci							
		Input for 32.	768kHz cryst	al oscillation					
		When not in u	ise, connect t	o V _{DD} 1.					
CF2/XT2	0	<ceramic osc<="" td=""><td></td><td></td><td></td><td></td><td></td><td></td><td>No</td></ceramic>							No
		Output term							
		< crystal osci							
	1	Output for 3 When not in u	-	stal oscillation					

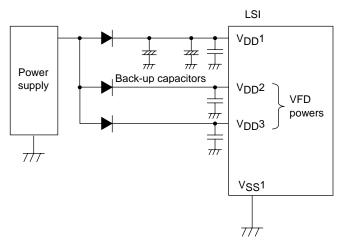
Port Output Types

Output configuration and pull-up/pull-down resistor options are shown in the following table. Input/output is possible even when port is set to output mode.

Terminal	Option Selected in Units of	Options	Output Format	Pull-up Resistor	Pull-down Resistor
P00 to P07	each bit	1	CMOS	Programmable	-
(Note 1)		2	Nch-open drain	Programmable	-
P10 to P17	each bit	1	CMOS	Programmable	-
		2	Nch-open drain	Programmable	-
P70	-	None	Nch-open drain	Programmable	-
P71	-	None	CMOS	Programmable	-
S0/T0 to S15/T15 S16 to S53	-	None	High voltage Pch-open drain	-	Fixed

Note 1: Programmable pull-up resisters of Port 0 can be attached in nibble units (P00 to P03, P04 to P07).

* Note: Connect as follows to reduce noise on V_{DD} and increase the back-up time. V_{SS1} must be connected together and grounded.



	Parameter	Symbol	Pin/Remarks	Conditions		<u> </u>	Specif	ication	
	Parameter	Symbol	Pin/Remarks	Conditions	V _{DD} [V]	min	typ	max	uni
Su	pply voltage	V _{DD} max	V_{DD} 1, V_{DD} 2, V_{DD} 3	V _{DD} 1=V _{DD} 2=V _{DD} 3		-0.3		+6.5	
Inp	out voltage	V _I (1)	CF1/XT1, RES			-0.3		V _{DD} +0.3	1
		V _I (2)	VP			V _{DD} -45		V _{DD} +0.3	
Ou	itput voltage	V _O (1)	S0/T0 to S15/T15 S16 to S53			V _{DD} -45		V _{DD} +0.3	V
		V _O (2)	CF2/XT2			-0.3		V _{DD} +0.3	
	out/Output Itage	V _{IO} (1)	Ports 0, 1, 7			-0.3		V _{DD} +0.3	
Peak output current		IOPH(1)	Ports 0, 1	CMOS output selected Current at each pin		-10			
		IOPH(2)	Port 71	Current at each pin		-5			1
		IOPH(3)	S0/T0 to S15/T15	Current at each pin		-30			
		IOPH(4)	S16 to S53	Current at each pin		-15			
	Average output current	IOMH(1)	Ports 0, 1	CMOS output selected Current at each pin		-7.5			
		IOMH(2)	Port 71	Current at each pin		-3			
ent		IOMH(3)	S0/T0 to S15/T15	Current at each pin		-15			
curre		IOMH(4)	S16 to S53	Current at each pin		-10			
put (Total output	ΣIOAH(1)	Port 0	Total of all pins		-30			
l out	current	ΣIOAH(2)	Port 1	Total of all pins		-30			
leve		ΣIOAH(3)	Ports 0, 1	Total of all pins		-30			
High level output current		ΣIOAH(4)	Port 71	Total of all pins		-5			
-		ΣIOAH(5)	S0/T0 to S15/T15	Total of all pins		-60			ĺ
		ΣIOAH(6)	S16 to S33	Total of all pins		-60			m
		ΣΙΟΑΗ(7)	S0/T0 to S15/T15 S16 to S33	Total of all pins		-60			
		ΣIOAH(8)	S34 to S39	Total of all pins		-60			
		ΣIOAH(9)	S40 to S47	Total of all pins		-60			
		ΣIOAH(10)	S48 to S53	Total of all pins		-60			
		ΣIOAH(11)	S34 to S53	Total of all pins		-60			
	Peak output	IOPL(1)	Ports 0, 1	Current at each pin				20	
ent	current	IOPL(2)	Port 7	Current at each pin				10	
current	Total output	IPML(1)	Ports 0, 1	Current at each pin				15	
tput	current	IOML(2)	Port 7	Current at each pin				7.5	
el ou	Total output	ΣIOAL(1)	Port 0	Total of all pins				50	
leve	current	ΣIOAL(2)	Port 1	Total of all pins				50	
Low level output		ΣIOAL(3)	Port 7	Total of all pins				20	
		ΣIOAL(4)	Ports 0, 1, 7	Total of all pins				80	
	aximum power sipation	Pd max	QFP80(14×14)	Ta=-40 to +85°C					m
Op ter	perating nperature nge	Topr				-40		+85	
Sto ter	orage nperature nge	Tstg				-55		+125	• •(

Absolute Maximum Ratings at $Ta = 25^{\circ}C$, $V_{SS}1 = 0V$

Parameter	Symbol	Pin/Remarks	Conditions			Specific	ation	
Falailletei	Symbol	FIII/Remarks	Conditions	V _{DD} [V]	min	typ	max	unit
Operating	V _{DD} (1)	V _{DD} 1=V _{DD} 2=V _{DD} 3	0.300µs≤tCYC≤200µs		3.0		5.5	
supply voltage range (Note 2-1)	V _{DD} (2)		0.735µs≤tCYC≤200µs		2.5		5.5	
Hold voltage	VHD	V _{DD} 1	RAM and the register data are kept in HOLD mode.		2.0		5.5	
Pull-down supply voltage	VP	VP			-35		V _{DD}	
Input high voltage Input low voltage	V _{IH} (1)	Ports 0, 1	Output disable	2.5 to 5.5	0.3V _{DD} +0.7		V _{DD}	
	V _{IH} (2)	Port 70 Watchdog timer	Output disable	2.5 to 5.5	0.9V _{DD}		V _{DD}	V
	V _{IH} (3)	XT1/CF1, RES		2.5 to 5.5	0.75V _{DD}		V _{DD}]
	V _{IL} (1)	Ports 0, 1 Port 71 Port 70 port input/interrupt	Output disable	2.5 to 5.5	V _{SS}		0.1V _{DD} +0.4	
	V _{IL} (2)	Port 70 Watchdog timer	Output disable	2.5 to 5.5	V _{SS}		0.8V _{DD} -1.0	
	V _{IL} (3)	XT1/CF1, RES		2.5 to 5.5	VSS		0.25V _{DD}	
Operation	tCYC			3.0 to 5.5	0.300		200	
cycle time				2.5 to 5.5	0.735		200	μs
External	FEXCF(1)	CF1	CF2 open circuit	3.0 to 5.5	0.1		10	
system clock frequency			 system clock divider set to 1/1 external clock DUTY=50±5% 	2.5 to 5.5	0.1		4	мн
			CF2 open circuit	3.0 to 5.5	0.2		20	
			 system clock divider set to 1/2 external clock DUTY=50±5% 	2.5 to 5.5	0.2		8	
Oscillation stabilizing time period	FmCF(1)	CF1, CF2	 10MHz ceramic resonator oscillation Refer to figure 1 	3.0 to 5.5		10		
(Note 2-2)	FmCF(2)	CF1, CF2	4MHz ceramic resonator oscillation Refer to figure 1	2.5 to 5.5		4		мн
	FmRC		RC oscillation	2.5 to 5.5	0.3	1.0	2.0	1
	FmVMRC		Frequency variable RC oscillation circuit	2.5 to 5.5		4		
	FsX'tal	XT1, XT2	32.768kHz crystal resonator oscillation Refer to figure 2	2.5 to 5.5		32.768		kH

Allowable Operating Conditions at $Ta = -40^{\circ}C$ to $+85^{\circ}C$, $V_{SS}1 = 0V$

Note 2-1: Re-writeable on board $V_{DD} \ge 4.5V$.

Note 2-2: The oscillation constant is shown in table 1 and table 2.

The CF oscillation terminal and the crystal oscillation terminal cannot be used at the same time because of commonness.

LC87F6D64A

Electrical Characteristics at $Ta = -40^{\circ}C$ to $+85^{\circ}C$, $V_{SS}1 = 0V$

Parameter	Symbol	Pin/Remarks	Conditions			Specifica	ation	-
Faiaillelei	Symbol	FININEIIIdIKS	Conditions	V _{DD} [V]	min	typ	max	unit
Input high current	l _{IH} (1)	Ports 0, 1, 7	 Output disable Pull-up resister OFF. VIN=VDD (including OFF state leak current of the output Tr.) 	2.5 to 5.5			1	
	I _{IH} (2)	RES	V _{IN} =V _{DD}	2.5 to 5.5			1	
	I _{IH} (3)	CF1/XT1	V _{IN} =V _{DD}	2.5 to 5.5			1	
Input low current	I _{IL} (1)	Ports 0, 1, 7	 Output disable Pull-up resister OFF. VIN=VSS (including OFF state leak current of the output Tr.) 	2.5 to 5.5	-1			μΑ
	I _{IL} (2)	RES	V _{IN} =V _{SS}	2.5 to 5.5	-1			
	IIL(3)	CF1/XT1	V _{IN} =V _{SS}	2.5 to 5.5	-1			
Output high	V _{OH} (1)	Port 0: CMOS	I _{OH} =-1.0mA	4.5 to 5.5	V _{DD} -1			
voltage	V _{OH} (2)	output option	I _{OH} =-0.5mA	3.0 to 5.5	V _{DD} -1			
	V _{OH} (3)	Ports 1	I _{OH} =-0.1mA	2.5 to 5.5	V _{DD} -0.5			
	V _{OH} (4)	Port 71	I _{OH} =-0.4mA	2.5 to 5.5	V _{DD} -1			
	V _{OH} (5)	S0/T0 to S15/T15	I _{OH} =-20.0mA	4.5 to 5.5	V _{DD} -1.8			
	V _{OH} (6)	4	I _{OH} =-10.0mA	3.0 to 5.5	V _{DD} -1.8			
	V _{OH} (7)	-	 I_{OH}=-1.0mA I_{OH} at any single pin is not over 1mA. 	2.5 to 5.5	V _{DD} -1			
	V _{OH} (8)	S16 to S53	I _{OH} =-5.0mA	4.5 to 5.5	V _{DD} -1.8			V
	V _{OH} (9)	4	I _{OH} =-2.5mA	3.0 to 5.5	V _{DD} -1.8			
	V _{OH} (10)		 I_{OH}=-1.0mA I_{OH} at any single pin is not over 1mA. 	2.5 to 5.5	V _{DD} -1			
Output low	V _{OL} (1)	Ports 0, 1	I _{OL} =10mA	4.5 to 5.5			1.5	
voltage	V _{OL} (2)		I _{OL} =5mA	3.0 to 5.5			1.5	
	V _{OL} (3)		I _{OL} =1.6mA	2.5 to 5.5			0.4	
	V _{OL} (4)	Port 7	I _{OL} =1mA	2.5 to 5.5			0.4	
Pull-up resistor	Rpu	Ports 0, 1, 7	V _{OH} =0.9V _{DD}	4.5 to 5.5	15	40	70	
				2.5 to 4.5	25	70	150	kΩ
Output off-leak current	IOFF(1)	S0/T0 to S15/T15, S16 to S53	Output P-ch Tr. OFF VOUT=VSS	2.5 to 5.5	-1			
	IOFF(2)		Output P-ch Tr. OFF VOUT=VDD-40V	2.5 to 5.5	-30			μA
Pull-down resistor	Rpd	• S0/T0 to S15/T15 • S16 to S53	 Output P-ch Tr. OFF V_{OUT}=3V Vp=-30V 	5.0	60	100	200	kΩ
Hysteresis voltage	VHYS(1)	• Ports 0, 1, 7 • RES		2.5 to 5.5		0.1V _{DD}		V
Pin capacitance	СР	All pins	 f=1MHz All other terminals connected to V_{SS}. Ta=25°C 	2.5 to 5.5		10		pF

Serial I/O Characteristics at $Ta = -40^{\circ}C$ to $+85^{\circ}C$, $V_{SS}1 = 0V$

1. SIO0 Serial I/O Characteristics (Note 4-1-1)

	Paramatar	Symbol	Pin/	Conditions			Spec	ification	
F	arameter	Symbol	Remarks	Conditions	V _{DD} [V]	min	typ	max	unit
	Frequency	tSCK(1)	SCK0(P12)	See Fig. 6.		2			
ĸ	Low level pulse width	tSCKL(1)				1			
put clo	High level pulse width	tSCKH(1)			2.5 to 5.5	1			tCYC
	tSCKHA(1)		 Continuous data transmission/reception mode See Fig. 6. (Note 4-1-2) 		4				
	Frequency	tSCK(2)	SCK0(P12)	CMOS output selected See Fig. 6.		4/3			
ock	Low level pulse width	tSCKL(2)					1/2		tSCK
한 High level tt 와 pulse width O	tSCKH(2)			2.5 to 5.5	1/2			ISCK	
	tSCKHA(2)		 Continuous data transmission/reception mode CMOS output selected See Fig. 6. 		tSCKH(2) +2tCYC		tSCKH(2) +(10/3) tCYC	tCYC	
Da	ta setup time	tsDI(1)	SB0(P11), SI0(P11)	 Must be specified with respect to rising edge of SIOCLK. See Fig. 6. 	2.5 to 5.5	0.03			
Da	ta hold time	thDI(1)			2.5 to 5.5	0.03			
clock	Output delay time	tdD0(1)	SO0(P10), SB0(P11)	Continuous data transmission/reception mode (Note 4-1-3)	2.5 to 5.5			(1/3)tCYC +0.05	
Input		tdD0(2)		Synchronous 8-bit mode (Note 4-1-3)	2.5 to 5.5			1tCYC +0.05	μs
Output clock Ir		tdD0(3)		(Note 4-1-3)	2.5 to 5.5			(1/3)tCYC +0.05	
	Input clock a Output clock Input clock	Low level pulse width High level pulse width Frequency Low level pulse width High level pulse width Data setup time Data hold time yooroor indute Vooroor indute	Frequency tSCK(1) Low level pulse width tSCKL(1) High level pulse width tSCKH(1) High level pulse width tSCKH(1) Frequency tSCKH(1) K tSCKHA(1) Total tSCKL(2) Low level pulse width tSCKL(2) High level pulse width tSCKH(2) Data setup time tSCKHA(2) Data hold time thDl(1) NOT time tdD0(1) time tdD0(2)	Parameter Symbol Remarks Frequency tSCK(1) SCK0(P12) Low level tSCKL(1) pulse width High level tSCKH(1) tSCKH(1) pulse width tSCKHA(1) tSCK0(P12) Voo 1000 Frequency tSCK1(2) Low level tSCKL(2) SCK0(P12) Low level tSCKL(2) SCK0(P12) Low level tSCKL(2) SCK0(P12) Dulse width tSCKL(2) SCK0(P12) Data setup time tSCKHA(2) SB0(P11), SI0(P11) Data hold time thDI(1) SO0(P10), SB0(P11), SI0(P11) yoo 1000 tdD0(1) tdD0(2) tdD0(2) tdD0(3) tdD0(3)	Parameter Symbol Remarks Conditions Frequency tSCK(1) SCK0(P12) See Fig. 6. Low level pulse width tSCKL(1)	Parameter Symbol Remarks Conditions VpD/I Frequency tSCK(1) SCK0(P12) See Fig. 6. 2.5 to 5.5 Low level pulse width tSCKL(1) tSCKH(1)	ParameterSymbolRemarksConditions $V_{DD}[V]$ minImage: space	$ \begin{array}{ c c c c } \hline Parameter & Symbol & Remarks & Conditions & V_Dp[V] & min & typ \\ \hline V_Dp[V] & min & tsCKL(1) \\ \hline V_Dp[V] & tsCKL(1) & tsCKH(1) \\ \hline V_Dp[V] & tsCKH(2) \\ \hline V_Dp[V] & $	$ \begin{array}{ c $

Note 4-1-1: These specifications are theoretical values. Add margin depending on its use.

Note 4-1-2: To use serial-clock-input in continuous trans/rec mode, a time from SIORUN being set when serial clock is "H" to the first negative edge of the serial clock must be longer than tSCKHA.

Note 4-1-3: Must be specified with respect to falling edge of SIOCLK. Must be specified as the time to the beginning of output state change in open drain output mode. See Fig. 6.

2. SIO1 Serial I/O Characteristics (Note 4-2-1)

		Parameter	Qumbal	Pin/	Conditions			Speci	fication	
	ŀ	Parameter	Symbol	Remarks	Conditions	V _{DD} [V]	min	typ	max	unit
	×	Frequency	tSCK(3)	SCK1(P15)	See Fig. 6.		2			
	Input clock	Low level pulse width	tSCKL(3)			2.5 to 5.5	1			tCYC
Serial clock	Ч	High level pulse width	tSCKH(3)				1			IC YC
Serial	сk С	Frequency	tSCK(4)	SCK1(P15)	CMOS output selected See Fig. 6.		2			
	Output clock	Low level pulse width	tSCKL(4)			2.5 to 5.5		1/2		tSCK
	õ	High level pulse width	tSCKH(4)				1/2			ISCK
Serial input	Da	ta setup time	tsDI(2)	SB1(P14), SI1(P14)	Must be specified with respect to rising edge of SIOCLK.	2.5 to 5.5	0.03			
Serial	Da	ta hold time	thDI(2)		• See Fig. 6.	2.5 to 5.5	0.03			
Serial output	Οι	tput delay time	tdD0(4)	SO1(P13), SB1(P14)	 Must be specified with respect to falling edge of SIOCLK. Must be specified as the time to the beginning of output state change in open drain output mode. See Fig. 6. 	2.5 to 5.5			(1/3)tCYC +0.05	μs

Note 4-2-1: These specifications are theoretical values. Add margin depending on its use.

Pulse Input Conditions at $Ta = -40^{\circ}C$ to $+85^{\circ}C$, VSS1 = 0V

Parameter	Symbol	Pin/Remarks	Conditions			Specit	ication	
Parameter	Symbol	Pin/Remarks	V _{DD} [V]		min	typ	max	unit
High/low level pulse width	tPIH(1) tPIL(1)	INT0(P70), INT1(P71), INT2(P16)	Interrupt acceptableEvents to timer 0, 1 can be input.	2.5 to 5.5	1			
	tPIH(2) tPIL(2)	INT3(P17) (Noise rejection ratio set to 1/1.)	Interrupt acceptableEvents to timer 0 can be input.	2.5 to 5.5	2			10,10
	tPIH(3) tPIL(3)	INT3(P17) (Noise rejection ratio set to 1/32.)	Interrupt acceptableEvents to timer 0 can be input.	2.5 to 5.5	64			tCYC
	tPIH(4) tPIL(4)	INT3(P17) (Noise rejection ratio set to 1/128.)	Interrupt acceptableEvents to timer 0 can be input.	2.5 to 5.5	256			
	tPIL(5)	RES	Reset possible	2.5 to 5.5	200			μs

Deremeter	Cumbal	Din/Domorko	Conditions			Specifi	cation	
Parameter	Symbol	Pin/Remarks	Conditions	V _{DD} [V]	min	typ	max	unit
Resolution	Ν	AN0(P00) to		3.0 to 5.5		8		bit
Absolute precision	ET	AN7(P07)	(Note 6-1)	3.0 to 5.5			±1.5	LSB
Conversion time tCAE	tCAD	tCAD	AD conversion time=32×tCYC (ADCR2=0)	4.5 to 5.5	15.62 (tCYC=		97.92 (tCYC=	
			(Note 6-2)		0.488µs)		3.06µs)	l
					23.52		97.92	
				3.0 to 5.5	(tCYC=		(tCYC=	
					0.735µs)		3.06µs)	μs
			AD conversion time=64×tCYC		18.82		97.92	μο
			(ADCR2=1)	4.5 to 5.5	(tCYC=		(tCYC=	
			(Note 6-2)		0.294µs)		1.53µs)	
					47.04		97.92	
				3.0 to 5.5	(tCYC=		(tCYC=	
					0.735µs)		1.53µs)	
Analog input voltage range	VAIN			3.0 to 5.5	V _{SS}		V _{DD}	V
Analog port	IAINH		VAIN=V _{DD}	3.0 to 5.5			1	
input current	IAINL		VAIN=V _{SS}	3.0 to 5.5	-1			μA

AD Converter Characteristics at $Ta = -40^{\circ}C$ to $+85^{\circ}C$, $V_{SS}1 = 0V$

Note 6-1: Absolute precision not including quantizing error ($\pm 1/2$ LSB).

Note 6-2: Conversion time means time from executing AD conversion instruction to loading complete digital value to register.

Consumption Current Characteristics at $Ta = -40^{\circ}C$ to $+85^{\circ}C$, $V_{SS}1 = 0V$

Parameter	Querra ha a l	Pin/	Que ditions		Specification				
i arameter	Symbol	Remarks	Conditions	V _{DD} [V]	min	typ	max	unit	
Current dissipation during basic	IDDOP(1)	V _{DD} 1 =V _{DD} 2 =V _{DD} 3	 FmCF=10Hz for ceramic resonator oscillation System clock: 10MHz 	4.5 to 5.5		8.0	24		
operation (Note 7-1)		-*003	 Internal RC oscillation stopped. 1/1 frequency division ratio 	3.0 to 4.5		6.1	19		
	IDDOP(2)		 CF1=15MHz for external clock System clock: CF1 oscillation 	4.5 to 5.5		10.5	32		
			 Internal RC oscillation stopped. 1/2 frequency division ratio 	3.0 to 4.5		9.5	28	mA	
	IDDOP(3)		 FmCF=4MHz for ceramic resonator oscillation 	4.5 to 5.5		3.8	9.5		
			 System clock: 4MHz Internal RC oscillation stopped. 1/1 frequency division ratio 	3.0 to 4.5		3.1	7.8		
	IDDOP(4)		• FmCF=0Hz (No oscillation)	4.5 to 5.5		0.72	3		
			System clock: RC oscillationDivider set to 1/2	2.5 to 4.5		0.53	2		
	IDDOP(5)		 FsX'tal=32.768kHz for crystal oscillation System clock: 32.768KHz 	4.5 to 5.5		39	220		
			 Internal RC oscillation stopped. 1/2 frequency division ratio 	2.5 to 4.5		25	150	μA	

Note 7-1: The currents of the output transistors and the pull-up MOS transistors are ignored.

Continued on next page.

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Parameter	Symbol	Pin/	Conditions		Specification				
Parameter	Symbol	Remarks	Conditions	min	typ	max	unit		
Current dissipation HALT mode	IDDHALT(1)	V _{DD} 1 =V _{DD} 2 =V _{DD} 3	HALT mode • FmCF=10MHz for Ceramic resonator oscillation	4.5 to 5.5		3.0	9		
(Note 7-1)			System clock : 10MHzInternal RC oscillation stopped.Divider: 1/1	3.0 to 4.5		2.1	6.3		
	IDDHALT(2)		HALT mode • CF1=15MHz for external clock • System clock : CF1 oscillation	4.5 to 5.5		4.2	12.5	mA	
			 System clock : CFT oscillation Internal RC oscillation stopped. Divider 1/2 	3.0 to 4.5		2.5	7.8	ma	
	IDDHALT(3)		HALT mode • FmCF=4MHz for Ceramic resonator oscillation	4.5 to 5.5		1.4	3.5		
			System clock : 4MHzInternal RC oscillation stopped.Divider: 1/1	2.5 to 4.5		1.0	2.5		
	IDDHALT(4)		HALT mode • FmCF=0Hz (When oscillation stops.)	4.5 to 5.5		420	1600		
			System clock : RC oscillationDivider: 1/2	2.5 to 4.5		280	1100		
	IDDHALT(5)		HALT mode FsX'tal=32.768kHz for crystal oscillation 	4.5 to 5.5		24	80		
			 Internal RC oscillation stopped. System clock : 32.768kHz Divider: 1/2 	2.5 to 4.5		14	60	μΑ	
Current dissipation	IDDHOLD(1)	V _{DD} 1	HOLD mode • CF1=V _{DD} or open circuit	4.5 to 5.5		0.10	20		
HOLD mode			(when using external clock)	2.5 to 4.5		0.02	15		
Current dissipation	IDDHOLD(2)	V _{DD} 1	Date/time clock HOLD mode • CF1=V _{DD} or open circuit	4.5 to 5.5		21	65		
Date/time clock HOLD mode			(when using external clock) • FsX'tal=32.768kHz for crystal oscillation	2.5 to 4.5		11	50		

Note 7-1: The currents of the output transistors and the pull-up MOS transistors are ignored.

F-ROM Programming Characteristics at $Ta = +10^{\circ}C$ to $+55^{\circ}C$, $V_{SS}1 = 0V$

Parameter	Symbol	Pin/	Conditions		Specifica			ation	
Parameter	Symbol	Remarks	Conditions	V _{DD} [V]	min	typ	max	unit	
On-board writing current	IDDFW(1)	V _{DD} 1	 The current dissipation of the microcomputer is excluded. 	4.5 to 5.5		5	10	mA	
Writing time	tFW(1)		Erase time	451.55		20	30	ms	
	tFW(2)		Writing time	4.5 to 5.5		40	60	μs	

Characteristics of a Sample Main System Clock Oscillation Circuit

The characteristics in the table bellow is based on the following conditions:

- 1. Use the standard evaluation board SANYO has provided.
- 2. Use the peripheral parts with indicated value externally.

3. The peripheral parts value is a recommended value of oscillator manufacturer.

- N ()			Circuit Parameters		Operating Supply	Oscillation Stabilizing Time				
Frequency	Manufacturer	Manufacturer Oscillator		C2	Rd1	Voltage Range	typ	max	Notes	
		1	[pF]	[pF]	[Ω]	[V]	[ms]	[ms]		
10MHz			CSTCE10M0G52-R0	10	10	1k	2.8 to 5.5	0.029		
TOIVIEZ	MURATA	CSTLS10M0G53-B0	15	15	1k	3.0 to 5.5	0.028			
45411-		CSTCR4M00G53-R0	15	15	2.2k	2.3 to 5.5	0.034			
4MHz MURATA		CSTLS4M00G53-B0	15	15	2.2k	2.3 to 5.5	0.030			

Table 1 Characteristics of a Sample Main System Clock Oscillator Circuit with a Ceramic Oscillator

The oscillation stabilizing time is a period until the oscillation becomes stable after V_{DD} becomes higher than minimum operating voltage. (Refer to Figure 4)

Characteristics of a Sample Subsystem Clock Oscillator Circuit

The characteristics in the table bellow is based on the following conditions:

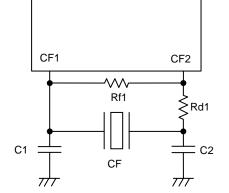
- 1. Use the standard evaluation board SANYO has provided.
- 2. Use the peripheral parts with indicated value externally.
- 3. The peripheral parts value is a recommended value of oscillator manufacturer

Table 2 Char	acteristics of a Sa	mple Subsystem	Clock Oscillator	Circuit with a Cr	vstal Oscillator

Frequency			Circuit Parameters Manufacturer Oscillator			i	Operating Supply Voltage	Oscillation Stabilizing Time		Notos
Frequency	Manufacturer	Oscillator	C3	C4	Rf	Rd2	Range	typ	max	Notes
			[pF]	[pF]	[Ω]	[Ω]	[V]	[s]	[s]	

The oscillation stabilizing time is a period until the oscillation becomes stable after executing the instruction which starts the sub-clock oscillation or after releasing the HOLD mode. (Refer to Figure 4)

Notes: Since the circuit pattern affects the oscillation frequency, place the oscillation-related parts as close to the oscillation pins as possible with the shortest possible pattern length.



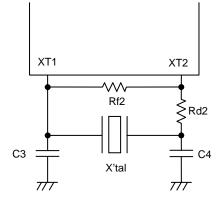
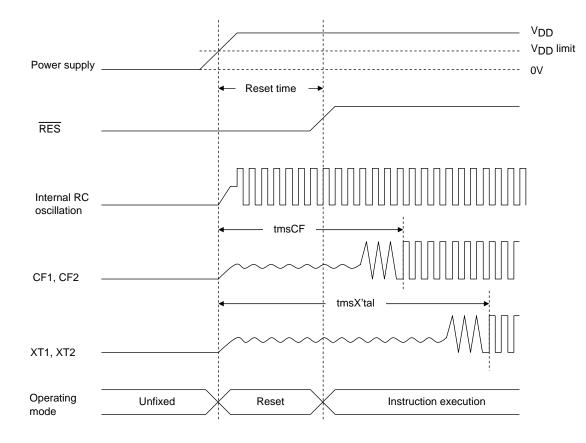


Figure 1 Ceramic Oscillation Circuit

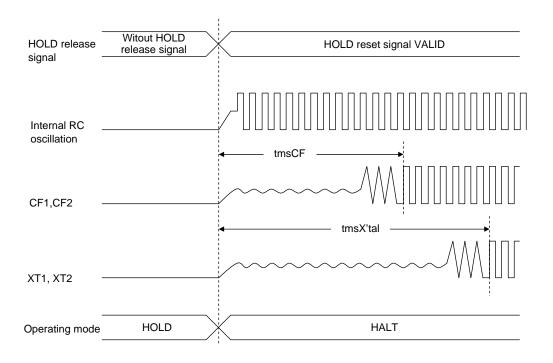
Figure 2 Crystal Oscillation Circuit



Figure 3 AC Timing Measurement Point

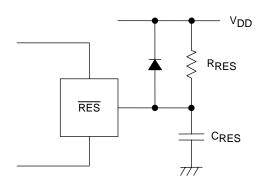


Reset Time and Oscillation Stabilization Time



HOLD Reset Signal and Oscillation Stabilization Time

Figure 4 Oscillation Stabilization Time



Note: Set C_{RES} , R_{RES} values such that reset time exceeds 200 μ s.



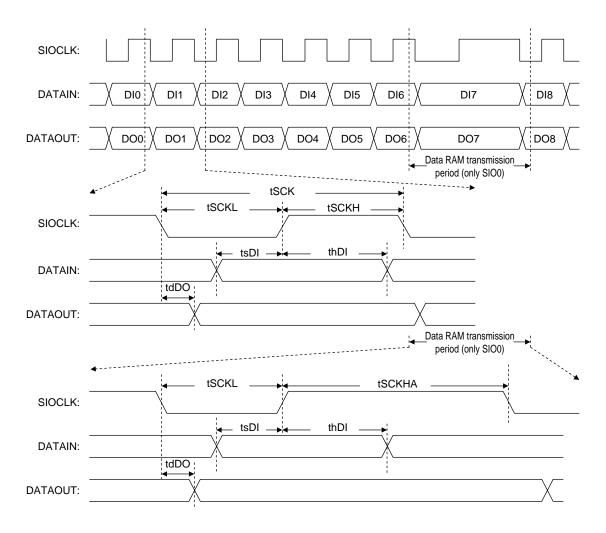


Figure 6 Serial I/O Waveform

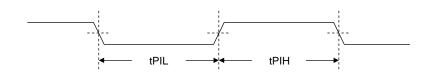


Figure 7 Pulse Input Timing Signal Waveform

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