



SANYO Semiconductors

DATA SHEET

LC87F5864C

CMOS IC
FROM 64K byte, RAM 2048 byte on-chip

8-bit 1-chip Microcontroller

Overview

The SANYO LC87F5864C is an 8-bit microcomputer that, centered around a CPU running at a minimum bus cycle time of 83.3ns, integrates on a single chip a number of hardware features such as 64K-byte flash ROM (onboard programmable), 2048-byte RAM, sophisticated 16-bit timers/counters (may be divided into 8-bit timers), a 16-bit timer/counter (may be divided into 8-bit timers/counters or 8-bit PWMs), four 8-bit timers with a prescaler, a base timer serving as a time-of-day clock, a high-speed clock counter, a synchronous SIO interface (with automatic block transmission/reception capabilities), an asynchronous/synchronous SIO interface, a UART interface (full duplex), an 8-bit 11-channel AD converter, two 12-bit PWM channels, a system clock frequency divider, ROM correction function, and a 23-source 10-vector interrupt feature.

Features

■Flash ROM

- Capable of on-board-programing with wide range, 3.0 to 5.5V, of voltage source.
- Block-erasable in 128 byte units
- 65536 × 8-bits (LC87F5864C)

■RAM

- 2048 × 9 bits (LC87F5864C)

■Minimum Bus Cycle

- 83.3ns (12MHz) $V_{DD}=3.0$ to 5.5V
- 125ns (8MHz) $V_{DD}=2.5$ to 5.5V
- 500ns (2MHz) $V_{DD}=2.2$ to 5.5V

Note: The bus cycle time here refers to the ROM read speed.

■Minimum Instruction Cycle Time

- 250ns (12MHz) $V_{DD}=3.0$ to 5.5V
- 375ns (8MHz) $V_{DD}=2.5$ to 5.5V
- 1.5μs (2MHz) $V_{DD}=2.2$ to 5.5V

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TOKYO OFFICE Tokyo Bldg., 1-10, 1 Chome, Ueno, Taito-ku, TOKYO, 110-8534 JAPAN

■ Ports

- Normal withstand voltage I/O ports
 - Ports whose I/O direction can be designated in 1-bit units 46 (P1n, P2n, P70 to P73, P80 to P86, PBn, PCn, PWM2, PWM3, XT2)
 - Ports whose I/O direction can be designated in 4-bit units 8 (P0n)
- Normal withstand voltage input port 1 (XT1)
- Dedicated oscillator ports 2 (CF1, CF2)
- Reset pins 1 (RES)
- Power pins 6 (VSS1 to 3, VDD1 to 3)

■ Timers

- Timer 0 : 16-bit timer/counter with a capture register
 - Mode 0 : 8-bit timer with an 8-bit programmable prescaler (with an 8-bit capture register) × 2-channels
 - Mode 1 : 8-bit timer with an 8-bit programmable prescaler (with an 8-bit capture register) + 8-bit counter (with an 8-bit capture register)
 - Mode 2 : 16-bit timer with an 8-bit programmable prescaler (with a 16-bit capture register)
 - Mode 3 : 16-bit counter (with a 16-bit capture register)
- Timer 1 : 16-bit timer/counter that supports PWM/toggle outputs
 - Mode 0 : 8-bit timer with an 8-bit prescaler (with toggle outputs) + 8-bit timer/counter with an 8-bit prescaler (with toggle outputs)
 - Mode 1 : 8-bit PWM with an 8-bit prescaler × 2-channels
 - Mode 2 : 16-bit timer/counter with an 8-bit prescaler (with toggle outputs) (toggle outputs also possible from the lower-order 8-bits)
 - Mode 3 : 16-bit timer with an 8-bit prescaler (with toggle outputs) (the lower-order 8 bits can be used as PWM)
- Timer 4 : 8-bit timer with a 6-bit prescaler
- Timer 5 : 8-bit timer with a 6-bit prescaler
- Timer 6 : 8-bit timer with a 6-bit prescaler (with toggle outputs)
- Timer 7 : 8-bit timer with a 6-bit prescaler (with toggle outputs)
- Base timer
 - 1) The clock is selectable from the subclock (32.768kHz crystal oscillation), system clock, and timer 0 prescaler output.
 - 2) Interrupts programmable in 5 different time schemes

■ High-speed Clock Counter

- 1) Can count clocks with a maximum clock rate of 20MHz (at a main clock of 10MHz)
- 2) Can generate output real-time

■ SIO

- SIO0 : 8-bit synchronous serial interface
 - 1) LSB first/MSB first mode selectable
 - 2) Built-in 8-bit baudrate generator (maximum transfer clock cycle=4/3 tCYC)
 - 3) Automatic continuous data transmission (1 to 256 bits, specifiable in 1 bit units, suspension and resumption of data transmission possible in 1 byte units)
- SIO1 : 8-bit asynchronous/synchronous serial interface
 - Mode 0 : Synchronous 8-bit serial I/O (2- or 3-wire configuration, 2 to 512 tCYC transfer clocks)
 - Mode 1 : Asynchronous serial I/O (half-duplex, 8 data bits, 1 stop bit, 8 to 2048 tCYC baudrates)
 - Mode 2 : Bus mode 1 (start bit, 8 data bits, 2 to 512 tCYC transfer clocks)
 - Mode 3 : Bus mode 2 (start detect, 8 data bits, stop detect)

■ UART

- Full duplex
- 7/8/9 bit data bits selectable
- 1 stop bit (2-bit in continuous data transmission)
- Built-in baudrate generator

■AD Converter : 8 bits × 11 channels

■PWM : Multifrequency 12-bit PWM × 2-channels

■Remote Control Receiver Circuit (sharing pins with P73, INT3, and T0IN)

- Noise rejection function (noise filter time constant selectable from 1 tCYC, 32 tCYC, and 128 tCYC)

■Watchdog Timer

- External RC watchdog timer
- Interrupt and reset signals selectable

■Clock Output Function

- 1) Able to output selected oscillation clock 1/1, 1/2, 1/4, 1/8, 1/16, 1/32, 1/64 as system clock.
- 2) Able to output oscillation clock of sub clock.

■Interrupts

- 23 sources, 10 vector addresses
 - 1) Provides three levels (low (L), high (H), and highest (X)) of multiplex interrupt control. Any interrupt requests of the level equal to or lower than the current interrupt are not accepted.
 - 2) When interrupt requests to two or more vector addresses occur at the same time, the interrupt of the highest level takes precedence over the other interrupts. For interrupts of the same level, the interrupt into the smallest vector address takes precedence.

No.	Vector Address	Level	Interrupt Source
1	00003H	X or L	INT0
2	0000BH	X or L	INT1
3	00013H	H or L	INT2/T0L/INT4
4	0001BH	H or L	INT3/INT5/base timer0/base timer1
5	00023H	H or L	T0H
6	0002BH	H or L	T1L/T1H
7	00033H	H or L	SIO0/UART1 receive
8	0003BH	H or L	SIO1/UART1 transmit
9	00043H	H or L	ADC/T6/T7
10	0004BH	H or L	Port 0/T4/T5/PWM2, PWM3

- Priority levels X > H > L
- Of interrupts of the same level, the one with the smallest vector address takes precedence.

■Subroutine Stack Levels : 1024 levels (the stack is allocated in RAM)

■High-speed Multiplication/Division Instructions

- 16 bits × 8 bits (5 tCYC execution time)
- 24 bits × 16 bits (12 tCYC execution time)
- 16 bits ÷ 8 bits (8 tCYC execution time)
- 24 bits ÷ 16 bits (12 tCYC execution time)

■Oscillation Circuits

- RC oscillation circuit (internal) : For system clock
- CF oscillation circuit : For system clock, with internal Rf
- Crystal oscillation circuit : For low-speed system clock, with internal Rf

■System Clock Divider Function

- Can run on low current.
- The minimum instruction cycle selectable from 300ns, 600ns, 1.2μs, 2.4μs, 4.8μs, 9.6μs, 19.2μs, 38.4μs, and 76.8μs (at a main clock rate of 10MHz).

■ Standby Function

- HALT mode : Halts instruction execution while allowing the peripheral circuits to continue operation.
 - 1) Oscillation is not halted automatically.
 - 2) Canceled by a system reset or occurrence of an interrupt
- HOLD mode : Suspends instruction execution and the operation of the peripheral circuits.
 - 1) The CF, RC, and crystal oscillators automatically stop operation.
 - 2) There are three ways of resetting the HOLD mode.
 - (1) Setting the reset pin to the low level
 - (2) Setting at least one of the INT0, INT1, INT2, INT4, and INT5 pins to the specified level
 - (3) Having an interrupt source established at port 0
- X'tal HOLD mode : Suspends instruction execution and the operation of the peripheral circuits except the base timer.
 - 1) The CF and RC oscillators automatically stop operation.
 - 2) The state of crystal oscillation established when the X'tal HOLD mode is entered is retained.
 - 3) There are four ways of resetting the X'tal HOLD mode.
 - (1) Setting the reset pin to the low level
 - (2) Setting at least one of the INT0, INT1, INT2, INT4, and INT5 pins to the specified level
 - (3) Having an interrupt source established at port 0
 - (4) Having an interrupt source established in the base timer circuit

■ Package Form

- VQFN64 (10 × 10): Lead-free type
- TQFP64J (7 × 7): Lead-free type

■ Development Tools

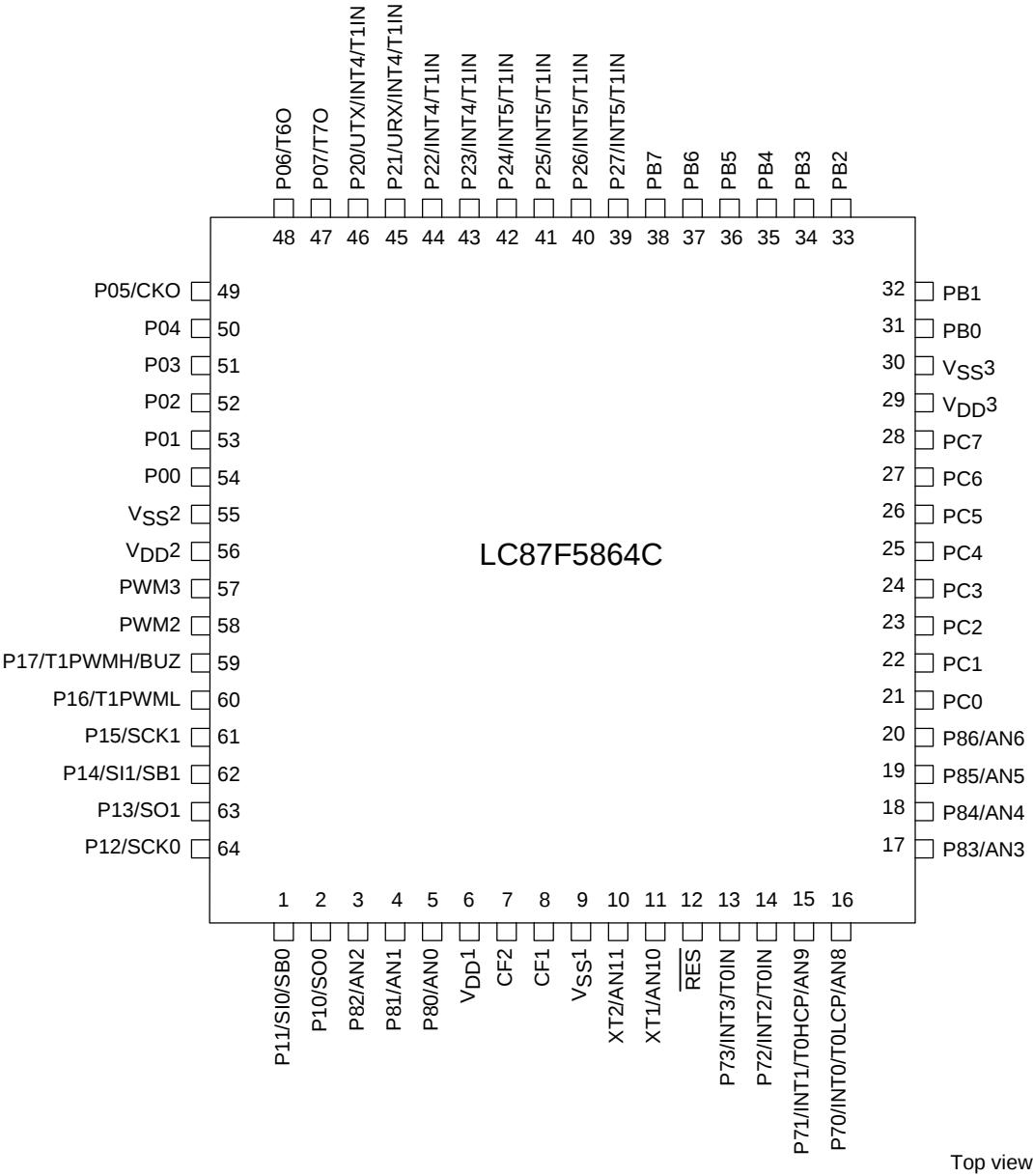
- Evaluation chip : LC87EV690
- Emulator : EVA62S + ECB876600D + SUB875800

■ Programming Boards

- W87F58256VQ (For VQFN64 (10 × 10) package)
- W87F58256TQ7 (For TQFP64J (7 × 7) packages)

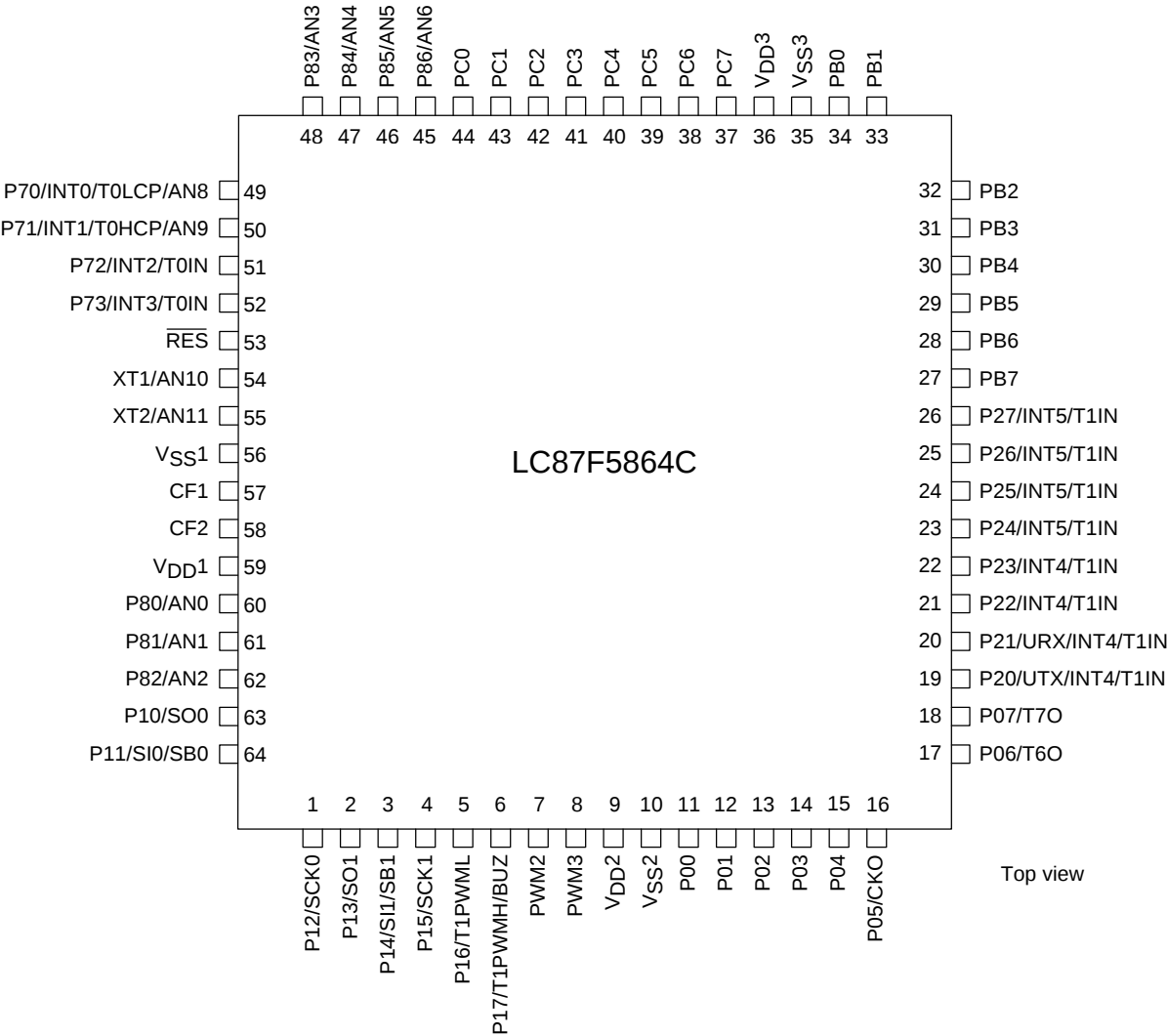
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Pin Assignments



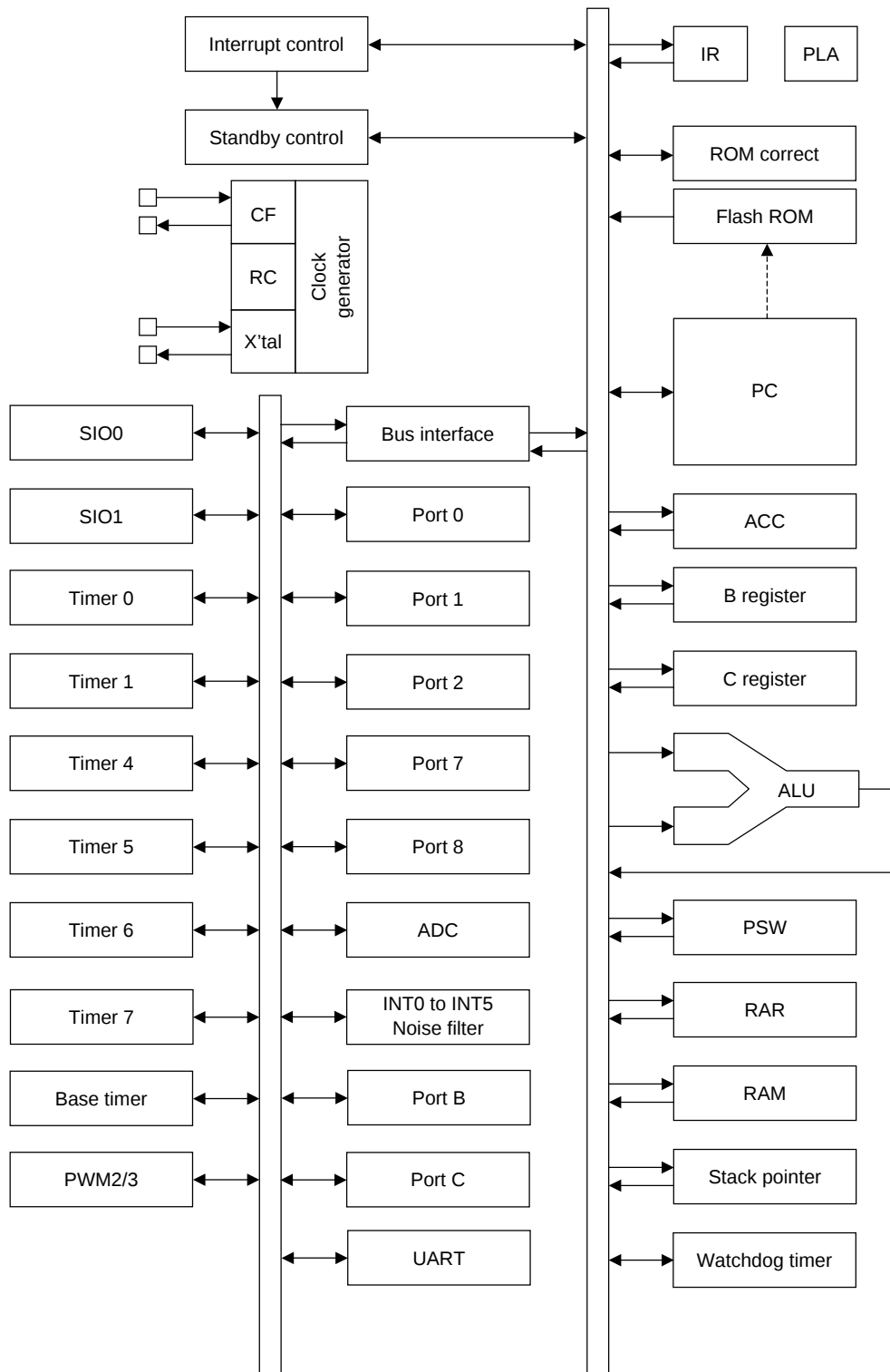
SANYO: VQFN64 (10 × 10) “Lead-free Type”

LC87F5864C



SANYO: TQFP64J (7 × 7) “Lead-free Type”

System Block Diagram



Pin Description

Pin Name	I/O	Description	Option																														
V _{SS} 1, V _{SS} 2 V _{SS} 3	-	- Power supply pin	No																														
V _{DD} 1, V _{DD} 2 V _{DD} 3	-	+ Power supply pin	No																														
Port 0	I/O	• 8-bit I/O port • I/O specifiable in 4-bit units • Pull-up resistor can be turned on and off in 4-bit units • HOLD release input • Port 0 interrupt input • Shared Pins P05 : Clock output (system clock / can selected from sub clock) P06 : Timer 6 toggle output P07 : Timer 7 toggle output	Yes																														
P00 to P07																																	
Port 1	I/O	• 8-bit I/O port • I/O specifiable in 1-bit units • Pull-up resistor can be turned on and off in 1-bit units • Pin functions P10 : SIO0 data output P11 : SIO0 data input/bus I/O P12 : SIO0 clock I/O P13 : SIO1 data output P14 : SIO1 data input/bus I/O P15 : SIO1 clock I/O P16 : Timer 1 PWML output P17 : Timer 1 PWMH output/beeper output	Yes																														
P10 to P17																																	
Port 2	I/O	• 8-bit I/O port • I/O specifiable in 1-bit units • Pull-up resistors can be turned on and off in 1-bit units • Pin functions P20 : UART transmit P21 : UART receive P20 to P23 : INT4 input/HOLD reset input/timer 1 event input/timer 0L capture input /timer 0H capture input P24 to P27 : INT5 input/HOLD reset input/timer 1 event input/timer 0L capture input /timer 0H capture input • Interrupt acknowledge type <table><tr><td></td><td>Rising</td><td>Falling</td><td>Rising/ Falling</td><td>H level</td><td>L level</td></tr><tr><td>INT4</td><td>enable</td><td>enable</td><td>enable</td><td>disable</td><td>disable</td></tr><tr><td>INT5</td><td>enable</td><td>enable</td><td>enable</td><td>disable</td><td>disable</td></tr></table>		Rising	Falling	Rising/ Falling	H level	L level	INT4	enable	enable	enable	disable	disable	INT5	enable	enable	enable	disable	disable	Yes												
			Rising	Falling	Rising/ Falling	H level	L level																										
INT4	enable	enable	enable	disable	disable																												
INT5	enable	enable	enable	disable	disable																												
P20 to P27																																	
Port 7	I/O	• 4-bit I/O port • I/O specifiable in 1-bit units • Pull-up resistor can be turned on and off in 1-bit units • Shared pins P70 : INT0 input/HOLD reset input/timer 0L capture input/watchdog timer output P71 : INT1 input/HOLD reset input/timer 0H capture input P72 : INT2 input/HOLD reset input/timer 0 event input/timer 0L capture input/ high speed clock counter input P73 : INT3 input (with noise filter)/timer 0 event input/timer 0H capture input AD converter input port: AN8 (P70), AN9 (P71) • Interrupt acknowledge type <table><tr><td></td><td>Rising</td><td>Falling</td><td>Rising/ Falling</td><td>H level</td><td>L level</td></tr><tr><td>INT0</td><td>enable</td><td>enable</td><td>disable</td><td>enable</td><td>enable</td></tr><tr><td>INT1</td><td>enable</td><td>enable</td><td>disable</td><td>enable</td><td>enable</td></tr><tr><td>INT2</td><td>enable</td><td>enable</td><td>enable</td><td>disable</td><td>disable</td></tr><tr><td>INT3</td><td>enable</td><td>enable</td><td>enable</td><td>disable</td><td>disable</td></tr></table>		Rising	Falling	Rising/ Falling	H level	L level	INT0	enable	enable	disable	enable	enable	INT1	enable	enable	disable	enable	enable	INT2	enable	enable	enable	disable	disable	INT3	enable	enable	enable	disable	disable	No
			Rising	Falling	Rising/ Falling	H level	L level																										
INT0	enable	enable	disable	enable	enable																												
INT1	enable	enable	disable	enable	enable																												
INT2	enable	enable	enable	disable	disable																												
INT3	enable	enable	enable	disable	disable																												
P70 to P73																																	

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LC87F5864C

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Pin Name	I/O	Description	Option
Port 8	I/O	• 7-bit I/O port • I/O specifiable in 1-bit units • Shared pins - AD converter input port : AN0 (P80) to AN6 (P86)	No
P80 to P86			
PWM2	I/O	• PWM2 and PWM3 output ports • General-purpose I/O available	No
PWM3			
Port B	I/O	• 8-bit I/O port • I/O specifiable in 1-bit units • Pull-up resistor can be turned on and off in 1-bit units	Yes
PB0 to PB7			
Port C	I/O	• 8-bit I/O port • I/O specifiable in 1-bit units • Pull-up resistor can be turned on and off in 1-bit units	Yes
PC0 to PC7			
RES	Input	Reset pin	No
XT1	Input	• 32.768kHz crystal oscillator input pin • Shared pins - General-purpose input port - AD converter input port : AN10 - Must be connected to V_{DD1} if not to be used.	No
XT2	I/O	• 32.768kHz crystal oscillator output pin • Shared pins - General-purpose I/O port - AD converter input port : AN11 - Must be set for oscillation and kept open if not to be used.	No
CF1	Input	Ceramic resonator input pin	No
CF2	Output	Ceramic resonator output pin	No

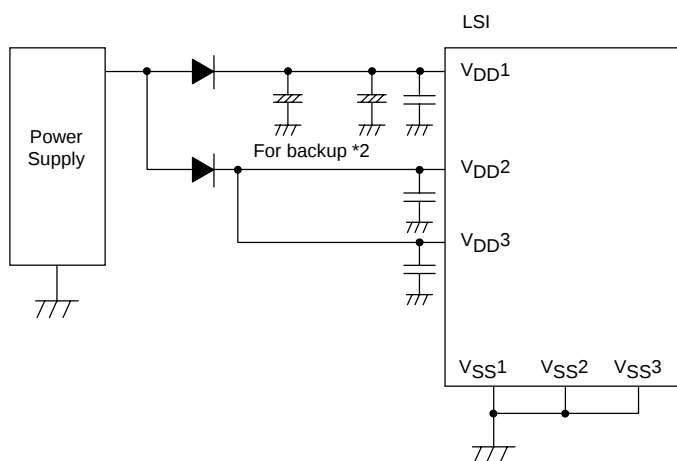
Port Output Types

The table below lists the types of port outputs and the presence/absence of a pull-up resistor.
Data can be read into any input port even if it is in the output mode.

Port Name	Option Selected in Units of	Option Type	Output Type	Pull-up Resistor
P00 to P07	1 bit	1	CMOS	Programmable (Note 1)
		2	Nch-open drain	No
P10 to P17	1 bit	1	CMOS	Programmable
		2	Nch-open drain	Programmable
P20 to P27	1 bit	1	CMOS	Programmable
		2	Nch-open drain	Programmable
P70	-	No	Nch-open drain	Programmable
P71 to P73	-	No	CMOS	Programmable
P80 to P86	-	No	Nch-open drain	No
PWM2, PWM3	-	No	CMOS	No
PB0 to PB7	1 bit	1	CMOS	Programmable
		2	Nch-open drain	Programmable
PC0 to PC7	1 bit	1	CMOS	Programmable
		2	Nch-open drain	Programmable
XT1	-	No	Input for 32.768kHz crystal oscillator (Input only)	No
XT2	-	No	Output for 32.768kHz crystal oscillator (Nch-open drain when in general-purpose output mode)	No

Note 1 : Programmable pull-up resistors for port 0 are controlled in 4-bit units (P00 to 03, P04 to 07).

*1 : Connect the IC as shown below to minimize the noise input to the V_{DD1} pin.
Be sure to electrically short the V_{SS1} , V_{SS2} , and V_{SS3} pins.



*2 : The internal memory is sustained by V_{DD1} . If none of V_{DD2} and V_{DD3} are backed up, the high level output at the ports are unstable in the HOLD backup mode, allowing through current to flow into the input buffer and thus shortening the backup time.
Make sure that the port outputs are held at the low level in the HOLD backup mode.

LC87F5864C

Absolute Maximum Ratings at Ta = 25°C, VSS1 = VSS2 = VSS3 = 0V

Parameter		Symbol	Pin/Remarks	Conditions	Specification			
					VDD [V]	min	typ	max
Maximum supply voltage		VDD max	VDD 1, VDD2, VDD3	VDD1=VDD2=VDD3		-0.3		+6.5
Input voltage		VI(1)	XT1, CF1			-0.3		VDD+0.3
Input/output voltage		VIO(1)	Ports 0, 1, 2 Ports 7, 8 Ports B, C PWM2, PWM3, XT2			-0.3		VDD+0.3
High level output current	Peak output current	IOPH(1)	Ports 0, 1, 2 Ports B, C	CMOS output select Per 1 applicable pin		-10		
		IOPH(2)	PWM2, PWM3	Per 1 applicable pin		-20		
		IOPH(3)	P71 to P73	Per 1 applicable pin		-5		
	Mean output current (Note 1-1)	IOMH(1)	Ports 0, 1, 2 Ports B, C	CMOS output select Per 1 applicable pin		-7.5		
		IOMH(2)	PWM2, PWM3	Per 1 applicable pin		-15		
		IOMH(3)	P71 to P73	Per 1 applicable pin		-3		
	Total output current	ΣIOAH(1)	P71 to P73	Total of all applicable pins		-10		
		ΣIOAH(2)	Port 1 PWM2, PWM3	Total of all applicable pins		-25		
		ΣIOAH(3)	Ports 0, 2	Total of all applicable pins		-25		
		ΣIOAH(4)	Ports 0, 1, 2 PWM2, PWM3	Total of all applicable pins		-45		
		ΣIOAH(5)	Port B	Total of all applicable pins		-25		
		ΣIOAH(6)	Port C	Total of all applicable pins		-25		
		ΣIOAH(7)	Ports B, C	Total of all applicable pins		-45		
Low level output current	Peak output current	IOPL(1)	P02 to P07 Ports 1, 2 Ports B, C PWM2, PWM3	Per 1 applicable pin				20
		IOPL(2)	P00, P01	Per 1 applicable pin				30
		IOPL(3)	Ports 7, 8, XT2	Per 1 applicable pin				10
	Mean output current (Note 1-1)	IOML(1)	P02 to P07 Ports 1, 2 Ports B, C PWM2, PWM3	Per 1 applicable pin				15
		IOML(2)	P00, P01	Per 1 applicable pin				20
		IOML(3)	Ports 7, 8, XT2	Per 1 applicable pin				7.5
	Total output current	ΣIOAL(1)	Port 7 P83 to P86, XT2	Total of all applicable pins				15
		ΣIOAL(2)	P80 to P82	Total of all applicable pins				15
		ΣIOAL(3)	Ports 7, 8, XT2	Total of all applicable pins				20
		ΣIOAL(4)	Port 1 PWM2, PWM3	Total of all applicable pins				45
		ΣIOAL(5)	Ports 0, 2	Total of all applicable pins				45
		ΣIOAL(6)	Ports 0, 1, 2 PWM2, PWM3	Total of all applicable pins				80
		ΣIOAL(7)	Port B	Total of all applicable pins				45
		ΣIOAL(8)	Port C	Total of all applicable pins				45
		ΣIOAL(9)	Ports B, C	Total of all applicable pins				80
Power dissipation	Pdmx		VQFN64(10×10)	Ta=-20 to +70°C				190
			TQFP64J(7×7)					188
Operating ambient temperature	Topr					-20		70
Storage ambient temperature	Tstg					-55		125

Note 1-1 : The mean output current is a mean value measured over 100ms.

LC87F5864C

Allowable Operating Conditions at Ta = -20°C to +70°C, V_{SS1} = V_{SS2} = V_{SS3} = 0V

Parameter	Symbol	Pin/Remarks	Conditions	Specification				
				V _{DD} [V]	min	typ	max	unit
Operating supply voltage (Note 2-1)	V _{DD} (1)	V _{DD1} =V _{DD2} =V _{DD3}	0.245μs ≤ tCYC ≤ 200μs		3.0		5.5	V
			0.367μs ≤ tCYC ≤ 200μs		2.5		5.5	
			1.47μs ≤ tCYC ≤ 200μs		2.2		5.5	
Memory sustaining supply voltage	V _{HD}	V _{DD1} =V _{DD2} =V _{DD3}	RAM and register contents sustained in HOLD mode.		2.0		5.5	
High level input voltage	V _{IH} (1)	Ports 1, 2 P71 to P73 P70 port input /interrupt side		2.2 to 5.5	0.3V _{DD} +0.7		V _{DD}	
	V _{IH} (2)	Ports 0, 8, B, C PWM2, PWM3		2.2 to 5.5	0.3V _{DD} +0.7		V _{DD}	
	V _{IH} (3)	Port 70 watchdog timer side		2.2 to 5.5	0.9V _{DD}		V _{DD}	
	V _{IH} (4)	XT1, XT2, CF1, $\overline{\text{RES}}$		2.2 to 5.5	0.75V _{DD}		V _{DD}	
Low level input voltage	V _{IL} (1)	Ports 1, 2 P71 to P73 P70 port input /interrupt side		4.0 to 5.5	V _{SS}		0.1V _{DD} +0.4	
				2.2 to 4.0	V _{SS}		0.2V _{DD}	
	V _{IL} (2)	Ports 0, 8, B, C PWM2, PWM3		4.0 to 5.5	V _{SS}		0.15V _{DD} +0.4	
				2.2 to 4.0	V _{SS}		0.2V _{DD}	
	V _{IL} (3)	Port 70 watchdog timer side		2.2 to 5.5	V _{SS}		0.8V _{DD} -1.0	
	V _{IL} (4)	XT1, XT2, CF1, $\overline{\text{RES}}$		2.2 to 5.5	V _{SS}		0.25V _{DD}	
Instruction cycle time (Note 2-2)	tCYC			3.0 to 5.5	0.245		200	μs
				2.5 to 5.5	0.367		200	
				2.2 to 5.5	1.47		200	
Oscillation frequency range (Note 2-3)	FmCF(1)	CF1, CF2	12MHz ceramic oscillation See Fig. 1.	3.0 to 5.5		12		MHz
	FmCF(2)	CF1, CF2	8MHz ceramic oscillation See Fig. 1.	2.5 to 5.5		8		
	FmCF(3)	CF1, CF2	4MHz ceramic oscillation See Fig. 1.	2.2 to 5.5		4		
	FmRC		Internal RC oscillation	2.2 to 5.5	0.3	1.0	2.0	
	FsX'tal	XT1, XT2	32.768kHz crystal oscillation See Fig. 2.	2.2 to 5.5		32.768		kHz

Note 2-1 : V_{DD} must be held greater than or equal to 3.0V in the flash ROM onboard programming mode.

Note 2-2 : Relationship between tCYC and oscillation frequency is 3/FmCF at a division ratio of 1/1 and 6/FmCF at a division ratio of 1/2.

Note 2-3 : See Tables 1 and 2 for the oscillation constants.

LC87F5864C

Electrical Characteristics at Ta = -20°C to +70°C, VSS1 = VSS2 = VSS3 = 0V

Parameter	Symbol	Pins	Conditions	Specification				
				VDD[V]	min	typ	max	unit
High level input current	I _{IH} (1)	Ports 0, 1, 2 Ports 7, 8 Ports B, C RES PWM2, PWM3	Output disabled Pull-up resistor off V _{IN} =V _{DD} (Including output Tr's off leakage current)	2.2 to 5.5			1	μA
	I _{IH} (2)	XT1, XT2	For input port specification V _{IN} =V _{DD}	2.2 to 5.5			1	
	I _{IH} (3)	CF1	V _{IN} =V _{DD}	2.2 to 5.5			15	
Low level input current	I _{IL} (1)	Ports 0, 1, 2 Ports 7, 8 Ports B, C RES PWM2, PWM3	Output disabled Pull-up resistor off V _{IN} =V _{SS} (Including output Tr's off leakage current)	2.2 to 5.5	-1			μA
	I _{IL} (2)	XT1, XT2	For input port specification V _{IN} =V _{SS}	2.2 to 5.5	-1			
	I _{IL} (3)	CF1	V _{IN} =V _{SS}	2.2 to 5.5	-15			
High level output voltage	V _{OH} (1)	Ports 0, 1, 2 Ports B, C	I _{OH} =-1mA	4.5 to 5.5	V _{DD} -1			V
	V _{OH} (2)		I _{OH} =-0.4mA	3.0 to 5.5	V _{DD} -0.4			
	V _{OH} (3)		I _{OH} =-0.2mA	2.2 to 5.5	V _{DD} -0.4			
	V _{OH} (4)	P71 to P73	I _{OH} =-0.4mA	3.0 to 5.5	V _{DD} -0.4			
	V _{OH} (5)		I _{OH} =-0.2mA	2.2 to 5.5	V _{DD} -0.4			
	V _{OH} (6)	PWM2, PWM3	I _{OH} =-10mA	4.5 to 5.5	V _{DD} -1.5			
	V _{OH} (7)		I _{OH} =-1.6mA	3.0 to 5.5	V _{DD} -0.4			
	V _{OH} (8)		I _{OH} =-1mA	2.2 to 5.5	V _{DD} -0.4			
Low level output voltage	V _{OL} (1)	Ports 0, 1, 2 Ports B, C PWM2, PWM3	I _{OL} =10mA	4.5 to 5.5			1.5	V
	V _{OL} (2)		I _{OL} =1.6mA	3.0 to 5.5			0.4	
	V _{OL} (3)		I _{OL} =1mA	2.2 to 5.5			0.4	
	V _{OL} (4)	Ports 7, 8 XT2	I _{OL} =1.6mA	3.0 to 5.5			0.4	
	V _{OL} (5)		I _{OL} =1mA	2.2 to 5.5			0.4	
	V _{OL} (6)	P00, P01	I _{OL} =30mA	4.5 to 5.5			1.5	
	V _{OL} (7)		I _{OL} =5mA	3.0 to 5.5			0.4	
	V _{OL} (8)		I _{OL} =2.5mA	2.2 to 5.5			0.4	
Pull-up resistance	R _{pu} (1)	Ports 0, 1, 2, 7	V _{OH} =0.9V _{DD}	4.5 to 5.5	15	35	80	kΩ
	R _{pu} (2)	Ports B, C		2.2 to 5.5	18	50	150	
Hysteresis voltage	V _{HYS}	RES Ports 1, 2, 7		2.2 to 5.5		0.1 V _{DD}		V
Pin capacitance	CP	All pins	For pins other than that under test: V _{IN} =V _{SS} f=1MHz Ta=25°C	2.2 to 5.5		10		pF

Serial Input/Output Characteristics at $T_a = -20^{\circ}\text{C}$ to $+70^{\circ}\text{C}$, $V_{SS1} = V_{SS2} = V_{SS3} = 0\text{V}$

1. SIO0 Serial I/O Characteristics (Note 4-1-1)

Parameter			Symbol	Pin/Remarks	Conditions	V _{DD} [V]	Specification			
							min	typ	max	unit
Serial clock	Input clock	Frequency	tSCK(1)	SCK0(P12)	See Fig. 6.	2.2 to 5.5	2			tCYC
		Low level pulse width	tSCKL(1)				1			
		High level pulse width	tSCKH(1)		1					
			tSCKHA(1)		4					
	Output clock	Frequency	tSCK(2)	SCK0(P12)	• CMOS output selected • See Fig. 6.	2.2 to 5.5	4/3			tSCK
		Low level pulse width	tSCKL(2)				1/2		tCYC	
		High level pulse width	tSCKH(2)		1/2		tSCKH(2) + _(10/3) tCYC			
			tSCKHA(2)		• Continuous data transmission/reception mode • CMOS output selected • See Fig. 6.					
Serial input	Data setup time		tsDI(1)	SB0(P11), SIO(P11)	• Must be specified with respect to rising edge of SIOCLK. • See Fig. 6.	2.2 to 5.5	0.03			
	Data hold time		thDI(1)			2.2 to 5.5	0.03			
Serial output	Input clock	Output delay time	tdD0(1)	SO0(P10), SB0(P11)	• Continuous data transmission/reception mode • (Note 4-1-3)	2.2 to 5.5			(1/3)tCYC +0.05	μs
			tdD0(2)		• Synchronous 8-bit mode • (Note 4-1-3)	2.2 to 5.5			1tCYC +0.05	
	Output clock		tdD0(3)		(Note 4-1-3)	2.2 to 5.5			(1/3)tCYC +0.15	

Note 4-1-1: These specifications are theoretical values. Add margin depending on its use.

Note 4-1-2: To use serial-clock-input in continuous trans / rec mode, a time from SIO0RUN being set when serial clock is "H" to the first negative edge of the serial clock must be longer than tSCKHA.

Note 4-1-3: Must be specified with respect to falling edge of SIOCLK. Must be specified as the time to the beginning of output state change in open drain output mode. See Fig. 6.

2. SIO1 Serial I/O Characteristics (Note 4-2-1)

Parameter			Symbol	Pin/Remarks	Conditions	V _{DD} [V]	Specification			
							min	typ	max	unit
Serial clock	Input clock	Frequency	tSCK(3)	SCK1(P15)	See Fig. 6.	2.2 to 5.5	2			tCYC
		Low level pulse width	tSCKL(3)				1			
		High level pulse width	tSCKH(3)				1			
	Output clock	Frequency	tSCK(4)	SCK1(P15)	• CMOS output selected • See Fig. 6.	2.2 to 5.5	2			tSCK
		Low level pulse width	tSCKL(4)				1/2			
		High level pulse width	tSCKH(4)				1/2			
Serial input	Data setup time		tsDI(2)	SB1(P14), SI1(P14)	• Must be specified with respect to rising edge of SIOCLK. • See Fig. 6.	2.2 to 5.5	0.03			
	Data hold time		thDI(2)			2.2 to 5.5	0.03			
Serial output	Output delay time		tdD0(4)	SO1(P13), SB1(P14)	• Must be specified with respect to falling edge of SIOCLK. • Must be specified as the time to the beginning of output state change in open drain output mode. • See Fig. 6.	2.2 to 5.5			(1/3)tCYC +0.05	μs

Note 4-2-1: These specifications are theoretical values. Add margin depending on its use.

LC87F5864C

Pulse Input Conditions at Ta = -20°C to +70°C, V_{SS1} = V_{SS2} = V_{SS3} = 0V

Parameter	Symbol	Pins/Remarks	Conditions	Specification				
				V _{DD} [V]	min	typ	max	unit
High/low level pulse width	tPIH(1) tPIL(1)	INT0(P70), INT1(P71), INT2(P72), INT4(P20 to P23), INT5(P24 to P27)	• Interrupt source flag can be set. • Event inputs for timer 0 or 1 are enabled.	2.2 to 5.5	1			tCYC
	tPIH(2) tPIL(2)	INT3(P73) when noise filter time constant is 1/1	• Interrupt source flag can be set. • Event inputs for timer 0 are enabled.	2.2 to 5.5	2			
	tPIH(3) tPIL(3)	INT3(P73) when noise filter time constant is 1/32	• Interrupt source flag can be set. • Event inputs for timer 0 are enabled.	2.2 to 5.5	64			
	tPIH(4) tPIL(4)	INT3(P73) when noise filter time constant is 1/128	• Interrupt source flag can be set. • Event inputs for timer 0 are enabled.	2.2 to 5.5	256			
	tPIL(5)	$\overline{\text{RES}}$	Resetting is enabled.	2.2 to 5.5	200			μs

AD Converter Characteristics at Ta = -20°C to +70°C, V_{SS1} = V_{SS2} = V_{SS3} = 0V

Parameter	Symbol	Pins/Remarks	Conditions	Specification				
				V _{DD} [V]	min	typ	max	unit
Resolution	N	AN0(P80) to AN6(P86), AN8(P70), AN9(P71), AN10(XT1), AN11(XT2)		3.0 to 5.5		8		bit
Absolute accuracy	ET		(Note 6-1)	3.0 to 5.5			±1.5	LSB
Conversion time	TCAD		AD conversion time = 32 × tCYC (when ADCR2 = 0) (Note 6-2)	4.5 to 5.5	15.68 (tCYC= 0.49μs)		97.92 (tCYC= 3.06μs)	μs
				3.0 to 5.5	23.52 (tCYC= 0.735μs)		97.92 (tCYC= 3.06μs)	
			AD conversion time = 64 × tCYC (when ADCR2 = 1) (Note 6-2)	4.5 to 5.5	18.82 (tCYC= 0.294μs)		97.92 (tCYC= 1.53μs)	
				3.0 to 5.5	47.04 (tCYC= 0.735μs)		97.92 (tCYC= 1.53μs)	
Analog input voltage range	VAIN			3.0 to 5.5	V _{SS}		V _{DD}	V
Analog port input current	IAINH		VAIN=V _{DD}	3.0 to 5.5			1	μA
	IAINL		VAIN=V _{SS}	3.0 to 5.5	-1			

Note 6-1 : The quantization error (±1/2LSB) is excluded from the absolute accuracy value.

Note 6-2 : The conversion time refers to the interval from the time the instruction for starting the converter is issued till the time the complete digital value corresponding to the analog input value is loaded in the required register.

LC87F5864C

Consumption Current Characteristics at Ta = -20°C to +70°C, VSS1 = VSS2 = VSS3 = 0V

Parameter	Symbol	Pin/ Remarks	Conditions	VDD[V]	Specification			
					min	typ	max	unit
Normal mode consumption current (Note 7-1)	IDDOP(1)	VDD1 =VDD2 =VDD3	• FmCF=12MHz ceramic oscillation mode • FmX'tal=32.768kHz crystal oscillation mode • System clock set to 12MHz side • Internal RC oscillation stopped. • 1/1 frequency division ratio	4.5 to 5.5		8.7	22	mA
	IDDOP(2)			3.0 to 3.6		5	12.5	
	IDDOP(3)		• FmCF=8MHz ceramic oscillation mode • FmX'tal=32.768kHz crystal oscillation mode • System clock set to 8 MHz side • Internal RC oscillation stopped. • 1/1 frequency division ratio	4.5 to 5.5		6.6	16.5	
	IDDOP(4)			3.0 to 3.6		3.8	9.6	
	IDDOP(5)			2.5 to 3.0		2.5	7.4	
	IDDOP(6)		• FmCF=4MHz ceramic oscillation mode • FmX'tal=32.768kHz crystal oscillation mode • System clock set to 4 MHz side • Internal RC oscillation stopped. • 1/2 frequency division ratio	4.5 to 5.5		2.5	6.3	
	IDDOP(7)			3.0 to 3.6		1.4	3.5	
	IDDOP(8)			2.2 to 3.0		0.9	2.7	
	IDDOP(9)		• FmCF=0Hz (oscillation stopped) • FmX'tal=32.768kHz crystal oscillation mode • System clock set to internal RC oscillation • 1/2 frequency division ratio	4.5 to 5.5		0.75	3.1	
	IDDOP(10)			3.0 to 3.6		0.4	1.7	
	IDDOP(11)			2.2 to 3.0		0.28	1.35	
	IDDOP(12)		• FmCF=0Hz (oscillation stopped) • FmX'tal=32.768kHz crystal oscillation mode • System clock set to 32.768kHz side • Internal RC oscillation stopped. • 1/2 frequency division ratio	4.5 to 5.5		35	115	μA
	IDDOP(13)			3.0 to 3.6		18	65	
	IDDOP(14)			2.2 to 3.0		12	46	
HALT mode consumption current (Note 7-1)	IDDHALT(1)		• HALT mode • FmCF=12MHz ceramic oscillation mode • FmX'tal=32.768kHz crystal oscillation mode • System clock set to 12MHz side • Internal RC oscillation stopped. • Frequency variable RC oscillation stopped. • 1/1 frequency division ratio	4.5 to 5.5		3.6	8.2	mA
	IDDHALT(2)			3.0 to 3.6		2	4.6	
	IDDHALT(3)		• HALT mode • FmCF=8MHz ceramic oscillation mode • FmX'tal=32.768kHz crystal oscillation mode • System clock set to 8MHz side • Internal RC oscillation stopped. • Frequency variable RC oscillation stopped. • 1/1 frequency division ratio	4.5 to 5.5		2.6	5.9	
	IDDHALT(4)			3.0 to 3.6		1.4	3.3	
	IDDHALT(5)			2.5 to 3.0		1	2.5	
	IDDHALT(6)		• HALT mode • FmCF=4MHz ceramic oscillation mode • FmX'tal=32.768kHz crystal oscillation mode • System clock set to 4MHz side • Internal RC oscillation stopped. • Frequency variable RC oscillation stopped. • 1/2 frequency division ratio	4.5 to 5.5		1.15	2.65	
	IDDHALT(7)			3.0 to 3.6		0.6	1.5	
	IDDHALT(8)			2.2 to 3.0		0.4	1.1	
	IDDHALT(9)		• HALT mode • FmCF=0Hz (oscillation stopped) • FmX'tal=32.768kHz crystal oscillation mode • System clock set to internal RC oscillation • Frequency variable RC oscillation stopped. • 1/2 frequency division ratio	4.5 to 5.5		0.37	1.3	
	IDDHALT(10)			3.0 to 3.6		0.2	0.75	
	IDDHALT(11)			2.2 to 3.0		0.13	0.54	

Note 7-1 : The consumption current value includes none of the currents that flow into the output Tr and internal pull-up resistors.

Continued on next page.

LC87F5864C

Continued from preceding page.

Parameter	Symbol	Pin/ Remarks	Conditions	Specification				
				V _{DD} [V]	min	typ	max	unit
HALT mode consumption current (Note 7-1)	IDDH _{HALT} (12)	V _{DD1} =V _{DD2} =V _{DD3}	• HALT mode • FmCF=0Hz (oscillation stopped) • FmX'tal=32.768kHz crystal oscillation mode • System clock set to 32.768kHz side • Internal RC oscillation stopped. • Frequency variable RC oscillation stopped. • 1/2 frequency division ratio	4.5 to 5.5		18.5	68	μA
	IDDH _{HALT} (13)			3.0 to 3.6		10	38	
	IDDH _{HALT} (14)			2.2 to 3.0		6.5	26	
HOLD mode consumption current	IDDH _{HOLD} (1)	V _{DD1}	• HOLD mode • CF1=V_{DD} or open (External clock mode)	4.5 to 5.5		0.05	20	
	IDDH _{HOLD} (2)			3.0 to 3.6		0.03	12	
	IDDH _{HOLD} (3)			2.2 to 3.0		0.02	8	
Timer HOLD mode consumption current	IDDH _{HOLD} (4)		• Timer HOLD mode • CF1=V_{DD} or open (External clock mode) • FmX'tal=32.768kHz crystal oscillation mode	4.5 to 5.5		16	58	
	IDDH _{HOLD} (5)			3.0 to 3.6		8.5	32	
	IDDH _{HOLD} (6)			2.2 to 3.0		5	20	

Note 7-1 : The consumption current value includes none of the currents that flow into the output Tr and internal pull-up resistors.

F-ROM Programming Characteristics at Ta = +10°C to +55°C, V_{SS1} = V_{SS2} = V_{SS3} = 0V

Parameter	Symbol	Pin/ Remarks	Conditions	Specification				
				V _{DD} [V]	min	typ	max	unit
Onboard programming current	IDDFW(1)	V _{DD1}	• 128-byte programming • Erasing current included	3.0 to 5.5		25	40	mA
Programming time	tFW(1)		• 128-byte programming • Erasing current included • Time for setting up 128-byte data is excluded.	3.0 to 5.5		22.5	45	ms

UART (Full Duplex) Operating Conditions at Ta = -20°C to +70°C, V_{SS1} = V_{SS2} = V_{SS3} = 0V

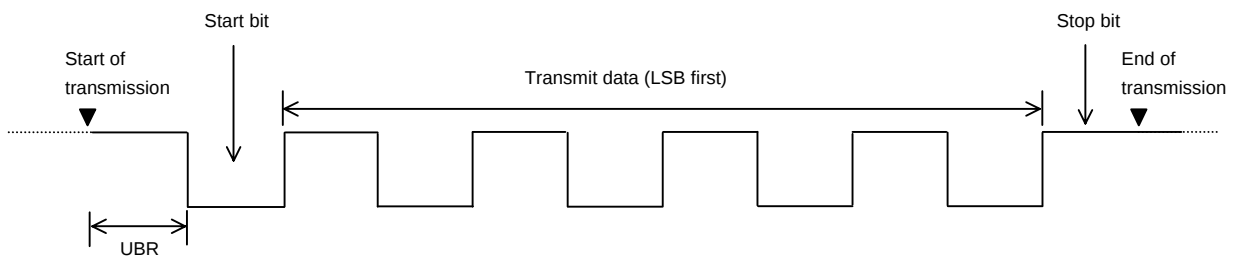
Parameter	Symbol	Pin/Remarks	Conditions	Specification				
				V _{DD} [V]	min	typ	max	unit
Transfer rate	UBR	P20, P21		2.2 to 5.5	16/3		8192/3	tCYC

Data length: 7, 8, and 9 bits (LSB first)

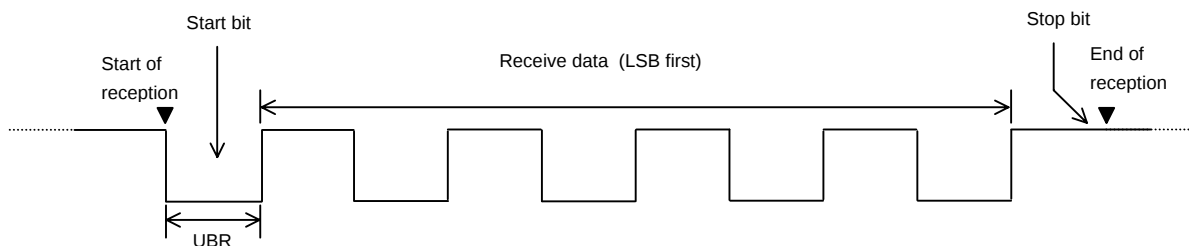
Stop bits: 1 bit (2-bit in continuous data transmission)

Parity bits: None

Example of Continuous 8-bit Data Transmission Mode Processing (first transmit data=55H)



Example of Continuous 8-bit Data Reception Mode Processing (first receive data=55H)



Characteristics of a Sample Main System Clock Oscillation Circuit

Given below are the characteristics of a sample main system clock oscillation circuit that are measured using a SANYO-designated oscillation characteristics evaluation board and external components with circuit constant values with which the oscillator vendor confirmed normal and stable oscillation.

Table 1 Characteristics of a Sample Main System Clock Oscillator Circuit with a Ceramic Oscillator

Nominal Frequency	Vendor Name	Oscillator Name	Circuit Constant				Operating Voltage Range [V]	Oscillation Stabilization Time		Remarks
			C1 [pF]	C2 [pF]	Rf1 [Ω]	Rd1 [Ω]		typ [ms]	max [ms]	
12MHz	MURATA	CSTCE12M0G52-R0	(10)	(10)	Open	470	2.8 to 5.5	0.05	0.15	Internal C1, C2
8MHz	MURATA	CSTCE8M00G52-R0	(10)	(10)	Open	2.2k	2.7 to 5.5	0.05	0.15	Internal C1, C2
		CSTLS8M00G53-B0	(15)	(15)	Open	680	2.5 to 5.5	0.05	0.15	
4MHz	MURATA	CSTCR4M00G53-R0	(15)	(15)	Open	3.3k	2.2 to 5.5	0.05	0.15	Internal C1, C2
		CSTLS4M00G53-B0	(15)	(15)	Open	3.3k	2.2 to 5.5	0.05	0.15	

The oscillation stabilization time refers to the time interval that is required for the oscillation to get stabilized after VDD goes above the operating voltage lower limit (see Figure 4).

Characteristics of a Sample Subsystem Clock Oscillator Circuit

Given below are the characteristics of a sample subsystem clock oscillation circuit that are measured using a SANYO-designated oscillation characteristics evaluation board and external components with circuit constant values with which the oscillator vendor confirmed normal and stable oscillation.

Table 2 Characteristics of a Sample Subsystem Clock Oscillator Circuit with a Crystal Oscillator

Nominal Frequency	Vendor Name	Oscillator Name	Circuit Constant				Operating Voltage Range [V]	Oscillation Stabilization Time		Remarks
			C3 [pF]	C4 [pF]	Rf2 [Ω]	Rd2 [Ω]		typ [s]	max [s]	
32.768kHz	SEIKO EPSON	MC-306	18	18	Open	510k	2.2 to 5.5	1.0	3.0	Applicable CL value =12.5pF

The oscillation stabilization time refers to the time interval that is required for the oscillation to get stabilized after the instruction for starting the subclock oscillation circuit is executed and to the time interval that is required for the oscillation to get stabilized after the HOLD mode is reset (see Figure 4).

Note : The components that are involved in oscillation should be placed as close to the IC and to one another as possible because they are vulnerable to the influences of the circuit pattern.

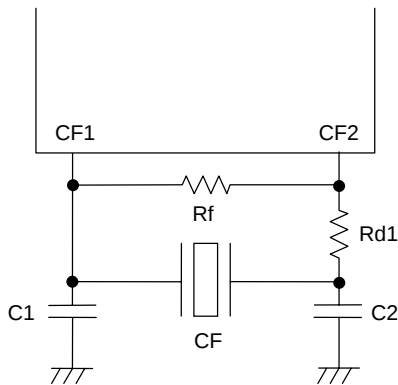


Figure 1 CF Oscillator Circuit

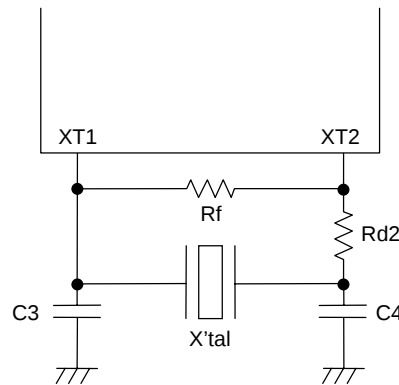


Figure 2 XT Oscillator Circuit

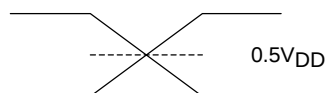
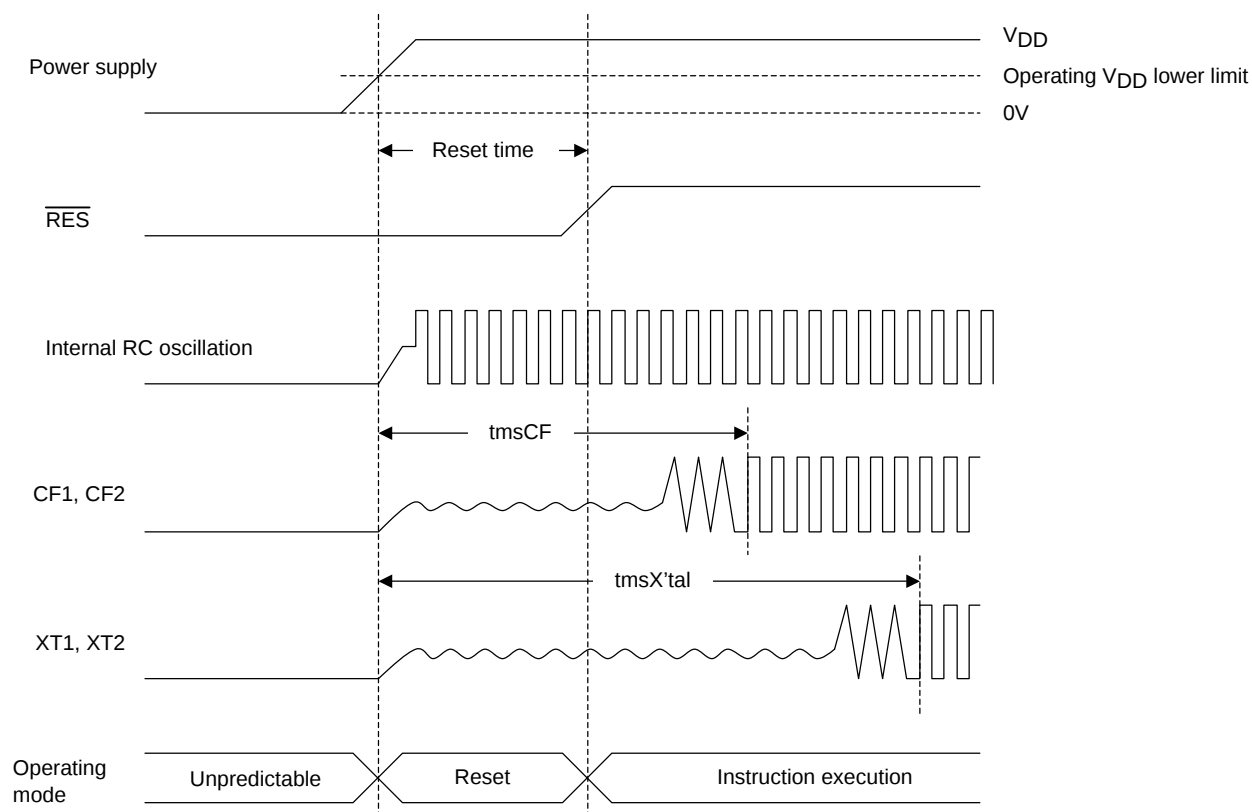
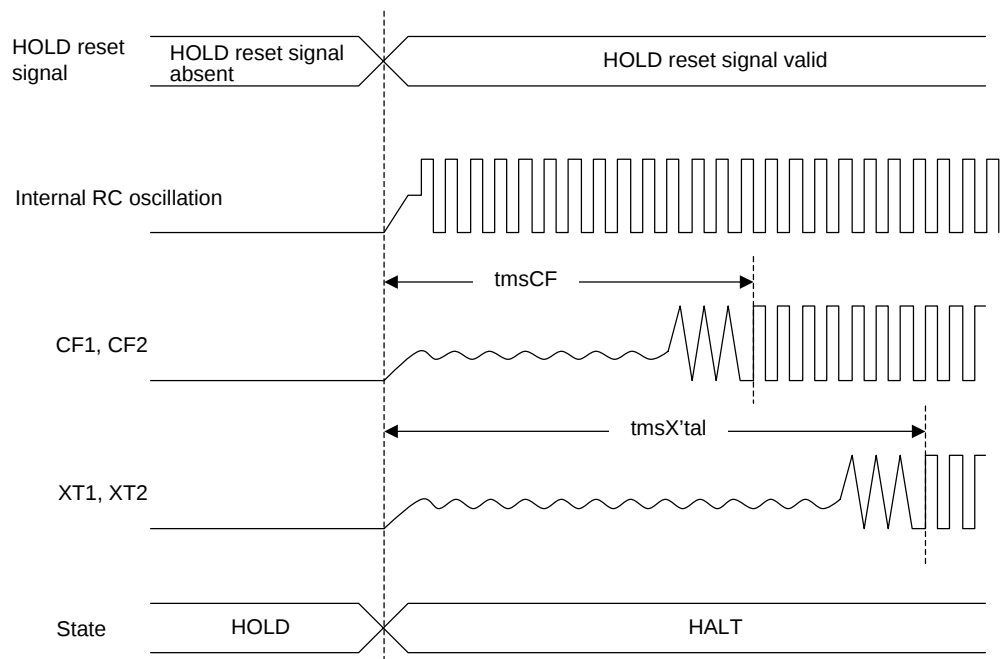


Figure 3 AC Timing Measurement Point

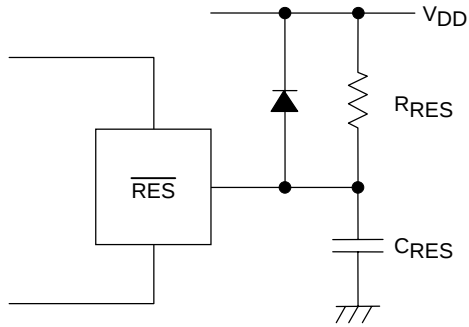


Reset Time and Oscillation Stabilization Time



HOLD Reset Signal and Oscillation Stabilization Time

Figure 4 Oscillation Stabilization Times



Note :

Determine the value of C_{RES} and R_{RES} so that the reset signal is present for a period of $200\mu s$ after the supply voltage goes beyond the lower limit of the IC's operating voltage.

Figure 5 Reset Circuit

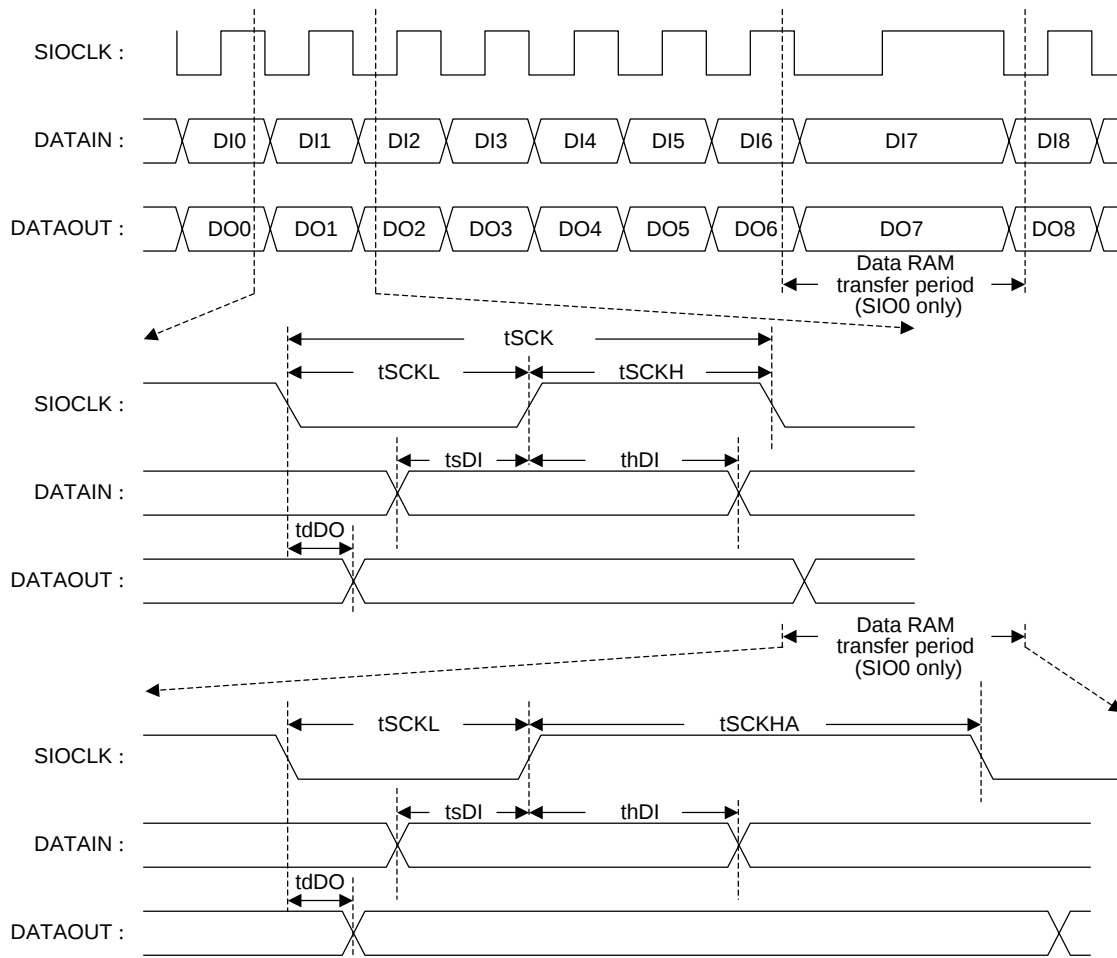


Figure 6 Serial I/O Output Waveforms

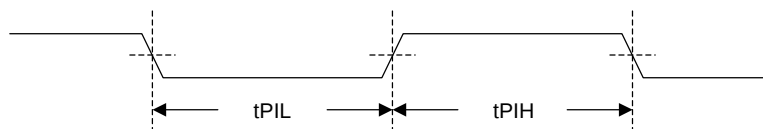


Figure 7 Pulse Input Timing Signal Waveform

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