



SANYO Semiconductors DATA SHEET

LC877816A LC877812A — CMOS IC LC877808A 16K/12K/8K-byte ROM and 512-byte RAM 8-bit 1-chip Microcontroller

Overview

The LC877816A/12A/08A is an 8-bit single chip microcontroller with the following on-chip functional blocks:

- CPU: operable at a minimum bus cycle time of 250ns
- ROM: 16 K/12K/8K bytes
- RAM: 512 × 9 bits
- LCD controller/driver
- 16bit timer × 2ch + 8bit timer × 1ch or more
- Synchronous serial I/O port (with automatic block transmit/receive function)
- Asynchronous/synchronous serial I/O port
- System clock divider
- 8-bit AD converter × 9-channel
- 17-source 10-vectored interrupt system
- Power save mode

All of the above functions are fabricated on a single chip.

Features

■ROM

- 16384 × 8 bits
- 12288 × 8 bits
- 8192 × 8 bits

■RAM

- 512 × 9 bits

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■ Minimum Bus Cycle Time

- 250ns (4MHz)

Note: The bus cycle time indicates ROM read time.

■ Minimum Instruction Cycle Time (tCYC)

- 750ns (4MHz)

■ Power Save Mode

- Power save mode is available, when system clock is RC oscillation or crystal oscillation.

■ Ports

- Input/output ports

Data direction programmable for each bit individually: 12 (P1n, P70 to P73)

Data direction programmable in nibble units: 8 (P0n)

(When N-channel open drain output is selected, data can be input in bit units.)

- LCD ports

Segment output: 24 (S00 to S23)

Common output: 4 (COM0 to COM3)

Bias terminals for LCD driver 5 (V1 to V3, CUP1, CUP2)

Other functions

Input/output ports: 8(PCn)

- Oscillator pins: 4 (CF1, CF2, XT1, XT2)

- Reset pin: 1 (RES)

- Power supply: 4 (VSS1 to 2, VDD1 to 2)
1 (VDC)

■ LCD Controller

- Seven display modes are available.
- Segment output (S16 to S23) can be switched to general purpose input/output ports.
- Duty: 1/3duty, 1/4duty
- Bias: 1/2bias, 1/3bias
- LCD power
 - 1) 1/3bias V1: 1.2V to 1.8V
V2: 2.4V to 3.6V
V3: 3.6V to 5.4V
 - 2) 1/2bias V1: 1.2V to 1.8V
V2: 2.4V to 3.6V
V3: 2.4V to 3.6V
(connect V2 and V3)

■ Timers

- Timer 0: 16 bit timer/counter with capture register
 - Mode 0: 2 channel 8-bit timer with programmable 8 bit prescaler and 8 bit capture register
 - Mode 1: 8 bit timer with 8 bit programmable prescaler and 8 bit capture register
+ 8 bit counter with 8-bit capture register
 - Mode 2: 16 bit timer with 8 bit programmable prescaler and 16 bit capture register
 - Mode 3: 16 bit counter with 16 bit capture register
- Timer 1: PWM/16 bit timer/counter with toggle output function
 - Mode 0: 2 channel 8 bit timer/counter (with toggle output)
 - Mode 1: 2 channel 8 bit PWM
 - Mode 2: 16 bit timer/counter (with toggle output) Toggle output from lower 8 bits is also possible.
 - Mode 3: 16 bit timer (with toggle output) Lower order 8 bits can be used as PWM.
- Timer 4: 8-bit timer with 6-bit prescaler
- Timer 5: 8-bit timer with 6-bit prescaler
- Timer 6: 8-bit timer with 6-bit prescaler (with toggle output)
- Timer 7: 8-bit timer with 6-bit prescaler (with toggle output)

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- Base Timer
 - 1) The clock signal can be selected from any of the following :
Sub-clock (32.768kHz crystal oscillator), system clock, and prescaler output from timer 0
 - 2) Interrupts of five different time intervals are possible.

■SIO

- SIO0: 8 bit synchronous serial interface
 - 1) LSB first/MSB first is selectable
 - 2) Internal 8 bit baud rate generator (fastest clock period 4/3 tCYC)
 - 3) Consecutive automatic data communication (1 to 256 bits)
- SIO1: 8 bit asynchronous/synchronous serial interface
 - Mode 0: Synchronous 8 bit serial I/O (2-wire or 3-wire, transmit clock 2 to 512 tCYC)
 - Mode 1: Asynchronous serial I/O (half duplex, 8 data bits, 1 stop bit, baud rate 8 to 2048 tCYC)
 - Mode 2: Bus mode 1 (start bit, 8 data bits, transmit clock 2 to 512 tCYC)
 - Mode 3: Bus mode 2 (start detection, 8 data bits, stop detection)

■AD Converter:

- 8 bits × 9 channels

■Remote Control Receiver Circuit (connected to P73/INT3/T0IN terminal)

- Noise rejection function (noise rejection filter's time constant can be selected from 1/32/128 tCYC)

■Watchdog Timer

- Watchdog timer can produce interrupt or system reset.
- Watchdog timer has two types.
 - 1) Use an external RC circuit
 - 2) Use the microcontroller's base timer

■Interrupts

- 17 sources, 10 vectors
 - 1) Three priority (low, high and highest) multiple interrupts are supported. During interrupt handling, an equal or lower priority interrupt request is postponed.
 - 2) If interrupt requests to two or more vector addresses occur at once, the higher priority interrupt takes precedence.
In the case of equal priority levels, the vector with the lowest address takes precedence.

No.	Vector Address	Level	Interrupt Source
1	00003H	X or L	INT0
2	0000BH	X or L	INT1
3	00013H	H or L	INT2/T0L
4	0001BH	H or L	INT3/Base timer
5	00023H	H or L	T0H
6	0002BH	H or L	T1L/T1H
7	00033H	H or L	SIO0
8	0003BH	H or L	SIO1
9	00043H	H or L	ADC/T6/T7
10	0004BH	H or L	Port 0/T4/T5

- Priority levels X > H > L
- For equal priority levels, vector with lowest address takes precedence.

■Subroutine Stack Levels

- 256 levels maximum (the stack is allocated in RAM)

■High-speed Multiplication/Division Instructions

- 16 bits × 8 bits (5 tCYC execution time)
- 24 bits × 16 bits (12 tCYC execution time)
- 16 bits ÷ 8 bits (8 tCYC execution time)
- 24 bits ÷ 16 bits (12 tCYC execution time)

■ Oscillation Circuits

- On-chip RC oscillation for system clock use.
- CF oscillation (4MHz) for system clock use. (Rf built in)
- Crystal oscillation (32.768kHz) low speed system clock use. (Rf built in)

■ System Clock Divider Function

- Low power consumption operation is available
- Minimum instruction cycle time (0.75μs, 1.5μs, 3μs, 6μs, 12μs, 24μs, 48μs, 96μs, 192μs can be switched by program (when using 4MHz main clock)

■ Standby Function

- HALT mode: HALT mode is used to reduce power consumption. During the HALT mode, program execution is stopped but peripheral circuits keep operating (some parts of serial transfer operation stop.)
 - 1) Oscillation circuits are not stopped automatically.
 - 2) Released by the system reset or interrupts.
- HOLD mode: HOLD mode is used to reduce power consumption. Program execution and peripheral circuits are stopped.
 - 1) CF, RC and crystal oscillation circuits stop automatically.
 - 2) Released by any of the following conditions.
 - (1) Low level input to the reset pin
 - (2) Specified level input to one of INT0, INT1, INT2
 - (3) Port 0 interrupt
- X'tal HOLD mode: X'tal HOLD mode is used to reduce power consumption. Program execution is stopped. All peripheral circuits except the base timer are stopped.
 - 1) CF and RC oscillation circuits stop automatically.
 - 2) Crystal oscillator operation is kept in its state at HOLD mode inception.
 - 3) Released by any of the following conditions
 - (1) Low level input to the reset pin
 - (2) Specified level input to one of INT0, INT1, INT2
 - (3) Port 0 interrupt
 - (4) Base-timer interrupt

■ Development Tools

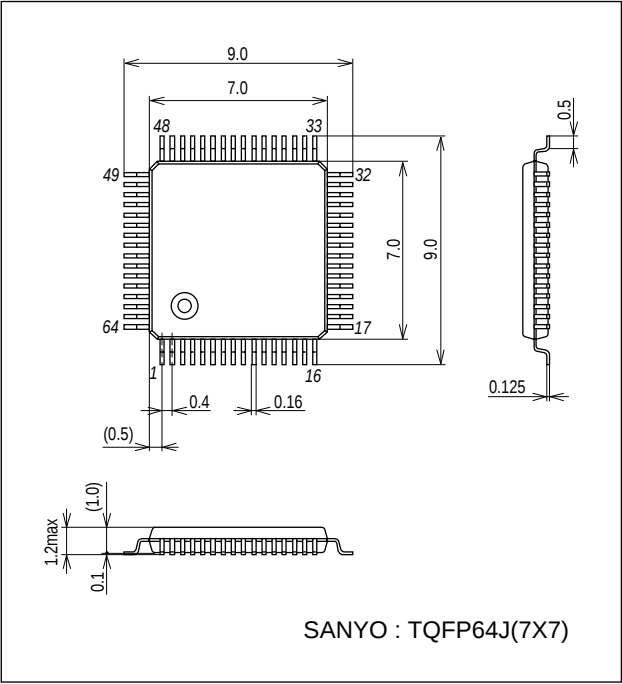
- On chip debugger (LC87F7032A)
LC87F7032A and LC877816A differ in following points.
When LC87F7032A is power save mode, Current consumption doesn't decrease.
When LC87F7032A is power save mode, X'tal voltage level doesn't change.
LC87F7032A has P2 registers (P2, P2DDR). But, LC877816A doesn't have them.

■ Package Form

- TQFP64J(7×7): Lead-free type
- QIP64E(14×14): Lead-free type

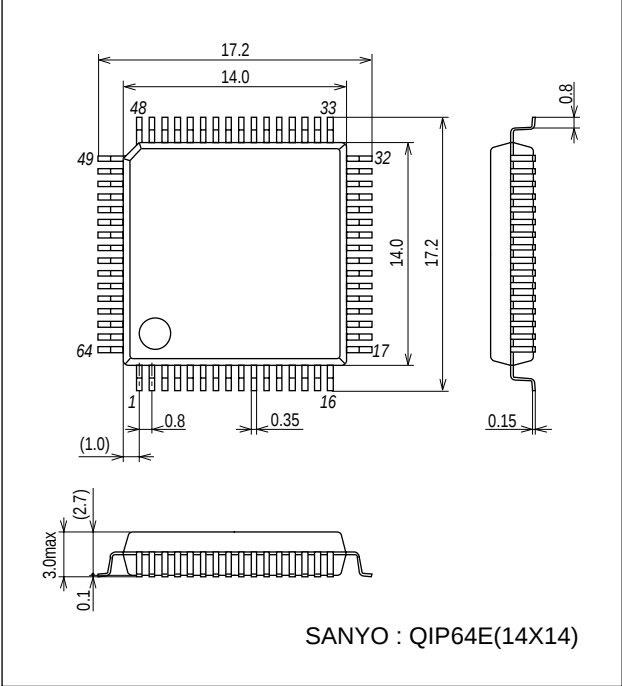
Package Dimensions

unit : mm (typ)
3289



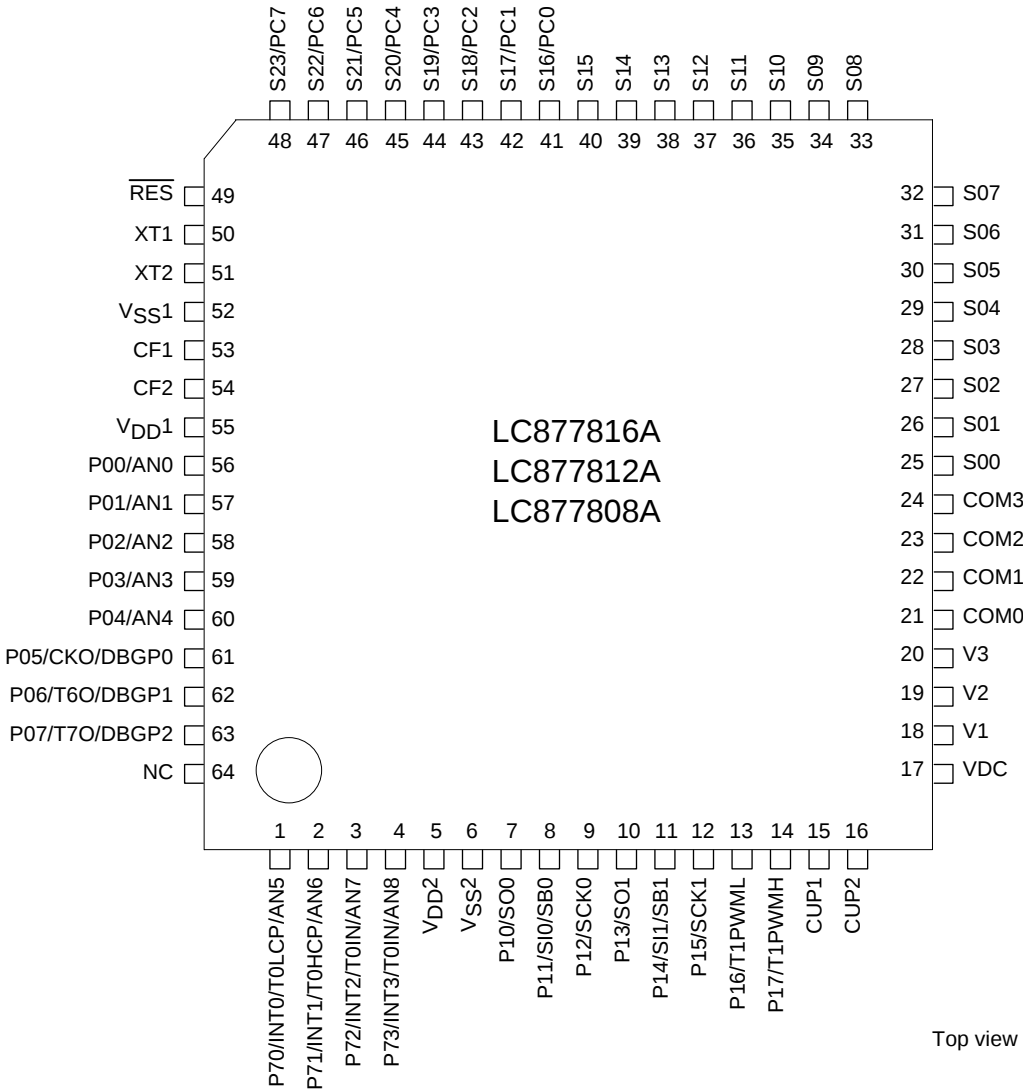
Package Dimensions

unit : mm (typ)
3159A



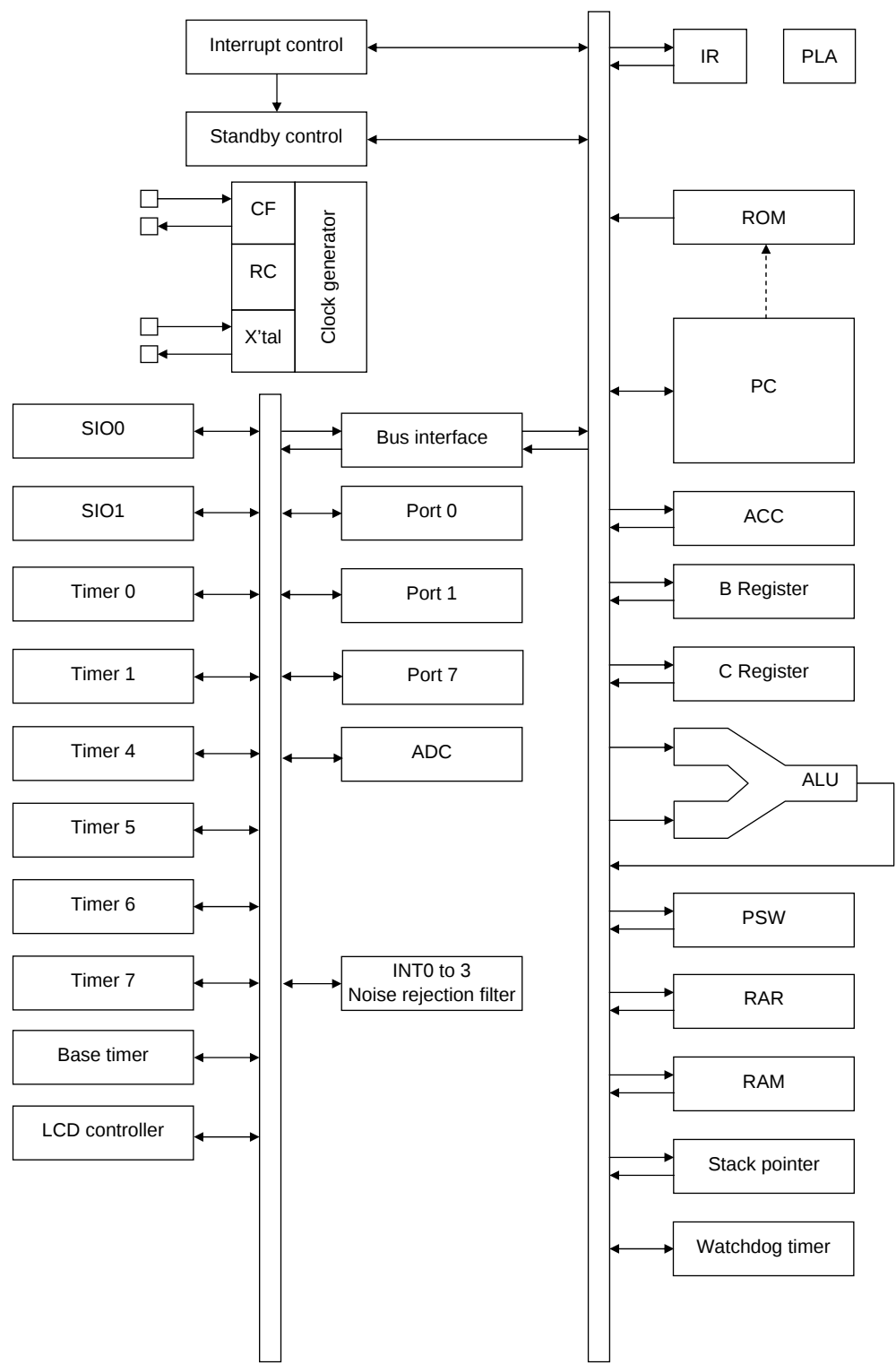
LC877816A/12A/08A

Pin Assignment



SANYO: TQFP64J(7×7) “Lead-free Type”
SANYO: QIP64E(14×14) “Lead-free Type”

System Block Diagram



LC877816A/12A/08A

Pin Description

Pin name	I/O	Function	Option																														
V _{SS} 1, V _{SS} 2	-	- Power supply	No																														
V _{DD} 1, V _{DD} 2	-	+ Power supply	No																														
VDC	-	+ Power supply	No																														
CUP1, CUP2	-	• Capacitor connecting terminals for step-up/step-down	No																														
PORT0 P00 to P07	I/O	• 8bit input/output port • Data direction programmable in nibble units • Use of pull-up resistor can be specified in nibble units • Input for HOLD release • Input for port 0 interrupt • Other pin functions Input for ADC channel (AN0 to AN4) P05: Clock output (system clock/subclock) When it's LC87F7032A, P05 uses as DBGP0. P06: Timer 6 toggle output When it's LC87F7032A, P06 uses as DBGP1. P07: Timer 7 toggle output When it's LC87F7032A, P07 uses as DBGP2.	Yes																														
PORT1 P10 to P17	I/O	• 8bit input/output port • Data direction programmable for each bit • Use of pull-up resistor can be specified for each bit individually • Other pin functions P10: SIO0 data output P11: SIO0 data input or bus input/output P12: SIO0 clock input/output P13: IO1 data output P14: SIO1 data input or bus input/output P15: SIO1 clock input/output P16: Timer 1 PWML output P17: Timer 1 PWMH output/Buzzer output	Yes																														
PORT7 P70 to P73	I/O	• 4bit Input/output port • Data direction can be specified for each bit • Use of pull-up resistor can be specified for each bit individually • Other functions P70: INT0 input/HOLD release input/Timer 0L capture input/output for watchdog timer/AN5 P71: INT1 input/HOLD release input/Timer 0H capture input/AN6 P72: INT2 input/HOLD release input/timer 0 event input/Timer 0L capture input/AN7 P73: INT3 input (noise rejection filter attached)/timer 0 event input/Timer 0H capture input/AN8 Input for ADC channel (AN5 to AN8) • Interrupt acknowledge type <table><tr><td></td><td>Rising</td><td>Falling</td><td>Rising & falling</td><td>H level</td><td>L level</td></tr><tr><td>INT0</td><td>enable</td><td>enable</td><td>disable</td><td>enable</td><td>enable</td></tr><tr><td>INT1</td><td>enable</td><td>enable</td><td>disable</td><td>enable</td><td>enable</td></tr><tr><td>INT2</td><td>enable</td><td>enable</td><td>enable</td><td>disable</td><td>disable</td></tr><tr><td>INT3</td><td>enable</td><td>enable</td><td>enable</td><td>disable</td><td>disable</td></tr></table>		Rising	Falling	Rising & falling	H level	L level	INT0	enable	enable	disable	enable	enable	INT1	enable	enable	disable	enable	enable	INT2	enable	enable	enable	disable	disable	INT3	enable	enable	enable	disable	disable	No
	Rising	Falling	Rising & falling	H level	L level																												
INT0	enable	enable	disable	enable	enable																												
INT1	enable	enable	disable	enable	enable																												
INT2	enable	enable	enable	disable	disable																												
INT3	enable	enable	enable	disable	disable																												
S0 to S15	O	• Segment output for LCD	No																														
S16/PC0 to S23/PC7	I/O	• Segment output for LCD • Can be used as general purpose input/output port (PC)	No																														
COM0 to COM3	O	• Common output for LCD	No																														
V1 to V3	I/O	• LCD output bias power supply • Capacitor connecting terminals for step-up/step-down	No																														
RES	I	• Reset terminal	No																														
XT1	I	• Input for 32.768kHz crystal oscillation • When not in use, connect to V_{DD}2	No																														
XT2	I/O	• Output for 32.768kHz crystal oscillation • When not in use, set to oscillation mode and leave open	No																														
CF1	I	• Input terminal for ceramic oscillator • When not in use, connect to V_{DD}2	No																														
CF2	O	• Output terminal for ceramic oscillator • When not in use, leave open	No																														

Port Output Types

Port form and pull-up resistor options are shown in the following table.

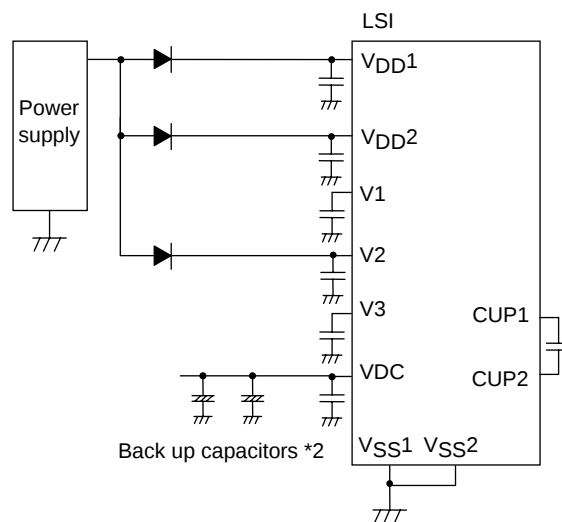
Port status can be read even when port is set to output mode.

Port Name	Option Selected in Units of	Option Type	Output Type	Pull-up Resistor
P00 to P07	1 bit	1	CMOS	Programmable(Note 1)
		2	Nch-open drain	No
P10 to P17	1 bit	1	CMOS	Programmable
		2	Nch-open drain	Programmable
P70	-	No	Nch-open drain	Programmable
P71 to P73	-	No	CMOS	Programmable
S16(PC0) to S23(PC7)	-	1	CMOS	No
		2	Pch-open drain	
		3	Nch-open drain	

Note 1: Attachment of Port0 programmable pull-up resistors is controllable in nibble units (P00 to 03, P04 to 07).

*1: Connect as follows to reduce noise on VDD.

VSS1 and VSS2 must be connected together and grounded.



*2: The power supply for the internal memory is VDC. VDD1 and VDD2 are used as the power supply for ports.

When VDD1 and VDD2 are not backed up, the port level does not become “H” even if the port latch is in the “H” level. Therefore, when VDD1 and VDD2 are not backed up and the port latch is “H” level, the port level is unstable in the HOLD mode, and the back up time becomes shorter because the through current runs from VDD to GND in the input buffer. If VDD1 and VDD2 are not backed up, output “L” by the program or pull the port to “L” by the external circuit in the HOLD mode so that the port level becomes “L” level and unnecessary current consumption is prevented.

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Absolute Maximum Ratings at Ta = 25°C, VSS1 = VSS2 = 0V

Parameter	Symbol	Pin/Remarks	Conditions	VDD[V]	Specification			
					min	typ	max	unit
Supply voltage	VDD max	VDD1, VDD2, V2	VDD1=VDD2=V2		-0.3		+4.3	V
Supply voltage For LCD	VLCD	V1			-0.3		1/2 VDD	
		V2			-0.3		VDD	
		V3			-0.3		3/2 VDD	
Input voltage	VI	XT1, CF1, RES			-0.3		VDD+0.3	
Input/Output voltage	VI/O(1)	• Ports 0, 1, 7, C			-0.3		VDD+0.3	
High level output current	Peak output current	IOPH(1)	Ports 0, 1, 7, C • CMOS output selected • Current at each pin		-4			mA
	Total output current	ΣIOAH(1)	Port 7	Total of all pins	-10			
		ΣIOAH(2)	Port 0	Total of all pins	-25			
		ΣIOAH(3)	Port 1	Total of all pins	-25			
		ΣIOAH(4)	Port C	Total of all pins	-15			
Low level output current	Peak output current	IOPL(1)	Ports 02 to 07 Port 1, 7, C	Current at each pin			6	
		IOPL(2)	Port 00, 01	Current at each pin			15	
	Total output current	ΣIOAL(1)	Port 7	Total of all pins			10	
		ΣIOAL(2)	Port 0	Total of all pins			35	
		ΣIOAL(3)	Port 1	Total of all pins			25	
		ΣIOAL(4)	Port C	Total of all pins			15	
Allowable power dissipation	Pd max	TQFP64J(7×7)	Ta=-30 to +70°C				200	mW
		QIP64E(14×14)					420	
Operating ambient temperature	Topr				-30		+70	°C
Storage ambient temperature	Tstg				-55		+125	

Note 1-1: The average current per applicable pin must not exceed 1mA

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Allowable Operating Conditions at Ta = -30°C to +70°C, VSS1 = VSS2 = 0V

Parameter	Symbol	Pin/Remarks	Conditions	Specification				
				VDD	min	typ	max	unit
Operating supply voltage range	VDD(1)	VDD1=VDD2=V2 Normal mode	0.37μs≤tCYC≤200μs		3.0		3.6	V
	VDD(2)		0.75μs≤tCYC≤200μs		2.4		3.6	
	VDD(3)	VDD1=VDD2=V2	2.25μs≤tCYC≤200μs		3.0		3.6	
	VDD(4)	Power save mode	4.28μs≤tCYC≤200μs		2.4		3.6	
Supply voltage range in Hold mode	VHD	VDD1=VDD2=V2	Keep RAM and register data in HOLD mode.		2.2		3.6	
Input high voltage	VIH(1)	• Ports 1 • P71 to P73 • Port 70 input/interrupt	Output disable	2.4 to 3.6	0.3VDD +0.7		VDD	
	VIH(2)	• Ports 0, C	Output disable	2.4 to 3.6	0.3VDD +0.7		VDD	
	VIH(3)	Port 70 Watchdog timer	Output disable	2.4 to 3.6	0.9VDD		VDD	
	VIH(4)	XT1, CF1, RES		2.4 to 3.6	0.75VDD		VDD	
Input low Voltage	VIL(1)	• Ports 1 • P71 to P73 • Port 70 input/interrupt	Output disable	2.4 to 3.6	VSS		0.2VDD	
	VIL(2)	• Ports 0, C	Output disable	2.4 to 3.6	VSS		0.2VDD	
	VIL(3)	Port 70 Watchdog timer	Output disable	2.4 to 3.6	VSS		0.8VDD -1.0	
	VIL(4)	XT1, CF1, RES		2.4 to 3.6	VSS		0.25VDD	
Operation cycle time	tCYC (Note 2-1)		Power save mode	3.0 to 3.6	2.25		200	μs
				2.4 to 3.6	4.28		200	
External system clock frequency	FEXCF(1)	CF1	• CF2 open • System clock divider:1/1 • External clock DUTY=50 ± 5% • Normal mode	2.4 to 3.6	0.1		4	MHz
Oscillation frequency range (Note 2-2)	FmCF	CF1, CF2	4MHz ceramic resonator oscillation See fig. 1	2.4 to 3.6		4		MHz
	FmRC		RC oscillation VDD=3.0V, Ta=25°C	2.4 to 3.6	300	500	700	kHz
	FsX'tal	XT1, XT2	32.768kHz crystal resonator oscillation See fig. 2	2.4 to 3.6		32.768		kHz

Note 2-1: Relationship between tCYC and oscillation frequency is 3/FmCF at a division ratio 1/1 and 6/FmCF at a division ratio of 1/2.

Note 2-2: See Table 1 and 2 for the oscillation constants.

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Electrical Characteristics at Ta = -30°C to +70°C, VSS1 = VSS2 = 0V

Parameter	Symbol	Pin/Remarks	Conditions	VDD[V]	Specification			
					min	typ	max	unit
High level input current	I _{IH} (1)	• Ports 0, 1, 7 • Port C • $\overline{\text{RES}}$	• Output disabled • Pull-up resistor OFF. • V _{IN} =V _{DD} (including OFF state leak current of the output Tr.)	2.4 to 3.6			1	μA
	I _{IH} (2)	XT1, XT2	When configured as an input port V _{IN} =V _{DD}	2.4 to 3.6			1	
	I _{IH} (3)	CF1	V _{IN} =V _{DD}	2.4 to 3.6			8	
Low level input current	I _{IL} (1)	• Ports 0, 1, 7 • Port C • $\overline{\text{RES}}$	• Output disabled • Pull-up resistor OFF. • V _{IN} =V _{SS} (including OFF state leak current of the output Tr.)	2.4 to 3.6	-1			μA
	I _{IL} (2)	XT1, XT2	When configured as an input port V _{IN} =V _{SS}	2.4 to 3.6	-1			
	I _{IL} (3)	CF1	V _{IN} =V _{SS}	2.4 to 3.6	-8			
High level output voltage	V _{OH} (1)	Ports 0, 1, 7 CMOS output option	I _{OH} =-0.4mA	3.0 to 3.6	V _{DD} -0.4			V
			I _{OH} =-0.2mA	2.4 to 3.6	V _{DD} -0.4			
	V _{OH} (2)	Port C	I _{OH} =-0.1mA	2.4 to 3.6	V _{DD} -0.4			
Low level output voltage	V _{OL} (1)	Ports 0, 1, 7	I _{OL} =1.6mA	3.0 to 3.6			0.4	
			I _{OL} =0.8mA	2.4 to 3.6			0.4	
	V _{OL} (2)	P00, P01	I _{OL} =5.0mA	3.0 to 3.6			0.4	
			I _{OL} =2.5mA	2.4 to 3.6			0.4	
	V _{OL} (3)	Port C	I _{OL} =0.1mA	2.4 to 3.6			0.4	
LCD output voltage regulation	VODLS	S0 to S23	I _O =0mA V1, V2, V3 LCD level output	2.4 to 3.6	0		±0.2	V
	VODLC	COM0 to COM3	I _O =0mA V1, V2, V3 LCD level output	2.4 to 3.6	0		±0.2	
Resistance of pull-up MOS Tr.	Rpu	• Ports 0, 1, 7	V _{OH} =0.9V _{DD}	2.4 to 3.6	25	50	200	kΩ
Hysteresis voltage	VHYS	• Ports 1, 7 • $\overline{\text{RES}}$		2.4 to 3.6		0.1 ×V _{DD}		V
Pin capacitance	CP	All pins	• All other terminals connected to V _{SS} . • F=4MHz • Ta=25°C	2.4 to 3.6		10		pF

Serial I/O Characteristics at Ta = -30°C to +70°C, V_{SS1} = V_{SS2} = 0V

1. SIO0 Serial I/O Characteristics (Note 4-1-1)

Parameter			Symbol	Pin/Remarks	Conditions	V _{DD}	Specification			
							min	typ	max	unit
Serial clock	Input clock	Frequency	tSCK(1)	SCK0(P12)	See Fig. 6.	2.4 to 3.6	2			tCYC
		Low level pulse width	tSCKL(1)		1					
		High level pulse width	tSCKH(1)		1					
			tSCKHA(1)		4					
	Output clock	Frequency	tSCK(2)	SCK0(P12)	• CMOS output selected • See Fig. 6.	2.4 to 3.6	4/3			tSCK
		Low level pulse width	tSCKL(2)		1/2					
		High level pulse width	tSCKH(2)		1/2					
			tSCKHA(2)		• Continuous data transmission/reception mode • CMOS output selected • See Fig. 6.		tSCKH(2) +2tCYC		tSCKH(2) +(10/3) tCYC	tCYC
Serial input	Data setup time		tsDI(1)	SB0(P11), SIO(P11)	• Must be specified with respect to rising edge of SIOCLK. • See Fig. 6.	2.4 to 3.6	0.03			
	Data hold time		thDI(1)			2.4 to 3.6	0.03			
Serial output	Input clock	Output delay time	tdD0(1)	SO0(P10), SB0(P11)	• Continuous data transmission/reception mode • (Note 4-1-3)	2.4 to 3.6			(1/3)tCYC +0.05	μs
			tdD0(2)		• Synchronous 8-bit mode • (Note 4-1-3)	2.4 to 3.6			1tCYC +0.05	
	Output clock		tdD0(3)		• (Note 4-1-3)	2.4 to 3.6				

Note 4-1-1: These specifications are theoretical values. Add margin depending on its use.

Note 4-1-2: To use serial-clock-input in continuous trans/rec mode, a time from SIO₀RUN being set when serial clock is "H" to the first negative edge of the serial clock must be longer than tSCKHA.

Note 4-1-3: Must be specified with respect to falling edge of SIOCLK. Must be specified as the time to the beginning of output state change in open drain output mode. See Fig. 6.

2. SIO1 Serial I/O Characteristics (Note 4-2-1)

Parameter		Symbol	Pin/Remarks	Conditions	V _{DD}	Specification			
						min	typ	max	unit
Serial clock	Input clock	Frequency	SCK1(P15)	See Fig. 6.	2.4 to 3.6	2			tCYC
		Low level pulse width				1			
		High level pulse width				1			
	Output clock	Frequency	SCK1(P15)	- CMOS output selected - See Fig. 6.	2.4 to 3.6	2			tSCK
		Low level pulse width				1/2			
		High level pulse width				1/2			
Serial input	Data setup time	tsDI(2)	SB1(P14), SI1(P14)	- Must be specified with respect to rising edge of SIOCLK. - See Fig. 6.	2.4 to 3.6	0.03			
	Data hold time	thDI(2)			2.4 to 3.6	0.03			
Serial output	Output delay time	tdD0(4)	SO1(P13), SB1(P14)	- Must be specified with respect to falling edge of SIOCLK. - Must be specified as the time to the beginning of output state change in open drain output mode. - See Fig. 6.	2.4 to 3.6			(1/3)tCYC + 0.05	μs

Note 4-2-1: These specifications are theoretical values. Add margin depending on its use.

Pulse Input Conditions at Ta = -30°C to +70°C, V_{SS1} = V_{SS2} = 0V

Parameter	Symbol	Pin/Remarks	Conditions	V _{DD} [V]	Specification			
					min	typ	max	unit
High/low level pulse width	tPIH(1) tPIL(1)	INT0(P70), INT1(P71), INT2(P72)	- Condition that interrupt is accepted - Condition that event input to timer 0 is accepted	2.4 to 3.6	1			tCYC
	tPIH(2) tPIL(2)	INT3(P73) (Noise rejection ratio is 1/1.)	- Condition that interrupt is accepted - Condition that event input to timer 0 is accepted	2.4 to 3.6	2			
	tPIH(3) tPIL(3)	INT3(P73) (Noise rejection ratio is 1/32.)	- Condition that interrupt is accepted - Condition that event input to timer 0 is accepted	2.4 to 3.6	64			
	tPIH(4) tPIL(4)	INT3(P73) (Noise rejection ratio is 1/128.)	- Condition that interrupt is accepted - Condition that event input to timer 0 is accepted	2.4 to 3.6	256			
	tPIL(5)	RES	Condition that reset is accepted	2.4 to 3.6	200			μs

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AD Converter Characteristics at Ta = -30°C to +70°C, VSS1 = VSS2 = 0V

Parameter	Symbol	Pin/Remarks	Conditions	Specification				
				V _{DD} [V]	min	typ	max	unit
Resolution	N	AN0(P00) to AN4(P04), AN5(P70) to AN8(P73)		2.4 to 3.6		8		bit
Absolute accuracy	ET		(Note 6-1)	2.4 to 3.6			±1.5	LSB
Conversion time	tCAD		AD conversion time=32×tCYC (ADCR2=0) (Note 6-2) Normal mode	3.0 to 3.6	22.4 (tCYC=0.70μs)		640 (tCYC=20μs)	μs
				2.4 to 3.6	128 (tCYC=4.00μs)		640 (tCYC=20μs)	
			AD conversion time=32×tCYC (ADCR2=0) (Note6-2) Power save mode	2.4 to 3.6	128 (tCYC=4.00μs)		640 (tCYC=20μs)	
			AD conversion time=64×tCYC (When ADCR2=1) (Note 6-2) Normal mode	3.0 to 3.6	44.8 (tCYC=0.70μs)		1280 (tCYC=20μs)	
				2.4 to 3.6	256 (tCYC=4.00μs)		1280 (tCYC=20μs)	
			AD conversion time=32×tCYC (ADCR2=0) (Note6-2) Power save mode	2.4 to 3.6	256 (tCYC=4.00μs)		1280 (tCYC=20μs)	
Analog input voltage range	VAIN			2.4 to 3.6	V _{SS}		V _{DD}	V
Analog port input current	IAINH		VAIN=V _{DD}	2.4 to 3.6			1	μA
	IAINL		VAIN=V _{SS}	2.4 to 3.6	-1			

Note 6-1: The quantization error ($\pm 1/2\text{LSB}$) is excluded from the absolute accuracy value.

Note 6-2: The conversion time refers to the interval from the time the instruction for starting the converter is issued till the time the complete digital value corresponding to the analog input value is loaded in the required register.

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Consumption Current Characteristics at Ta = -30°C to +70°C, VSS1 = VSS2 = 0V

Parameter	Symbol	Pins/ Remarks	Conditions	Specification				
				VDD[V]	min	typ	max	unit
Current consumption during normal operation (Note 7-1)	IDDOP(1)	VDD1=VDD2=V2	- FmCF=4MHz Ceramic resonator oscillation - FsX'tal=32.768kHz crystal oscillation - System clock: CF 4MHz oscillation - Internal RC oscillation stopped. - Divider: 1/1 - Normal mode	2.4 to 3.6		1100	3200	μA
	IDDOP(2)		- FmCF=0Hz (No oscillation) - FsX'tal=32.768kHz crystal oscillation - System clock: RC oscillation - Divider: 1/1 - Normal mode	2.4 to 3.6		150	600	
	IDDOP(3)		- FmCF=0Hz (No oscillation) - FsX'tal=32.768kHz crystal oscillation - System clock: RC oscillation - Divider: 1/1 - Power save mode	2.4 to 3.6		50	225	
	IDDOP(4)		- FmCF=0Hz (No oscillation) - FsX'tal=32.768kHz crystal oscillation - System clock: RC oscillation - Divider: 1/2 - Power save mode	2.4 to 3.6		40	180	
	IDDOP(5)		- FmCF=0Hz (No oscillation) - FsX'tal=32.768kHz crystal oscillation - System clock: 32.768kHz - Internal RC oscillation stopped. - Divider: 1/1 - Normal mode	2.4 to 3.6		15	60	
	IDDOP(6)		- FmCF=0Hz (No oscillation) - FsX'tal=32.768kHz crystal oscillation - System clock: 32.768kHz - Internal RC oscillation stopped. - Divider: 1/1 - Power save mode	2.4 to 3.6		2.5	17	
	IDDOP(7)		- FmCF=0Hz (No oscillation) - FsX'tal=32.768kHz crystal oscillation - System clock: 32.768kHz - Internal RC oscillation stopped. - Divider: 1/2 - Power save mode	2.4 to 3.6		1.5	15	
Current consumption during HALT mode (Note 7-1)	IDDHALT(1)		HALT mode - FmCF=4MHz Ceramic resonator oscillation - FsX'tal=32.768kHz crystal oscillation - System clock: CF 4MHz oscillation - Internal RC oscillation stopped. - Divider: 1/1 - Normal mode	2.4 to 3.6		460	1600	
	IDDHALT(2)		HALT mode - FmCF=0H (Oscillation stop) - FsX'tal=32.768kHz crystal oscillation - System clock: RC oscillation - Divider: 1/1 - Normal mode	2.4 to 3.6		50	300	
	IDDHALT(3)		HALT mode - FmCF=0H (Oscillation stop) - FsX'tal=32.768kHz crystal oscillation - System clock: RC oscillation - Divider: 1/1 - Power save mode	2.4 to 3.6		35	150	

Note 7-1: The currents through the output transistors and the pull-up MOS transistors are ignored.

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Parameter	Symbol	Pins/ Remarks	Conditions	Specification				
				V _{DD} [V]	min	typ	max	unit
Current consumption during HALT mode (Note 7-1)	IDDHALT(4)	V _{DD1} = V _{DD2} = V2	HALT mode • FmCF=0H (Oscillation stop) • FsX'tal=32.768kHz crystal oscillation • System clock: RC oscillation • Divider: 1/2 • Power save mode	2.4 to 3.6		30	135	μA
	IDDHALT(5)		HALT mode • FmCF=0Hz (Oscillation stop) • FsX'tal=32.768kHz crystal oscillation • System clock: 32.768kHz • Internal RC oscillation stopped. • Divider: 1/1 • Normal mode	2.4 to 3.6		7.0	60	
	IDDHALT(6)		HALT mode • FmCF=0Hz (Oscillation stop) • FsX'tal=32.768kHz crystal oscillation • System clock: 32.768kHz • Internal RC oscillation stopped. • Divider: 1/1 • Power save mode	2.4 to 3.6		1.0	15	
	IDDHALT(7)		HALT mode • FmCF=0Hz (Oscillation stop) • FsX'tal=32.768kHz crystal oscillation • System clock: 32.768kHz • Internal RC oscillation stopped. • Divider: 1/2 • Power save mode	2.4 to 3.6		0.8	14	
HOLD mode consumption current	IDDHOLD(1)		HOLD mode • CF1=V _{DD} or open (when using external clock)	2.4 to 3.6		0.03	30	
Timer HOLD mode consumption current (Note 7-1)	IDDHOLD(2)		Date/time clock HOLD mode • CF1=V _{DD} or open (when using external clock) • FmX'tal=32.768kHz crystal oscillation • Internal RC oscillation stopped. • Divider: 1/1 • Normal mode	2.4 to 3.6		5.0	45	
	IDDHOLD(3)		Date/time clock HOLD mode • CF1=V _{DD} or open (when using external clock) • FmX'tal=32.768kHz crystal oscillation • Internal RC oscillation stopped. • Divider: 1/1 • Power save mode	2.4 to 3.6		0.5	15	

Note 7-1: The currents through the output transistors and the pull-up MOS transistors are ignored.

Main System Clock Oscillation Circuit Characteristics

The characteristics in the table below is based on the following conditions:

Use the standard evaluation board SANYO has provided.

Use the peripheral parts with indicated value externally.

The peripheral parts value is a recommended value of oscillator manufacturer

Table 1. Main system clock oscillation circuit characteristics using ceramic resonator

Frequency	Manufacturer	Type	Oscillator	Circuit parameters			Operating supply voltage range[V]	Oscillation stabilizing time		Notes
				C1 [pF]	C2 [pF]	Rd [Ω]		typ [ms]	max [ms]	
4.00MHz	Murata	SMD	CSTCR4M00G53-R0	(15)	(15)	1k	2.4 to 3.6	0.2	0.6	Internal C1, C2
		Lead	CSTLS4M00G53-B0	(15)	(15)	2.2k	2.4 to 3.6	0.2	0.6	

The oscillation stabilizing time is a period until the oscillation becomes stable after V_{DD} becomes higher than minimum operating voltage. (See Fig. 4)

Subsystem Clock Oscillation Circuit Characteristics

The characteristics in the table below is based on the following conditions:

Use the standard evaluation board SANYO has provided.

Use the peripheral parts with indicated value externally.

The peripheral parts value is a recommended value of oscillator manufacturer

Table 2. Subsystem clock oscillation circuit characteristics using crystal oscillator

Frequency	Manufacturer	Oscillator	Circuit parameters				Operating supply voltage range [V]	Oscillation stabilizing time		Notes
			C3 [pF]	C4 [pF]	Rf [Ω]	Rd2 [Ω]		typ [s]	max [s]	
32.768kHz	Epson Toyocom	MC-146	10	10	Open	0	2.4 to 3.6	1	3	Applicable CL value = 12.5pF

The oscillation stabilizing time is a period until the oscillation becomes stable after executing the instruction which starts the sub-clock oscillation or after releasing the HOLD mode. (See Fig. 4)

Notes: Since the circuit pattern affects the oscillation frequency, place the oscillation-related parts as close to the oscillation pins as possible with the shortest possible pattern length.

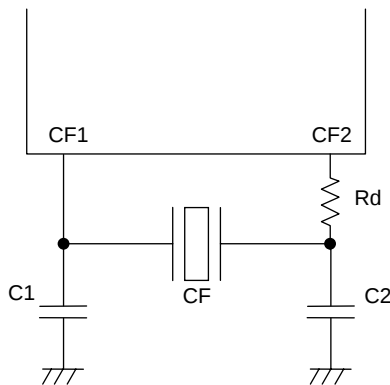


Figure 1 Ceramic Oscillation Circuit

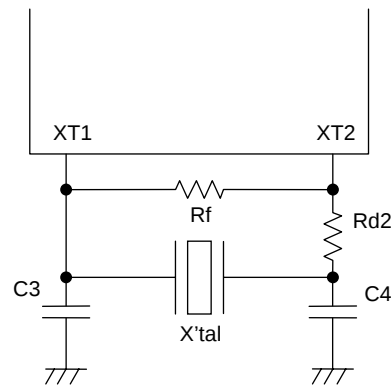


Figure 2 Crystal Oscillation Circuit

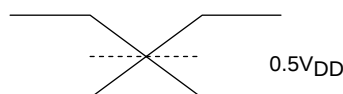
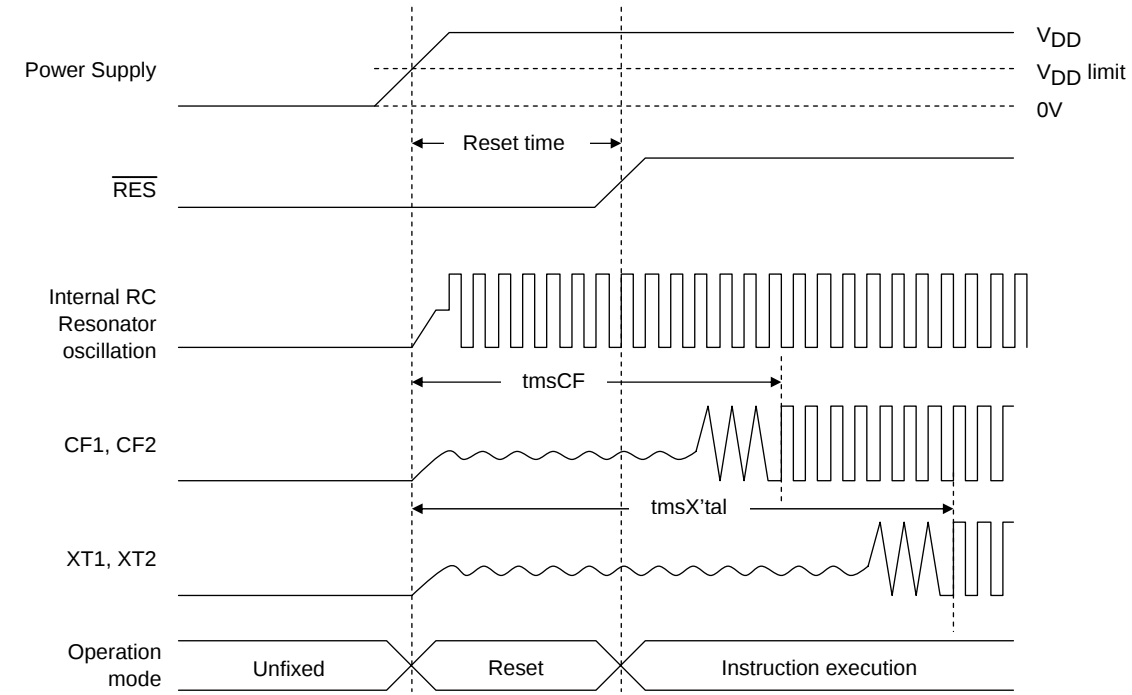
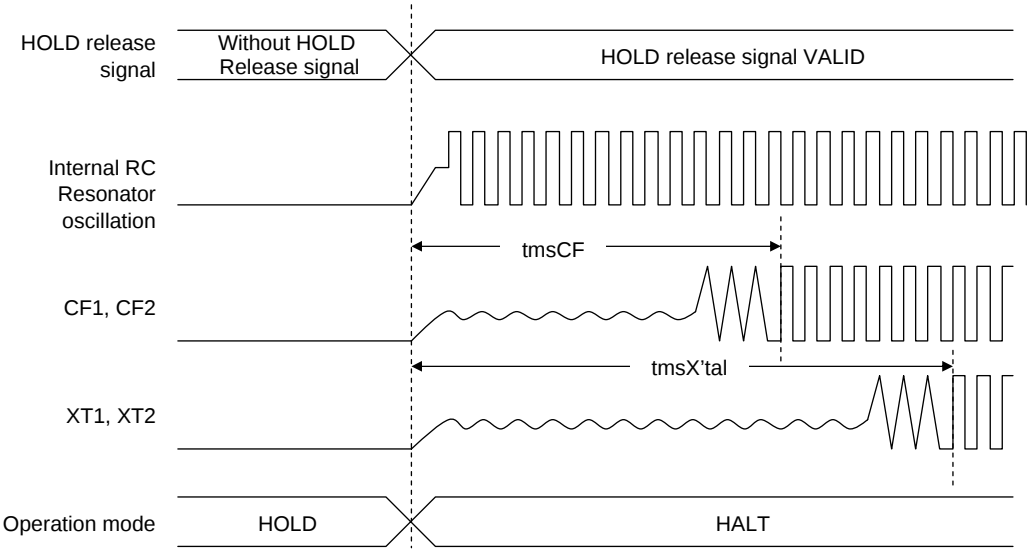


Figure 3 AC Timing Measurement Point

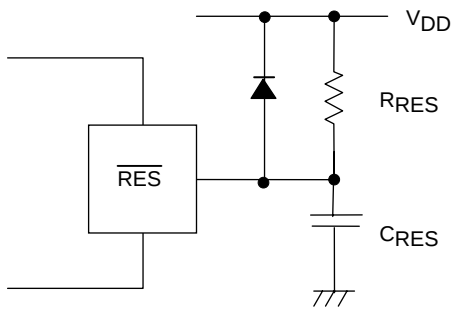


Reset Time and Oscillation Stabilization Time



HOLD Release Signal and Oscillation Stabilization Time

Figure 4 Oscillation Stabilizing Time



Note:
Select C_{RES} and R_{RES} value to assure that at least $200\mu s$ reset time is generated after the V_{DD} becomes higher than the minimum operating voltage.

Figure 5 Reset Circuit

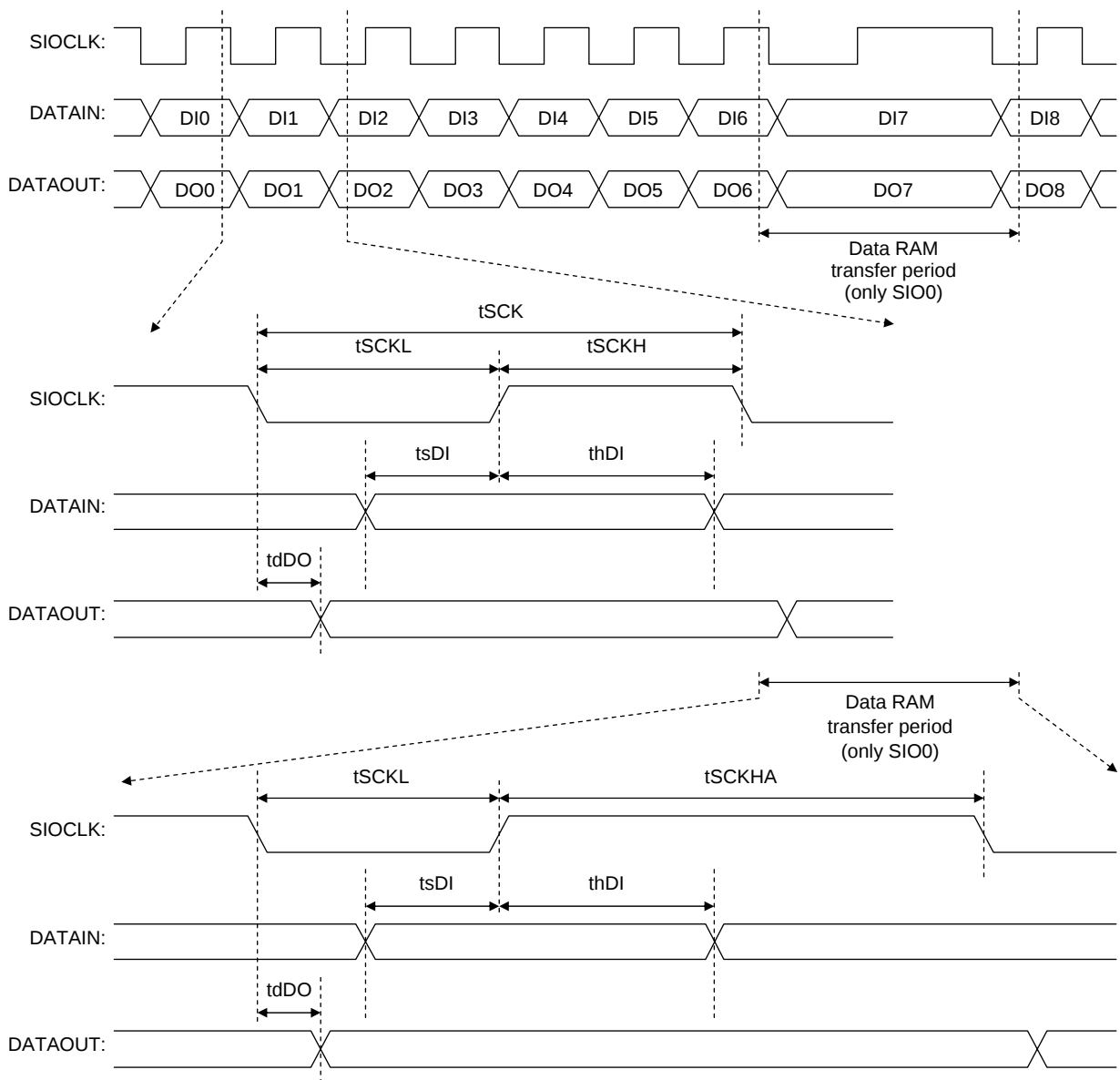


Figure 6 Serial I/O Waveforms

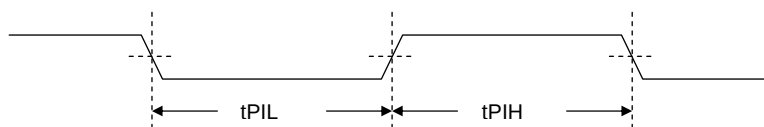


Figure 7 Pulse Input Timing Signal Waveform

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