CMOS LSI

LC86P4564



One-time PROM built-in 8-bit Single Chip Microcontroller

Preliminary

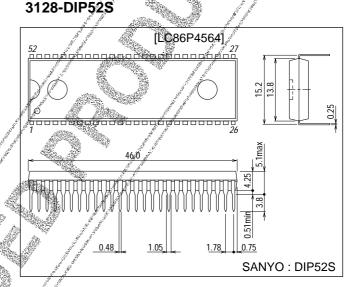
Overview

The LC86P4564 is a CMOS 8-bit single chip microcontroller with One-time PROM for the LC864500 series.

This microcontroller has the function and the pin assignment identical to those of the LC864500 series mask ROM version, and has the built-in 64K-byte PROM.

Package Dimensions

unit : mm



Features

- (1) Options switchable by PROM data The option functions of the LC864500 series can be specified by the PROM data. The functions of the trial pieces can be evaluated using mass production board.
- 65512 bytes (For program) (2) Internal PROM capacity
 - 8192 × 12 bits (For character)
- 256 bytes (3) Internal RAM capacity The LC86P4564 contains a 65512 byte PROM and a 256 byte RAM. Each size is the maximum capacity of the LC86P4564 mask-ROM series. de la company

	Mask ROM version	ROM capacity	RAM capacity
	LC864532	32768 bytes	256 bytes
	LC864528	28672 bytes	256 bytes
	LC864524	24576 bytes	256 bytes
	LC864520	20480 bytes	256 bytes
	LC864516	16384 bytes	256 bytes
and the second se	LC864512	12288 bytes	256 bytes
	LC864508	8192 bytes	256 bytes
Tree to	TO THE AT I S		

- (4) Operating supply voltage
- : 4.5 V to 5.5 V
- (5) Instruction cycle tinfe : 1.0 µs to 366 µs
- (6) Operating temperature
- : $-30^{\circ}C$ to $+70^{\circ}C$ The pin and the package compatible with the LC864500 series mask ROM version
- (7) (8)Applicable mask ROM version

- : LC864532/LC864528/LC864524/LC864520/LC864516/LC864512/LC864508 : DIP52S
- (9) Factory shipment

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Usage Notes

When using, take note of the followings.

(1) Differences between the LC86P4564 and the LC864500 series

Item	LC86P4564	LC864532/28/24/20/46/12/08
Operation after reset releasing	The option must be set internally within 3 ms after a high-level signal is applied to the reset terminal. In this period options are switched gradually, and after that, the program is executed from 00H of the program counter.	The program is executed from 00H of the program counter as soon as a high-level signal is applied to the reset terminal.
Operating supply voltage range (V_{DD})	4.5 V to 5.5 V	2.5 V to 6.0 V
Current drain under normal operation	Refer to 'electrical characteristics' on the semie	onductor news

Port format of the LC86P4564 during the reset is identical to that of the LC864533/28/24/20/16/12/08. The LC86P4564 uses 256-byte spaces addressed 0FF00H to 0FFFH in the program memory to set options. In this way, all options of the LC864500 series cannot be executed.

Some of the LC864500 series options, which the LC86P4564 can support are as shown in the table below.

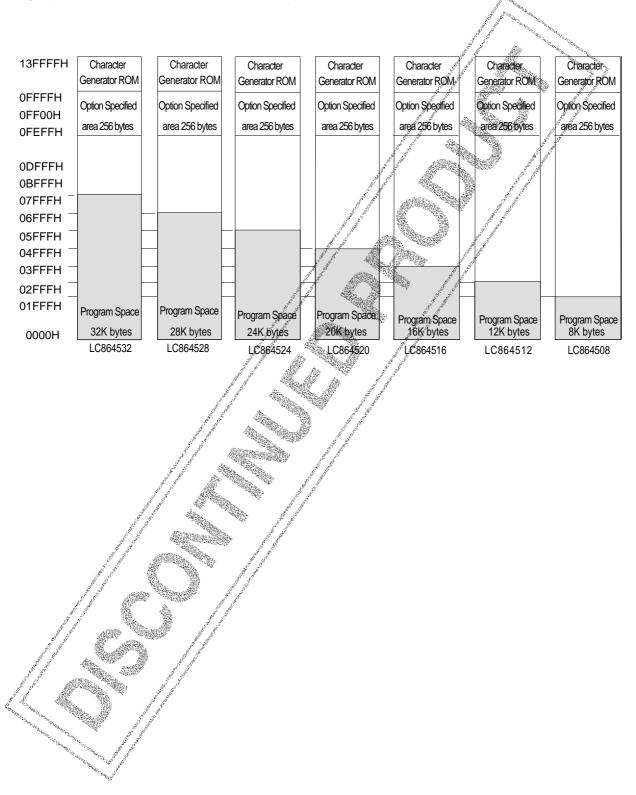
LC86P4564 options

Option types	Pins, circuits
Input/output specifications of input/output ports	Port 0 1. N-channel open-drain output 2. CMOS output *1
	1. Pull-up MOS transistor provided 2. Pull-up MOS transistor not provided
	Port 1 // Input : Programmable pull-up MOS transistor Output : N-channel open drain
	2. Input : Programmable pull-up MOS transistor Output : CMOS
Pull-up MOS transistor of	Fort 7 1. Pull-up MOS transistor not provided.
input port.	2. Pull-up MOS transistor provided.

- *1) Specified in bit units
- *2) When the "CMOS output" is selected as an output format, the pull-up MOS transistor will be provided, and when the "nchannel open-drain output" is selected, the pull-up MOS transistor will not be provided.
- (2) Option setting program The option data is written with the option specifying program "SU86K.EXE". The option data is linked to the program area by the linkage loader "L86K.EXE".

(3) ROM space

The LC86P4564 and LC864500 series use 256 bytes addressed on 0FF00H to 0FFFFH in the program memory as the option specified data area. The program memory capacity of the series is 65280 bytes addressed on 0000H to 0FEFFH. Note that the capacity of the LC86P4564 user-available PROM is 32768 bytes addressed on 0000H to 7FFFH, because the maximum ROM capacity of the LC864500 series ROM version is 32 K byte.



How to Use

(1) Create a programming data for LC86P4564

Programming data for PROM of the LC86P4564 is required.

Debugged evaluation file (EVA file) must be converted to an INTEL-HEX formatted file (HEX file) with file converter program EVA2HEX.EXE. The HEX file is used as the programming data for the LC86P4564.

(2) How to program for the PROM The LC86P4564 can be programmed by the general purpose EPROM programmer with an attachment; W86EP4564D

• Recommended EPROM programmers are as shown in the table below.

Manufacturer	EPROM programmer
Advantest	R4945, R4944
Andou	AF-9704
AVAL	PKW-1100, PKW-3000
Minato electronics	MODEL1890A

• The "27010 (Vp-p = 12.5 V) Intel high speed programming" mode requires to be used for writing. The storage area addressed "0 to 13FFFH" requires to be selected for address setting and the jumper (DASEC) must be set to 'OFF' at programming.

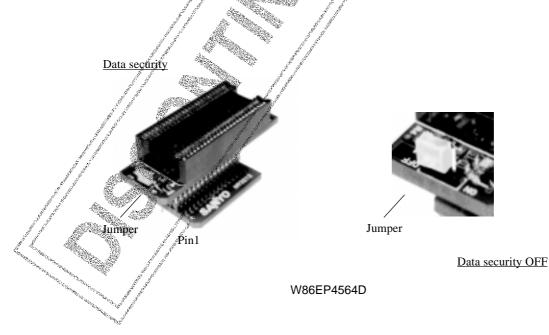
(3) How to use the data security function

"Data security" is the function to prevent the EPROM data from being read out.

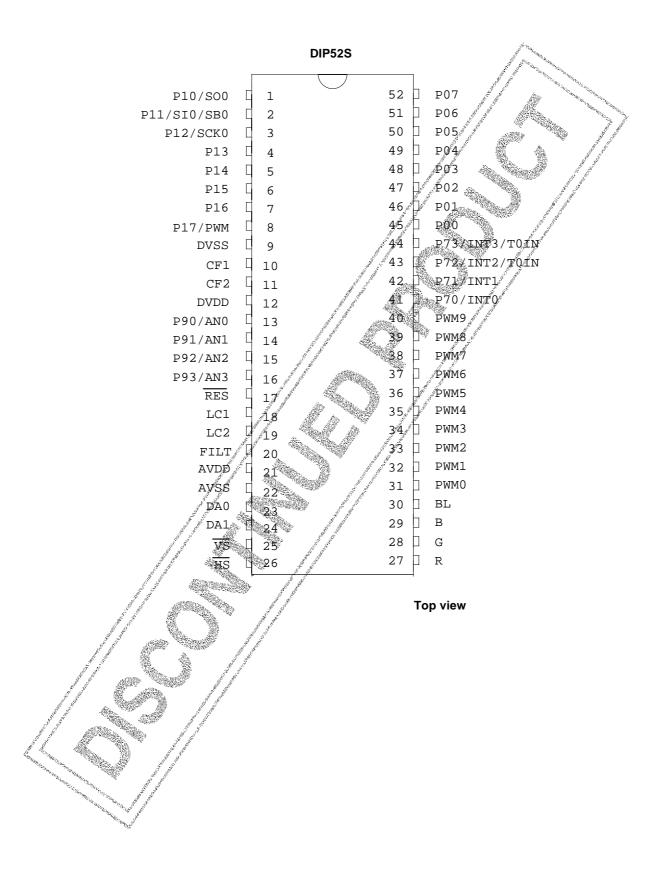
- The following is the process in order to execute the data security.
- 1. Set the jumper of attachment 'ON'.
- 2. Program again. The EPROM programmer will display an error. The error indication means normal activity of the data security. It does not mean a trouble of the EPROM programmer or the LSI.

Notes

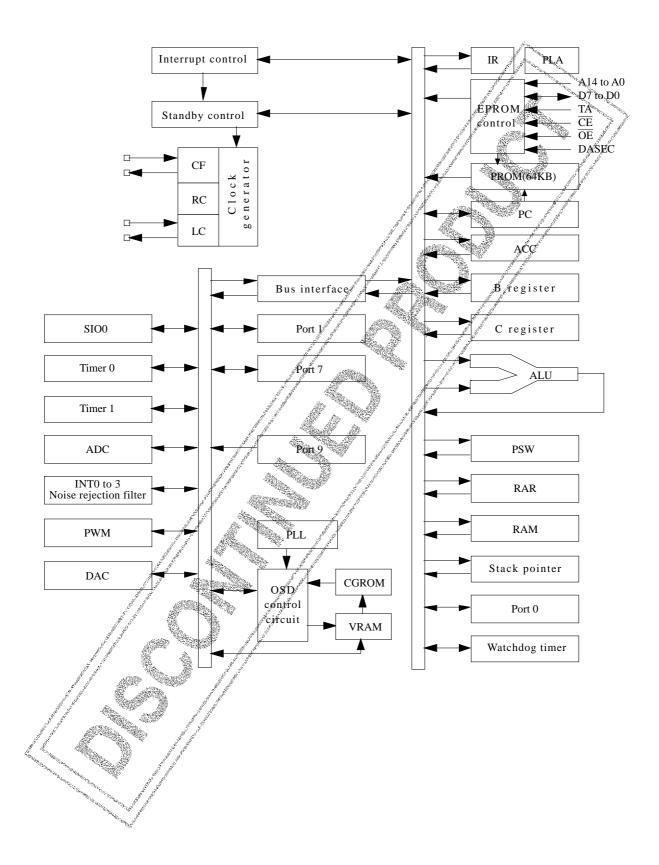
- Data security is not executed when the data of all address have 'FF' at sequence 2 above.
- Data security cannot be executed by programming the sequential operation "BLANK=>PROGRAM=>VERIFY" at sequence 2 above.
- Set the jumper 'OFF' after executing the data security



Pin Assignment



System Block Diagram



Pin Description

Pin Description Table

Pin name	Pin No.	I/O	Function description	Option	PROM mode
DVSS	9	_	Negative power supply for digital circuit	j.	
CF1	10	Ι	Input for ceramic oscillator	م م ^ع لو الم	and the second sec
CF2	11	0	Output for ceramic oscillator		A second se
DVDD	12	—	Positive power supply for digital circuit		2 Nr. 77
RES	17	I	Reset	// <i>@</i>	
LC1	18	I	LC oscillation circuit input	// a.R	San Alexander II.
LC2	19	0	LC oscillation circuit output		
FILT	20	0	Filter for PLL		
AVDD	21	—	Positive power supply for analog circuit	1/ 200	set and the set of the
AVSS	22	_	Negative power supply for analog circuit	11 400 348	Jo and a second s
DA0	23	I/O	DA0 output/General purpose I/O port		Ç.
DA1	24	I/O	DA1 output/General purpose I/O port	/ .as. Not //	ी
VS	25	Ι	Vertical synchronization signal input	<u> 2205 //</u>	
HS	26	I	Horizontal synchronization signal input	1/ 1.00 March 1/	
R	27	0	Red (R) output of RGB image output		A4 (*1)
G	28	0	Green (G) output of RGB image output	- ****** //	A5 (*1)
В	29	0	Blue (B) output of RGB image output	N //	A6 (*1)
BL	30	0	Fast blanking control signal TV image signal or OSD image signal selecting	le se	A7 (*1)
PWM0 to PWM9	31 to 40	0	PWM0 to PWM9 output 15V withstand	and the second sec	PWM 0 to PWM 8 : A8 to A16 (*1) PWM 9 : fixed to "L"
Port0			8-bit Input/output port	Pull-up resistor	
P00 to P07	45 to 52	I/O	Input/output can be specified in nibble units HØLD release input Interrupt input	provided/not provided Output Format CMOS/Nch-OD	
Port1		and a start	8-bit Input/output port		D0 to D7 (*2)
P10 to P17	1 to 8	10	Input/output can be specified in bit units. Other functions P10 SIO0 data output P11 SIO0 data input /bus input/output P12 SIO0 clock input/output P17 Timer 1 (PWM) output	Output Format CMOS/Nch-OD	
			and the second sec		

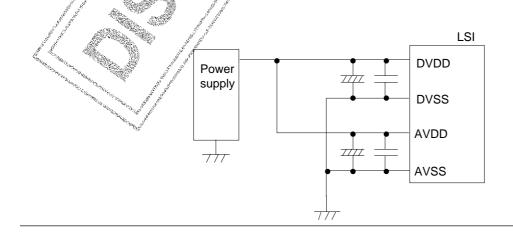
Terminal	No.	I/O		Functio	on descriptio	n	Op	otion	PROM mode
Port7			4-bit i	nput port			Pull-up re	esistor	P70 : VPP (*3)
P70	41	I/O	Other	function			provided	/	P71 : DASEC (*4)
P71 to P73	42 to 44	I	P70	INT0 input/l	HOLD releas	se input/	not provi	ded	P72 : OE (*5)
				n-ch transist	tor output for	watchdog timer	(in bit un	its)	P73:CE (*6)
			P71	INT1 input/I	HOLD releas	e input	`	,	
				•	imer 0 even	•			
				•	noise rejecti	•		, and a second se	
					out/timer 0 e			AL AND A	
					format vecto			and the second	
				Rise	Fall	Rise/Fall	H level	Lievel	Vector
				Rise	Fall	RISE/Fall	n ievei		
			INT0	enable	enable	disable	enable	enable	03H
			INT1	enable	enable	disable	enable 🤞	enable	OBH
			INT2	enable	enable	enable	disable 🦯	disable	13₩
			INT3	enable	enable	enable	disable	disable	1BH
Port9			4-bit i	hput port		<u>ا</u> ا	and the set		A0 to A3 (*1)
P90 to P93	13 to 16	1	Other	function			/ 《		
1 30 10 1 93	131010				ut port (4 lin	ee) (20			and a second
			ADC	uverter inp				utilityet.	je je

- *1 An \rightarrow Address input
- *2 Data I/O
- *3 Power for programming
- *4 Memory select input/output for data security
- *5 Output enable input
- *6 Chip enable input
- All of port options except the pull-up resistor option of Port 0 can be specified in bit units.
- When the "CMOS output" is selected for port 0 as an output format, the pull-up resistor will be provided, and when the "n-channel open-drain output" is selected, the pull-up resistor will not be provided.
- Whichever the "CMOS" or the "n-channel open-drain" output format is selected, the programmable pull-up resistor will be provided.

· Port states during reset

		S S AND MARKA
Terminal	I/O	/Pull-up resistor status at selecting pull-up option
Port 0	Input	Pull-up resistor OFF, ON after reset release
Port 1	Input	Programmable pull-up resistor OFF
Port 7	Input	Eixed pull-up resistor provided
	and a state	X X 1/

* AVDD and AVSS are the power supply terminals for the analog operation block. DVDD and DVSS are the power supply terminals for the digital operation block. Connect as shown in the following figure to reduce the mutual noise influence.



Specifications

1. Absolute Maximum Ratings at Ta = 25° C, V_{SS} = 0 V

Para	meter	Symbol	Pins	Conditions		and the second	Ratings	5	Unit
					V _{DD} [V]	min /	typ	max	
Supply vo	oltage	V _{DD} max	DVDD, AVDD	DVDD = AVDD		-0.3	Â	+7.0	V
Input volta	age	V _I (1)	• P71, 72, 73 • Port 9 • RES, HS, VS		and the second	-0.3		V _{DD} +0.3	Ì
Output vo	oltage	V _O (1)	R, G, B, BL, FILT		and the second	~0.3	10.10	V _{D0} +0.3	
		V _O (2)	PWM0 to PWM9		/ 8	-0.3	ě.	+15	
Input/outp voltage	out	V _{IO} (1)	Ports 0, 1, P70 DA0, 1			-0.3	and the second sec	V _{DD} +0.3	
High- level output	Peak output current	I _{ОРН} (1)	Ports 0, 1	Pull-up MOS transistor output At each pin		-2	y de la constante de la consta		mA
current		I _{OPH} (2)	Ports 0, 1 DA0, 1	CMOS output At each pin	n strader. Refer	4			
		I _{ОРН} (3)	R, G, B, BL	CMOS output At each pin		-5			
	Total	ΣI_{OAH} (1)	Port 1	The total of all pins	a start and a start and a start	-10			
	output current	∑I _{OAH} (2)	Port 0	The total of all pins	e and a second	-10			
	current	ΣI_{OAH} (3)	R, G, B, BL	The total of all pins	e ^{llente}	-15			
Low-	Peak	I _{OPL} (1)	Ports 0, 1 DA0, 1	At each pin				20	
level output	output current	I _{OPL} (2)	P70	At each pin				30	
current	current	I _{OPL} (3)	R, G, B, BL PWM0 to PWM9	At each pin				5	
	Total	ΣI_{OAL} (1)	Port 0	The total of all pins				40	
	output current	ΣI_{OAL} (2)	Port 1, P70	The total of all pins				40	
	ourroint	ΣI _{OAL} (3)	R, G, B, BL	The total of all pins				15	
		ΣI_{OAL} (4)	PWM0 to PWM9	The total of all pins				30	
Allowable dissipatio	•	Pd max	DIP52S	Ta = −30 to +70°C				430	mW
Operating temperatu range		Topr	3//			-30		+70	°C
Storage temperatu range	ure set and the set of	Tstg				-55		+150	

The same level voltage must be applied to both DVSS and AVSS. The same level voltage must be applied to both DVDD and AVDD.

 $V_{SS} = DVSS = AVSS$ $V_{DD} = DVDD = AVDD$

2. Allowable Operating Range at Ta = -30° C to $+70^{\circ}$ C, V_{SS} = 0 V

Parameter	Symbol	Pins	Conditions			Ratings	3	Unit
				V _{DD} [V]	min	typ	max	
Operating supply voltage range	V _{DD}	DVDD, AVDD	0.98 μs ≤ tCYC tCYC ≤ 1.02 μs		4,5	and the second	5.5	V
Hold voltage	Vhd	DVDD, AVDD	RAMs and the registers held at HOLD mode.		2.0		5.5	
High-level input	V _{IH} (1)	Port 0 (Schmitt)	Output disable	4.5 to 5.5	0.6V _{DD}		Убр	
voltage	V _{IH} (2)	• Port 1 (Schmitt) • <u>P72, 73</u> • HS, VS	Output disable	4.5 to 5.5	0.75V∰		AND YOD	
	∨ін(3)	P70 port input / interrupt <u>P71</u> RES (Schmitt)	Output n-channel transistor OFF	4.5 to 5.5	0.75¥бо	and the second second	VDD	
	Vін(4)	P70 Watchdog timer input	Output n-channel transistor OFF	4.5 to 5.5	VDD-0.5	<u>.</u>	Vdd	
	V _{IH} (5)	Port 9 DA0, 1 port input		4.5 to 5.5	0.7 V _{DD}		V _{DD}	
Low-level input	Vı∟(1)	Port 0 (Schmitt)	Output disable	4.5 to 5.5	Vss		0.2V _{DD}	
voltage	V _{IL} (2)	Port 1 (Schmitt) P72, 73 HS, VS Port 9 Port 9	Output disable	4.5 to 5.5	Vss		0.25V _{DD}	
	Vı∟(3)	P70 port input / interrupt P71 RES (Schmitt)	N-channel-transistor OFF	4.5 to 5.5	Vss		0.25V _{DD}	
	VIL(4)	P70 Watchdog timer input	N-channel transistor OFF	4.5 to 5.5	Vss		0.6V _{DD}	
	V _{IL} (5)	Port 9 DA0, 1 Port input	and the second se	4.5 to 5.5	Vss		$0.3V_{DD}$	
Operation	tCYC(1)		OSD function	4.5 to 5.5	0.98	1	1.02	μs
cycle time	tCYC(2)	destrongen /	No OSD function	4.5 to 5.5	0.98		30	

LC86P4564

Parameter	Symbol	Pin	Conditions			Ratings		Unit
				V _{DD} [V]	min	typ	max	
Oscillation frequency range (Note 1)	FmCF	CF1, CF2	12 MHz (ceramic resonator oscillation) Refer to Figure 1	4.5 to 5.5	11.76	12	12.24	MHz
	FmLC	LC1, LC2	14.11 MHz (LC oscillation) Refer to Figure 2	4.5 to 5.5	and the second second	14.11	A MERCENCE AND A MERCENCE	
	FmRC		RC oscillation	4.5 to 5.5	0.4	0.8	2:0	Con Marine
Oscillation stable time period (Note 2)	tmsCF	CF1, CF2	12 MHz (ceramic resonator oscillation) Refer to Figure 3	4.5 to 5.5		0.02) 0.2 ⁴	ms

(Note 1) Refer to Table 1 and Table 2 for the oscillation constant.

(Note 2) The oscillation stable time is a period necessary for the oscillation to be stable after the power first applied, the HOLD mode released and the main-clock oscillation stop instruction released. Refer to the Figure 3 for details.

3. Electrical Characteristics at Ta = -30° C to $+70^{\circ}$ C , V_{SS} = 0 V

Parameter	Symbol	Pins	Conditions			Rating	3	Unit
				V _{DD} [V]	min	typ	max	
Input high- level current	l _{iH} (1)	 Port 1 DA0, 1 Port 0 without pull-up MOS transistor 	 Output disable Pull-up MOS transistor OFF V_{IN} = V_{DD} (including the off-leakage current of the output transistor) 	4.5 to 5.5	and a second sec		1	μA
	I _{IH} (2)	 Port 7 without pull-up MOS transistor Port 9 RES HS, VS 	VIN = VDD	4,5 to 5.5			and a second sec	
Input Iow- Ievel current	I _{IL} (1)	 Port 1 DA0, 1 Port 0 without pull-up MOS transistor 	Output disable Pull-up MOS transistor OFF VIN = VSS (including the offs leakage current of the output transistor)	4.5.10 5.5	-10 ⁰			
	I _{IL} (2)	Port 7 without pull-up MOS transistor Port 9	V _{IN} = V _{SS}	4.5 to 5.5	-1			
	l _{IL} (3)	• RES • HS, VS	V _{IN} ⇒ Vss	4.5 to 5.5	-1			
Output high- level voltage	V _{OH} (1)	CMOS output of ports 0, 1 DA0, 1	loн = −1.0 mA	4.5 to 5.5	V _{DD} -1			V
	Vон(2)	R, G, B, BL	и _{он} =0.1 mA	4.5 to 5.5	V _{DD} -0.5			
Output low-	Vol(1)	Ports 0, 1	l _{OL} = 10 mA	4.5 to 5.5			1.5	
level voltage	Vol(2)	Ports 0, 1 DA0, 1	 I_{OL} = 1.6 mA The total current of the ports 0, 1 is not over 40 mA. 	4.5 to 5.5			0.4	
	Vol(3)	• R, G, B, BL • PWM0 to PWM9	• loL = 3.0 mA The current of any pin is 3 mA or less.	4.5 to 5.5			0.4	
	Vou(4)	P70	IoL = 1 mA	4.5 to 5.5			0.4	
Pull-up MOS transistor resistance	Rpu	• Ports 0, 1 • Port 7	V _{OH} = 0.9 V _{DD}	4.5 to 5.5	13	38	80	kΩ
Output off	Югг	PWM0 to PWM9	V _{OUT} = 13.5 V	4.5 to 5.5			5	μΑ
Hysteresis voltage	Veis	Ports 0, 1 Port 7 RES HS, VS	Output disable	4.5 to 5.5		0.1V _{DD}		V

Parameter	Symbol	Pins	Conditions			Ratings		Unit
				Vdd [V]	min	typ	max	
Pin capacitance	СР	All pins	 f = 1 MHz Unmeasured input pins are set to V_{SS} level. Ta = 25°C 	4.5 to 5.5	and the second second	10	No. of Street Stre	pF

4. Serial Input/Output Characteristics at Ta = -30° C to $+70^{\circ}$ C , V_{SS} = 0 V

			Currents and	Dina	Canditions	and the second s	22			Linit
	Pai	rameter	Symbol	Pins	Conditions	A A		Ratings	5 <i>5</i> 5	Unit
						/ Vbd [V] 🐇	min	typ	max	
		Cycle	tCKCY(1)	• SCK0	Refer to Figure 5	4.5 to 5.5	2	E 1	and the second	tCYC
	nput clock	Low-level pulse width	tCKL(1)	• SCLK0	and the second second	4.5 to 5.5		al and a second and a second		
Serial clock	Idul	High-level pulse width	tCKH(1)			4.5 to 5.5	1	and the second second		
ial c	<u>×</u>	Cycle	tCKCY(2)	• SCK0	• Use a pull-up	4.5 to 5.5	2/	ľ		
Ser	Output clock	Low-level pulse width	tCKL(2)	• SCLK0	resistor (1 kΩ) when open-drain	4.5 to 5.5		1/2tCKCY		
		High-level pulse width	tCKH(2)	للا _ت	output •Refer to Figure 5	4.5 to 5.5		1/2tCKCY		
input	Data set-up time		tICK	SIO	Synchronized with the rising edge of	4.5 to 5.5	0.1			μs
Serial input	Data hold time		tCKI		SCK0, • Refer to Figure 5	³⁴ 4.5 to 5.5	0.1			
Serial output	(External serial clock)		tCKO(1)	SO0	• Use a pull-up resistor (1kΩ) when open-drain output	4.5 to 5.5			7/12tCYC +0.2	μs
			tCKO(2), March		Synchronized with the falling edge of SCK0. Refer to Figure 5	4.5 to 5.5			1/3tCYC +0.2	

5. Pulse Input Conditions at Ta = -30° C to $+70^{\circ}$ C, V_{SS} = 0 V

Parameter	Symbol	Pins	Conditions			Rating	6	Unit
				Vdd [v]	min	typ	max	
High/low level pulse width	tPIH(1) tPIL(1)	• INT0, INT1 • INT2/T0IN	 Interrupt factor flag settable. Timer and counter 0 pulse-countable. 	4.5 to 5.5	and the second second		and the second	tCYC
	tPIH(2) tPIL(2)	INT3/T0IN (The noise rejection filter time constant is 1/1)	 Interrupt factor flag settable. Timer and counter 0 pulse-countable. 	4.5 to 5.5	2			
	tPIH(3) tPIL(3)	INT3/T0IN (The noise rejection filter time constant is 1/16)	 Interrupt factor flag settable. Timer and counter 0 pulse-countable. 	4,5 to 5.5	32		and the second sec	
	tPIL(4)	RES	Reset acceptable	4.5 to 5.5	200	and the second		μs
	tPIH(5) tPIL(5)	HS, VS	Display position can be controlled Each active edge of HS, VS must be set apart more than 1tCYC. Refer to Figure 7	4.5 to 5 5	10,0 Martin and a second secon			tCYC
Rise/fall time	tTHL tTLH	HS	Refer to Figure 7	4.5 to 5,5			500	ns
Horizontal pull-in range	FH	HS	The monitor point in Figure 10 is 1/2 V _{DD}	4.5 to 5.5	15.23	15.73	16.23	kHz

6. A/D Converter Characteristics at Ta = -30° C to $+70^{\circ}$ C, V_{SS} = 0 V

	4							
Parameter	Symbol	Pins	Conditions			Ratings	;	Unit
	and the second		en such some	V _{DD} [V]	min	typ	max	
Resolution	N ,#			4.5 to 5.5		4		bit
Absolute precision	ĘΤ	(Note 3)	07	4.5 to 5.5		±1/4	±1/2	LSB
Conversion time	tCAD	After the Vref	1 bit conversion time =	4.5 to 5.5			1.96	μs
and the second se		selected till the	2tCYC					
and the second		conversion						
		completed.						
Reference current	NREE N		(Regulate the ladder	4.5 to 55		1.0	2.0	mA
		and the second s	resistor)					
Analog input	VAIN	AN0 to AN3		4.5 to 5.5	Vss		V_{DD}	V
voltage range								
Analog port input			V _{AIN} = V _{DD}	4.5 to 5.5			1	μA
current	1.4.1			1 E to E E	4			
and the second s	lainu		VAIN = VSS	4.5 to 5.5	-1			

Note 3 : Absolute precision excepts quantizing error ($\pm 1/2$ LSB).

7. D/A Converter Characteristics at $Ta=-30^\circ C$ to $+70^\circ C,~V_{SS}=0~V$

Parameter	Symbol	Pins	Conditions		Ratings	Unit
				V _{DD} [V]	min typ max	
Resolution	NDA			4.5 to 5.5	7	bit
Absolute precision	ETDA		7 bits mode (Note 4)	4.5 to 5.5	±2.0	LSB
Settling time	tSDA		(Note 5)	4.5 to 5.5	1.0	μs
Analog input voltage range	VAOUT	DA0 to DA1		4.5 to 525	Vss V _{DD}	V
Output resistor	RODA		(Note 6)	4.5 to 5.5	8	kΩ
	·	•			the State of A	

Note 4 : The $\pm 1/2$ -LSB quantization error is not included. (No load.)

Note 5 : Settling time refers to the time from when the D/A conversion instruction is executed to when the analog voltage output corresponding to the digital voltage on the specific port is generated.

Note 6 : D/A data = 80H

8. Current Drain Characteristics at Ta = -30° C to $+20^{\circ}$ C , $V_{58} = 0$ V

Parameter	Symbol	Pins	Conditions		per series and series a	Ratings		Unit
				V _{DD} {V}	min	typ	max	
Current drain during basic operation (Note 7)	IDDOP(1)	DVDD, AVDD	 FmCF = 12 MHz when ceramic oscillation FmLC = 14 11MHz when LC oscillation System clock : 12 MHz Internal RC when oscillation stops 	4.5, to 5.5		21	32	mA
Current drain in HALT mode (Note 7)	IDDHALT(1)	DVDD, AVØB	 HALT mode FmCF = 12 MHz when ceramic oscillation FmLC = 0 Hz (when oscillation stops) System clock : 12 MHz Internal RC when oscillation stops. 	4.5 to 5.5		5	10	mA
	IDOHALT(2)		 HALT mode FmCF = 0 MHz (when oscillation stops) FmLC = 0 Hz (when oscillation stops) System clock : Internal RC 	4.5 to 5.5		400	800	μΑ
Current drain in HOLD mode (Note 7)	Іррноср(1) Іррноср(2)	DVDD, AVDD	HOLD mode All oscillation stops.	4.5 to 5.5		0.05	20	μA

Note 7: The current into the output transistors and the pull-up MOS transistors are ignored.

Oscillation type	Manufacturer	Oscillator	C1	C2
12 MHz ceramic resonator	Murata	CSA12.0MTZ	33 pF	33 pF
oscillation		CST12.0MTW	on	chip
	Kyocera	KBR-12.0M	47 pF	47 pF 🧳

* Both C1 and C2 must use an K rank (±10%) and an SL characteristics.

Table 1 Ceramic Resonator Oscillation Guaranteed Constant (main-clock)

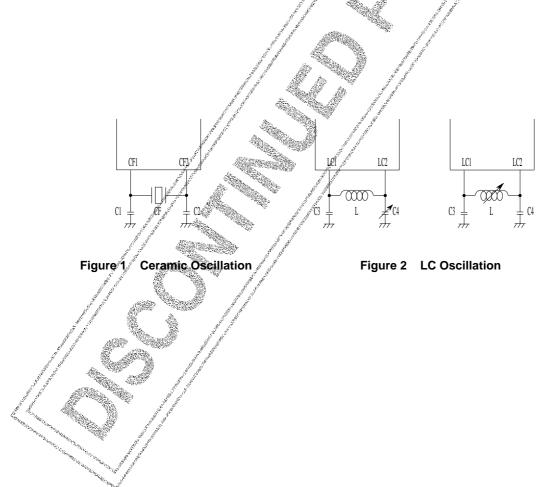
Oscillation type	L	C3	Q4
14.11 MHz LC oscillation	4.7 μΗ	33 pF	45 pF (Trimmer)
	4.7 μH ±10%	33 pH	33 pH
	(Variable)		

* See Figures 11 and 12.

Table 2 LC Oscillation Guaranteed Constant (OSD clock)

(Notes) • Since the circuit pattern affects the oscillation frequency, place the oscillation-related parts as close to the oscillation pins as possible with the shortest possible pattern length.

- If you use other oscillators herein, we provide no guarantee for the characteristics.
- Adjust the voltage of monitor point in Figure 10 to $1/2V_{DD}\pm 10\%$ by the LC oscillation constant 'L' or 'C' to lock the PLL circuit.



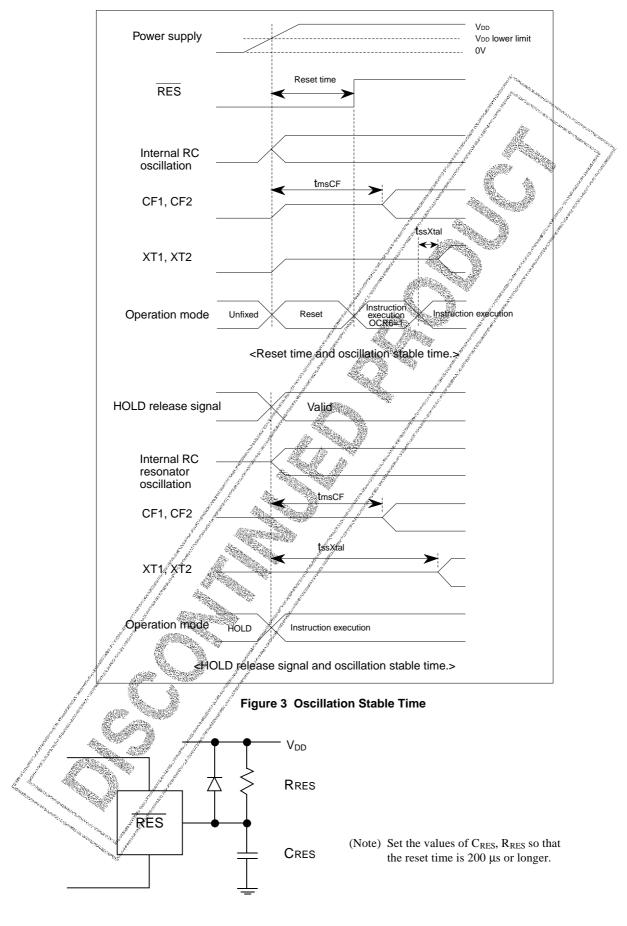
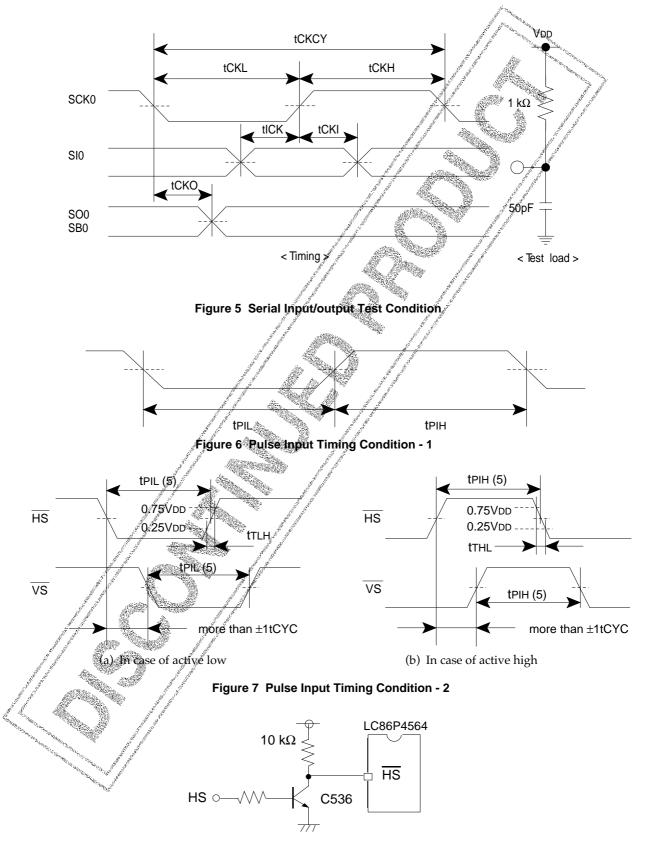


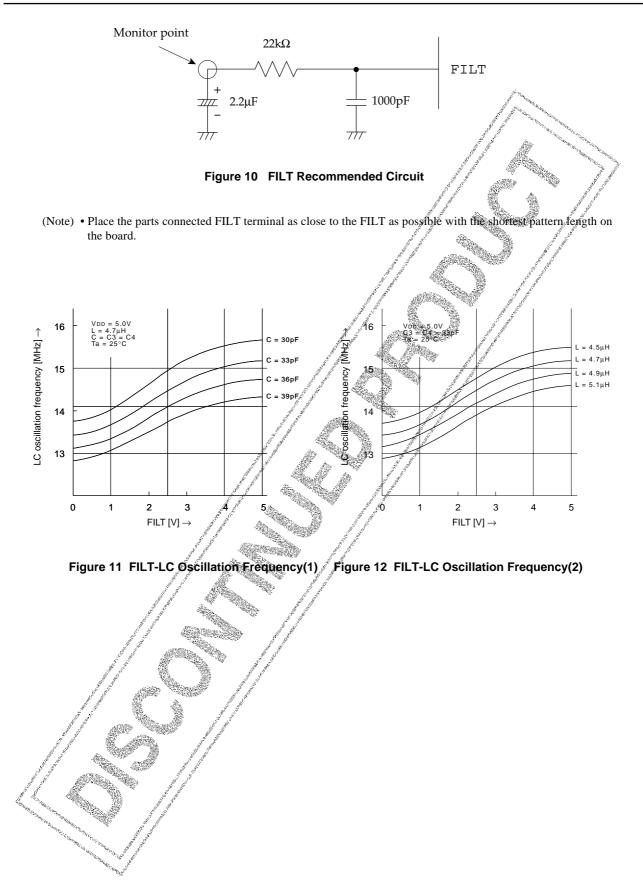
Figure 4 Reset Circuit



<AC timing point >







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