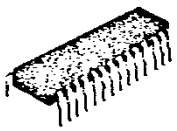
T-74-05-01

LC7520



3012A

CMOS LSI

Electronic Volume Control for Graphic Equalizer

The 3-chip configuration consisting of the LC7520, a controller (LC7060 or general-purpose microcomputer LC6502,etc.), and a display LSI (LC7560→LCD, LC7565 ⟶ FLT, LED) provides an electronic graphic equalizer system having the following features.

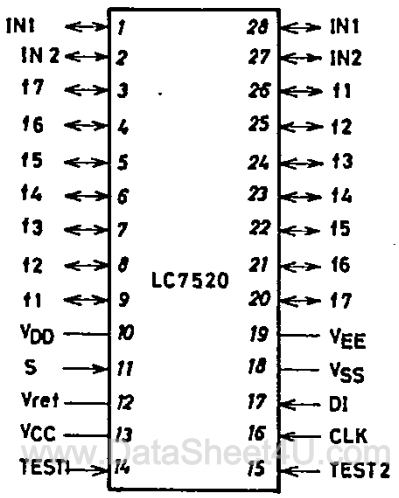
Functions

- On-chip electronic volume control for graphic equalizer with 7 bands each of right/left.
- 2dB/step variable in each band.
- Maximum boost of +10dB, maximum cut of -10dB, and 11 positions in each band.
- Setting can be made separately for right/left band.
- Band setting is made by serial data input. There are 2 control lines.
- Wide dynamic range.
- CMOS LSI of 40V breakdown voltage.

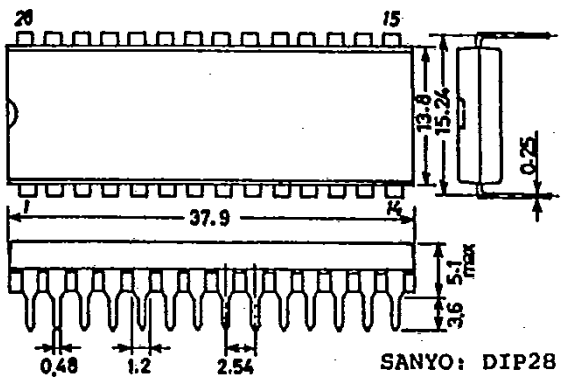
Features

- The gain in each band can be increased/decreased with one touch.
- Since the preset memory contents can be called with one touch, your desired frequency characteristic to the music can be selected.
  (Example) User option 2 modes + Maker option 3 modes + Last channel memory
- '0dB in each band (flat function)', 'The frequency characteristic in each band is reversed with respect to 0dB (reverse function).' - These functions can be software-controlled with one touch.
- Spectrum analyzing display facilitates recording equalization.
- Since 2 control lines can be also used for a display LSI, wiring between microcomputer and LSI is facilitated.

Pin Assignment



Case Outline 3012A-D28IC
(unit:mm)



SANYO: DIP28

Absolute Maximum Ratings at Ta=25°C, V_{SS}=0V

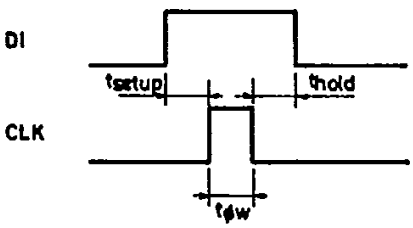
					unit
Maximum Supply Voltage	V_{DD}max	V_{DD}	$V_{EE} \leqq V_{SS}$	$V_{DD}-V_{EE} \leqq 40$	V
	V_{EE}max	V_{EE}			
	V_{ref}	V_{ref}	$V_{SS} \leqq V_{ref}$	$V_{DD}-V_{ref} \leqq 11$	V
	V_{CC}max	V_{CC}		V_{SS} to V_{SS}+7	V
Maximum Input Voltage	V_{I1}max	CLK,DI		V_{SS}-0.3 to V_{CC}+0.3	V
	V_{I2}max	f1 to f7,IN1,2		V_{EE}-0.3 to V_{DD}+0.3	V
	V_{I3}max	S,TEST1,2		Vref-0.3 to V_{DD}+0.3	V
Allowable Power Dissipation	Pdmax		Ta≦75°C	150	mW
Operating Temperature	Topg			-30 to +75	°C
Storage Temperature	Tstg			-40 to +125	°C

Allowable Operating Conditions at Ta=25°C, V_{SS}=0V

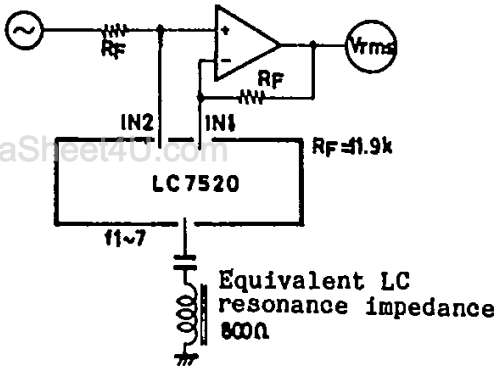
					unit
Supply Voltage	V_{DD}	V_{DD}	$V_{EE} \leqq V_{SS}$	$8 \leqq V_{DD}-V_{EE} \leqq 37$	V
	V_{EE}	V_{EE}	$V_{CC} \leqq V_{DD}$		
	V_{ref}	V_{ref}	$V_{DD}-V_{ref} \leqq 10$	0 to V_{DD}-4.5	V
	V_{CC}	V_{CC}		4.5 to (5.0typ) to 5.5	V
Input "H"-Level Voltage	V_{IH1}	CLK,DI		0.8V_{CC} to V_{CC}	V
	V_{IH2}	S		V_{ref}+0.9($V_{DD}-V_{ref}$) to V_{DD}	V
Input "L"-Level Voltage	V_{IL1}	CLK,DI		V_{SS} to 0.2V_{CC}	V
	V_{IL2}	S		V_{ref} to V_{ref}+0.1($V_{DD}-V_{ref}$)	V
Input Pulse Width	$t_{\phi w}$	CLK		1 min.	us
Setup Time	t_{setup}	DI		1 min.	us
Hold Time	t_{hold}	DI		1 min.	us

Electrical Characteristics at Ta=25°C, V_{SS}=0V

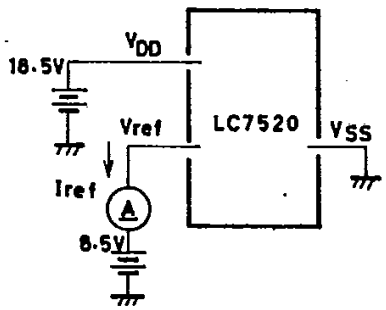
				min	typ	max	unit
Total Harmonic Distortion	THD1	IN1,2:All bands flat, f=20kHz,output 1V				0.005	%
	THD2	IN1,2:Boost,f=20kHz,output 1V				0.05	%
Closstalk	CT	:f=1kHz		60			dB
Setting Error	ΔB	Other band flat, Test Circuit 1, (No reversion occurs.)	±10dB	±9	±10	±11.5	dB
			±8dB	±6.6	±7.6	±9.0	dB
			±6dB	±4.9	±5.9	±7.2	dB
			±4dB	±3.0	±3.8	±4.9	dB
			±2dB	±1.0	±1.9	±3.0	dB
Analog SW OFF Leak Current	I_{off}	IN1,IN2,f1tof7				10	uA
Pull-down Resistance	R_{PD}	S :V_{DD}=13V,S			100		kohm
Current Dissipation	I_{DD}					1	mA
	I_{CC}					0.5	mA
Current Dissipation	I_{ref}	$V_{DD}-V_{ref}$:$V_{DD}-V_{ref}$=10V Test Circuit 2		-1			mA



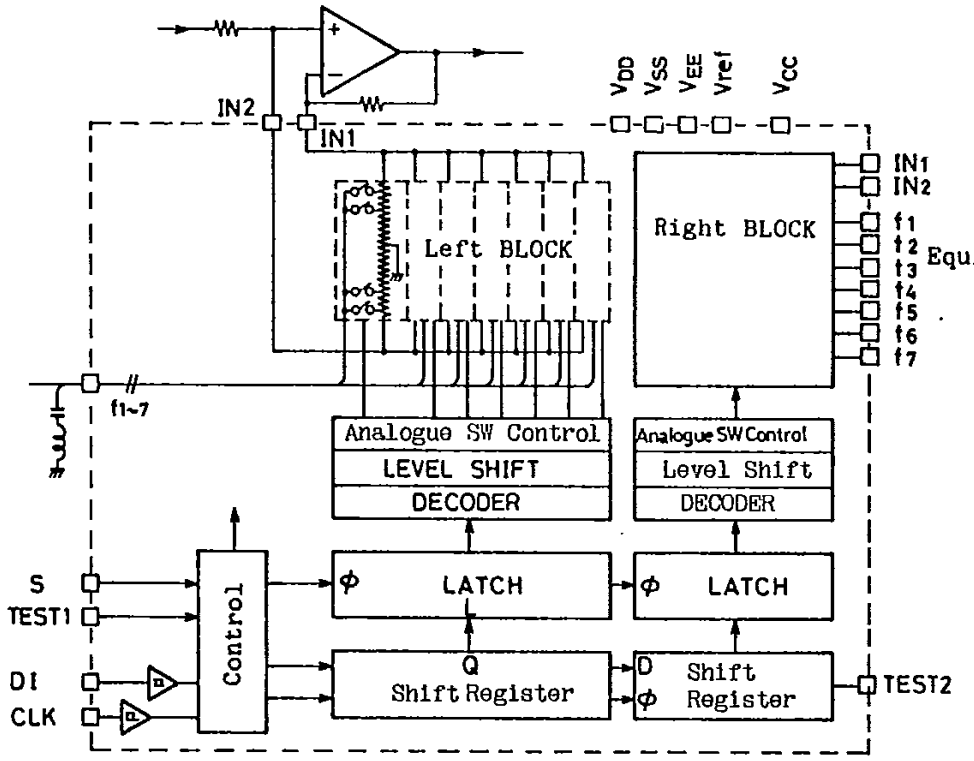
Test Circuit 1



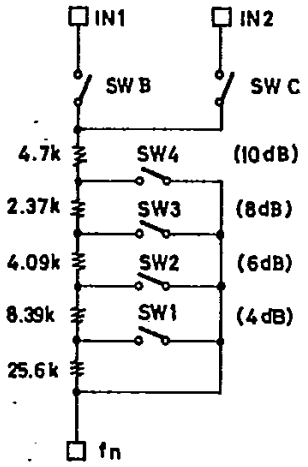
Test Circuit 2



Equivalent Circuit Block Diagram

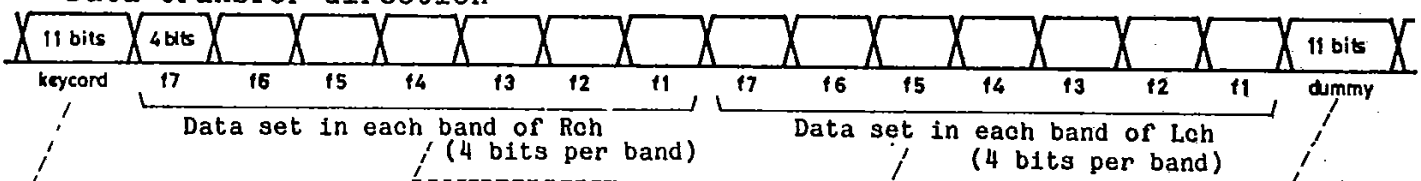


Equivalent resistance constants



Data Code 78 bits in all

→ Data transfer direction



Data set in each band of Rch (4 bits per band)

Data set in each band of Lch (4 bits per band)

LC7520 Pin S='0'

1 1 1 1 1 0 0 0 0 1 0

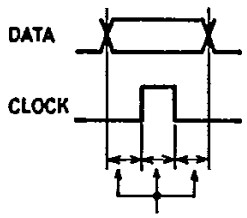
Pin S='1'

1 1 1 1 1 0 0 0 0 1 1

Transfer →direction	
10 dB	0 1 0 1
8	0 1 0 0
6	0 0 1 1
4	0 0 1 0
2	0 0 0 1
0	0 1 1 0
-2	1 0 0 1
-4	1 0 1 0
-6	1 0 1 1
-8	1 1 0 0
-10	1 1 0 1

0 0 0 0 0 0 0 0 0 0 0 0

last bit

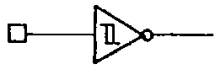
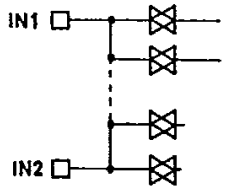
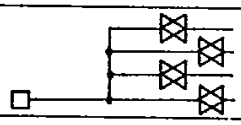
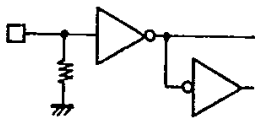


1us or greater

Note 1. When power is applied, data "0" must be first transferred for 67 clocks (initial clock) or more. If data transfer is stopped halfway, the transfer of the remaining data must be completed or data transfer must be started after the initial clocks have been transferred.

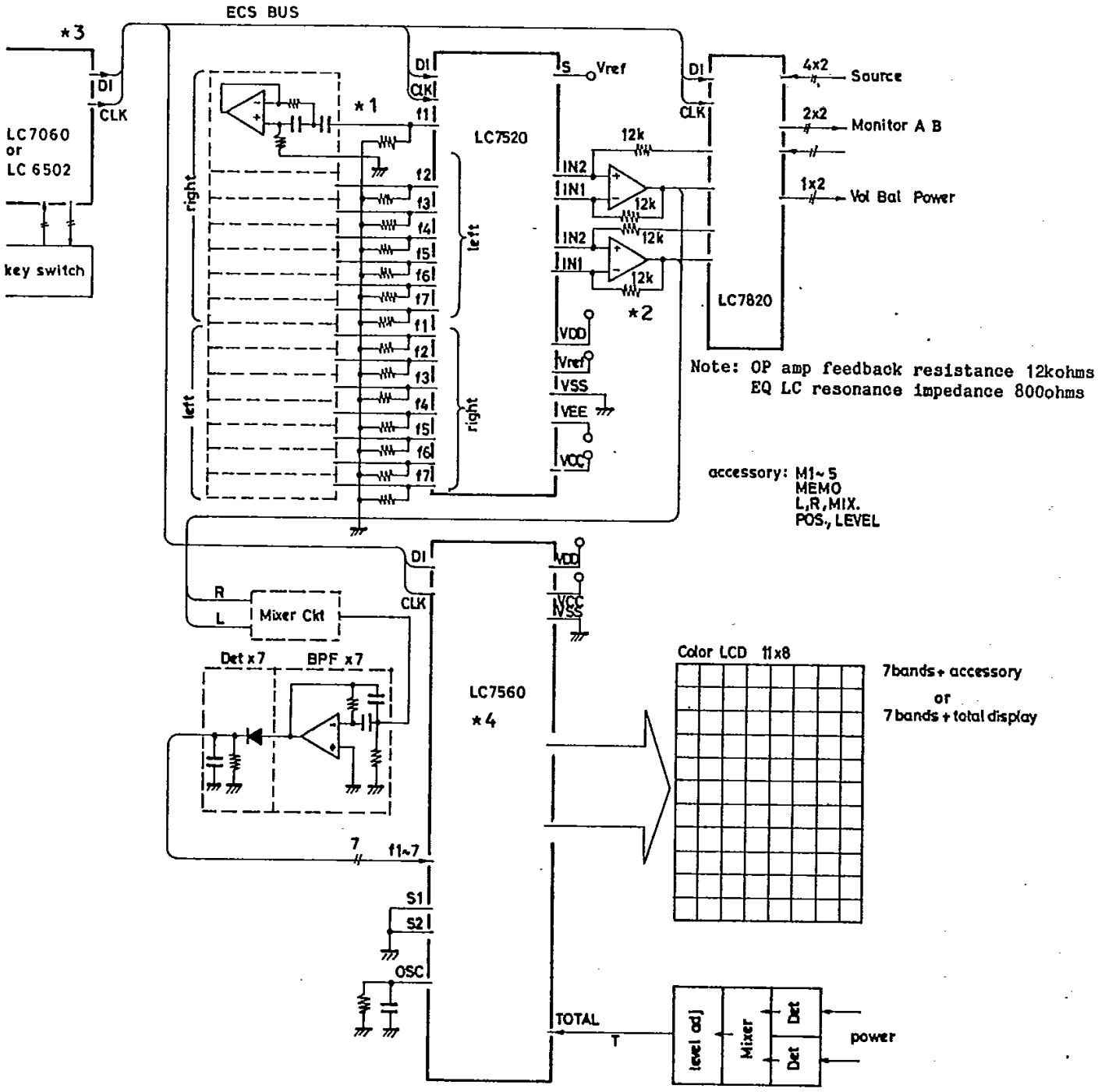
Note 2. When the DI, CLK pins are shared with the LC7560, etc., the maximum initial clocks for such device must be transferred.

Pin Description

Pin Name	Pin No.	Pin Configuration	Description
V_{DD}	10		Power supply pin, +18V(typ)., power supply for audio signal.
V_{ref}	12		Power supply pin, V_{DD}-5V(typ)., power supply for logic drive.
V_{SS}	18		Power supply pin 0V.
V_{EE}	19		Power supply pin, -18V(typ)., power supply for audio signal.
V_{CC}	13		Power supply pin, +5V.
D_I	17		. Used to input data from CPU. . Schmitt inverter type.
CLK	16		. Used to input CLK from CPU. . Schmitt inverter type.
IN1 IN2	1,28 2,27		. Audio signal input pin. . Normally, IN1 is connected to inverting input of OP amp. . Normally, IN2 is connected to noninverting input of OP amp. . Provided in Lch/Rch.
f1tof7	3to9 20to26		. Bandpass filter connecting pin. . f1 to f7 x 2 (right/left) = 14 pins in all.
S	11		. Select pin at 2-chip used mode. . With pull-down resistor. . To accept data under key code 7C3, S must be set to '1'.⟶Connected to V_{DD}. . To accept data under key code 7C2, S must be set to '0'.⟶Connected to Vref.
TEST1 TEST2	14 15		. IC test pin. . Open during operation.

Sample Application Circuit

(1) 7-Band LCD MIX Display (LC7520 x 1, LC7560 x 1)



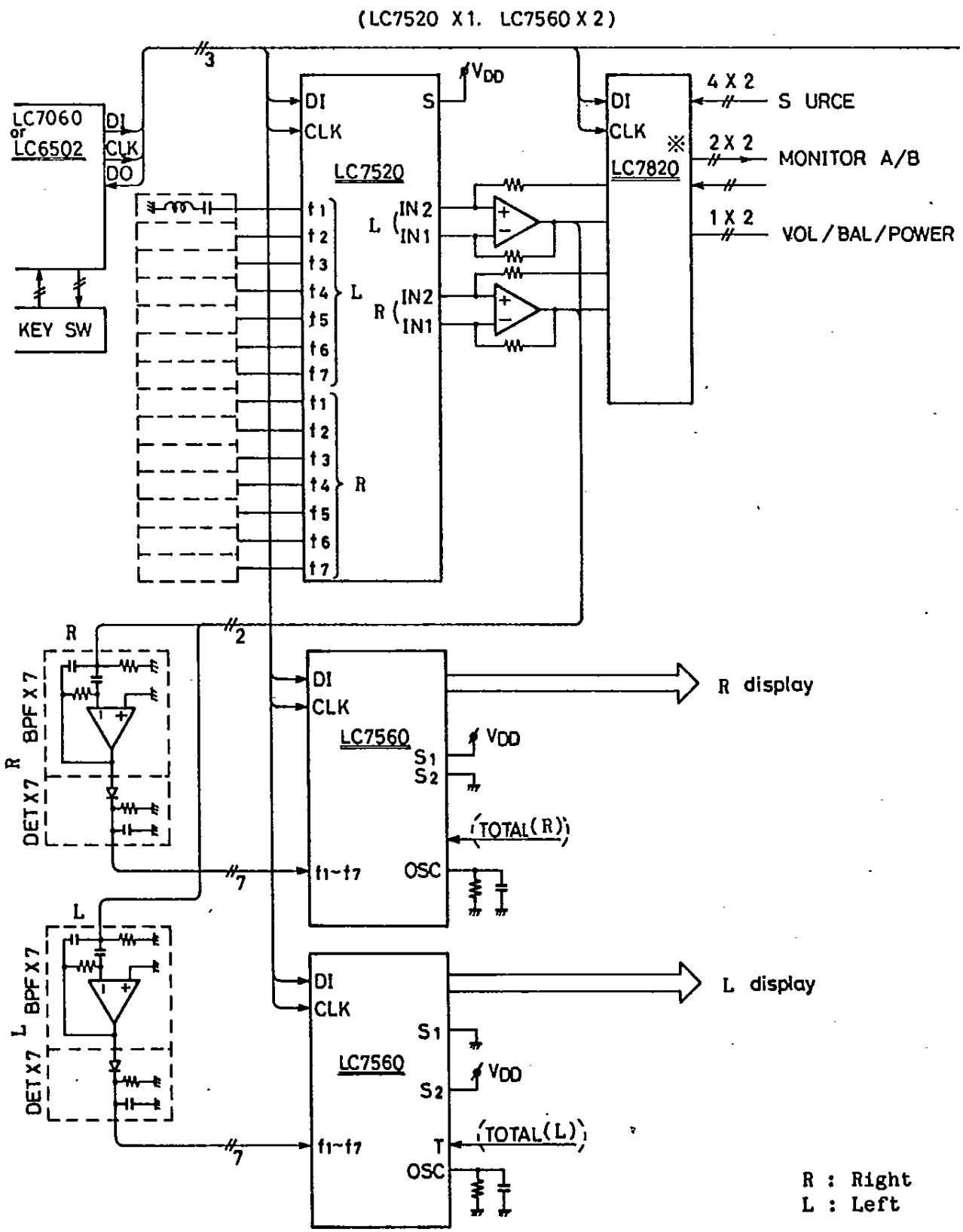
*1 It is recommended that pins f1 to f7 are connected to the signal Gnd through resistors of 1Mohm so that noise is minimized at the select mode.

*2 The optimum conditions for 2dB/step are as follows:
OP amp feedback resistance: 12kohms
Equivalent LC resonance impedance: 800ohms

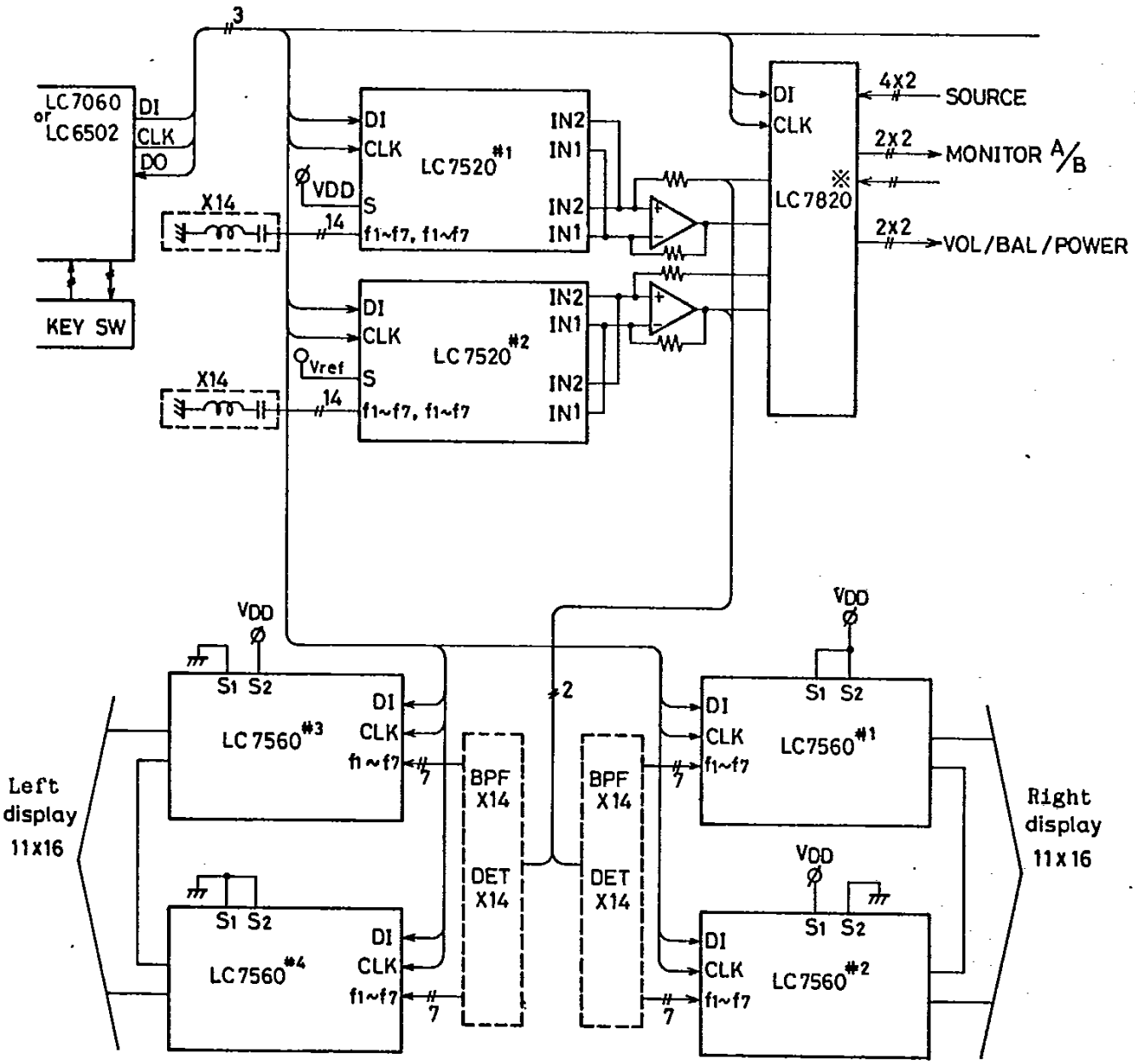
*3 The LC7060 is available as a standard controller.

*4 The LC7560 (LCD driver), LC7565 (FLT, LED driver) are available as spectrum analyzing display drivers for graphic equalizer output signal.

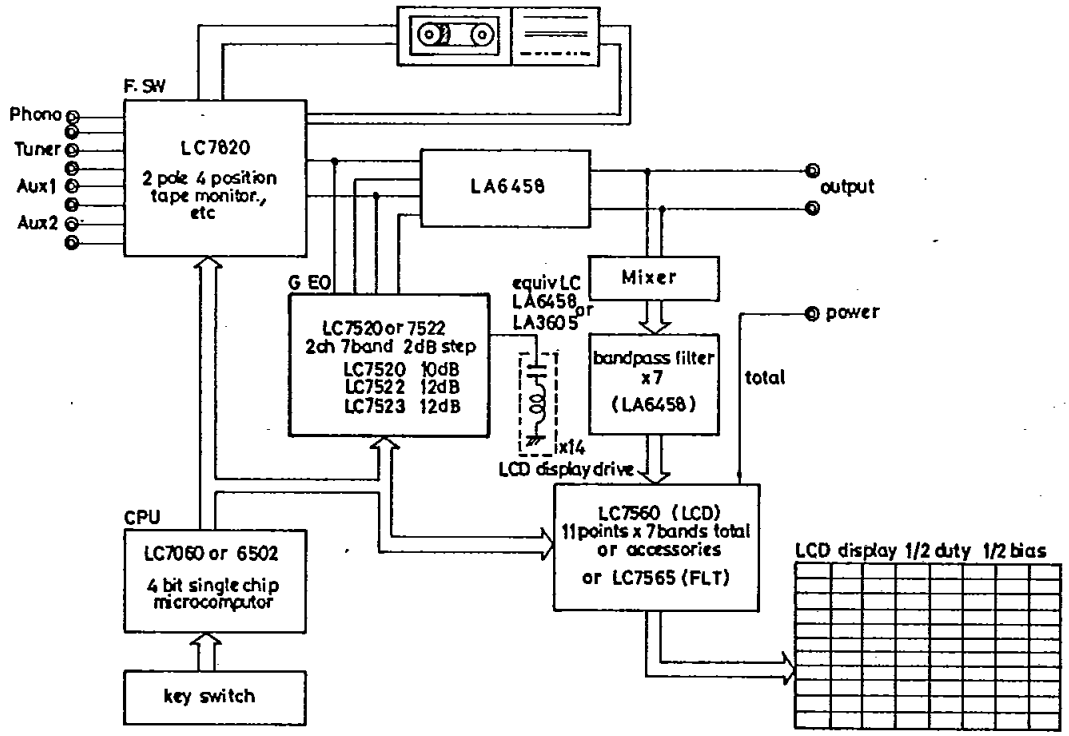
(2) 7-Band R/L Separate Display (LC7520 x 1, LC7560 x 1)



(3) 14-Band R/L Separate Display (LC7520 x 2, LC7560 x 4)
By combining various modes of pin S, a further extension of the application circuit is made possible to such an extent as shown below.



[Reference 1] ECS System/Graphic Equalizer Application Circuit Block Diagram



[Reference 2] Main Specifications for LC7060 (Graphic Equalizer Controller)

Use

Controller LSI for graphic equalizer electronic volume control LSI: LC7520, 7522, 7523; LCD driver: LC7560; FLT driver: LC7565

Functions

- 7 bands, 2dB/step, ±10dB(±12dB) variable,
  ( ): LC7522/7565/7565-combined use.
- Max. 8 memories (user option 5 modes, maker option 3 modes) + last channel memory.
- Possible to control function switch (5 positions) and electronic volume control.
- 2 control lines for graphic equalizer electronic volume control and display IC.
- Buzzer sound is generated when a key is operated.
- On-chip remote control reception program.

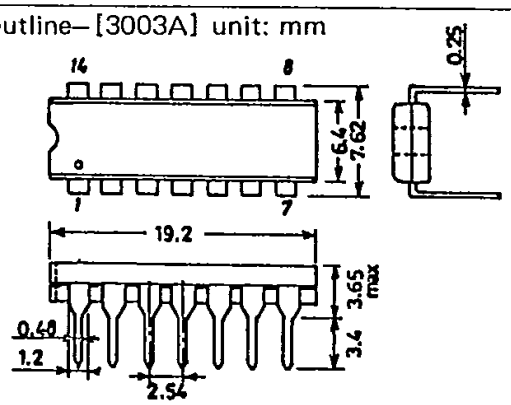
Features

- Any combination of graphic equalizer electronic volume control LSI LC7520, 7522, 7523 and display driver LSI LC7560, 7565 may be used. (Port-selectable)
- FLAT function to permit the FLAT mode to be entered with one touch.
- REVERSE function to permit the frequency characteristic to be reversed with respect to 0dB with one touch.
- Tuner band select and SCAN outut.
- MUTE and MUTE output.
- Backup operation available.

AUDIO-USE MOS IC CASE OUTLINES

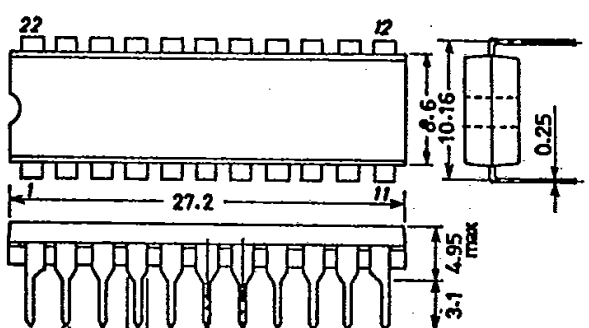
- All of Sanyo audio-use MOS IC case outlines are illustrated below.
- All dimensions are in mm, and dimensions which are not followed by min. or max. are represented by typical values.
- No marking is indicated.

Case Outline–[3003A] unit: mm



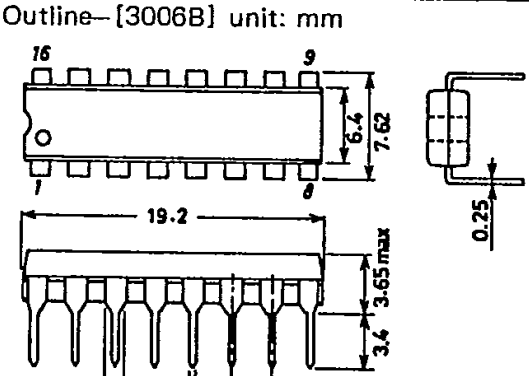
SANYO: DIP14

Case Outline–[3010A] unit: mm



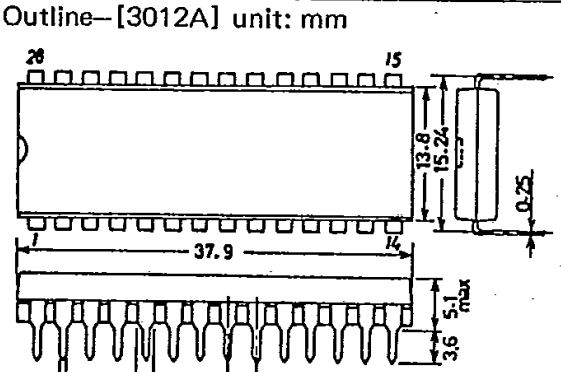
SANYO: DIP22

Case Outline–[3006B] unit: mm



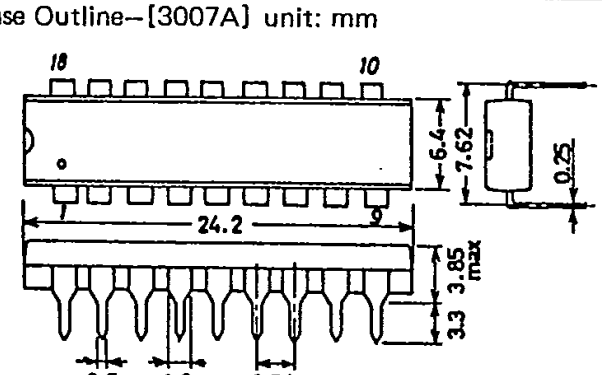
SANYO: DIP16

Case Outline–[3012A] unit: mm



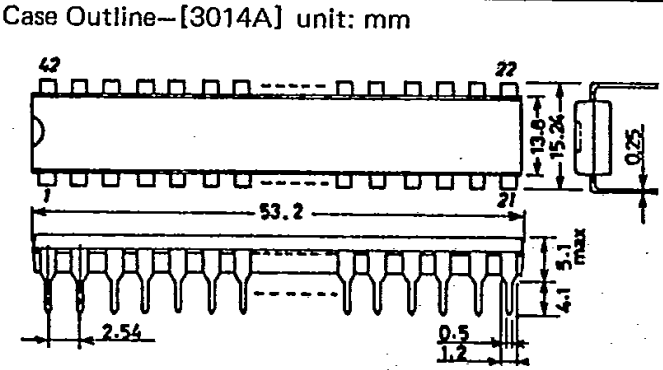
SANYO: DIP28

Case Outline–[3007A] unit: mm



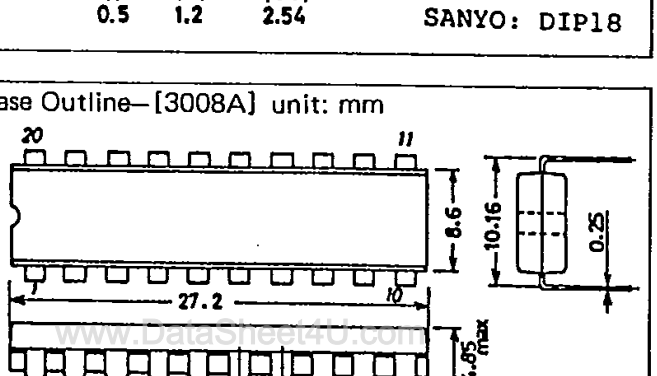
SANYO: DIP18

Case Outline–[3014A] unit: mm



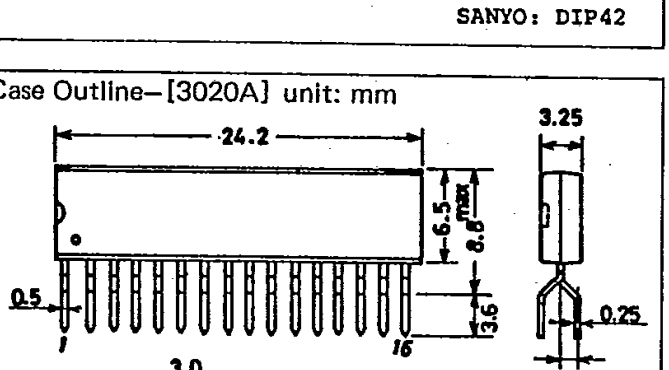
SANYO: DIP42

Case Outline–[3008A] unit: mm



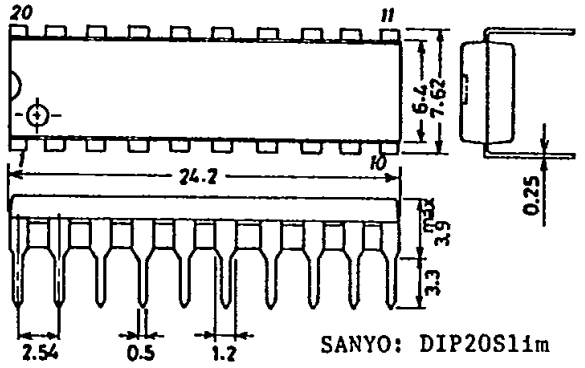
SANYO: DIP20

Case Outline–[3020A] unit: mm



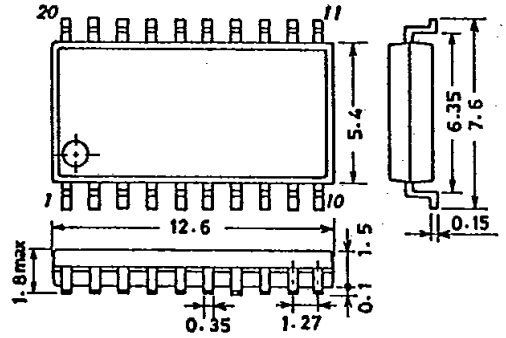
SANYO: SEP16

Case Outline—[3021B] unit: mm



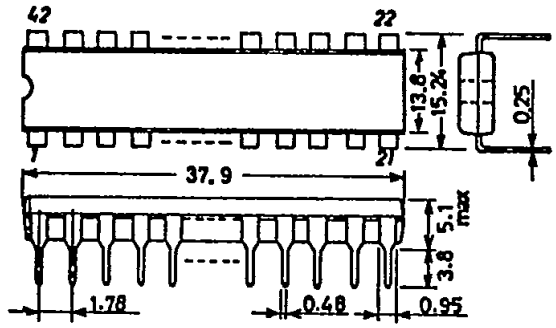
SANYO: DIP20S11m

Case Outline—[3036B] unit: mm



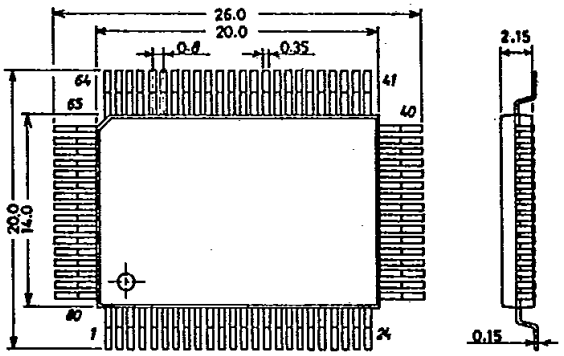
SANYO: MFP20

Case Outline—[3025B] unit: mm



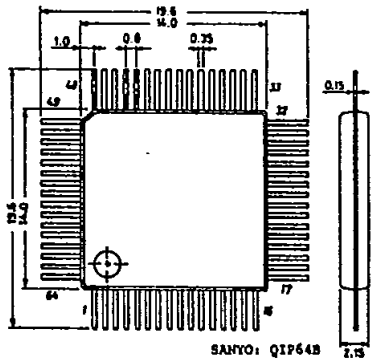
SANYO: DIP42S

Case Outline—[3044B] unit: mm



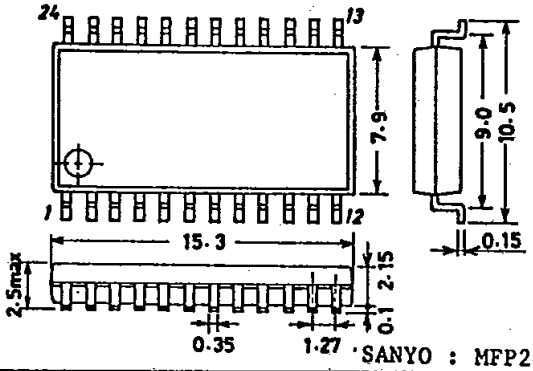
SANYO: QIP80A

Case Outline—[3026B] unit: mm



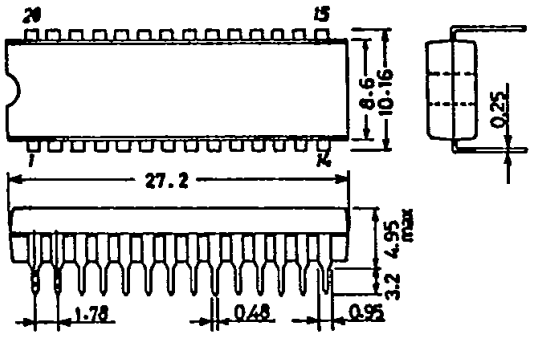
SANYO: QIP64B

Case Outline—[3045B] unit: mm



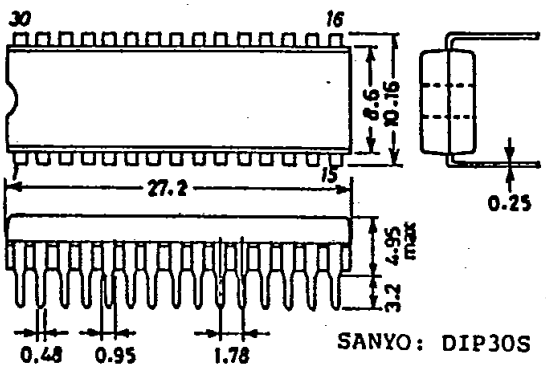
SANYO : MFP24

Case Outline—[3029A] unit: mm



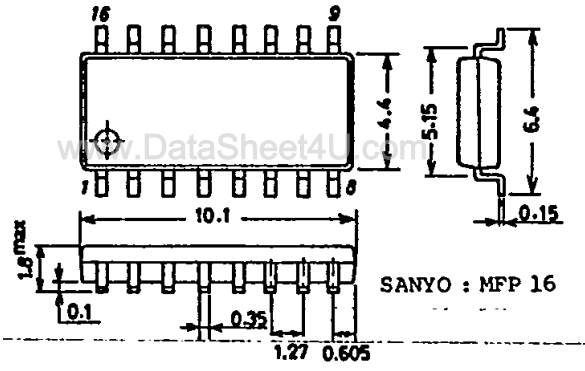
SANYO: DIP28S

Case Outline—[3047A] unit: mm



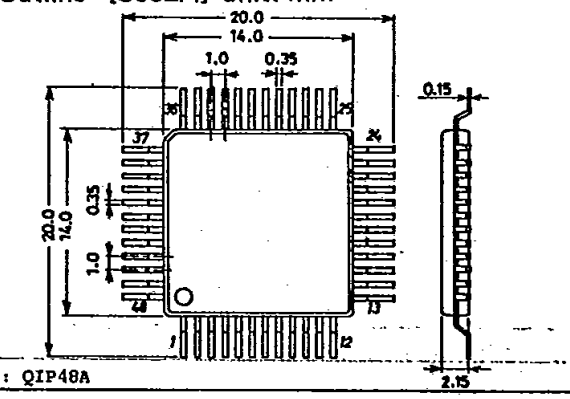
SANYO: DIP30S

Case Outline—[3035A] unit: mm



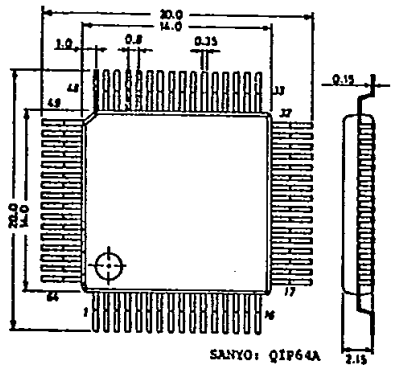
SANYO : MFP 16

Case Outline—[3052A] unit: mm

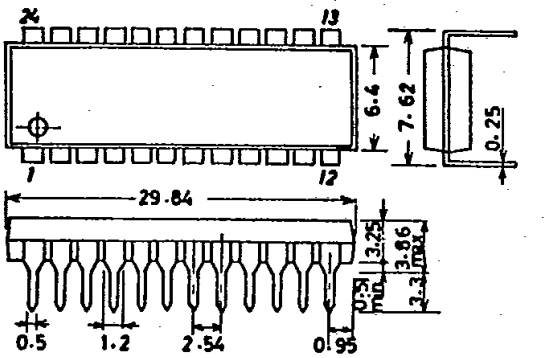


SANYO: QIP48A

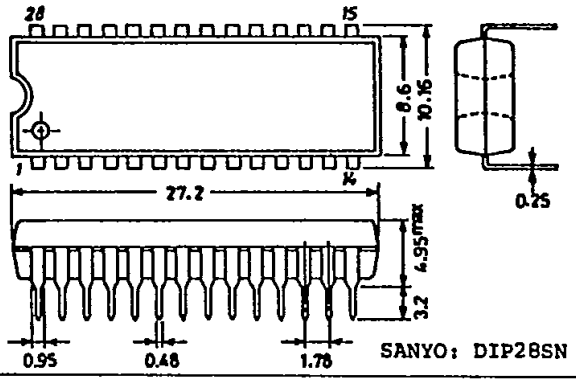
Case Outline—[3057] unit: mm



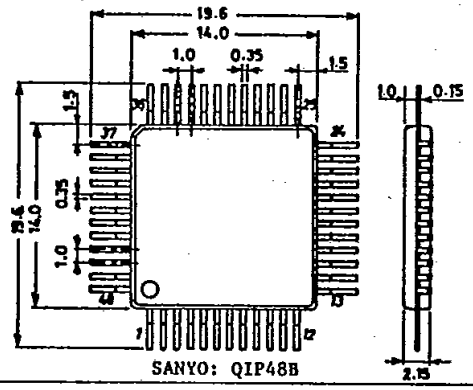
Case Outline—[3084] unit: mm



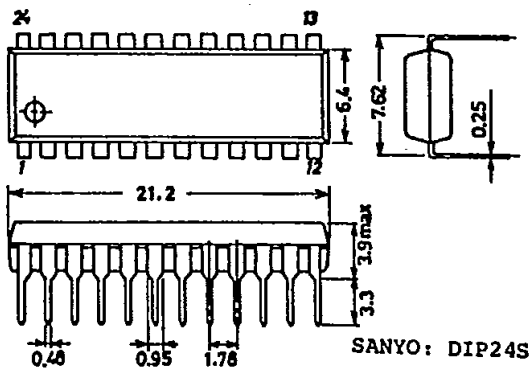
Case Outline—[3063] unit: mm



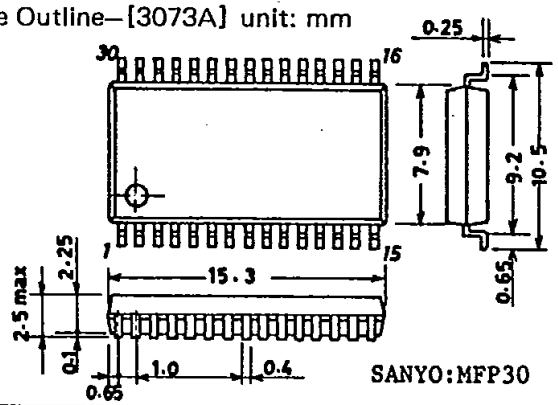
Case Outline—[3118] unit: mm



Case Outline—[3067] unit: mm



Case Outline—[3073A] unit: mm



Case Outline—[3074] unit: mm