LG Display

SPECIFICATION
FOR
APPROVAL

( ) Preliminary Specification
(●) Final Specification

Title	72.0” WUXGA TFT LCD

BUYER	LGE
MODEL	

SUPPLIER	LG. Display Co., Ltd.
*MODEL	LC720DUC
SUFFIX	SCM1 (RoHS Verified)

*When you obtain standard approval,
please use the above model name without suffix

APPROVED BY	SIGNATURE / DATE
/	
/	
/	

Please return 1 copy for your confirmation with your signature and comments.

APPROVED BY	SIGNATURE / DATE
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TV Products Development Dept.
LG. Display LCD Co., Ltd

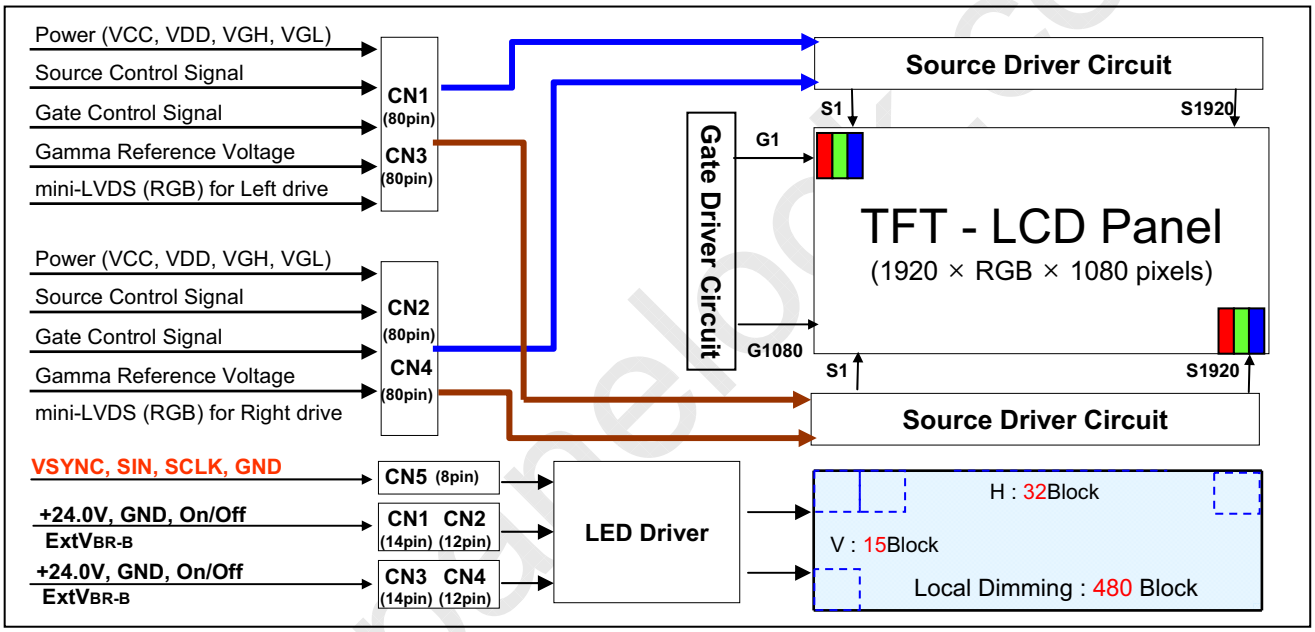
CONTENTS

RECORD OF REVISIONS

Revision No.	Revision Date	Page	Description
0.1	DEC, 30, 2009	-	Preliminary Specification (First Draft)
0.2	Feb, 04, 2010	14	3-2-3. Local Dimming Interface revise
		27~28	Mechanical dimmension update
		34	# APPENDIX-I, add Pallet Ass'y
		37~39	# APPENDIX-IV, Local Dimming Interface Design Guide revise
0.3	May, 06, 2010	29	vibration, shock test condition update
		6	Table 2. ELECTRICAL CHARACTERISTICS
		20	3-6. Power Sequence T3 change
		14	Local dimming pin map change
		9~12	Source FFC Pin map change
		37	Local dimming command byte change
0.4	May.24.2010	8	LED Driver Electrical Characteristics change
0.5	July. 27. 2010	27	Add notes.
		22	Table10. OPTICAL CHARACTERISTICS update
		29	Shock test delete
0.6	July. 28. 2010	30	International Standards update
0.7	Aug. 02. 2010	20	T2 spec change
0.8	Aug. 07. 2010	22	Gy update
0.9	Sep. 06. 2010	-	TBD update
1.0	Dec. 17. 2010		Final Specification
1.1	Jan. 18. 2011	8	Min duty changed
		31	Information of LCM Label changed. note1

1. General Description

The LC720DUC is a Color Active Matrix Liquid Crystal Display with an integral Light Emitting Diode (LED) backlight system. The matrix employs a-Si Thin Film Transistor as the active element. It is a transmissive type display operating in the normally black mode. It has a 72.07 inch diagonally measured active display area with WUXGA resolution (1080 vertical by 1920 horizontal pixel array). Each pixel is divided into Red, Green and Blue sub-pixels or dots which are arranged in vertical stripes. Gray scale or the luminance of the sub-pixel color is determined with a 8-bit gray scale signal for each dot. Therefore, it can present a palette of more than 16.7M(true) colors.
It is intended to support LCD TV, PCTV where high brightness, super wide viewing angle, high color gamut, high color depth and fast response time are important.



General Features

Active Screen Size	72.07 inches(1830.616mm) diagonal
Outline Dimension	1666.0(H) x 968.0 (V) x 54.0 mm(D) (Typ.)
Pixel Pitch	0.831 mm x 0.831 mm
Pixel Format	1920 horiz. by 1080 vert. Pixels, RGB stripe arrangement
Color Depth	8-bit, 16.7 M colors (※ 1.06B colors @ 10 bit (D) System Output)
Drive IC Data Interface	Source D-IC : 8-bit mini-LVDS, gamma reference voltage, and control signals
Luminance, White	500 cd/m^2 (Center 1point ,Typ.)
Viewing Angle (CR>10)	Viewing angle free (R/L 178 (Min.), U/D 178 (Min.))
Power Consumption	Total 385W (Typ.) (Logic=22 W with T-CON , LED Driver =363W(Typ) @EXTVBR-B = 100%)
Weight	37Kg (Typ.)
Display Mode	Transmissive mode, Normally black
Surface Treatment	Hard coating(3H), Anti-glare treatment of the front polarizer (Haze 10%)

2. Absolute Maximum Ratings

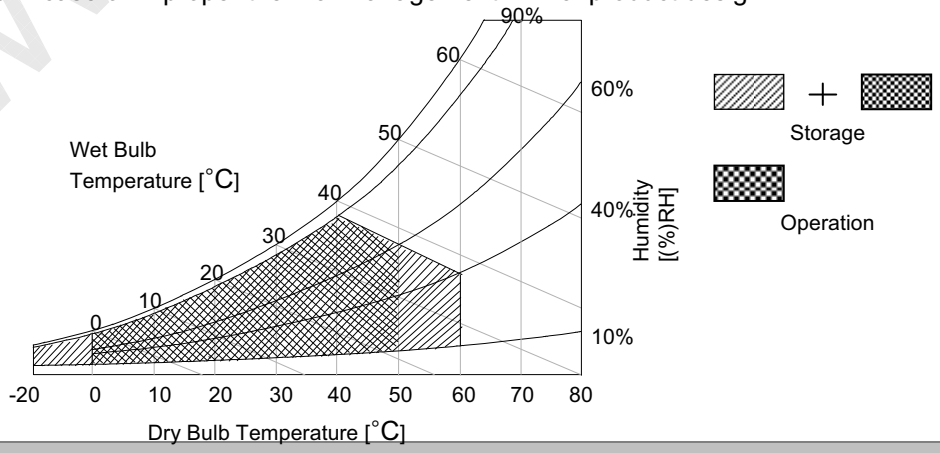
The following items are maximum values which, if exceeded, may cause faulty operation or damage to the LCD module.

Table 1. ABSOLUTE MAXIMUM RATINGS

Parameter		Symbol	Value		Unit	Note
			Min	Max		
LED Driver Power Input Voltage		V_{BL}	-0.3	+27.0	V_{DC}	1
LED Driver Control Voltage	ON/OFF	V_{OFF} / V_{ON}	-0.3	+5.5	V_{DC}	
	Brightness	EXTV$_{BR-B}$	0.0	+5.5	V_{DC}	
Logic Power Voltage		VCC	-0.5	+4.0	V_{DC}	
Gate High Voltage		VGH	+18.0	+30.0	V_{DC}	
Gate Low Voltage		VGL	-8.0	-4.0	V_{DC}	
Source D-IC Analog Voltage		VDD	-0.3	+18.0	V_{DC}	
Gamma Ref. Voltage (Upper)		VGMH	½VDD-0.5	VDD+0.5	V_{DC}	
Gamma Ref. Voltage (Low)		VGML	-0.3	½ VDD+0.5	V_{DC}	
Panel Front Temperature		T_{SUR}	-	+68	°C	4
Operating Temperature		T_{OP}	0	+50	°C	2,3
Storage Temperature		T_{ST}	-20	+60	°C	
Operating Ambient Humidity		H_{OP}	10	90	%RH	
Storage Humidity		H_{ST}	10	90	%RH	

Note: 1. Ambient temperature condition (Ta = 25 ± 2 °C)

2. Temperature and relative humidity range are shown in the figure below. Wet bulb temperature should be Max 39 °C and no condensation of water.
3. Gravity mura can be guaranteed below 40℃ condition.
4. The maximum operating temperature is based on the test condition that the surface temperature of display area is less than or equal to 68 ℃ with LCD module alone in a temperature controlled chamber. Thermal management should be considered in final product design to prevent the surface temperature of display area from being over 68 ℃. The range of operating temperature may degrade in case of improper thermal management in final product design.



3. Electrical Specifications

3-1. Electrical Characteristics

It requires several power inputs. The VCC is the basic power of LCD Driving power sequence, Which is used to logic power voltage of Source D-IC and Gate D-IC.

Table 2. Electrical Characteristics

Parameter	Symbol	Condition	MIN	TYP	MAX	Unit	Note
Logic Power Voltage	VCC	-	3.0	3.3	3.6	VDC	
Logic High Level Input Voltage	VIH		2.7		VCC	VDC	
Logic Low Level Input Voltage	VIL		0		0.6	VDC	
Source D-IC Analog Voltage	VDD	-	Typ.-200mV	16.6	Typ.+200mV	VDC	
Half Source D-IC Analog Voltage	H_VDD	-	GMA10+50mV	8.2	GMA9-50mV	VDC	
Gamma Reference Voltage	V_{GMH}	(GMA1 ~ GMA9)	½*VDD		VDD-0.2		
	V_{GML}	(GMA10 ~ GMA18)	0.2		½*VDD		
Common Voltage	Vcom	-	Typ.-300mV	6.0	Typ.+300mV	V	
Mini-LVDS Clock frequency	CLK	3.0V≤VCC ≤3.6V				MHz	
mini-LVDS input Voltage (Center)	VIB	Mini-LVDS Clock and Data	0.7 + (VID/2)		(VCC-1.2) - VID / 2	V	5
mini-LVDS input Voltage Distortion (Center)	ΔVIB				0.8	V	
mini-LVDS differential Voltage range	VID		150		800	mV	
mini-LVDS differential Voltage range Dip	ΔVID		25		800	mV	
Gate High Voltage	VGH		Typ.-300mV	26.5	Typ.+300mV	VDC	
Gate Low Voltage	VGL		Typ.-200mV	-5	Typ.+200mV	VDC	
Gate High Modulation Voltage	VGHM			-		V	
Total Power Current	ILCD	-		-		mA	2
Total Power Consumption	PLCD	-		-		Watt	2

Note:

1. The specified current and power consumption are under the VLCD=12V., 25 ± 2°C, f_V=240Hz condition whereas mosaic pattern(8 x 6) is displayed and f_V is the frame frequency.
2. The above spec is based on the basic model.
3. All of the typical gate voltage should be controlled within 1% voltage level
4. Ripple voltage level is recommended under 10%
5. In case of mini-LVDS signal spec, refer to Fig 2 for the more detail.
6. Logic Level Input Signal : SOE,POL,GSP,H_CONV,OPT_N

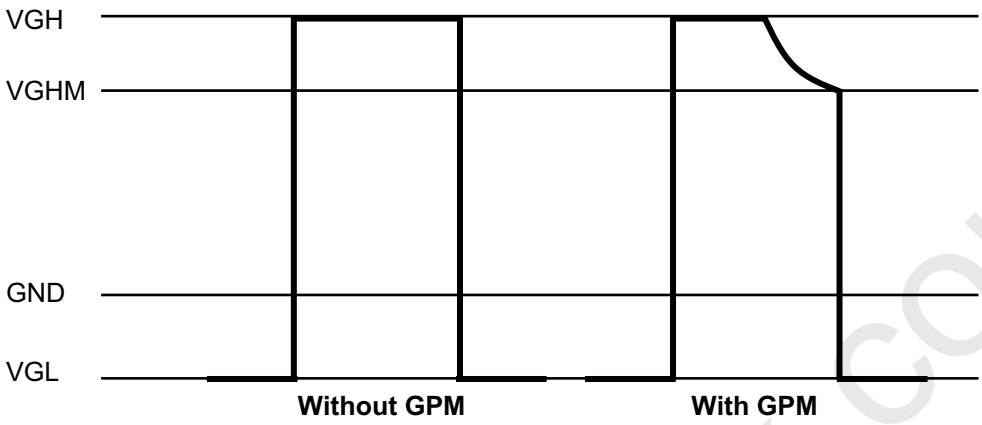


FIG. 1 Gate Output Wave form without GPM and with GPM

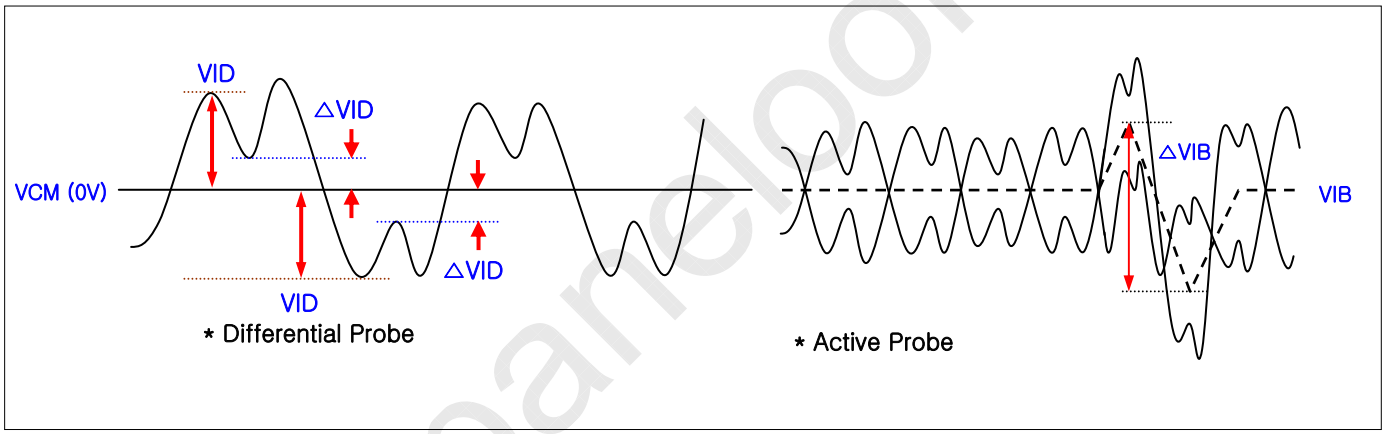


FIG. 2 Description of VID, ΔVIB, ΔVID

* Source PCB

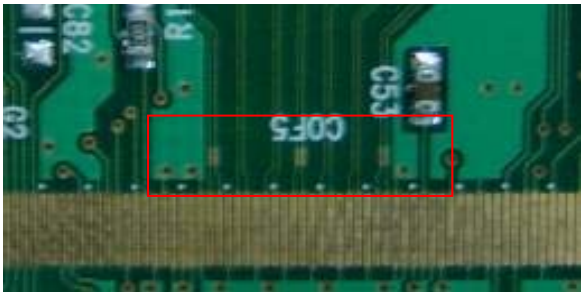


FIG. 3 Measure point

Table 3. Electrical Characteristics (Continue)

Parameter			Symbol	Values			Unit	Notes
				Min	Typ	Max		
LED Driver :								
Power Supply Input Voltage			VBL	22.8	24.0	25.2	Vdc	1
Power Supply Input Current			IBL_A	–	15.1	16.8	A	Ext V_{BR-B} = 100%
Power Supply Input Current (In-Rush)			Irush	–	–	17.6	A	V_{BL} = 22.8V Ext V_{BR-B} = 100% 4
Power Consumption			PBL	–	363	399	W	Ext V_{BR-B} = 100%
Input Voltage for Control System Signals	On/Off	On	V on	2.5	–	5.0	Vdc	
		Off	V off	-0.3	0.0	0.5	Vdc	
	Brightness Adjust		ExtV_{BR-B}	5	–	100	%	On Duty
	PWM Frequency for NTSC & PAL		PAL		200		Hz	3
			NTSC		240		Hz	3
	Pulse Duty Level (PWM)		High Level	2.5	–	5.0	Vdc	HIGH : on duty LOW : off duty
			Low Level	0.0	–	0.5	Vdc	
	VSYNC, SIN, SCLK, Reverse (Local Dimming)		High Level	2.7	3.3	3.6	Vdc	
			Low Level	-0.3	0.0	0.4	Vdc	
LED :								
Life Time				30,000			Hrs	2

Notes :

1. Electrical characteristics are determined after the unit has been 'ON' and stable for approximately 60 minutes at 25±2°C. The specified current and power consumption are under the typical supply Input voltage 24Vand V_{BR} (Ext V_{BR-B} : 100%), it is total power consumption.
2. The life time(MTTF) is determined as the time which luminance of the LED is 50% compared to that of initial value at the typical LED current (Ext V_{BR-B} : 100%), on condition of continuous operating in LCM state at 25±2°C.
3. LGD recommend that the PWM freq. is synchronized with One time harmonic of Vsync signal of system. Though PWM frequency is over 252Hz(Max), function of LED Driver is not affected.
4. The duration of rush current is about 10ms.
5. Even though inrush current is over the specified value, there is no problem if I^2T spec of fuse is satisfied.

3-2. Interface Connections

This LCD module employs two kinds of interface connection, two 80-pin FFC connector are used for the module electronics and 12-pin,14-pin connectors are used for the integral backlight system.

3-2-1. LCD Module

-LCD Connector (CN1): TF06L-80S-0.5SH (Manufactured by Hirose)

Table 4-1. MODULE CONNECTOR(CN1) PIN CONFIGURATION

No	Symbol	Description	No	Symbol	Description
1	VDD	Driver Power Supply Voltage	41	GND	Ground
2	VDD	Driver Power Supply Voltage	42	POL_UP	Polarity Output Signal
3	GND	Ground	43	GSP	Gate Start Pulse
4	VCC	Logic Power Supply Voltage	44	H_CONV	Horizontal 2 Inversion Signal
5	VCC	Logic Power Supply Voltage	45	OPT_N	"H" Normal Display / "L" Rotation Display
6	GND	Ground	46	GND	Ground
7	HVDD	Half Driver Power Supply Voltage	47	LRV5 –	Left Right Mini LVDS Receiver Signal(5–)
8	HVDD	Half Driver Power Supply voltage	48	LRV5 +	Left Right Mini LVDS Receiver Signal(5+)
9	GND	Ground	49	LRV4 –	Left Right Mini LVDS Receiver Signal(4–)
10	VGL	Gate Low Voltage	50	LRV4 +	Left Right Mini LVDS Receiver Signal(4+)
11	GND	Ground	51	LRV3 –	Left Right Mini LVDS Receiver Signal(3–)
12	GOE	Gate Output Enable	52	LRV3 +	Left Right Mini LVDS Receiver Signal(3+)
13	GSC	Gate Shift Clock	53	GND	Ground
14	GND	Ground	54	LRVCLK –	Left Right Mini LVDS Receiver Clock(–)
15	VGH	Gate High Voltage	55	LRVCLK +	Left Right Mini LVDS Receiver Clock(+)
16	GND	Ground	56	GND	Ground
17	GND	Ground	57	LRV2 –	Left Right Mini LVDS Receiver Signal(2–)
18	VCOM_L	Left Vcom Output	58	LRV2 +	Left Right Mini LVDS Receiver Signal(2+)
19	GND	Ground	59	LRV1 –	Left Right Mini LVDS Receiver Signal(1–)
20	ZOUT	LTD Output	60	LRV1 +	Left Right Mini LVDS Receiver Signal(1+)
21	NC	No connection	61	LRV0 –	Left Right Mini LVDS Receiver Signal(0–)
22	GND	Ground	62	LRV0 +	Left Right Mini LVDS Receiver Signal(0+)
23	GND	Ground	63	GND	Ground
24	GMA18	Gamma Voltage 18	64	LLV5 –	Left Left Mini LVDS Receiver Signal(5–)
25	GMA16	Gamma Voltage 16	65	LLV5 +	Left Left Mini LVDS Receiver Signal(5+)
26	GMA15	Gamma Voltage 15	66	LLV4 –	Left Left Mini LVDS Receiver Signal(4–)
27	GMA14	Gamma Voltage 14	67	LLV4 +	Left Left Mini LVDS Receiver Signal(4+)
28	GMA13	Gamma Voltage 13	68	LLV3 –	Left Left Mini LVDS Receiver Signal(3–)
29	GMA12	Gamma Voltage 12	69	LLV3 +	Left Left Mini LVDS Receiver Signal(3+)
30	GMA10	Gamma Voltage 10	70	GND	Ground
31	GMA9	Gamma Voltage 9	71	LLVCLK –	Left Left Mini LVDS Receiver Clock(–)
32	GMA7	Gamma Voltage 7	72	LLVCLK +	Left Left Mini LVDS Receiver Clock(+)
33	GMA6	Gamma Voltage 6	73	GND	Ground
34	GMA5	Gamma Voltage 5	74	LLV2 –	Left Left Mini LVDS Receiver Signal(2–)
35	GMA4	Gamma Voltage 4	75	LLV2 +	Left Left Mini LVDS Receiver Signal(2+)
36	GMA3	Gamma Voltage 3	76	LLV1 –	Left Left Mini LVDS Receiver Signal(1–)
37	GMA1	Gamma Voltage 1	77	LLV1 +	Left Left Mini LVDS Receiver Signal(1+)
38	GND	Ground	78	LLV0 –	Left Left Mini LVDS Receiver Signal(0–)
39	GND	Ground	79	LLV0 +	Left Left Mini LVDS Receiver Signal(0+)
40	SOE_UL	Source Output Enable	80	GND	Ground

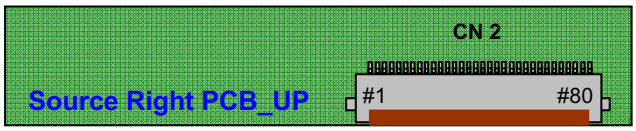
Note : 1. Please refer to application note (**Half VDD & Gamma Voltage setting & Control signal**) for details.

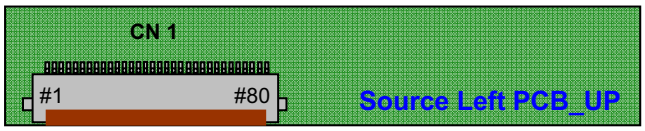
-LCD Connector (CN2): TF06L-80S-0.5SH (Manufactured by Hirose)

Table 4-2. MODULE CONNECTOR(CN2) PIN CONFIGURATION

No	Symbol	Description	No	Symbol	Description
1	WP_M	EEPROM Write Protection	41	SOE_UR	Source Output Enable
2	SCL_M	I2C CLOCK	42	GND	Ground
3	SDA_M	I2C DATA	43	POL_UP	Polarity Output Signal
4	GND	Ground	44	GSP	Gate Start Pulse
5	RRV5 –	Right Right Mini LVDS Receiver Signal(5–)	45	GND	Ground
6	RRV5 +	Right Right Mini LVDS Receiver Signal(5+)	46	GMA 18	Gamma Voltage 18
7	RRV4 –	Right Right Mini LVDS Receiver Signal(4–)	47	GMA 16	Gamma Voltage 16
8	RRV4 +	Right Right Mini LVDS Receiver Signal(4+)	48	GMA 15	Gamma Voltage 15
9	RRV3 –	Right Right Mini LVDS Receiver Signal(3–)	49	GMA 14	Gamma Voltage 14
10	RRV3 +	Right Right Mini LVDS Receiver Signal(3+)	50	GMA 13	Gamma Voltage 13
11	GND	Ground	51	GMA 12	Gamma Voltage 12
12	RRVCLK –	Right Right Mini LVDS Receiver Clock(–)	52	GMA 10	Gamma Voltage 10
13	RRVCLK +	Right Right Mini LVDS Receiver Clock(+)	53	GMA 9	Gamma Voltage 9
14	GND	Ground	54	GMA 7	Gamma Voltage 7
15	RRV2 –	Right Right Mini LVDS Receiver Signal(2–)	55	GMA 6	Gamma Voltage 6
16	RRV2 +	Right Right Mini LVDS Receiver Signal(2+)	56	GMA 5	Gamma Voltage 5
17	RRV1 –	Right Right Mini LVDS Receiver Signal(1–)	57	GMA 4	Gamma Voltage 4
18	RRV1 +	Right Right Mini LVDS Receiver Signal(1+)	58	GMA 3	Gamma Voltage 3
19	RRV0 –	Right Right Mini LVDS Receiver Signal(0–)	59	GMA 1	Gamma Voltage 1
20	RRV0 +	Right Right Mini LVDS Receiver Signal(0+)	60	NC	No connecttion
21	GND	Ground	61	ZOUT	LTD Output
22	RLV5 –	Right Left Mini LVDS Receiver Signal(5–)	62	GND	Ground
23	RLV5 +	Right Left Mini LVDS Receiver Signal(5+)	63	VCOM_R	Right Vcom Output
24	RLV4 –	Right Left Mini LVDS Receiver Signal(4–)	64	GND	Ground
25	RLV4 +	Right Left Mini LVDS Receiver Signal(4+)	65	VGH	Gate High Voltage
26	RLV3 –	Right Left Mini LVDS Receiver Signal(3–)	66	GND	Ground
27	RLV3 +	Right Left Mini LVDS Receiver Signal(3+)	67	GSC	Gate Shift Clock
28	GND	Ground	68	GOE	Gate Output Enable
29	RLVCLK –	Right Left Mini LVDS Receiver Clock(–)	69	GND	Ground
30	RLVCLK +	Right Left Mini LVDS Receiver Clock(+)	70	VGL	Gate Low Voltage
31	GND	Ground	71	OPT_P	"L" Normal Display / "H" Rotation Display
32	RLV2 –	Right Left Mini LVDS Receiver Signal(2–)	72	GND	Ground
33	RLV2 +	Right Left Mini LVDS Receiver Signal(2+)	73	HVDD	Half Driver Power Supply Voltage
34	RLV1 –	Right Left Mini LVDS Receiver Signal(1–)	74	HVDD	Half Driver Power Supply voltage
35	RLV1 +	Right Left Mini LVDS Receiver Signal(1+)	75	GND	Ground
36	RLV0 –	Right Left Mini LVDS Receiver Signal(0–)	76	VCC	Logic Power Supply Voltage
37	RLV0 +	Right Left Mini LVDS Receiver Signal(0+)	77	VCC	Logic Power Supply Voltage
38	GND	Ground	78	GND	Ground
39	OPT_N	"H" Normal Display / "L" Rotation Display	79	VDD	Driver Power Supply Voltage
40	H_CONV	Horizontal 2 Inversion Signal	80	VDD	Driver Power Supply Voltage

Note : 1.Please refer to application note (Half VDD & Gamma Voltage setting & Control signal) for details.





-LCD Connector (CN3): TF06L-80S-0.5SH (Manufactured by Hirose)

Table 4-3. MODULE CONNECTOR(CN3) PIN CONFIGURATION

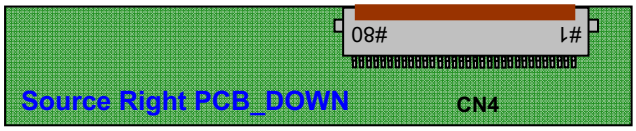
No	Symbol	Description	No	Symbol	Description
1	WP_S	EEPROM Write Protection	41	SOE_DL	Source Output Enable
2	SCL_S	I2C CLOCK	42	GND	Ground
3	SDA_S	I2C DATA	43	POL_DOWN	Polarity Output Signal
4	GND	Ground	44	GND	Ground
5	RRV5 –	Left Right Mini LVDS Receiver Signal(5–)	45	GND	Ground
6	RRV5 +	Left Right Mini LVDS Receiver Signal(5+)	46	GMA 18	Gamma Voltage 18
7	RRV4 –	Left Right Mini LVDS Receiver Signal(4–)	47	GMA 16	Gamma Voltage 16
8	RRV4 +	Left Right Mini LVDS Receiver Signal(4+)	48	GMA 15	Gamma Voltage 15
9	RRV3 –	Left Right Mini LVDS Receiver Signal(3–)	49	GMA 14	Gamma Voltage 14
10	RRV3 +	Left Right Mini LVDS Receiver Signal(3+)	50	GMA 13	Gamma Voltage 13
11	GND	Ground	51	GMA 12	Gamma Voltage 12
12	RRVCLK –	Left Right Mini LVDS Receiver Clock(–)	52	GMA 10	Gamma Voltage 10
13	RRVCLK +	Left Right Mini LVDS Receiver Clock(+)	53	GMA 9	Gamma Voltage 9
14	GND	Ground	54	GMA 7	Gamma Voltage 7
15	RRV2 –	Left Right Mini LVDS Receiver Signal(2–)	55	GMA 6	Gamma Voltage 6
16	RRV2 +	Left Right Mini LVDS Receiver Signal(2+)	56	GMA 5	Gamma Voltage 5
17	RRV1 –	Left Right Mini LVDS Receiver Signal(1–)	57	GMA 4	Gamma Voltage 4
18	RRV1 +	Left Right Mini LVDS Receiver Signal(1+)	58	GMA 3	Gamma Voltage 3
19	RRV0 –	Left Right Mini LVDS Receiver Signal(0–)	59	GMA 1	Gamma Voltage 1
20	RRV0 +	Left Right Mini LVDS Receiver Signal(0+)	60	ZOUT_DOWN	LTD Output
21	GND	Ground	61	NC	No connection
22	RLV5 –	Left Left Mini LVDS Receiver Signal(5–)	62	GND	Ground
23	RLV5 +	Left Left Mini LVDS Receiver Signal(5+)	63	VCOM_R	Right Vcom Output
24	RLV4 –	Left Left Mini LVDS Receiver Signal(4–)	64	GND	Ground
25	RLV4 +	Left Left Mini LVDS Receiver Signal(4+)	65	VGH	Gate High Voltage
26	RLV3 –	Left Left Mini LVDS Receiver Signal(3–)	66	GND	Ground
27	RLV3 +	Left Left Mini LVDS Receiver Signal(3+)	67	GSC	Gate Shift Clock
28	GND	Ground	68	GOE	Gate Output Enable
29	RLVCLK –	Left Left Mini LVDS Receiver Clock(–)	69	GND	Ground
30	RLVCLK +	Left Left Mini LVDS Receiver Clock(+)	70	VGL	Gate Low Voltage
31	GND	Ground	71	OPT_N	“H” Normal Display / “L” Rotation Display
32	RLV2 –	Left Left Mini LVDS Receiver Signal(2–)	72	GND	Ground
33	RLV2 +	Left Left Mini LVDS Receiver Signal(2+)	73	HVDD	Half Driver Power Supply Voltage
34	RLV1 –	Left Left Mini LVDS Receiver Signal(1–)	74	HVDD	Half Driver Power Supply voltage
35	RLV1 +	Left Left Mini LVDS Receiver Signal(1+)	75	GND	Ground
36	RLV0 –	Left Left Mini LVDS Receiver Signal(0–)	76	VCC	Logic Power Supply Voltage
37	RLV0 +	Left Left Mini LVDS Receiver Signal(0+)	77	VCC	Logic Power Supply Voltage
38	GND	Ground	78	GND	Ground
39	OPT_P	“L” Normal Display / “H” Rotation Display	79	VDD	Driver Power Supply Voltage
40	H_CONV	Horizontal 2 Inversion Signal	80	VDD	Driver Power Supply Voltage

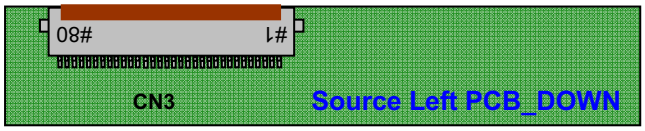
-LCD Connector (CN2): TF06L-80S-0.5SH (Manufactured by Hirose)

Table 4-4. MODULE CONNECTOR(CN4) PIN CONFIGURATION

No	Symbol	Description	No	Symbol	Description
1	VDD	Driver Power Supply Voltage	41	GND	Ground
2	VDD	Driver Power Supply Voltage	42	POL_DOWN	Polarity Output Signal
3	GND	Ground	43	NC	No connection
4	VCC	Logic Power Supply Voltage	44	H_CONV	Horizontal 2 Inversion Signal
5	VCC	Logic Power Supply Voltage	45	OPT_P	"L" Normal Display / "H" Rotation Display
6	GND	Ground	46	GND	Ground
7	HVDD	Half Driver Power Supply Voltage	47	LRV5 -	Right Right Mini LVDS Receiver Signal(5-)
8	HVDD	Half Driver Power Supply voltage	48	LRV5 +	Right Right Mini LVDS Receiver Signal(5+)
9	GND	Ground	49	LRV4 -	Right Right Mini LVDS Receiver Signal(4-)
10	VGL	Gate Low Voltage	50	LRV4 +	Right Right Mini LVDS Receiver Signal(4+)
11	GND	Ground	51	LRV3 -	Right Right Mini LVDS Receiver Signal(3-)
12	GOE	Gate Output Enable	52	LRV3 +	Right Right Mini LVDS Receiver Signal(3+)
13	GSC	Gate Shift Clock	53	GND	Ground
14	GND	Ground	54	LRVCLK -	Right Right Mini LVDS Receiver Clock(-)
15	VGH	Gate High Voltage	55	LRVCLK +	Right Right Mini LVDS Receiver Clock(+)
16	GND	Ground	56	GND	Ground
17	GND	Ground	57	LRV2 -	Right Right Mini LVDS Receiver Signal(2-)
18	VCOM_L	Left Vcom Output	58	LRV2 +	Right Right Mini LVDS Receiver Signal(2+)
19	GND	Ground	59	LRV1 -	Right Right Mini LVDS Receiver Signal(1-)
20	NC	No connection	60	LRV1 +	Right Right Mini LVDS Receiver Signal(1+)
21	ZOUT_DOWN	LTD Output	61	LRV0 -	Right Right Mini LVDS Receiver Signal(0-)
22	GND	Ground	62	LRV0 +	Right Right Mini LVDS Receiver Signal(0+)
23	GND	Ground	63	GND	Ground
24	GMA18	Gamma Voltage 18	64	LLV5 -	Right Left Mini LVDS Receiver Signal(5-)
25	GMA16	Gamma Voltage 16	65	LLV5 +	Right Left Mini LVDS Receiver Signal(5+)
26	GMA15	Gamma Voltage 15	66	LLV4 -	Right Left Mini LVDS Receiver Signal(4-)
27	GMA14	Gamma Voltage 14	67	LLV4 +	Right Left Mini LVDS Receiver Signal(4+)
28	GMA13	Gamma Voltage 13	68	LLV3 -	Right Left Mini LVDS Receiver Signal(3-)
29	GMA12	Gamma Voltage 12	69	LLV3 +	Right Left Mini LVDS Receiver Signal(3+)
30	GMA10	Gamma Voltage 10	70	GND	Ground
31	GMA9	Gamma Voltage 9	71	LLVCLK -	Right Left Mini LVDS Receiver Clock(-)
32	GMA7	Gamma Voltage 7	72	LLVCLK +	Right Left Mini LVDS Receiver Clock(+)
33	GMA6	Gamma Voltage 6	73	GND	Ground
34	GMA5	Gamma Voltage 5	74	LLV2 -	Right Left Mini LVDS Receiver Signal(2-)
35	GMA4	Gamma Voltage 4	75	LLV2 +	Right Left Mini LVDS Receiver Signal(2+)
36	GMA3	Gamma Voltage 3	76	LLV1 -	Right Left Mini LVDS Receiver Signal(1-)
37	GMA1	Gamma Voltage 1	77	LLV1 +	Right Left Mini LVDS Receiver Signal(1+)
38	GND	Ground	78	LLV0 -	Right Left Mini LVDS Receiver Signal(0-)
39	GND	Ground	79	LLV0 +	Right Left Mini LVDS Receiver Signal(0+)
40	SOE_DR	Source Output Enable	80	GND	Ground

Note : 1.Please refer to application note (Half VDD & Gamma Voltage setting & Control signal) for details.





3-2-2. Backlight Module

Board A(CN1101), Board B(CN2101)
- LED Driver Connector : 20022WR-14B1(Yeonho)
- Mating Connector : 20022HS-14 or Equivalent

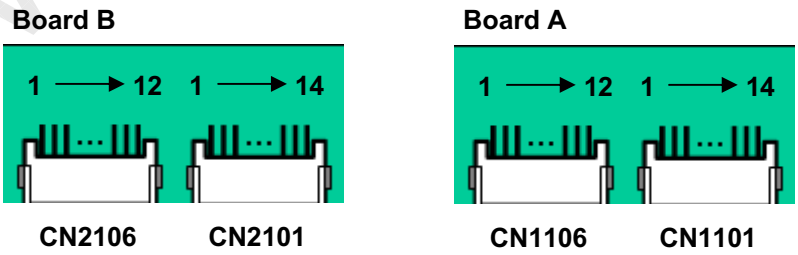
Board A(CN1106), Board B(CN2106)
- LED Driver Connector : 20022WR-12B1(Yeonho)
- Mating Connector : 20022HS-12 or Equivalent

Table 5. LED DRIVER CONNECTOR PIN CONFIGURATION

Pin No	Symbol	Description	Board A (CN1101) Board B (CN2101)	Board A (CN1106) Board B (CN2106)	Note
1	VBL	Power Supply +24.0V	VBL	VBL	
2	VBL	Power Supply +24.0V	VBL	VBL	
3	VBL	Power Supply +24.0V	VBL	VBL	
4	VBL	Power Supply +24.0V	VBL	VBL	
5	VBL	Power Supply +24.0V	VBL	VBL	
6	GND	Backlight Ground	GND	GND	
7	GND	Backlight Ground	GND	GND	
8	GND	Backlight Ground	GND	GND	1
9	GND	Backlight Ground	GND	GND	
10	GND	Backlight Ground	GND	GND	
11	NC	No connection	OPEN or GND	Don't Care	
12	VON/OFF	Backlight ON/OFF control	VON/OFF	Don't Care	
13	EXTVBR-B	External PWM	EXTVBR-B		2
14	GND	Backlight Ground	GND		3

Notes : 1. GND should be connected to the LCD module's metal frame.
2. High : on duty / Low : off duty, Pin#13 can be opened. (if Pin #13 is open , EXTVBR-B is 100%)
3. #14 of Input CNT Must be Connected to Backlight Ground.
4. Each impedance of pin #12 and 13 is over 50 [KΩ] and over 50 [KΩ].

◆ **Rear view of LCM**



3-2-3. Local Dimming Interface

Board A(CN1603)

- LED Driver Connector : 12507WR-08L(Yeonho)
- Mating Connector : 12507HS-08L(Yeonho) or Equivalent

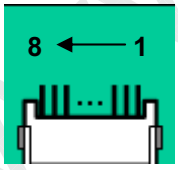
Table 5-2. LOCAL DIMMING INTERFACE CONNECTOR PIN CONFIGULATION

Pin No	Symbol	Description	Note
1	VSYNC	Vertical Sync signal	
2	GND	Backlight Ground	1
3	SIN	1'st SPI Data	
4	SCLK	1'st SPI Clock	
5	GND	Backlight Ground	1
6	SIN	2'nd SPI Data	
7	SCLK	2'nd SPI Clock	
8	GND	Backlight Ground	1

Notes : 1. GND should be connected to the LCD module's metal frame.

◆ **Rear view of LCM**

Board A



CN1603

3-3. Signal Timing Specifications

Table 6. Timing Requirements

Parameter	Symbol	Condition	Min	Typ	Max	Unit	Note
Mini Clock pulse period	T_1		3.2	3.4		ns	1
Mini Clock pulse low period	T_2		1.6	–	–	ns	
Mini Clock pulse high period	T_3		1.6	–	–	ns	
Mini Data setup time	T_6		0.5	–	–	ns	
Mini Data hold time	T_7		0.5	–	–	ns	
Reset low to SOE rising time	T_8		0	–	–	ns	
SOE to Reset input time	T_9		200	–	–	ns	
Receiver off to SOE timing	T_{10}		10	–	–	CLK cycle	
POL signal to SOE setup time	T_{11}		-5	–	–	ns	
POL signal to SOE hold time	T_{12}		6	–	–	ns	
Reset High Period	T_{13}		3			CLK cycle	
SOE signal GSP setup time	T_{14}		100			ns	
SOE signal GSP Hold time	T_{15}		100			ns	
SOE signal Pulse Width	T_{16}		200			ns	

Note : 1. Mini-LVDS timing measure conditions
: 268MHz < Clock Frequency < 312MHz , 150mV < VID < 800mV @ 3.0<VCC<3.3
2. Setup time and hold time couldn't be satisfied at the same time

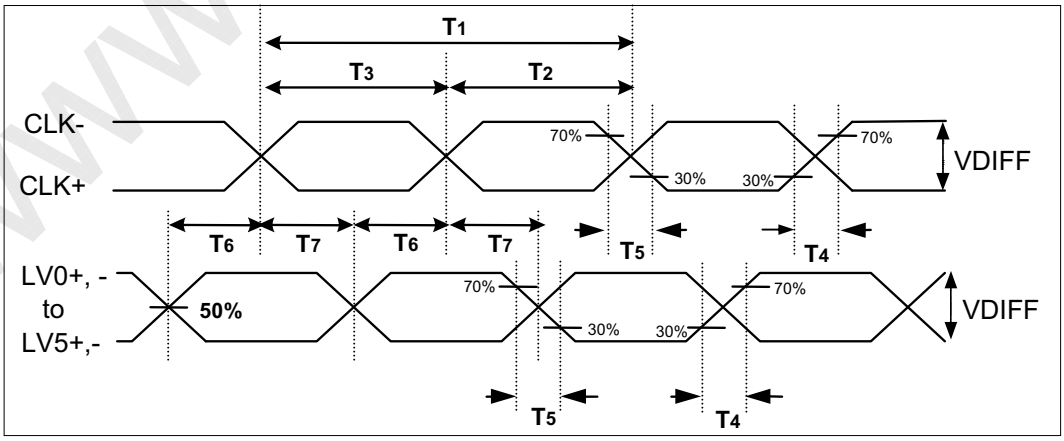


FIG 4. Source D-IC Input Data Latch Timing Waveform

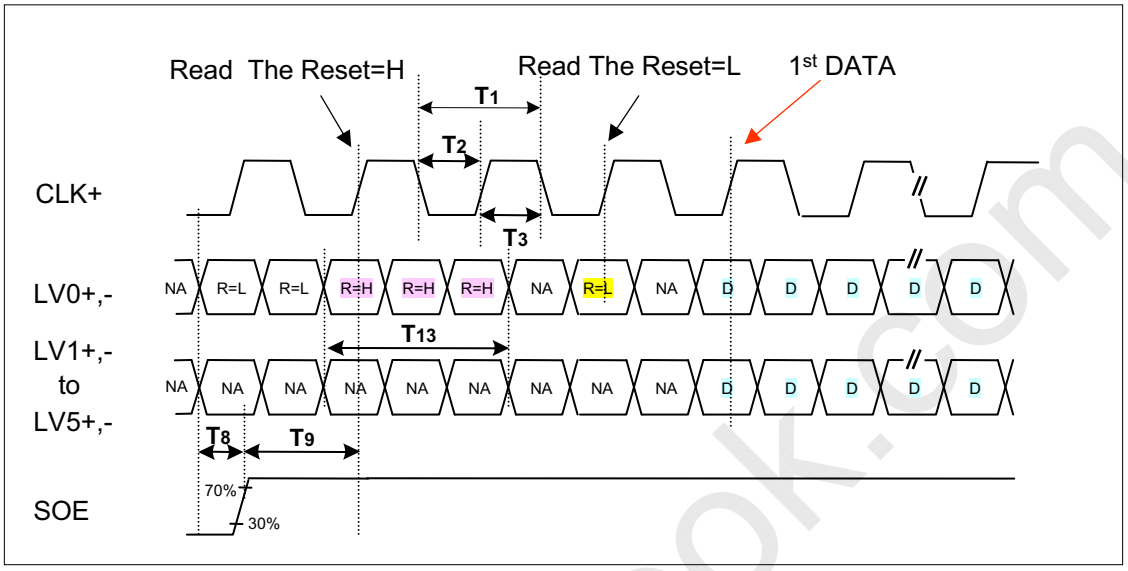


FIG 5-1. Input Data Timing for 1st Source D-IC Chip

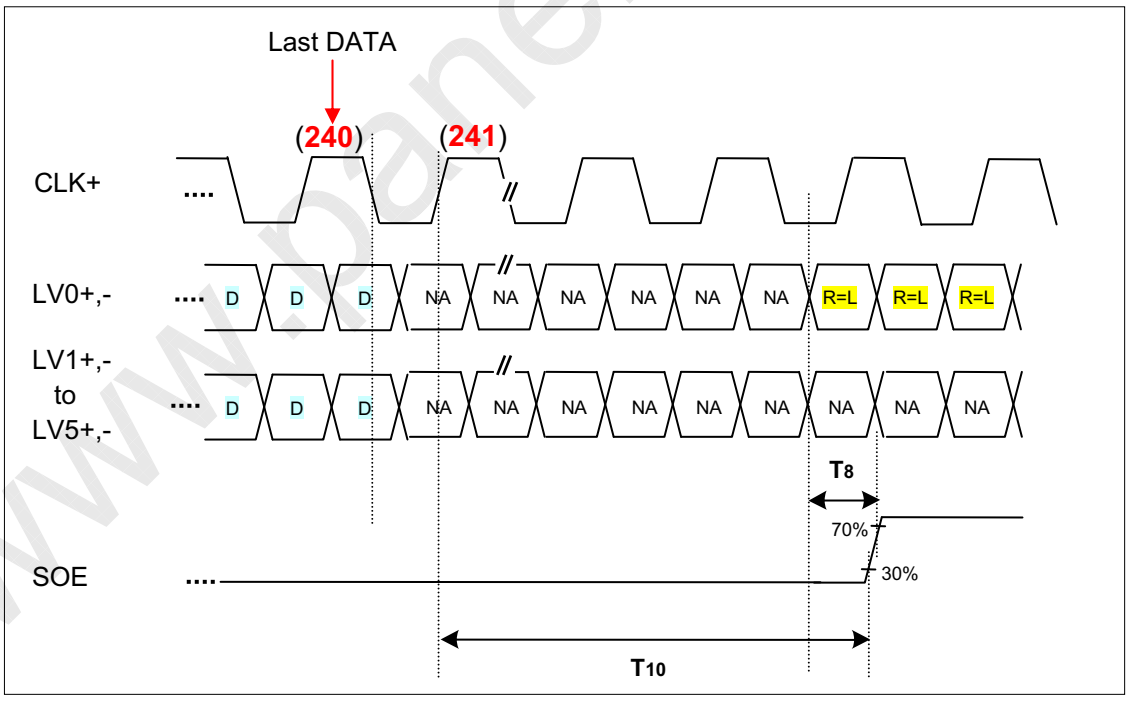


FIG 5-2. Last Data Latch to SOE Timing

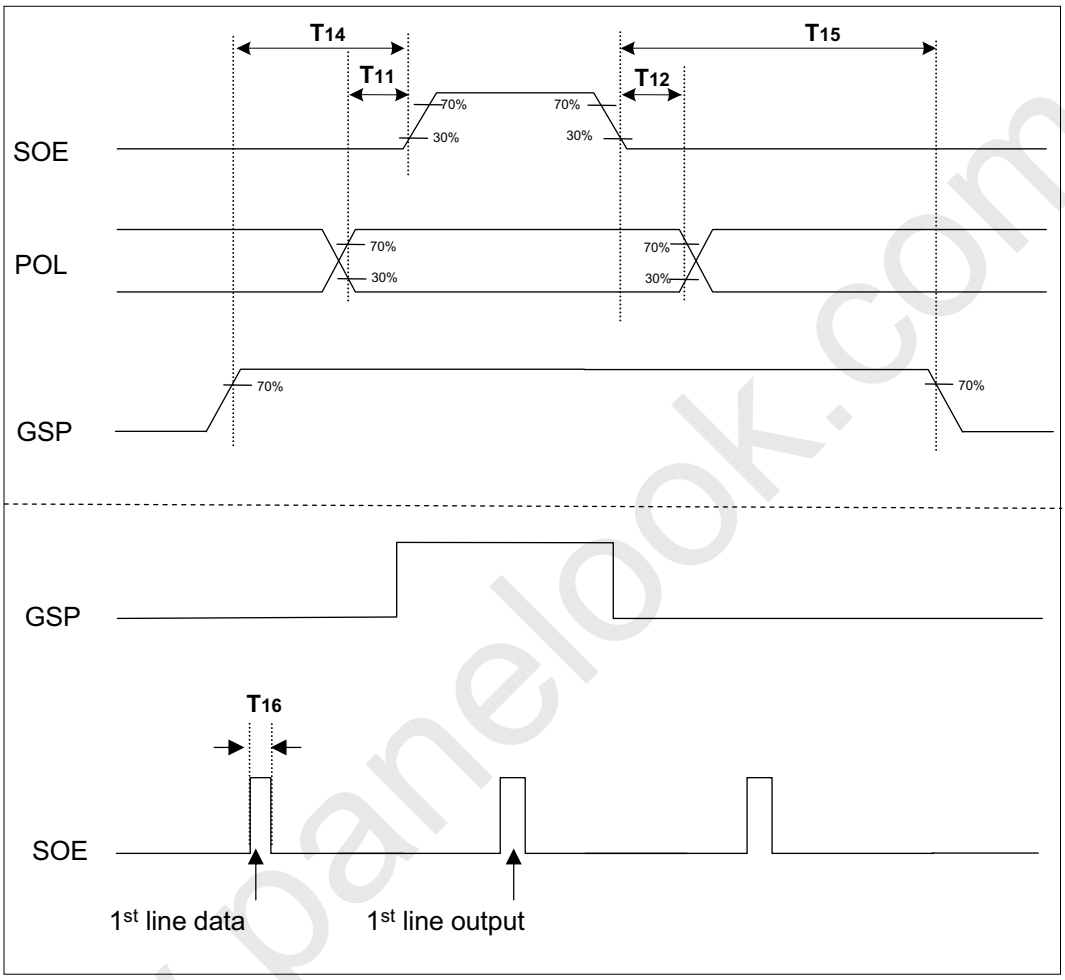
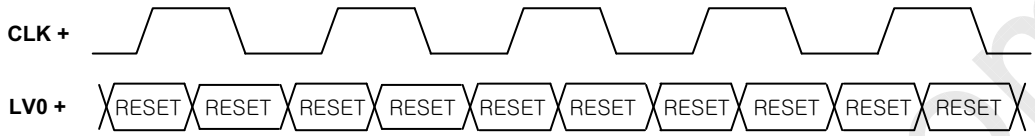


FIG 6. POL, GSP and SOE Timing Waveform

3-4. Data Mapping and Timing

Display data and control signal (RESET) are input to **LV0** to **LV5**.

3-4-1. Control signal input mode



3-4-2. Display data input mode

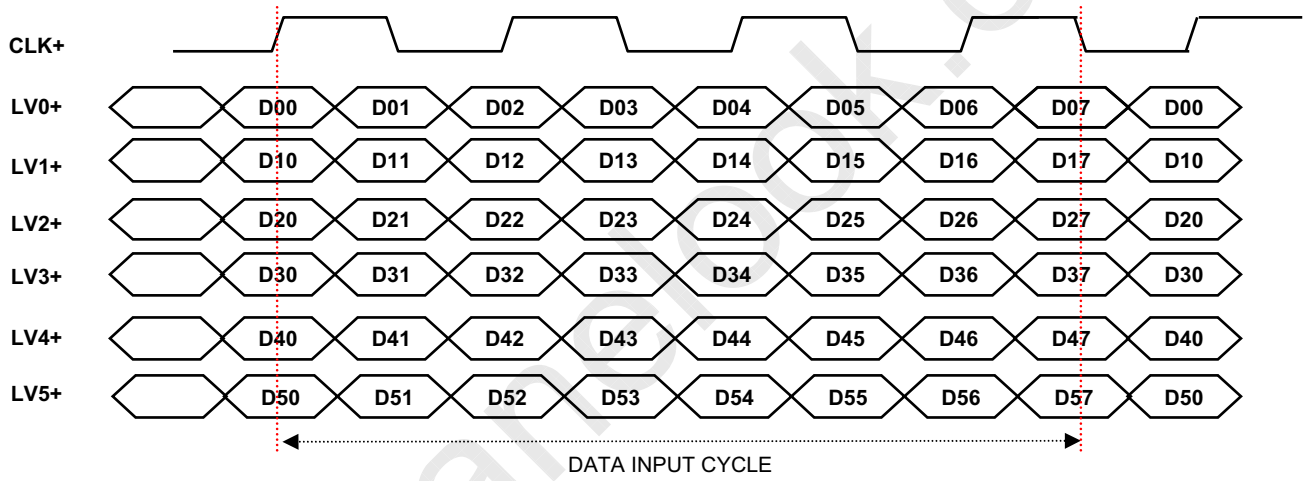


Fig. 7 Mini-LVDS Data

Note : 1. For data mapping, please refer to panel pixel structure Fig.8

3-5. Panel Pixel Structure

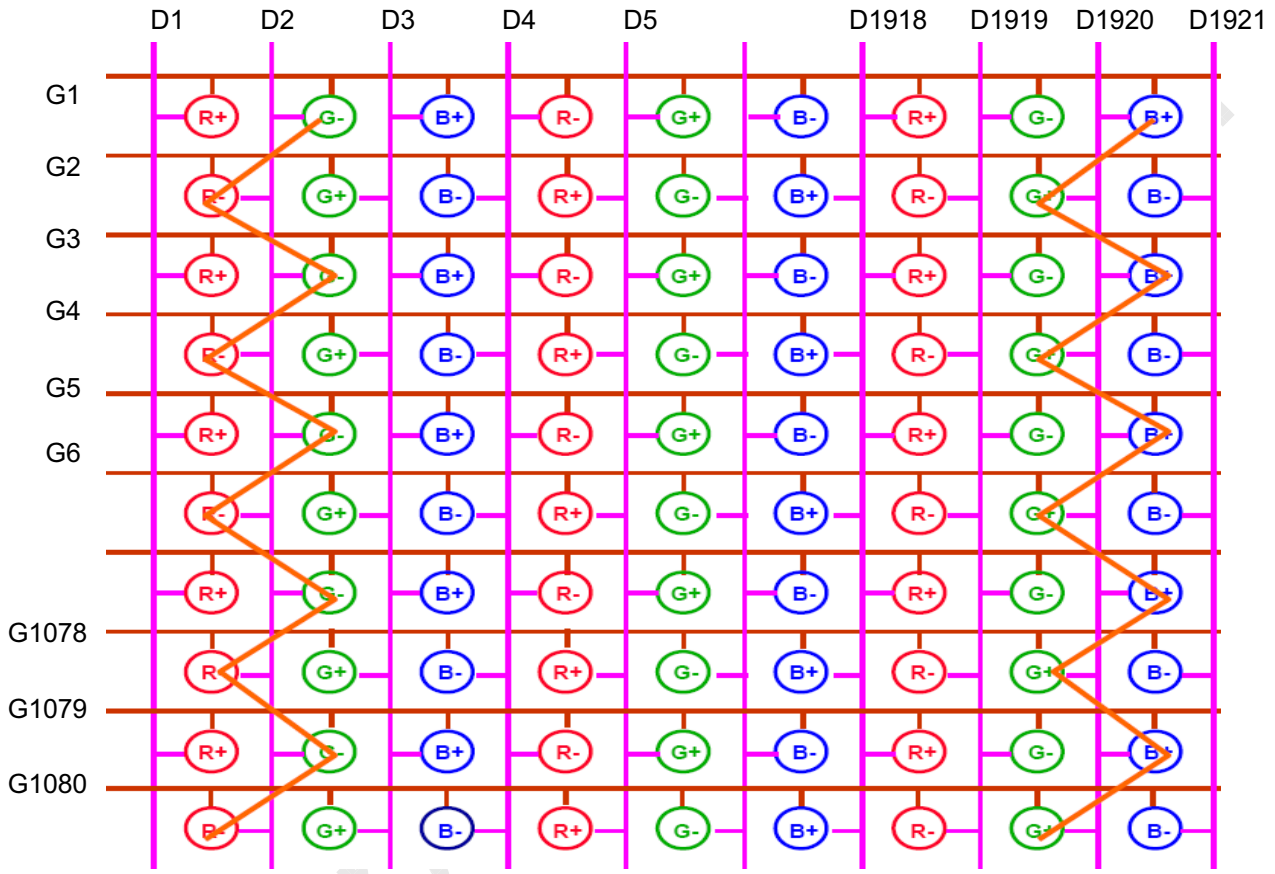


FIG. 8 Panel Pixel Structure

3-6. Power Sequence

3-6-1. LCD Driving circuit

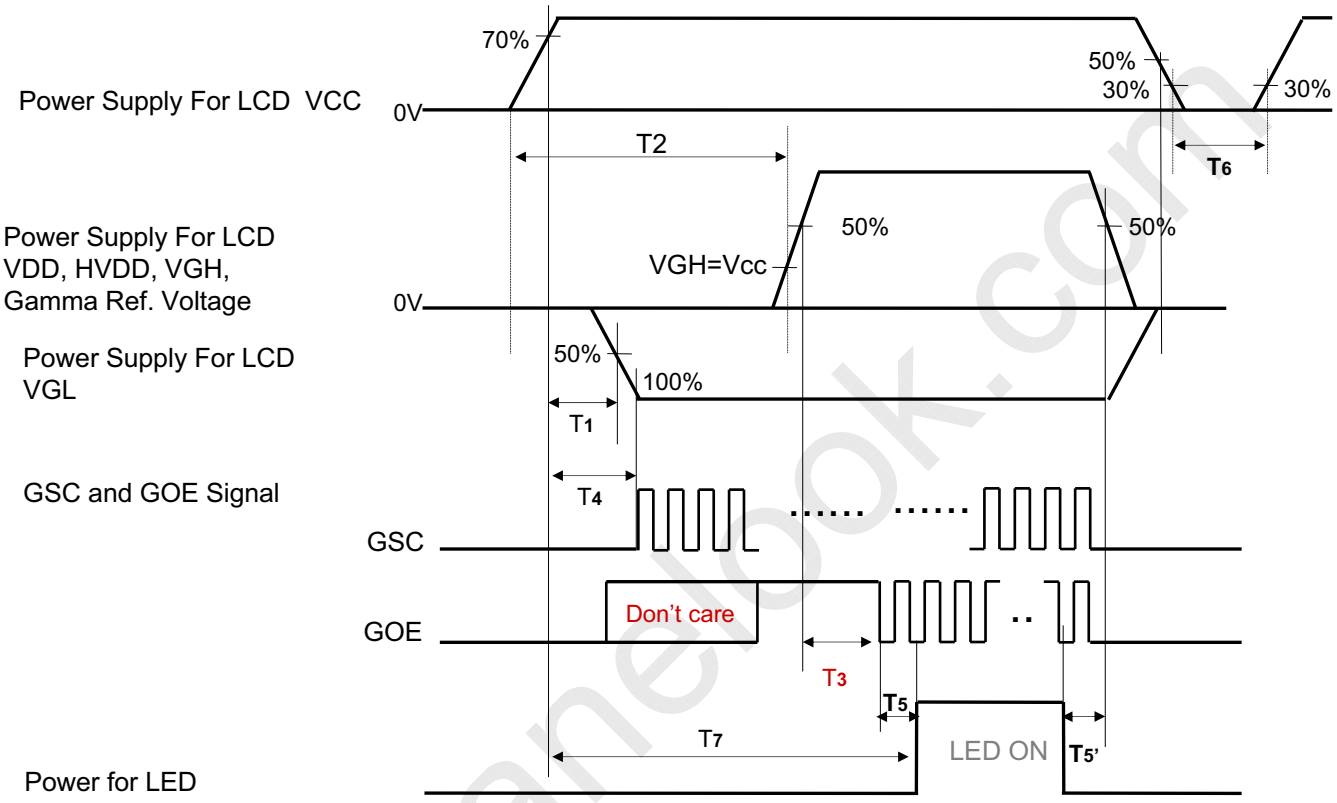


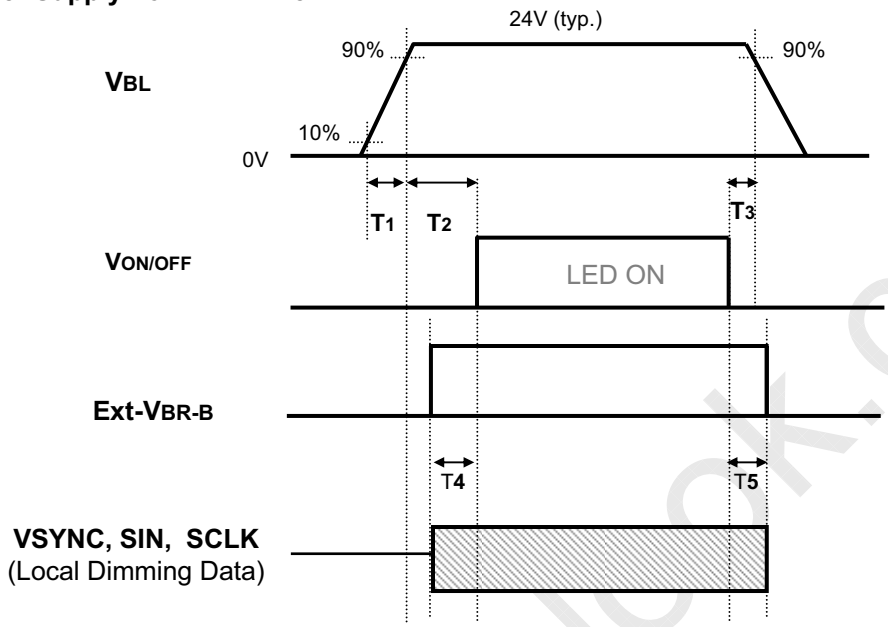
Table 7. POWER SEQUENCE

Parameter	Value			Unit	Notes
	Min	Typ	Max		
T1	0.5		-	ms	
T2	0.01		-	ms	
T3	10		-	ms	
T4	0		T2	ms	
T5 / T5'	20		-	ms	
T6	2		-	sec	
T7	0.5		-	sec	

Note : 1. Power sequence for Source D-IC must be kept. ※ Please refer to Appendix IV for more details
2. The Gate D-IC power on sequence must be VCC, VGL, logic input & VGH.
3. The 1st start of GSC is located between VGL and VGH.
4. GOE rising is before GSC.
5. Power off sequence order is reverse of power on sequence.

3-6-2. Sequence for LED Driver

Power Supply For LED Driver



3-6-3. Dip condition for LED Driver

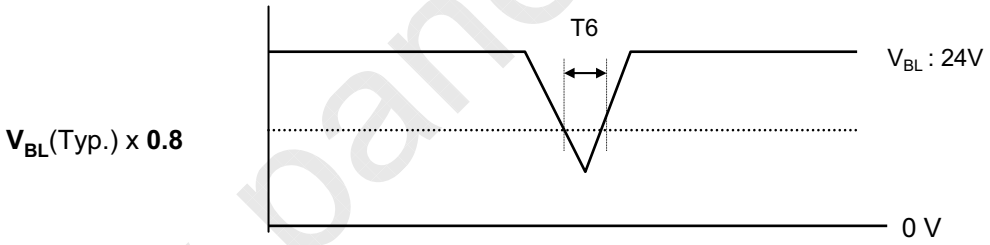


Table 9. Power Sequence for LED Driver

Parameter	Values			Units	Remarks
	Min	Typ	Max		
T1	20	–	–	ms	1
T2	500	–	–	ms	
T3	10		–	ms	
T4	0	–	–	ms	
T5	0	–	–	ms	
T6	–	–	10	ms	V_{BL}(Typ) x 0.8

Notes : 1. T1 describes rising time of 0V to 24V and this parameter does not applied at restarting time.
Even though T1 is over the specified value, there is no problem if I^2T spec of fuse is satisfied.

4. Optical Specification

Optical characteristics are determined after the unit has been 'ON' and stable in a dark environment at 25±2°C. The values are specified at an approximate distance 50cm from the LCD surface at a viewing angle of Φ and θ equal to 0 °.
It is presented additional information concerning the measurement equipment and method in FIG. 1.

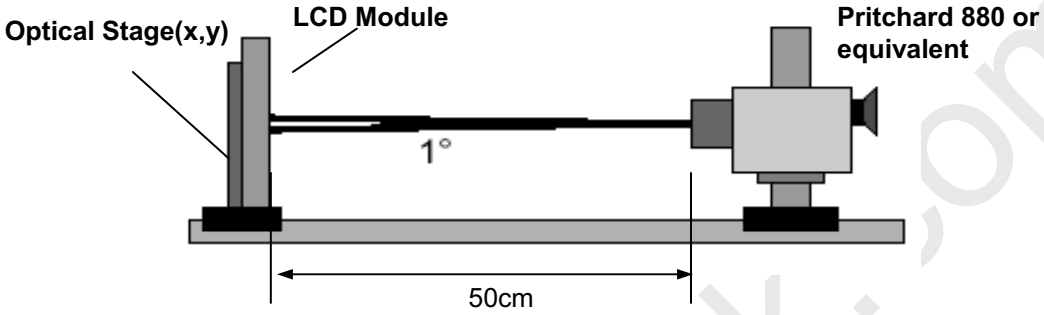


FIG. 1 Optical Characteristic Measurement Equipment and Method

Ta= 25±2°C, V_{LCD}=12.0V, fv=240Hz, Dclk=74.25MHz, **EXTV**BR-B =100%

Table 10. OPTICAL CHARACTERISTICS

Parameter		Symbol	Value			Unit	Note
			Min	Typ	Max		
Contrast Ratio		CR	1000	1200	–		1
Surface Luminance, white		L_{WH}	400	500	–	cd/m²	2
Luminance Variation		δ_{WHITE} 5P	–	–	1.3		3
Response Time (Black to White)	Rising	Tr	–	6	8	ms	4
	Falling	Tf	–	5	7		
Color Coordinates [CIE1931]	RED	Rx	Typ −0.03	0.646	Typ +0.03		
		Ry		0.330			
	GREEN	Gx		0.303			
		Gy		0.600			
	BLUE	Bx		0.152			
		By		0.059			
	WHITE	Wx		0.279			
		Wy		0.292			
Color Temperature				10,000		K	
Color Gamut				72		%	
Viewing Angle (CR>10)							
	x axis, right(ϕ=0°)	θr	89	–	–	degree	5
	x axis, left (ϕ=180°)	θl	89	–	–		
	y axis, up (ϕ=90°)	θu	89	–	–		
	y axis, down (ϕ=270°)	θd	89	–	–		
Gray Scale			–	–	–		6

Note : 1. Contrast Ratio(CR) is defined mathematically as :

$$CR = \frac{\text{Surface Luminance at all white pixels}}{\text{Surface Luminance at all black pixels}}$$

It is measured at center 1-point.

2. Surface luminance is determined after the unit has been 'ON' and 1Hour after lighting the backlight in a dark environment at 25±2°C. Surface luminance is the luminance value at center 1-point across the LCD surface 50cm from the surface with all pixels displaying white. For more information see the FIG. 10.

3. The variation in surface luminance , δ WHITE is defined as :
δ WHITE(5P) = Maximum(L_{on1},L_{on2}, L_{on3}, L_{on4}, L_{on5}) / Minimum(L_{on1},L_{on2}, L_{on3}, L_{on4}, L_{on5})
Where L_{on1} to L_{on5} are the luminance with all pixels displaying white at 5 locations .
For more information, see the FIG. 10.

4. Response time is the time required for the display to transit from G(255) to G(0) (Rise Time, Tr_R) and from G(0) to G(255) (Decay Time, Tr_D).

5. Viewing angle is the angle at which the contrast ratio is greater than 10. The angles are determined for the horizontal or x axis and the vertical or y axis with respect to the z axis which is normal to the LCD module surface. For more information, see the FIG. 12.

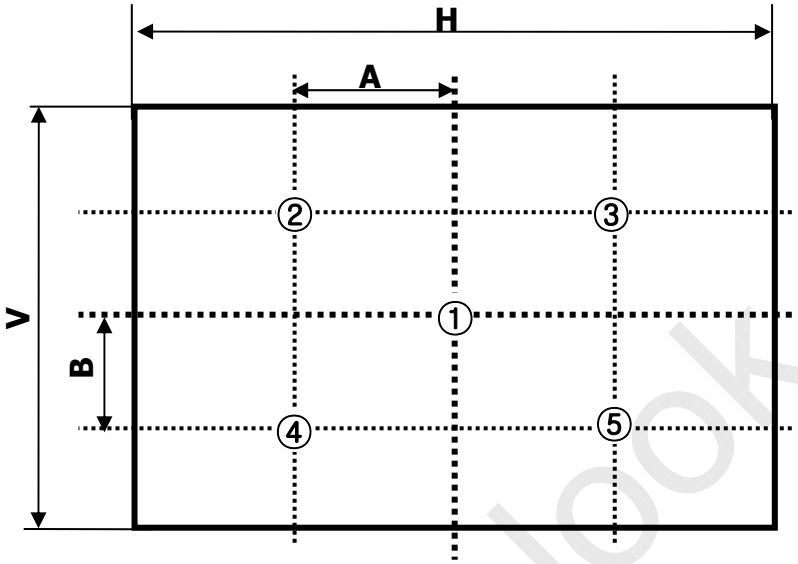
6. Gray scale specification
Gamma Value is approximately 2.2. For more information, see the Table 10.

Table 10. GRAY SCALE SPECIFICATION

Gray Level	Luminance [%] (Typ)
L0	0.08
L15	0.28
L31	1.05
L47	2.50
L63	4.69
L79	7.67
L95	11.47
L111	16.11
L127	21.64
L143	28.07
L159	35.43
L175	43.73
L191	52.99
L207	63.23
L223	74.47
L239	86.72
L255	100

	Gray Level	Gamma Ref.
Positive Voltage	L0	Gamma9
	L31	Gamma7
	L63	Gamma6
	L127	Gamma5
	L191	Gamma4
	L223	Gamma3
	L255	Gamma1
Negative Voltage	L255	Gamma18
	L223	Gamma16
	L191	Gamma15
	L127	Gamma14
	L63	Gamma13
	L31	Gamma12
	L0	Gamma10

Measuring point for surface luminance & luminance variation



A : H / 4 mm
B : V / 4 mm
@ H,V : Active Area

FIG. 10 5 Points for Luminance Measure

Response time is defined as the following figure and shall be measured by switching the input signal for Black and White

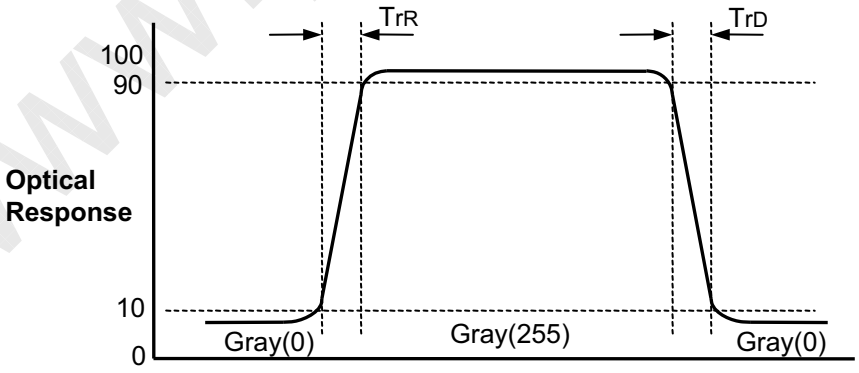


FIG. 11 Response Time

Dimension of viewing angle range

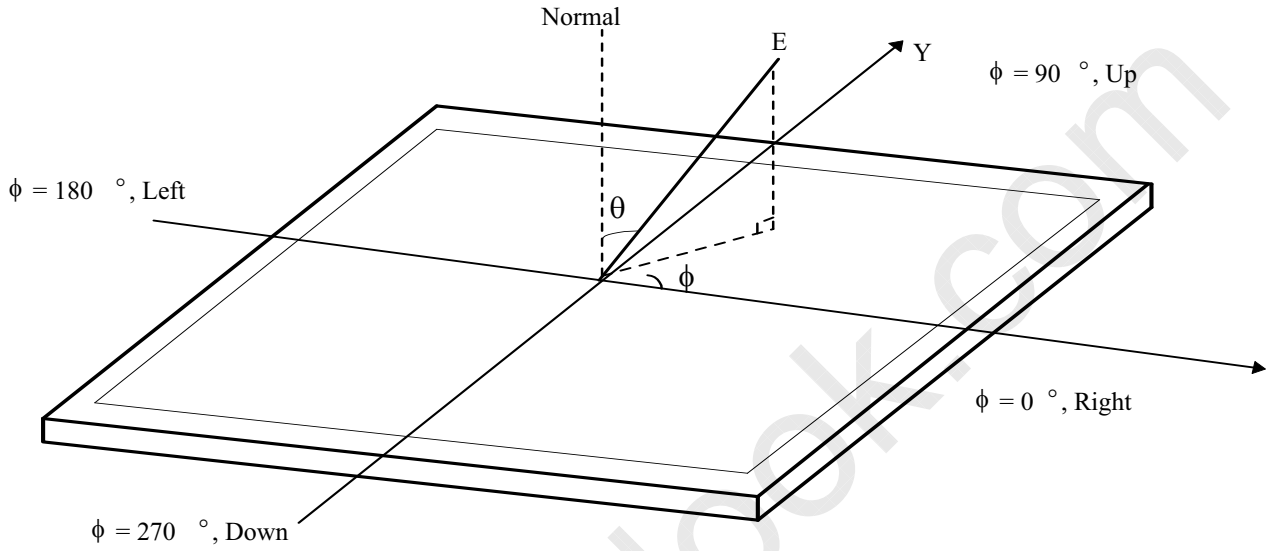


FIG.12 Viewing Angle

5. Mechanical Characteristics

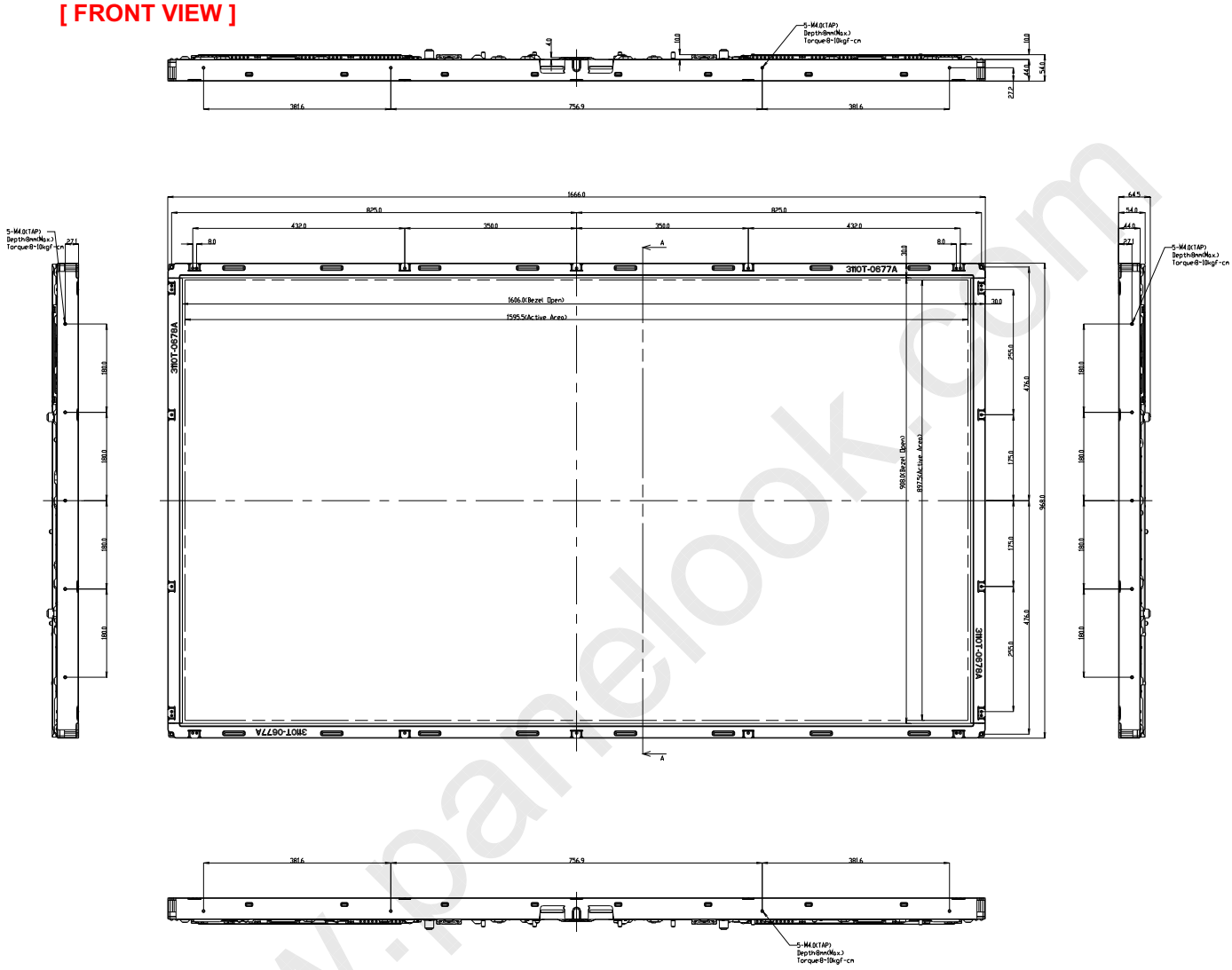
Table 11 provides general mechanical characteristics.

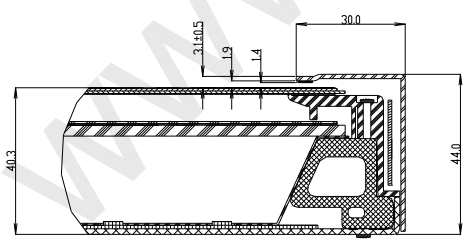
Table 11. MECHANICAL CHARACTERISTICS

Item	Value	
Outline Dimension	Horizontal	1666.0 mm
	Vertical	968.0 mm
	Depth	54.0 mm
Bezel Area	Horizontal	1606.0mm
	Vertical	908.0mm
Active Display Area	Horizontal	1595.52 mm
	Vertical	897.48 mm
Weight	37kg(Typ), 39Kg(Max)	

Note : Please refer to a mechanical drawing in terms of tolerance at the next page.

[FRONT VIEW]

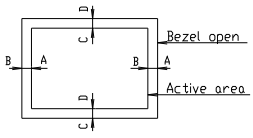




SECTION A-A

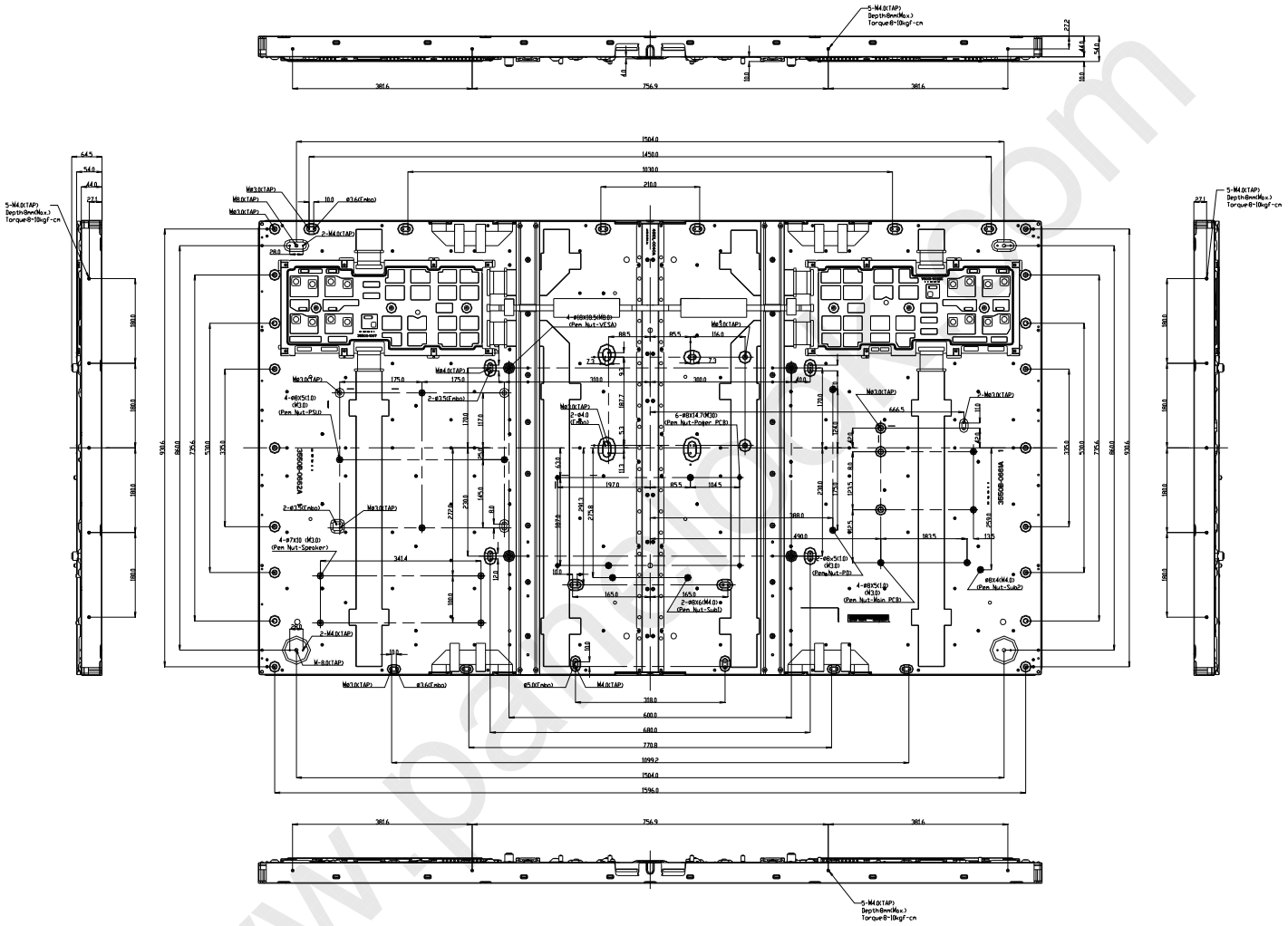
NOTES

1. Unspecified tolerances are to be ±1.0mm.
2. Tilt and partial disposition tolerance of display area are as following.
   (1) X-Direction : |A-B| ≤ 1.5mm
   (2) Y-Direction : |C-D| ≤ 1.5mm



3. Torque : 3.5 ~ 5.0Kgf.cm
4. This part should be contains Eco-hazardous substances (Pb, Cd, Hg, Cr6+, PBB, PBDE, etc.) within standard level of LG Display, Details should be followed Green Procurement standard[B-8022].
   Especially, Part should be followed and controlled the following specifications.
   (1) Eco-hazardous substances test report should be submitted when Part certification test and First Mass Production.
   (2) Don't flow Eco-hazardous substances into resin by using scrap.
   (3) Don't flow Eco-hazardous substances into metal by using impurities or improper stuff.

[REAR VIEW]



6. Reliability

Table 12. ENVIRONMENT TEST CONDITION

No.	Test Item	Condition
1	High temperature storage test	Ta= 60°C 240h
2	Low temperature storage test	Ta= -20°C 240h
3	High temperature operation test	Ta= 50°C 50%RH 240h
4	Low temperature operation test	Ta= 0°C 240h
5	Vibration test (non-operating)	Wave form : random Vibration level : 1.0Grms Bandwidth : 10-300Hz Duration : X,Y,Z, 30 min Each direction per 10 min
6	Humidity condition Operation	Ta= 40 °C ,90%RH
7	Altitude operating storage / shipment	0 - 15,000 ft 0 - 40,000 ft

Note : Before and after Reliability test, LCM should be operated with normal function.

7. International Standards

7-1. Safety

a) UL 60065, Seventh Edition, Underwriters Laboratories Inc.
Audio, Video and Similar Electronic Apparatus - Safety Requirements.

b) CAN/CSA C22.2 No.60065:03, Canadian Standards Association.
Audio, Video and Similar Electronic Apparatus - Safety Requirements.

c) EN 60065:2002 + A11:2008, European Committee for Electrotechnical Standardization (CENELEC).
Audio, Video and Similar Electronic Apparatus - Safety Requirements.

d) IEC 60065:2005 + A1:2005, The International Electrotechnical Commission (IEC).
Audio, Video and Similar Electronic Apparatus - Safety Requirements.
(Including report of IEC60825-1:2001 clause 8 and clause 9)

Notes

1. Laser (LED Backlight) Information

Class 1M LED Product IEC60825−1 : 2001 Embedded LED Power (Class 1M)

2. Caution
: LED inside.
Class 1M laser (LEDs) radiation when open.
Do not open while operating.

7-2. EMC

a) ANSI C63.4 "American National Standard for Methods of Measurement of Radio-Noise Emissions from Low-Voltage Electrical and Electronic Equipment in the Range of 9 kHz to 40 GHz." American National Standards Institute (ANSI), 2003.

b) CISPR 22 "Information technology equipment – Radio disturbance characteristics – Limit and methods of measurement." International Special Committee on Radio Interference (CISPR), 2005.

c) CISPR 13 "Sound and television broadcast receivers and associated equipment – Radio disturbance characteristics – Limits and method of measurement." International Special Committee on Radio Interference (CISPR), 2006.

7-3. Environment

a) RoHS, Directive 2002/95/EC of the European Parliament and of the council of 27 January 2003

8. Packing

8-1. Information of LCM Label

a) Lot Mark

A	B	C	D	E	F	G	H	I	J	K	L	M

A,B,C : SIZE(INCH)
D : YEAR
E : MONTH
F ~ M : SERIAL NO.

Note

1. YEAR

Year	2011	2012	2013	2014	2015	2016	2017	2018	2019	2020
Mark	A	B	C	D	E	F	G	H	J	K

2. MONTH

Month	Jan	Feb	Mar	Apr	May	Jun	Jul	Aug	Sep	Oct	Nov	Dec
Mark	1	2	4	4	5	6	7	8	9	A	B	C

b) Location of Lot Mark

Serial NO. is printed on the label. The label is attached to the backside of the LCD module.
This is subject to change without prior notice.

8-2. Packing Form

a) Package quantity in one Pallet : 6ea

b) Pallet Size : 1900mm X 1140mm X 1248mm

9. Precautions

Please pay attention to the followings when you use this TFT LCD module.

9-1. Mounting Precautions

(1) You must mount a module using specified mounting holes (Details refer to the drawings).
(2) You should consider the mounting structure so that uneven force (ex. Twisted stress) is not applied to the module. And the case on which a module is mounted should have sufficient strength so that external force is not transmitted directly to the module.
(3) Please attach the surface transparent protective plate to the surface in order to protect the polarizer. Transparent protective plate should have sufficient strength in order to the resist external force.
(4) You should adopt radiation structure to satisfy the temperature specification.
(5) Acetic acid type and chlorine type materials for the cover case are not desirable because the former generates corrosive gas of attacking the polarizer at high temperature and the latter causes circuit break by electro-chemical reaction.
(6) Do not touch, push or rub the exposed polarizers with glass, tweezers or anything harder than HB pencil lead. And please do not rub with dust clothes with chemical treatment.
Do not touch the surface of polarizer for bare hand or greasy cloth.(Some cosmetics are detrimental to the polarizer.)
(7) When the surface becomes dusty, please wipe gently with absorbent cotton or other soft materials like chamois soaks with petroleum benzine. Normal-hexane is recommended for cleaning the adhesives used to attach front / rear polarizers. Do not use acetone, toluene and alcohol because they cause chemical damage to the polarizer.
(8) Wipe off saliva or water drops as soon as possible. Their long time contact with polarizer causes deformations and color fading.
(9) Do not open the case because inside circuits do not have sufficient strength.

9-2. Operating Precautions

(1) The spike noise causes the mis-operation of circuits. It should be lower than following voltage :
V=±200mV(Over and under shoot voltage)
(2) Response time depends on the temperature.(In lower temperature, it becomes longer.)
(3) Brightness depends on the temperature. (In lower temperature, it becomes lower.)
And in lower temperature, response time(required time that brightness is stable after turned on) becomes longer
(4) Be careful for condensation at sudden temperature change.Condensation makes damage to polarizer or electrical contacted parts. And after fading condensation, smear or spot will occur.
(5) When fixed patterns are displayed for a long time, remnant image is likely to occur.
(6) Module has high frequency circuits. Sufficient suppression to the electromagnetic interference shall be done by system manufacturers. Grounding and shielding methods may be important to minimized the interference.
(7) Please do not give any mechanical and/or acoustical impact to LCM. Otherwise, LCM can't be operated its full characteristics perfectly.
(8) A screw which is fastened up the steels should be a machine screw.
(if not, it can causes conductive particles and deal LCM a fatal blow)
(9) Please do not set LCD on its edge.
(10) The conductive material and signal cables are kept away from LED driver inductor to prevent abnormal display, sound noise and temperature rising.

9-3. Electrostatic Discharge Control

Since a module is composed of electronic circuits, it is not strong to electrostatic discharge. Make certain that treatment persons are connected to ground through wrist band etc. And don't touch interface pin directly.

9-4. Precautions for Strong Light Exposure

Strong light exposure causes degradation of polarizer and color filter.

9-5. Storage

When storing modules as spares for a long time, the following precautions are necessary.

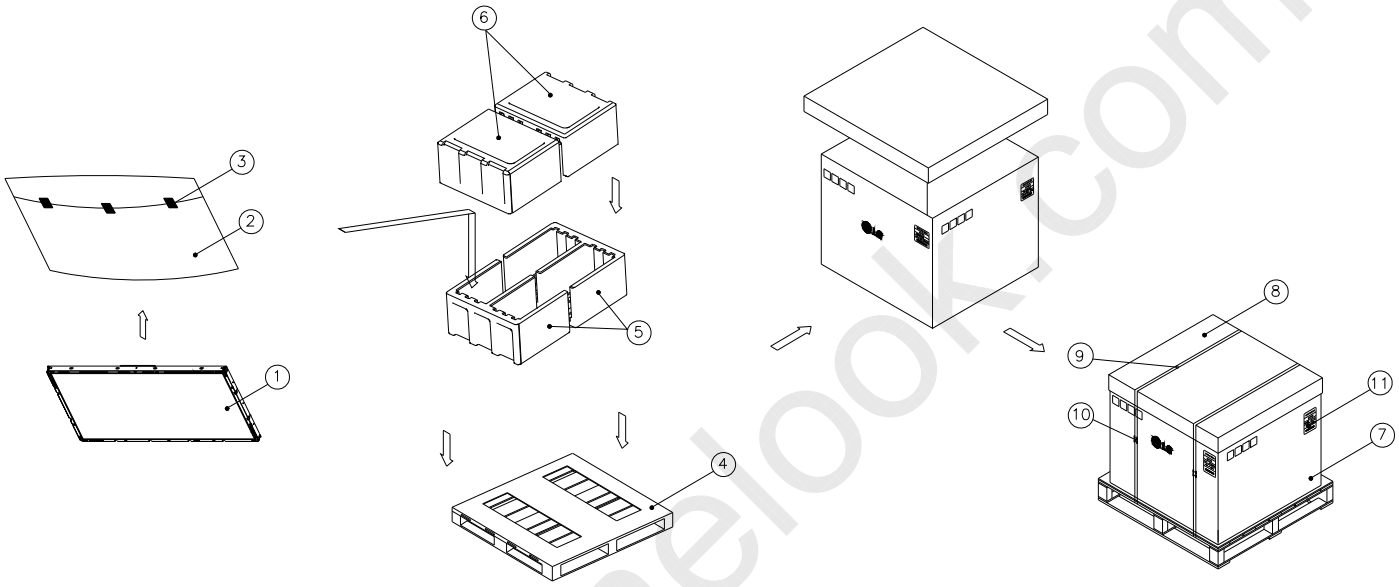
(1) Store them in a dark place. Do not expose the module to sunlight or fluorescent light. Keep the temperature between 5°C and 35°C at normal humidity.
(2) The polarizer surface should not come in contact with any other object.
It is recommended that they be stored in the container in which they were shipped.

9-6. Handling Precautions for Protection Film

(1) The protection film is attached to the bezel with a small masking tape.
When the protection film is peeled off, static electricity is generated between the film and polarizer.
This should be peeled off slowly and carefully by people who are electrically grounded and with well ion-blown equipment or in such a condition, etc.
(2) When the module with protection film attached is stored for a long time, sometimes there remains a very small amount of glue still on the bezel after the protection film is peeled off.
(3) You can remove the glue easily. When the glue remains on the bezel surface or its vestige is recognized, please wipe them off with absorbent cotton waste or other soft material like chamois soaked with normal-hexane.

APPENDIX-I

■ LC720DUC-SCM1 – Pallet Ass'y



NO.	DESCRIPTION	MATERIAL
1	LCD Module	
2	BAG	72INCH
3	TAPE	MASKING 20MM X 50M
4	PALLET	Plywood (1900X1140X126.5)
5	PACKING	EPS
6	PACKING	EPS
7	ANGLE PACKING	PAPER
8	ANGLE COVER	PAPER
9	BAND,CLIP	STEEL
10	BAND	PP
11	LABEL	YUPO PAPER 80G 100X70

 # APPENDIX- II-1

■ LC720DUC-SCM1-LCM Label