Ordering number: EN 2890

CMOS LSI

No.2890

LC7070N,7070NM,7071NM

Sync and Error Detection & Correction LSIs for RDS

Overview

The LC7070N, LC7070NM and LC7071NM CMOS Sync and Error Detection & Correction LSIs are designed for use in the RDS (Radio Data System) implemented by the EBU (European Broadcasting Union). RDS is used to multiplex various data on the FM broadcast signal.

When used with the Sanyo LA2231 RDS Decoder LSI, a simplified processor can be designed for demodulation, synchronization, and error detection & correction of the data multiplexed on the FM broadcast, significantly reducing the front-end load on the system controller.

The data with adjusted sync are obtained as a serial signal output which can be passed to the system controller for processing.

LC7070×× devices are fabricated using a low-power CMOS process and are available in 18-pin plastic DIPs and MFPs with and without output pull-ups.

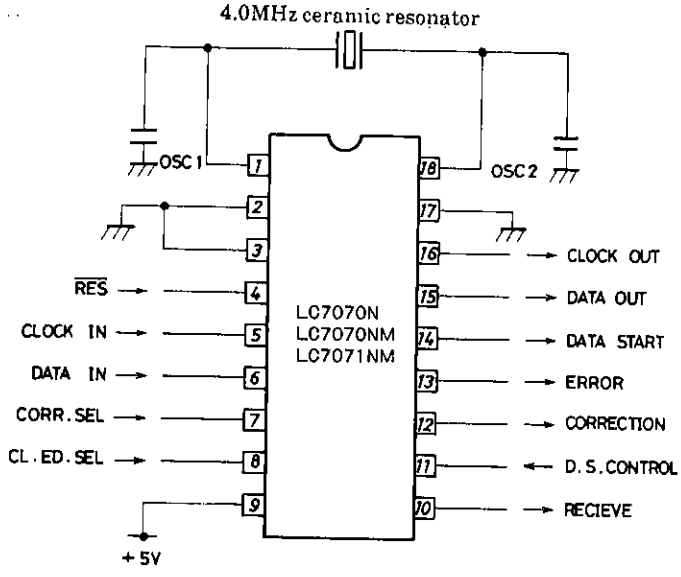
Features

- Group synchronization
- Selectable error detection & correction
- Serial data output
- Selectable serial data clock polarity
- Block DATA START signal output
- Low-power CMOS
- Single +5V supply
- 18-pin plastic DIP or MFP
- Optional pull-ups on serial data outputs.

Type No.	Package	Output Pull-up
LC7070N	DIP18	No
LC7070NM	MFP18	No
LC7071NM	MFP18	Yes*

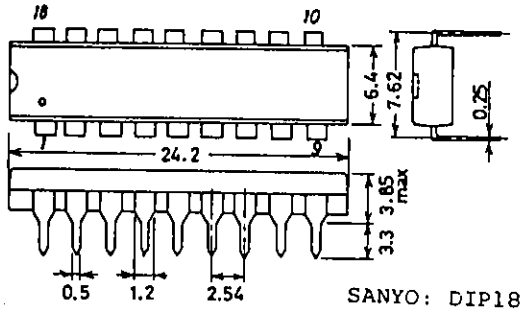
*: Only 3 pins for serial data output

Pin Assignment



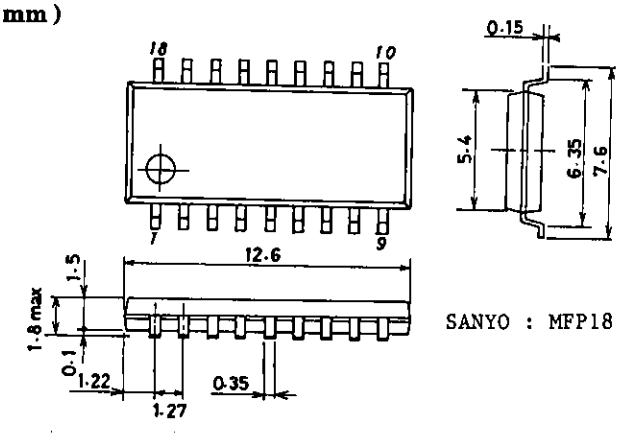
DIP <LC7070N>

Package Dimensions 3007A-D18IC
(unit: mm)



MFP <LC7070NM, LC7071NM>

Package Dimensions 3095-M18IC
(unit: mm)



Absolute Maximum Ratings at Ta = 25°C, V_{SS} = 0V

Parameter	Symbol	Conditions	Applicable Pin/ Package	Limits	unit
Maximum Supply Voltage	V_{DD} max		V_{DD}	−0.3 to +7.0	V
Output Voltage	$V_{O(1)}$		OSC 2	−0.3 to V_{DD}+0.3	V
Input Voltage	$V_{I(1)}$		OSC 1 (See Note 1.)	−0.3 to V_{DD}+0.3	V
	$V_{I(2)}$		TEST, $\overline{RES}$	−0.3 to V_{DD}+0.3	V
	$V_{I(3)}$		IN type 1 (See Note 2.)	−0.3 to +15	V
Output Voltage	$V_{O(2)}$		OUT type 1,2 (See Note 2.)	−0.3 to +15	V
Peak Output Current	I_{OP}	Peak current for each pin	OUT type 1,2 (See Note 2.)	−2 to +20	mA
Average Output Voltage (100ms interval)	I_{OA}	Average current for each pin	OUT type 1,2 (See Note 2.)	−2 to +20	mA
	ΣI_{OA}	Total current for all pins	OUT type 1,2 (See Note 2.)	−14 to +90	mA
Allowable Power Dissipation	Pd max	Ta = −40 to +85°C	DIP package	280	mW
			MFP package (See Note 3.)	200	mW
Operating Temperature	**Topr**			−40 to +85	°C
Storage Temperature	Tstg			−55 to +125	°C

Allowable Operating Conditions (at Ta = −40 to +85°C, V_{SS} = 0V, V_{DD} = 4.5 to 6.0V, unless otherwise specified.)

Parameter	Symbol	Conditions	Applicable Pin/ Package	Rating			unit
				min	typ	max	
Operating Supply Voltage	V_{DD}		V_{DD}	4.5		6.0	V
'H'-Level Input Voltage	$V_{IH(1)}$		IN type 1 (See Note 2.)	0.7V_{DD}		+13.5	V
	$V_{IH(2)}$		$\overline{RES}$	0.8V_{DD}		V_{DD}	V
'L'-Level Input Voltage	$V_{IL(1)}$		IN type 1 (See Note 2.)	V_{SS}		0.3V_{DD}	V
	$V_{IL(2)}$		TEST	V_{SS}		0.3V_{DD}	V
	$V_{IL(3)}$		$\overline{RES}$	V_{SS}		0.25V_{DD}	V
Guaranteed Constants for Ceramic Resonator Oscillation		See Figure 1.	OSC1,OSC2	See Table 1.			

Electrical Characteristics (at Ta = −40 to +85°C, V_{SS} = 0V, V_{DD} = 4.5 to 6.0V, unless otherwise specified.)

Parameter	Symbol	Conditions	Applicable Pin/ Package	Rating			unit
				min	typ	max	
'H'-Level Input Current	$I_{IH(1)}$	V_{IN} = +13.5V	IN type 1 (See Note 2.)			+5.0	μA
'L'-Level Input Current	$I_{IL(1)}$	V_{IN} = V_{SS}	IN type 1 (See Note 2.)	−1.0			μA
	$I_{IL(2)}$	V_{IN} = V_{SS}	$\overline{RES}$	−45	−10		μA
'H'-Level Output Voltage (LC7071NM only)	$V_{OH(1)}$	I_{OH} = −50μA	OUT type 2 (See Note 2.)	V_{DD} −1.2			V
	$V_{OH(2)}$	I_{OH} = −10μA	OUT type 2 (See Note 2.)	V_{DD} −0.5			V
'L'-Level Output Voltage	$V_{OL(1)}$	I_{OL} = 10mA	OUT type 1,2 (See Note 2.)			1.5	V
	$V_{OL(2)}$	I_{OL} = 1.8mA (See Note 4.)	OUT type 1,2 (See Note 2.)			0.4	V
Output OFF Leak Current (LC7071NM is OUT type 1 only.)	$I_{OFF(1)}$	V_O = 13.5V	OUT type 1,2 (See Note 2.)			+5.0	μA
	$I_{OFF(2)}$	V_O = V_{SS}	OUT type 1,2 (See Note 2.)	−1.0			μA
Hysteresis Voltage	V_{HIS}		$\overline{RES}$		0.1V_{DD}		V
Current Dissipation (See Note 5.)	I_{DD}	Using circuit shown in Figure 1.	V_{DD}		4.0	10	mA
Ceramic Resonator Oscillation Stabilization Time	t_{CFS}	See Figure 2.	OSC1,OSC2			10	ms
Reset Time	t_{RST}			See Figure 3.			

(Note 1) Should be sufficient for oscillation amplitude when oscillator circuit shown in Figure 1 is operated at recommended constants.
(Note 2) OUT type 1: ERROR, CORRECTION, RECEIVE
OUT type 2: CLOCK OUT, DATA OUT, DATA START
IN type 1 : CLOCK IN, DATA IN, CORR.SEL, CL.ED.SEL, D.S.CONTROL
(Note 3) Do not use solder dip (dipping in solder tank) when mounting MFP packaged devices to circuit board.
(Note 4) Except for four selectable output pins, other outputs are I_{OL} at less than 1mA.
(Note 5) Current dissipation with N-channel output transistors OFF, and input and output pin voltages = V_{DD}.

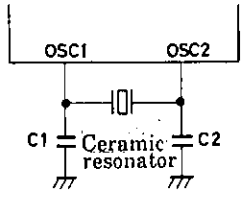


Figure 1. Oscillator Circuit

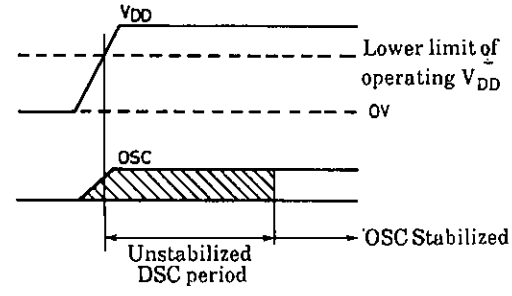


Figure 2. Stabilization Time

Table 1. Guaranteed Constants

4MHz	CSA4.00MG (Murata)	C_1	30pF±10%
		C_2	30pF±10%
	KBR4.0M (Kyocera)	C_1	33pF±10%
		C_2	33pF±10%

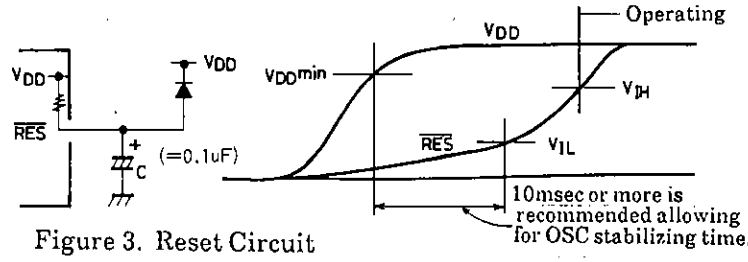
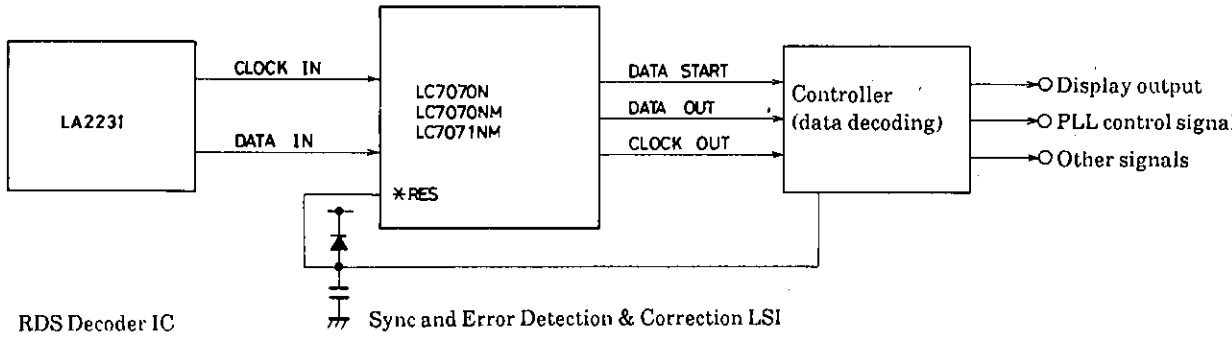


Figure 3. Reset Circuit

Pin Descriptions

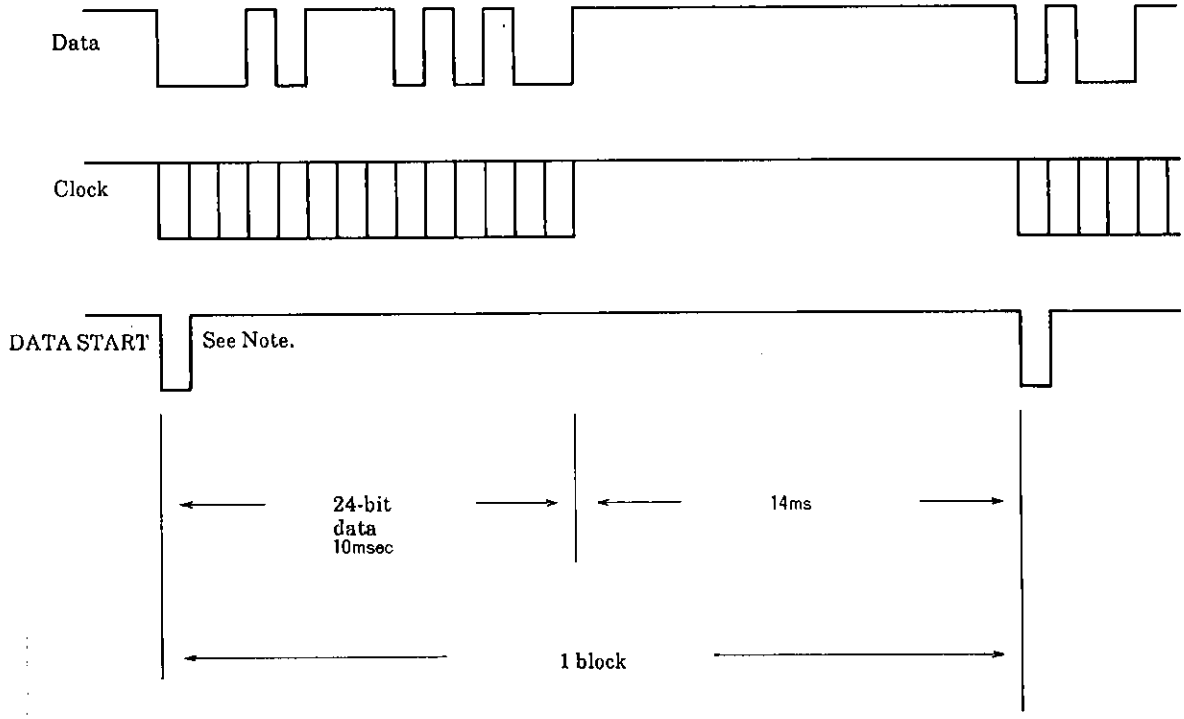
Signal	Pin No.	Input/ Output	Function	State on Reset
OSC1 OSC2	1 18	Input Output	· 4MHz ceramic resonator connection	
CLOCK IN	5	Input	· RDS (LA2231) demodulation clock input	'H'-level output
DATA IN	6	Input	· RDS (LA2231) demodulation data input	'H'-level output
CORR. SEL	7	Input	· Error correction ON/OFF select · Sets/inhibits error correction for RDS demodulation data. Input=0 : No correction Input=1 : Correction performed	'H'-level output
CL. ED. SEL	8	Input	· Serial data clock polarity select Input=0 : Serial data output enabled at rising edge of output clock (data update at falling edge). Input=1 : Serial data output enabled at falling edge of output clock (data update at rising edge). Note : Set at time of $\overline{RES}$ input.	'H'-level output
D. S. CONTROL	11	Input	· Block DATA START signal control Input=0 : All block DATA START signal output Input=1 : Only #2 block DATA START signal output	'H'-level output
RECEIVE	10	Output	· Output when receiving RDS data signal. · LOW-level during serial data output after sync detection. HIGH-level at other times. · Open drain	'H'-level output
CORRECTION	12	Output	· Error correction enable · LOW-level if serial data error is corrected or uncorrectable. HIGH-level if no corrections are required. · Open drain	'H'-level output
ERROR	13	Output	· Error correction enable · LOW-level if there are errors and they are uncorrectable. HIGH-level if there are no errors or correction is completed. · Open drain	'H'-level output
DATA START	14	Output	· Block DATA START signal for serial data output. Open drain : LC7070N, LC7070NM Pull-up : LC7071NM	'H'-level output
DATA OUT	15	Output	· Serial data Open drain : LC7070N, LC7070NM Pull-up : LC7071NM	'H'-level output
CLOCK OUT	16	Output	· Serial data clock Open drain : LC7070N, LC7070NM Pull-up : LC7071NM	'H'-level output
$\overline{RES}$	4	Input	· System reset · LOW-level for more than 4 clock cycles	

System Configuration

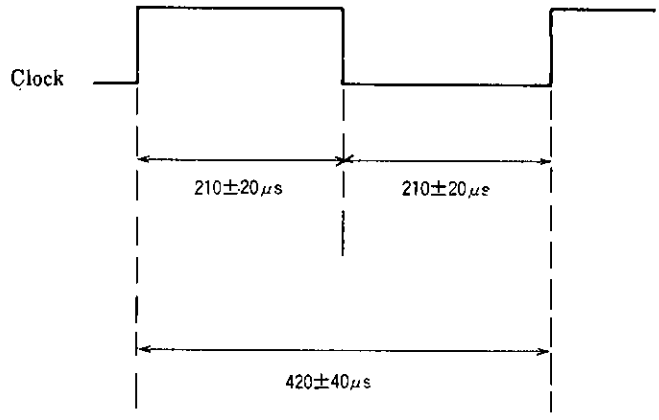


Timing Charts & Data Format

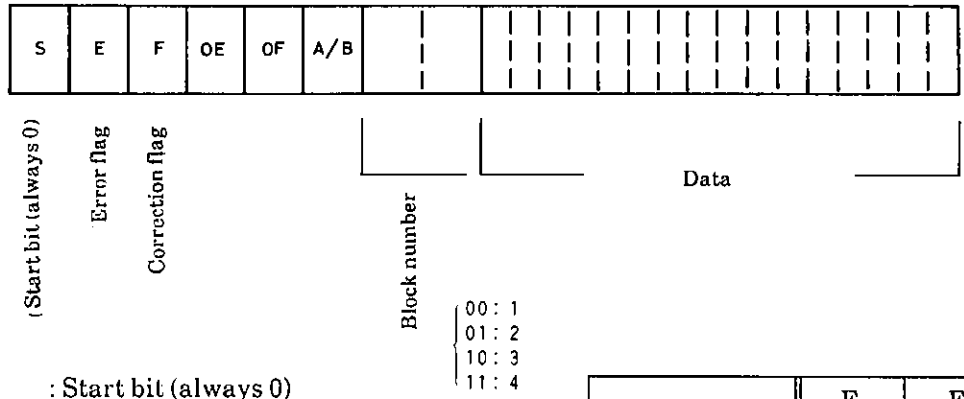
Serial Data Output



Note : All blocks or second block-only output selectable using D. S. CONTROL input.



Serial Data Output Format

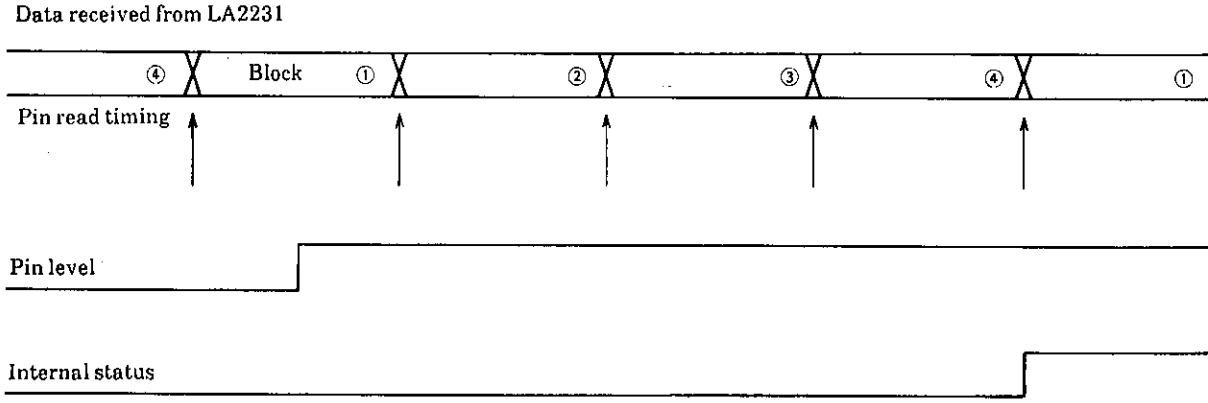


S : Start bit (always 0)
E : Error flag
F : Correction flag
OE : Offset E
OF : Offset F
A/B : Group type
0 Version A
1 Version B

	E	F
No errors	0	0
Corrected	0	1
Uncorrectable	1	1

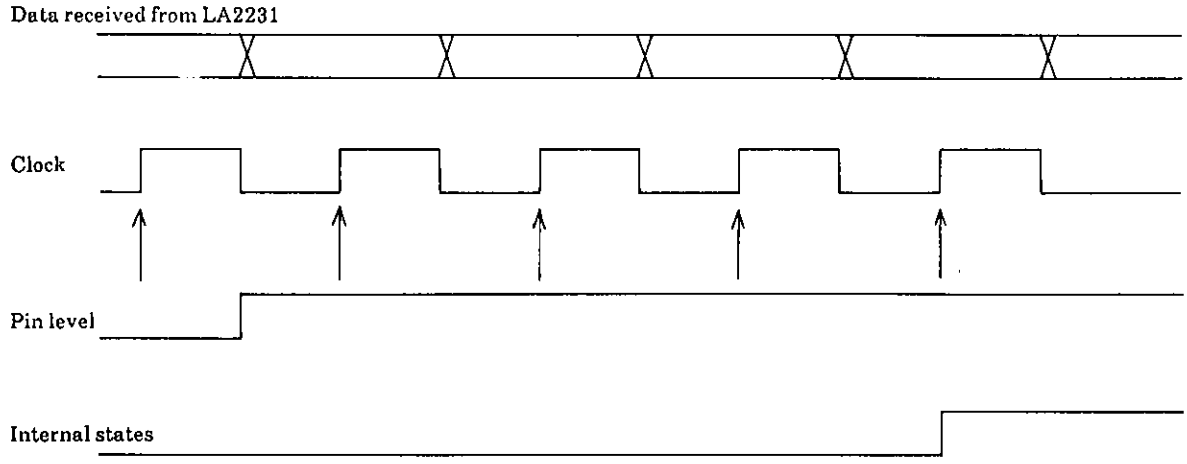
CORR. SEL, D. S. CONTROL Pin Read Timing

- After sync detection



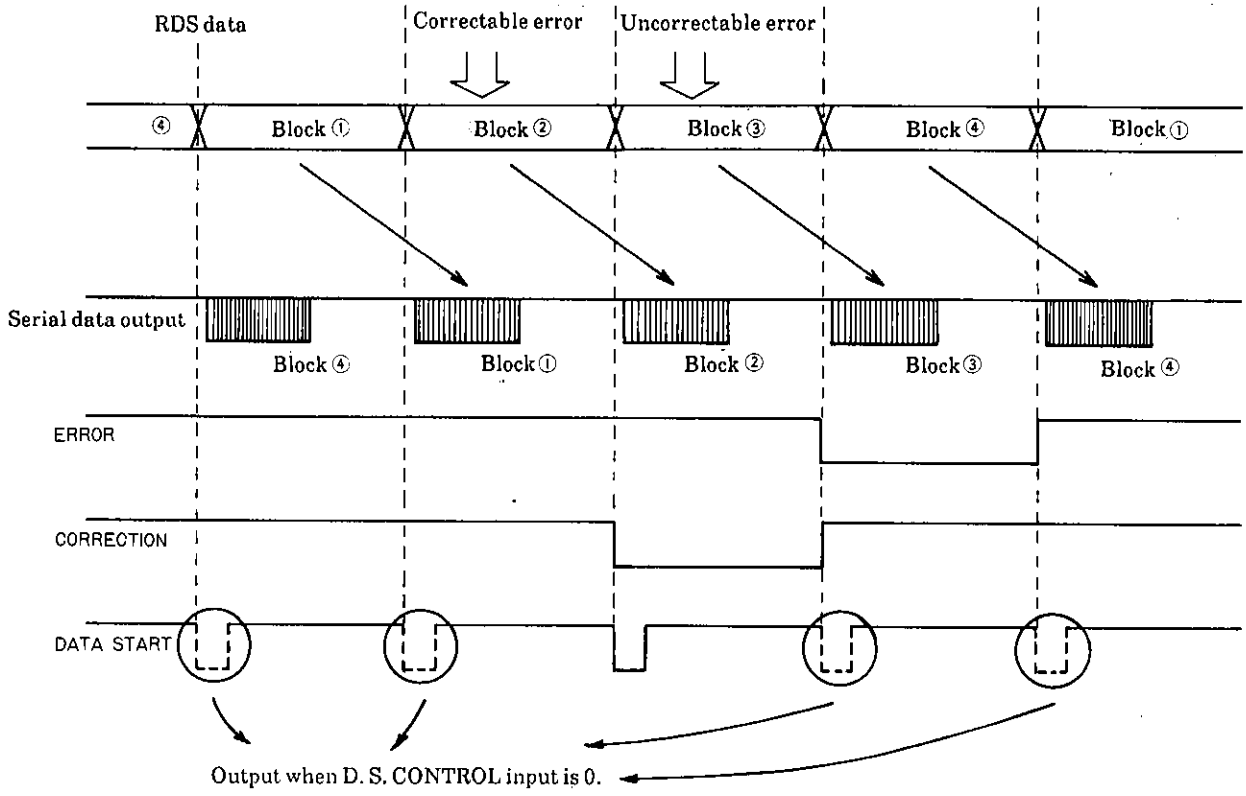
- States CORR. SEL and D. S. CONTROL are read at the start of each RDS demodulation data block. Four consecutive input states are then confirmed, inputs following the fourth are affected.

- During sync detection



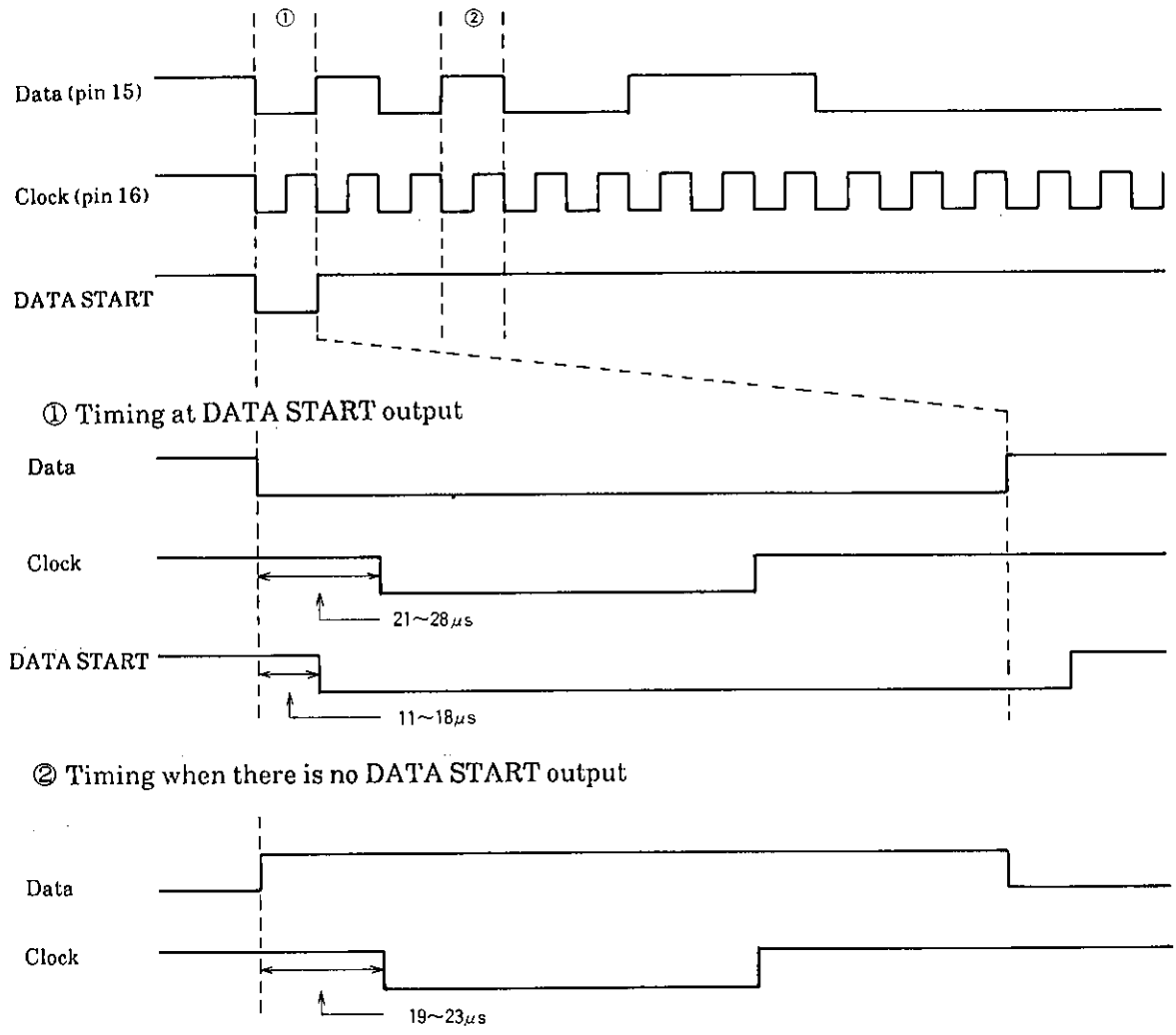
- RED demodulation data bits from LA2231 are read. Four consecutive pin states are confirmed. If all four states are the same, data are input internally.

Serial Data Output Timing (1)



- Serial data outputs from LC7070N, LC7070NM and LC7071NM are delayed one block from the RDS demodulation data from the LA2231.
- When sync is detected, serial data output starts from the beginning of the next group (1 clock cycle).
- ERROR and CORRECTION signal outputs are generated ahead of the serial data output. These outputs are continuous when errors are detected continuously.

Serial Data Output Timing (2)



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