CMOS IC

LC67F5104A

32-BIT SINGLE CHIP MICROCONTROLLER

UnderDevelopment

Overview

The LC67F5104A is a CMOS 32-bit RISC microcontroller which is ideally suited for CD-R/RW or DVD applications. This microcontroller contains the ARM7TDMI™ core produced by ARM, and various peripherals such as 4M-bit flash ROM, 128K-bit SRAM, DMA controller, interrupt controller, I/O ports, serial interface, 8-bit AD converter and timers all in a 100-pin package single chip.

Features

(1) Operating Power Supply Voltage 2.25 to 2.75V (I/O, ADC 3.0 to 3.6V)

(2) Operating Temperature 0 to 75°C

(3) Package Type TQFP-100

(4) CPU Core ARM7TDMI™

(5) Flash ROM 4M bits on chip

(6) SRAM 128K bits on chip

(7) Maximum Operating Frequency

Oscillator	CF Oscillator/external clock input	18MHz
	RC Oscillator	1MHz (Typical)

- The system clock frequency can be selected to be 1/1, 1/2, 1/4 or 1/8 of the oscillation frequency.
- The on-chip RC is automatically selected at reset or release of the standby mode.
- The clock selection is programmable.

(8) Write Protected Area in Flash

16KB (Located at the end of the 4M-bit memory area)

This area cannot be written to when the microcontroller is in normal operating mode. It can only be written to in the “Flash ROM Setting” mode.

(9) Ports

Input/output ports	56 ports
Input ports	8 ports

(10) Serial Interface (One channel)

Synchronous full duplex SIO with three lines

- Selectable 8 or 16-bit data length
- Selectable transfer bit order: LSB first or MSB first
- Transfer clock
  Internal or external clock selectable
  Internal clock can be selected ranging in value from 8 × system clock to 1024 × system clock by the on-chip 8-bit baud rate generator.
- Clock polarity selectable
  Clock pin level selectable when not transferring
- Error detection
  Overflow error
  Receive register over-write error

(11) UART (One channel)

Full duplex buffer enables continuous data transfer

- Selectable transfer rate
  Transfer rate can be selected ranging in value from 16× system clock to 4096 × system clock by the on-chip 8-bit baud rate generator.
  The transfer speed ranges from 4288bps to 1070000bps at 18MHz oscillation (while the UART standard is 110bps to 1152000bps).

  Table 1 shows transfer rate examples.

Operating Frequency	18MHz			17.2872MHz		
Bit Rate (Bits/s)	Set value	Transfer Rate	Difference(%)	Set value	Transfer Rate	Difference(%)
4800	22	4808	+0.16	31	4802	+0.04
9600	139	9615	+0.16	143	9562	-0.40
19200	197	19068	-0.69	200	19294	+0.49
38400	227	38793	+1.02	228	38588	+0.49
57600	236	56250	-2.34	237	56866	-1.27
115200	246	112500	-2.34	247	120050	+4.21
230400	251	225000	-2.34	251	216090	-6.21

Table 1 Transfer Rate Examples

  The formulae used to calculate are as follows:

  Set Value = 256 – {Operating Frequency / (16 × Bit Rate)}
  Transfer Rate = Operating Frequency / {16 × (256 – Set Value)}
  Difference = (Transfer Rate – Bit Rate) / Bit Rate × 100

- 1 or 2 stop bit(s) selectable
- 7 or 8-bit data length selectable
- Parity selection: even, odd or none
- Error detection: parity, framing and receive buffer overwrite error

(12) Plain Timer

(i) Watchdog Timer

- 8-bit baud rate generator and 16-bit free run counter
- Reset or interrupt generation selectable on counter overflow
- The counter clock can be selected to be 1/1, 1/2, 1/4 or 1/8 of the system clock
- The maximum time until overflow is 14.4 seconds at 18MHz oscillation

(ii) 16-Bit Free Run Counter

- The interrupt request is generated at counter overflow
- The counter clock can be selected to be 1/1, 1/2, 1/4 or 1/8 of the system clock
- Overflow interval can be selected to be 2.5, 5, 10 or 20ms at 18MHz oscillation

(13) ADC
- 8-channel 8-bit AD converter
- Successive approximation method
- Vref input (2.9 < Vref < AVcc)
- Interrupt at AD conversion completion
- Scan mode
- Conversion time : around 5.33μs at 18MHz oscillation

(14) DMA Controller
- 2 channels of independent operation
- Memory to memory transfer on the ASB bus
- Transfer between memory mapped device and memory on the ASB bus
- Transfer data size can be selected from byte, half word (2 bytes) or word (4 bytes)

(15) Interrupt Controller
- External interrupts 7 sources
- Internal interrupts 23 sources Total: 30 sources
- 2 vector addresses: FIQ and IRQ vectors
  FIQ has higher priority than IRQ
- Triggers for external interrupts (HPIRQ, EXT0IRQ ~ EXT5IRQ) can be selected to be rising edge/ high level or falling edge/ low level.
- Standby mode can be released by the level detection of any of external interrupts.
- Individual interrupt enabling/disabling is provided for every interrupts except HPIRQ
- Interrupt enabling/disabling of all interrupts together (except HPIRQ) is provided.
- FIQ or IRQ vector is selectable for each interrupt except HPIRQ.
- HPIRQ interrupt is fixed to FIQ vector. The vectors can be selected when all interrupts (except HPIRQ) are disabled.
- Status register indicating interrupt sources is provided.

(16) Power Save Mode

(i) Three Power Save Modes
Sleep mode, software standby mode and hardware standby mode

(ii) Module Standby Function
Clock for serial interface, UART, multiple timer, plain timer and AD converter can be stopped by program control to reduce the current consumption.

(17) Multiple Timer

5-channel 16-bit timer
- Maximum of 12 types of pulse output and 10 types of pulse input are provided.
- Counter input can be selected from the following:
  Internal clock Φ,Φ/2, Φ/4, Φ/8
  External clock TCK1, TCK2, TCK3, TCK4
- Operation mode for each channel can be selected from the following:
  • Waveform output by PCS (Phase Control Signal)
  Low, high or toggle output is selectable NOTE: Low or high only for channel 2
  • PLS (Pulse Length Scaler) function
  Rising edge, falling edge or both edges detection is selectable
  • Counter clear function
  Counter clear by PCS or PLS
  • Synchronous operation
  Simultaneous data write to multiple timer counters
  Simultaneous clear by PCS or PLS
  Synchronous input and output of registers by synchronous counter operation
  • PWM mode
  Duty programmable PWM output
  Maximum of 5 phases PWM output is possible by synchronous operation
- The following operation modes are selectable on channels 3 and 4
  • Reset Synchronous PWM mode
  Three-phase output of Positive or Negative PWM is possible by combining channels 3 and 4.

• Complementary PWM mode
Three-phase output of Positive or Negative PWM with no overlapping is possible by combining channels 3 and 4.
• Buffer operation
PLS can be double buffered.
PCS can be updated automatically.
• Interrupts
Each channel has 2 PCS or PLS interrupts and an overflow interrupt source. All interrupts can be requested independently.

(18) Memory Area

1GB of internal memory and 1GB of external memory area
The external memory area consists of 4 areas of 256MB each. (Area 0 to3)
NOTE: Only the first 16MB of each external memory area can be used.

The internal and external memory address map is shown in Table 2.

Memory Area	Address	Description	Note
External Memory	7FFF FFFFh ~ 7000 0000h	External memory (Area 3)	
	6FFF FFFFh ~ 6000 0000h	External memory (Area 2)	
	5FFF FFFFh ~ 5000 0000h	External memory (Area 1)	
	4FFF FFFFh ~ 4000 0000h	External memory (Area 0)	
Internal Memory	3FFF FFFFh ~ 2200 0000h	Access forbidden (Reserved)	
	21FF FFFFh ~ 2000 0000h	Peripheral input/output registers etc.	
	1FFF FFFFh ~ 1400 0000h	Access forbidden (Reserved) Some registers assigned	
	13FF FFFFh ~ 1000 0000h	On-chip RAM	
	0FFF FFFFh ~ 0000 0000h	On-chip ROM	

Table 2 Memory Address Map

• Configuration of Internal Memory Area
The memory address space 3FFF FFFF to 0000 0000 is allocated as 1GB internal memory area.
This area consists of the on-chip ROM, on-chip RAM, the peripheral input/output registers, etc.

Table 3 shows the address map of the internal memory area.

Memory Area	Address	Description	Note
Reserved Area	3FFF FFFFh ~ 2001 0000h	Access forbidden (Reserved)	
Peripheral I/O Registers, etc	2000 FFFFh ~ 2000 0000h	Peripheral input/output registers etc.	
Reserved Area	1FFF FFFFh ~ 1400 4000h	Access forbidden (Reserved)	
Registers, etc	1400 3FFFh ~ 1400 3000h	Registers, etc.	
Reserved Area	1400 2FFFh ~ 1400 2000h	Access forbidden (Reserved)	
Registers, etc	1400 1FFFh ~ 1400 0000h	Registers, etc.	
On-chip RAM Area	13FF FFFFh ~ 1000 4000h	Access forbidden (Reserved)	
	1000 3FFFh ~ 1000 0000h	On-chip RAM area	16KB
On-chip ROM Area	0FFF FFFFh ~ 0008 0000h	Access forbidden (Reserved)	
	0007 FFFFh ~ 0000 0000h	On-chip Flash ROM area	512KB

Table 3 Internal Memory Address Map Details

• Configuration of External Memory Area
Four areas (Area 0 to 3) are allocated as the external memory area.
Area 0 is also used for the external ROM operation mode at reset.
Each area has independent select signals (nCS0 ~ nCS3) and the number of waits can be set independently for each area.

Table 4 shows the address map of the external memory area.

Memory Area	Address	Description	Note
Area 3	7FFF FFFFh ~ 7100 0000h	Access forbidden (Reserved)	
	70FF FFFFh ~ 7000 0000h	External memory (Area 3)	16MB
Area 2	6FFF FFFFh ~ 6100 0000h	Access forbidden (Reserved)	
	60FF FFFFh ~ 6000 0000h	External memory (Area 2)	16MB
Area 1	5FFF FFFFh ~ 5100 0000h	Access forbidden (Reserved)	
	50FF FFFFh ~ 5000 0000h	External memory (Area 1)	16MB
Area 0	4FFF FFFFh ~ 4100 0000h	Access forbidden (Reserved)	
	40FF FFFFh ~ 4000 0000h	External memory (Area 0)	16MB

Table 4 External Memory Address Map Details

(19) External Memory Access

• Wait Control

The number of wait state cycles for each area can be selected by a dedicated register.

8 wait cycles are provided: 0,1,2,3,4,5,6 or 7 (1 ~7 for write accesses)

The number of waits (set in the dedicated register) can be extended by inserting the external wait control signal.

Note: When the CF oscillation (1/1 divider) is used as the system clock, at least 1 wait cycle should be set for a read access.

External memory data accesses are shown in Tables 5, 6.

Reading from External Memory

Data Width	Access from 8-bit Device	Access from 16-bit Device
8 bits	One 1-byte read	One 1-byte read
16 bits	Two 1-byte reads	One 2-byte read
32 bits	Four 1-byte reads	Two 2-bytes reads

Table 5 External Data Access (READ)

Writing to External Memory

Data Width	Access to 8-bit Device	Access to 16-bit Device
8 bits	One 1-byte write	One 1-byte write
16 bits	Two 1-byte writes	One 2-byte write
32 bits	Four 1-byte writes	Two 2-byte writes

Table 6 External Data Access (WRITE)

(20) External ROM Operation Mode

The following 7 modes can be selected by setting the mode control pins (M2, M1, M0) at reset.

For external ROM operation, 6 kinds of operating mode are provided with varying combinations of external data bus width and accessible memory address area.

Area 0 is always selected when external ROM operation mode is selected at reset.

Table 7 shows the details of external ROM operation mode.

Operation Mode	M1	M2	M3	External Memory Area on Boot	External Data Bus Width	Address Output
Internal ROM operation	0	0	0	-	*1	*1
External ROM operation 1	0	0	1	1MB	8 bits	A19 ~ A0
External ROM operation 2	0	1	0	8MB	8 bits	A22 ~ A0
External ROM operation 3	0	1	1	16MB	8 bits	A23 ~ A0
External ROM operation 4	1	0	0	1MB	16 bits	A19 ~ A0
External ROM operation 5	1	0	1	8MB	16 bits	A22 ~ A0
External ROM operation 6	1	1	0	16MB	16 bits	A23 ~ A0
	1	1	1	Forbidden	Forbidden	Forbidden

Table 7 Setting of the External ROM operation mode

*1 For internal ROM operation, ports can be selected by software to be used as address lines A0 to A23 or as normal input/output ports. (The default is ports are set to input for I/O.)
Also, for internal ROM operation ports can be selected by software to be used as the data bus or as normal input/output ports. (The default is ports are set to input for I/O.)

Table 8 shows data access in the external ROM operation mode

Data Width	Access to 8-bit Device	Access to 16-bit Device
8 bits	One 1-byte read	One 1-byte read
16 bits	Two 1-byte reads	One 2-byte read
32 bits	Four 1-byte reads	Two 2-byte reads

Table 8 Data Access in the External ROM Operation Mode

Please note that even in the case where Thumb instruction are used, the ARM core always executes ARM instructions first at reset. It should switch to the Thumb instruction mode after reset. This also applies to external ROM boots. Since the RC oscillator is selected at reset, no wait cycles are inserted for the external ROM operation modes. Before switching the clock to the CF, please set the appropriate number of wait cycles by software.

(21) On Board Rewrite Function for Flash ROM

16KB boot area is provided in order to support the on board rewrite function for the internal Flash ROM. This boot program area is from address 0x7C000 to 0x7FFFF and can not be erased or written in normal CPU setting mode. Therefore the program area for the normal operation mode consists of 496 KB from 0x00000 ~ 0x7BFFF.

- On board programming

Program execution will start from address 0x7C000 if the BOOT terminal is “High” at reset. The program data to be written is received by some methods such as serial interface and stored in the internal RAM by the boot program. The boot program then jumps to the internal RAM area and rewrites the contents of Flash ROM with the program data which was stored in RAM. After the boot program jumps to RAM, and before it starts the actual rewriting of the Flash ROM, the boot control register flag should be set (in software).

In order to use the on board Flash rewrite system, software is also required for the PC. Please contact the SANYO sales office for further information.

(22) Rewrite Function Using the PROM Writer

The general purpose PROM writer supports both the reading and writing of the internal Flash ROM using the dedicated conversion board.

(i) Conversion board name : W67F5106TQ

(ii) Available Flash ROM writer information

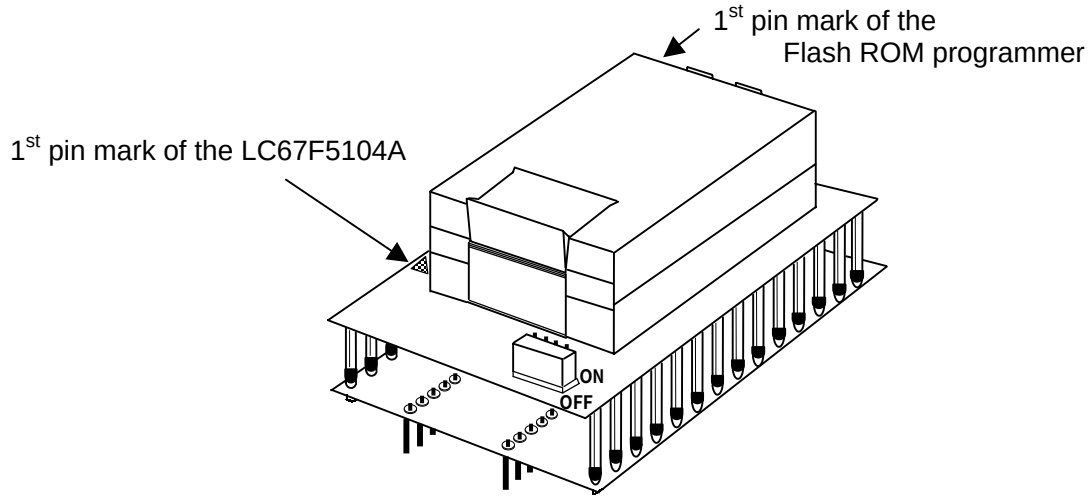
Maker Name	Model	Version Available	Device Code
ANDO	AF-9708	*	*

(23) Development Tools

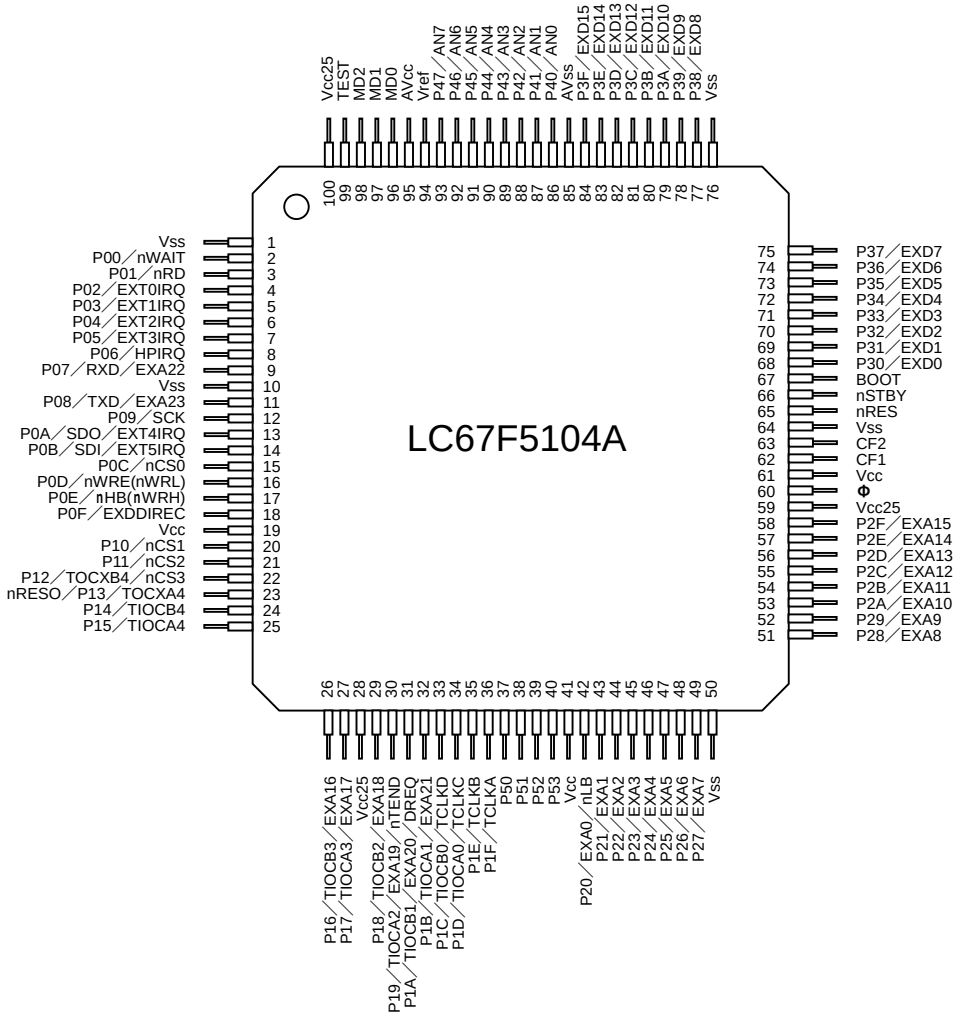
Emulator : ADVICE (PW920) produced by Yokogawa Digital Computer Corporation

(24) Flash ROM Programming Service

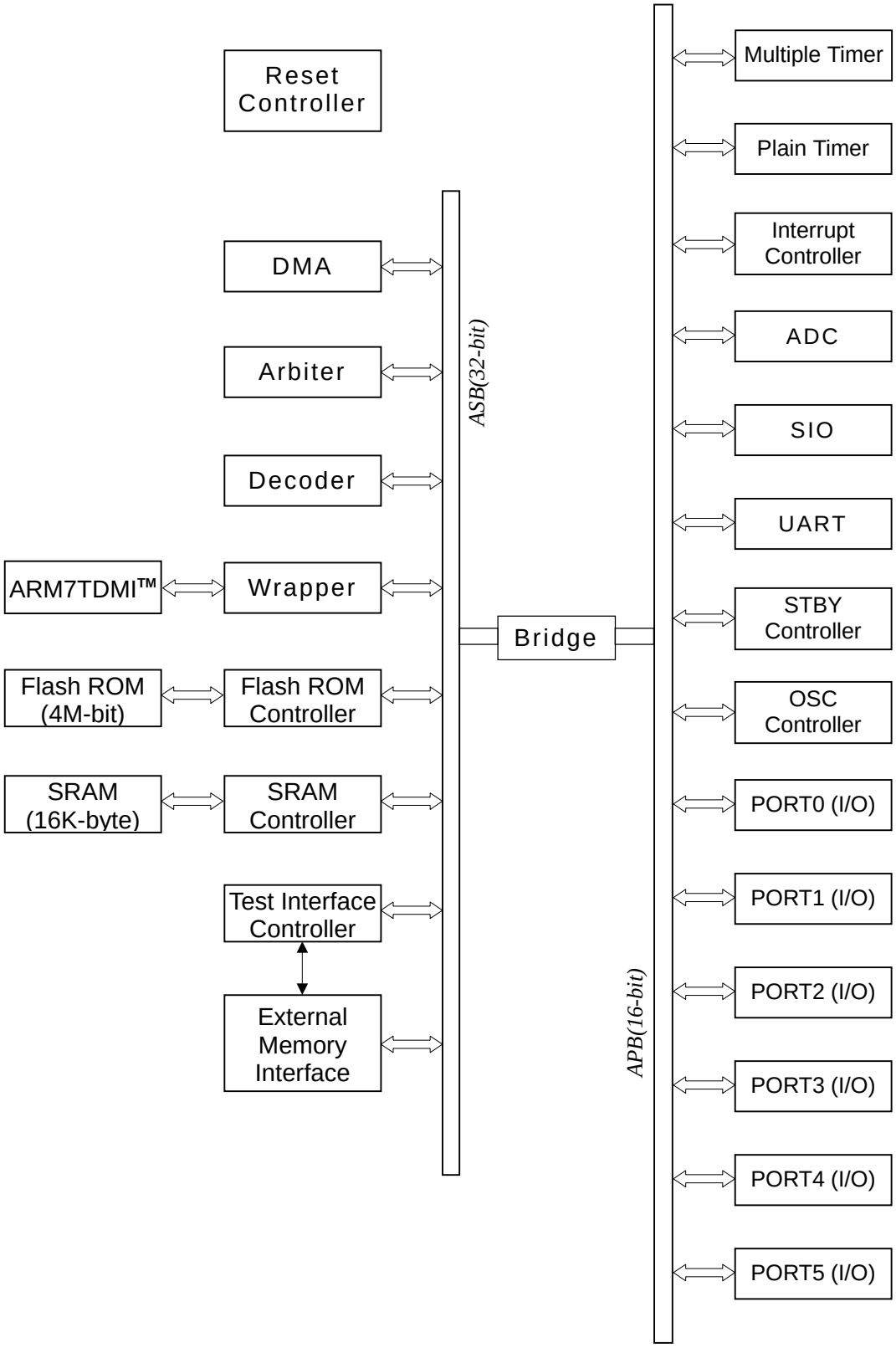
SANYO will perform Flash ROM programming and sealing on die encapsulation for a charge. For details, please contact your SANYO sales office.



Pin Assignment



System Block Diagram



Pin Descriptions

<table>
<tr><th>Type</th><th>Symbol</th><th>Pin Number</th><th>I/O</th><th>Name and function</th></tr>
<tr><td rowspan="3">Power supply</td><td>Vcc</td><td>19,41,61</td><td>-</td><td>3.3V power supply
For connection to the 3.3V power supply.</td></tr>
<tr><td>Vcc25</td><td>28, 59, 100</td><td>-</td><td>2.5V power supply
For connection to the 2.5V power supply.</td></tr>
<tr><td>Vss</td><td>1,10,50,64,76</td><td>-</td><td>Ground
For connection to ground.</td></tr>
<tr><td rowspan="3">Clock</td><td>CF1</td><td>62</td><td>Input</td><td>CF oscillator pin
For connection to the CF oscillator.
Can also be used as external clock input pin.</td></tr>
<tr><td>CF2</td><td>63</td><td>Output</td><td>CF oscillator pin
For connection to the CF oscillator.</td></tr>
<tr><td>Φ</td><td>60</td><td>Output</td><td>System clock
Supplies the system clock to external devices.</td></tr>
<tr><td rowspan="2">Operating mode control</td><td>MD2 ~ MD0</td><td>98,97,96</td><td>Input</td><td>Mode pins
For setting internal and external ROM modes, access area and data bus width (in external ROM modes).
• Internal ROM operation
Internal Flash ROM is selected after reset.
• External ROM operation (1 to 6)
ROM connected to the external access area 0 is selected after reset.
These pin states should not be changed during operation.
<table>
<tr><th>M2</th><th>M1</th><th>M0</th><th>Operating Mode</th></tr>
<tr><td>0</td><td>0</td><td>0</td><td>Internal ROM operation</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>External ROM operation 1</td></tr>
<tr><td>0</td><td>1</td><td>0</td><td>External ROM operation 2</td></tr>
<tr><td>0</td><td>1</td><td>1</td><td>External ROM operation 3</td></tr>
<tr><td>1</td><td>0</td><td>0</td><td>External ROM operation 4</td></tr>
<tr><td>1</td><td>0</td><td>1</td><td>External ROM operation 5</td></tr>
<tr><td>1</td><td>1</td><td>0</td><td>External ROM operation 6</td></tr>
<tr><td>1</td><td>1</td><td>1</td><td>Prohibited</td></tr>
</table></td></tr>
<tr><td>BOOT</td><td>67</td><td>Input</td><td>BOOT pin
Normally Low; High during boot mode.</td></tr>
<tr><td rowspan="3">System Control</td><td>nRES</td><td>65</td><td>Input</td><td>Reset Input
When driven Low, the chip is reset.</td></tr>
<tr><td>nRESO</td><td>23</td><td>Output</td><td>Reset Output
Outputs a reset signal to external devices.</td></tr>
<tr><td>nSTBY</td><td>66</td><td>Input</td><td>Standby
When driven Low, the chip enters Hardware Standby mode.</td></tr>
<tr><td rowspan="2">Interrupts</td><td>HPIRQ</td><td>8</td><td>Input</td><td>High priority external interrupt request
This pin is fixed as an FIQ interrupt.</td></tr>
<tr><td>EXT5IRQ ~ EXT0IRQ</td><td>14,13,7,6,5,4</td><td>Input</td><td>External Interrupt requests 0 to 5
Setting as FIQ or IRQ is programmable.</td></tr>
<tr><td rowspan="6">Timers</td><td>TCLKD ~ TCLKA</td><td>33 ~ 36</td><td>Input</td><td>Clock inputs A to D
Inputs external clock.</td></tr>
<tr><td>TIOCA4 ~ TIOCA0</td><td>25,27,30,32,34</td><td>Input/ output</td><td>Input capture/output compare A0 to A4
GRA0 to GRA4 output compare, input capture or PWM output pins.</td></tr>
<tr><td>TIOCB4 ~ TIOCB0</td><td>24,26,29,31,33</td><td>Input/ output</td><td>Input capture/output compare B0 to B4
GRB0 to GRB4 output compare, input capture or PWM output pins.</td></tr>
<tr><td>TOCXA4</td><td>23</td><td>Output</td><td>Output compare XA4
PWM output pin</td></tr>
<tr><td>TOCXB4</td><td>24</td><td>Output</td><td>Output compare XB4
PWM output pin</td></tr>
</table>

Type	Symbol	Pin Number	I/O	Name and function
Serial interface	SDI	14	Input	Receive data Serial interface data input pin
	SDO	13	Output	Transmit data Serial interface data output pin
	SCK	12	Input/ output	Serial clock Serial interface clock input/output pin
UART	TXD	11	Output	Transmit data UART data output pin
	RXD	9	Input	Receive data UART data input pin
AD converter	AN7 ~AN0	93 ~ 86	Input	Analog 0 to 7 Analog input pins
	AVcc	95	Input	Power supply(+3.3V) pin for the A/D converter Connect to the system power supply(+3.3V) when not using the A/D converter.
	AVss	85	Input	Ground pin for the A/D converter Connect to system ground(0V).
	Vref	94	Input	Reference voltage input pin for the A/D converter Connect to the system power supply(+3.3V) when not using the A/D converter.
Address bus	EXA23 ~ EXA0	11,9,32~29,27,26 58~51, 49~42	Output	External address bus Output address signals for external memory access.
Data bus	EXD15 ~ EXD0	84~77,75~68	Input/ output	External data bus Bi-directional data bus for external memory devices.
Bus control	nCS3 ~ nCS0	22,21,20,15	Output	Chip selection Signals for selecting external memory areas 0 to 3.
	EXDDIREC	18	Output	External data bus direction Indicates whether the access to the selected external memory area is read or write.
	nRD	3	Output	Read When Low, indicates reading from the selected external memory area.
	nWRE	16	Output	Write enable When Low, indicates writing to the external memory area selected.
	nWRL	16	Output	Write enable low signal Enables lower byte write of external device.
	nWRH	17	Output	Write enable high signal Enables upper byte write of external device.
	nLB	42	Output	Low byte selection Selects lower byte of external memory device.
	nHB	17	Output	High byte selection Selects upper byte of external memory device.
	nWAIT	2	Input	Wait Requests the insertion of wait state(s) (in the number of bus cycles) when accessing an external memory area.
DMAC	nTEND	30	Output	DMA transfer end
	DREQ	31	Input	DMA request

Type	Symbol	Pin Number	I/O	Name and function
I/O ports	P00 ~ P0F	2~9,11~18	Input/ output	Port 0 16-bit input/output pins The direction of each pin is programmable.
	P10 ~ P1F	20~27,29~36	Input/ output	Port 1 16-bit input/output pins The direction of each pin is programmable.
	P20 ~ P2F	42~49, 51~58	Input/ output	Port 2 16-bit input/output pins The direction of each pin is programmable.
	P30 ~ P3F	68~75, 77~84	Input/ output	Port 3 16-bit input/output pins The direction of each pin is programmable.
	P40 ~ P47	86 ~ 93	Input	Port 4 8-bit input pins
	P50 ~ P53	37 ~ 40	Input/ output	Port 5 4-bit input/output pins The direction of each pin is programmable.
TEST	TEST	99	Input	Test pin High in Test mode (otherwise Low).

Electrical Characteristics

1. Absolute Maximum Ratings / Ta=25°C, VSS=0V

Parameter	Symbol	Applicable Pins / Notes	Conditions	Ratings	Unit
Max. supply voltage	Vccmax	Vcc		-0.3 ~ +4.0	V
	Vcc25max	Vcc25		-0.3 ~ +3.0	V
Input voltage	V_I	All input only pins		-0.3 ~ Vcc+0.3	V
I/O voltage	V_{IO}	All I/O pins		-0.3 ~ Vcc+0.3	V
High level output peak current	I_{OPH}	All output and I/O pins	per pin value	10	mA
High level total output current	ΣI_{OAH}	Total of all output and I/O pins	total pins value	80	mA
Low level output peak current	I_{OPL}	All output and I/O pins	per pin value	10	mA
Low level total output current	ΣI_{OAL}	Total of all output and I/O pins	total pins value	120	mA
	ΣI_{OAL1}	P00~P0F, P10~P17	total pins value	60	mA
	ΣI_{OAL2}	P18~P1F, P50~P53, P20~P2F	total pins value	60	mA
	ΣI_{OAL3}	P30~P3F	total pins value	60	mA
Reference voltage	Vref	Vref *NOTE 1		-0.3 ~ AVcc+0.3	V
Analog supply voltage	AVccmax	AVcc *NOTE1		-0.3 ~ +4.0	V
Analog input voltage	V_{AN}	Each analog input pin		-0.3 ~ AVcc+0.3	V
Allowable power dissipation	Pdmax	TQFP100	Ta=0 ~ +75°C	500	mW
Operating temperature	Topg			0 ~ +75	°C
Storage temperature	Tstg			-55 ~ +125	°C

*NOTE 1 AVcc and Vref should be connected to the supply voltage (Vcc) when the A/D converter is not in use or when in Standby mode

2. DC Characteristics (preliminary specifications) / Ta=0 ~ 75°C, VSS=0V

Parameter	Symbol	Applicable Pins / Notes	Conditions	Rating			Unit
				Min.	Typical	Max.	
Operating supply voltage (I/O, ADC)	Vcc	Vcc, AVcc		3.0	3.3	3.6	V
Operating supply voltage (internal)	Vcc25	Vcc25		2.25	2.5	2.75	V
High level input voltage	V_{IH1}	P00~P0F, P10~P1F, P20~P2F P30~P3F, P40~P47, P50~P53 CF1 (External clock input)		0.75Vcc		Vcc	V
	V_{IH2}	nRES, nSTBY, TEST, MD0, MD1, MD2		0.80Vcc		Vcc	V
Low level input voltage	V_{IL}	All input and I/O pins CF1 (External clock input)		Vss		0.15Vcc	V
Schmitt trigger voltage	V_{SH}	All input and I/O pins			0.08Vcc		V
High level output voltage	V_{OH1}	All output and I/O pins (except for Φ, P50~P53)	I_{OH} = -4mA	Vcc –0.8			V
	V_{OH2}	Φ, P50~P53	I_{OH} = -4mA	Vcc –0.4			V
Low level output voltage	V_{OL}	All output and I/O pins	I_{OL} = 4mA			0.4	V
High level input current	I_{IH}	All input and I/O pins (output off for I/O pins)	Vin = Vcc	-10		+10	μA
Low level input current	I_{IL}	All input and I/O pins (output off for I/O pins)	Vin = Vss	-10		+10	μA
Input pin capacitance	C_{IN}	All input pins	f=1MHz, Ta=25°C, Vin = 0V			15	pF
Output pin capacitance	C_{OUT}	All output pins	f=1MHz, Ta=25°C, Vin=0V			15	pF
I/O pin capacitance	$C_{I/O}$	All I/O pins	f=1MHz, Ta=25°C, Vin = 0V			15	pF

3. Sample Current Dissipation Characteristics (preliminary specifications) / Ta=0 ~ 75°C, VSS=0V

The sample current dissipation characteristics were measured with Sanyo's evaluation board using the recommended circuit values indicated in Sample Oscillation Circuit Characteristics externally. The current through the LSI output transistor is not included.

Parameter		Symbol	Applicable Pins / Notes	Conditions	Rating			Unit
					Min.	Typical	Max.	
Current Dissipation	Normal operation 1 *NOTE 1	IDD_{RUN1}	Vcc	• System clock: CF17.28MHz (1/1 divider) • Internal RC oscillation stopped		23	34	mA
	Normal operation 2 *NOTE 2	IDD_{RUN2}				19	29	mA
	Sleep mode *NOTE 3	IDD_{SLP}				9	16	mA
	Module Standby mode *NOTE 4	IDD_{MSTBY}				6	13	mA
	Standby mode	IDD_{STBY}		All oscillation stopped		4	400	µA
	External clock operation 1 *NOTE 1	IDD_{EXCLC1}		• External clock: 36MHz (System clock: 1/2 divider)		23	34	mA
	External clock operation 2 *NOTE 2	IDD_{EXCLC2}				19	29	mA

*NOTE 1: These values are for when the program is fetched from the internal Flash ROM and ADC is operating.

*NOTE 2: These values are for when the program is fetched from the internal SRAM and ADC is operating. Writing to the internal Flash ROM is not included.

*NOTE 3: These values are for when ADC is halted.

*NOTE 4: These values are for sleep mode with all modules halted.

4. AC Characteristics(preliminary specifications) Figure 5 Load

4-1 Allowable operation clock / Ta=0 ~ 75°C, VSS=0V

Parameter	Symbol	Applicable Pins / Notes	Conditions	Rating			
				Min.	Typical	Max.	Unit
CF oscillator frequency range	f_{CFCK}	Ceramic resonator oscillation at 17.28MHz	Figure 1		17.28		MHz
RC oscillator frequency range	f_{RCCK}	Internal RC clock		0.4		2.0	MHz
External clock frequency range	f_{EXCK}	External clock input *NOTE 1	Figure 4	0.4		36.0	MHz
External clock pulse width	t_{CKL}	CF1: 0.5MHz~18MHz input	Figure 4	17			nS
	t_{CKH}	CF1: 18MHz~36MHz input		10			nS
External clock rising / falling edge time	t_{EXR} t_{EXF}	CF1: 18MHz input	Figure 4			10	nS
System clock frequency	f_{SYSCK}	*NOTE 2		0.05		18	MHz

*NOTE 1: For external clock operation, if the external oscillator frequency is more than 18MHz, set the oscillation divider ratio to at least 1/2 before switching the system clock from internal RC to external clock.

*NOTE 2: The system clock frequency is selectable from 1/1~1/8 division of the main clock. The divider is provided in the OSC module.

4-2 Control signal timing (preliminary specifications) / Ta=0 ~ +75°C, VSS=0V

Parameter	Symbol	Applicable Pins / Notes	Conditions	Rating			
				Min.	Typical	Max.	Unit
nRES pulse width (when supplying power)	t_{RESW1}	nRES	Figure 3	10			ms
nRES pulse width (during normal operation)	t_{RESW2}	nRES		40			μs
nRESO output delay time	t_{RESD}	nRESO	Figure 6a			20	ns
nRESO output pulse width (WDT reset)	t_{RESOW}	nRESO	Figure 6a	50			Tcyc
Reset release time	t_{RESREL}	nRES	Figure 6b			30	μs
External interrupt pulse width *NOTE 1	t_{EXINTW}	HPIRQ, EXT5IRQ~ EXT0IRQ	Figure 7	4			Tcyc
Oscillation stabilizing time (CF)	tmsCF		Figure 2	10			ms

*NOTE 1: Regarding the external interrupt pulse width when using a noise filter, please refer to the manual.

4-3 Multiple timer input/output timing (preliminary specifications) / Ta=0 ~ +75°C, VSS=0V

Parameter		Symbol	Applicable Pins / Notes	Conditions	Rating			
					Min.	Typical	Max.	Unit
Timer output delay time		t_{TOCD}	TIOCA0~TIOCA4, TIOCB0~TIOCB4 TOCXA4, TOCXB4	Figure 8			20	ns
Timer clock pulse width	Single edge detection	t_{TCKWH}	TCLKA~TCLKD	Figure 9	1.5			Tcyc
	Both edges detection	t_{TCKWL}	TIOCA0~TIOCA4 TIOCB0~TIOCB4	Figure 9	2.5			Tcyc

4-4 Serial input/output timing (preliminary specifications) / Ta=0 ~ +75°C, VSS=0V

Parameter	Symbol	Applicable Pins / Notes	Conditions	Rating			
				Min.	Typical	Max.	Unit
Input clock cycle	T_{SCK}	SCK	Figure 10	8			Tcyc
Input clock low pulse width	T_{SCKL}	SCK	Figure 10	4			Tcyc
Input clock high pulse width	T_{SCKH}	SCK	Figure 10	4			Tcyc
Output clock cycle	T_{SCKO}	SCK	Figure 10	8			Tcyc
Output clock low pulse width	T_{SCKOL}	SCK	Figure 10	4			Tcyc
Output clock high pulse width	T_{SCKOH}	SCK	Figure 10	4			Tcyc
Input data setup time	t_{SDI}	SCK(input), SDI	Figure 10	2			Tcyc
Input data hold time	T_{HDI}	SCK(input), SDI	Figure 10	2			Tcyc
Output delay time	T_{DDO}	SCK(output), SDO	Figure 10		2		Tcyc

4-5 DMAC input/output timing (preliminary specifications) / Ta=0 ~ +75°C, VSS=0V

Parameter	Symbol	Applicable Pins / Notes	Conditions	Rating			
				Min.	Typical	Max.	Unit
nTEND delay time 1	t_{TEC1}	nTEND	Figure 11			20	ns
nTEND delay time 2	t_{TEC2}	nTEND	Figure 11			20	ns
DREQ set up time	t_{DREQ}		Figure 12	35			ns

4-6 Bus timing (preliminary specifications) / Ta=0 ~ +75°C, VSS=0V

Parameter	Symbol	Applicable Pins / Notes	Conditions	Rating			
				Min.	Typical	Max.	Unit
Clock cycle time	t_{CYC}	Φ	Figures 14 a,b,c	55		20000	ns
Clock pulse width low level time	t_{CL}	Φ	Figures 14 a,b,c	15			
Clock pulse width high level time	t_{CH}	Φ	Figures 14 a,b,c	15			
Clock rising time	t_{CR}	Φ	Figures 14 a,b,c			10	
Clock falling time	t_{CF}	Φ	Figures 14 a,b,c			10	
Address delay time 1	t_{AD}	EXA23~0, Φ	Figures 14 a,b,c			25	
Address delay time 2	t_{ADA}	EXA23~0, Φ	Figures 14 a,b,c	-13			
Address hold time	t_{AH}	EXA23~0, NRD	Figures 14 b,c	5			
Address strobe delay time	t_{ASD}	Φ, NRD	Figures 14 a,b			25	
Write strobe delay time	t_{WSD}	Φ, NWRE, NWRL, NWRH	Figure 14 c			25	
Strobe delay time	t_{SD}	Φ, NRD, NWRE, NWRL, NWRH	Figures 14 a,b,c			25	
Write data strobe pulse width	t_{WSW}	NWRE, NWRL, NWRH	Figure14 c	35			
Address setup time	t_{AS}	EXA23~0, NRD, NWRE NWRL, NWRH	Figures 14 b,c	5			
Read data setup time	t_{RDS}	EXD15~0, Φ	Figures 14 a,b	20			
Read data hold time	t_{RDH}	EXD15~0, NRD	Figures 14 a,b	0			
Write data delay time	t_{WDD}	EXD15~0, Φ	Figure 14 c			25	
Write data set up time	t_{WDS}	EXD15~0, NWRE, NWRL, NWRH	Figure 14 c	20			
Write data hold time	t_{WDH}	EXD15~0, NWRE, NWRL, NWRH	Figure 14 c	15			
Read data access time 1	t_{ACC1}	EXD15~0, EXA23~0	Figure 14 a			10	
Read data access time 2	t_{ACC2}	EXD15~0, NRD	Figure 14 a			10	
Read data access time 3	t_{ACC3}	EXD15~0, EXA23~0	Figure 14 b			15	
Read data access time 4	t_{ACC4}	EXD15~0, NRD	Figure 14 b			7	
Wait setup time	t_{WTS}	Φ, NWAIT	Figure 14 d	15			
Wait hold time	t_{WTH}	Φ, NWAIT	Figure 14 d	0			

5. ADC Characteristics (preliminary specifications) / Ta=0 ~ 75°C, VSS=0V

Parameter	Symbol	Applicable Pins / Notes	Conditions	Rating			Unit
				Min.	Typical	Max.	
ADC Resolution	N	AN0~AN7			8		bit
ADC Differential linear error	Edef1	AN0~AN7	Vref =AVcc			±1	LSB
	Edef2		Vref =2.90V			±1	LSB
ADC Linear error	Elin1	AN0~AN7	Vref =AVcc			±1	LSB
	Elin2		Vref =2.90V			±1	LSB
ADC Conversion time *NOTE 1	Tcad	AN0~AN7	When system clock is 18MHz	5.33			µs
ADC Reference resistance	RAVref	Resistance value between Vref and AVss			25		kΩ
Input reference voltage	VAVref	Vref		2.90		AVcc	V
Analog input voltage range	VAin	AN0~AN7		AVss		Vref	V
0 scale offset voltage	VOoff					60	mV
Full scale offset voltage	Vfulloff			Vref - 60			mV
ADC Operating clock	ADC_{CLK}			0.1		2.25	MHz

*NOTE 1: The conversion time is for normal single mode operation with 18MHz system clock.

*NOTE 2: Please note that when the ADC returns from Standby mode, about 5µs is required for the internal ladder resistors to become stable.

6. Flash ROM Characteristics / Ta=0 ~ 75°C, VSS=0V

Parameter	Symbol	Applicable Pins / Notes	Conditions	Rating			Unit
				Min.	Typical	Max.	
On-board rewriting current	FICCW		VCC25=2.25~2.75V VCC=3.0~3.6V			10	mA
Erase time (Sector erase)	FTSE		1 sector is 2K bytes.	20			ms
Rewrite time	FTWP		32 bits			42	µs
Number of Sector rewrites	FSECWRT		*NOTE 1			1000	times

*NOTE 1: Definition of Flash ROM rewriting

- The data in the Flash ROM is rewritten in sector units (2K bytes).
- A pair of one erase and one write together of a sector unit is considered to be one rewrite. (The 2K bytes in one sector are assumed to be rewritten contiguously as one unit.)
- The same address cannot be written to more than twice (with respect to one erase).
- Cumulative writing time: A sector consists of 8 sub-blocks (each of 256K bytes) and the cumulative writing time for one of these sub-blocks should be 8ms at most.

Recommended Oscillation Circuit and Sample Characteristics

The oscillation circuit sample characteristics in the table below are based on the following:

- The recommended circuit parameters were verified by an oscillator manufacturer using Sanyo's oscillation evaluation board; and
- The sample characteristics provided are the result of evaluation performed with these recommended circuit parameters connected externally.

Recommended oscillation circuit and sample characteristics (Ta= 0 ~ +75°C)

Frequency	Manufacturer	Oscillator	Recommended circuit parameters				Operating supply voltage range	Time for Oscillation to Stabilize *NOTE	
			C1	C2	Rf	Rd		Typical	Min.
17.28MHz	MURATA	CSACV17M2X55J01-R0	10pF	10pF	Open	0Ω	3.0 ~ 3.6V		10ms
18.00MHz	MURATA	CSACV18MOX55J-R0	10pF	10pF	Open	0Ω	3.0 ~ 3.6V		10ms

*NOTE The time for oscillation to stabilize is the period of time required for the CF oscillator to stabilize either from the point when VCC reaches the minimum voltage level after power-on or from when standby mode is released. (Refer to Figure 2)

The values of the oscillation circuit sample characteristics may differ depending on the application board. For further assistance, please contact your oscillator manufacturer while taking note of the following.

- Since the precision of the oscillation frequency is affected by the amount of wiring on the application board etc., the oscillation frequency should be appropriately adjusted on the mass production board.
- The oscillation frequencies and operating supply voltage ranges in the above table are for an operating temperature range of 0 to +75°C. In the case the oscillation circuit is used out of this range or used for products requiring high reliability such as automotive products, please contact your oscillator manufacturer.
- When using an oscillator which is not mentioned in the oscillation circuit sample characteristics, please contact the Sanyo sales office.

Since the recommended oscillation circuit is easily affected by such things as noise and the amount of wiring please refer to the following points when performing wiring and layout. (As the circuit is designed to have low oscillation gain in order to reduce power dissipation, noise etc. will easily affect the circuit. Therefore, special care should be taken when putting together the recommended oscillation circuit.)

- The distance between the clock I/O pins (CF1, CF2 terminals) and external parts should be as short as possible.
- The capacitors' (C1 and C2) VSS pattern should be allocated as close as possible to the microcontroller's GND (Vss) pin and be used only for the oscillator.
- Signal lines which have rapid state changes or large current should be allocated away from the oscillation circuit as much as possible, and should not cross each other.

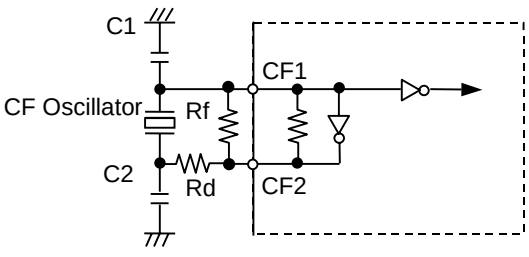


Figure 1 Recommended oscillation circuit

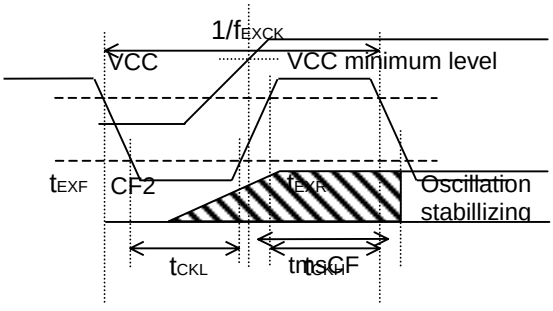


Figure 2 Time for Oscillation to Stabilize

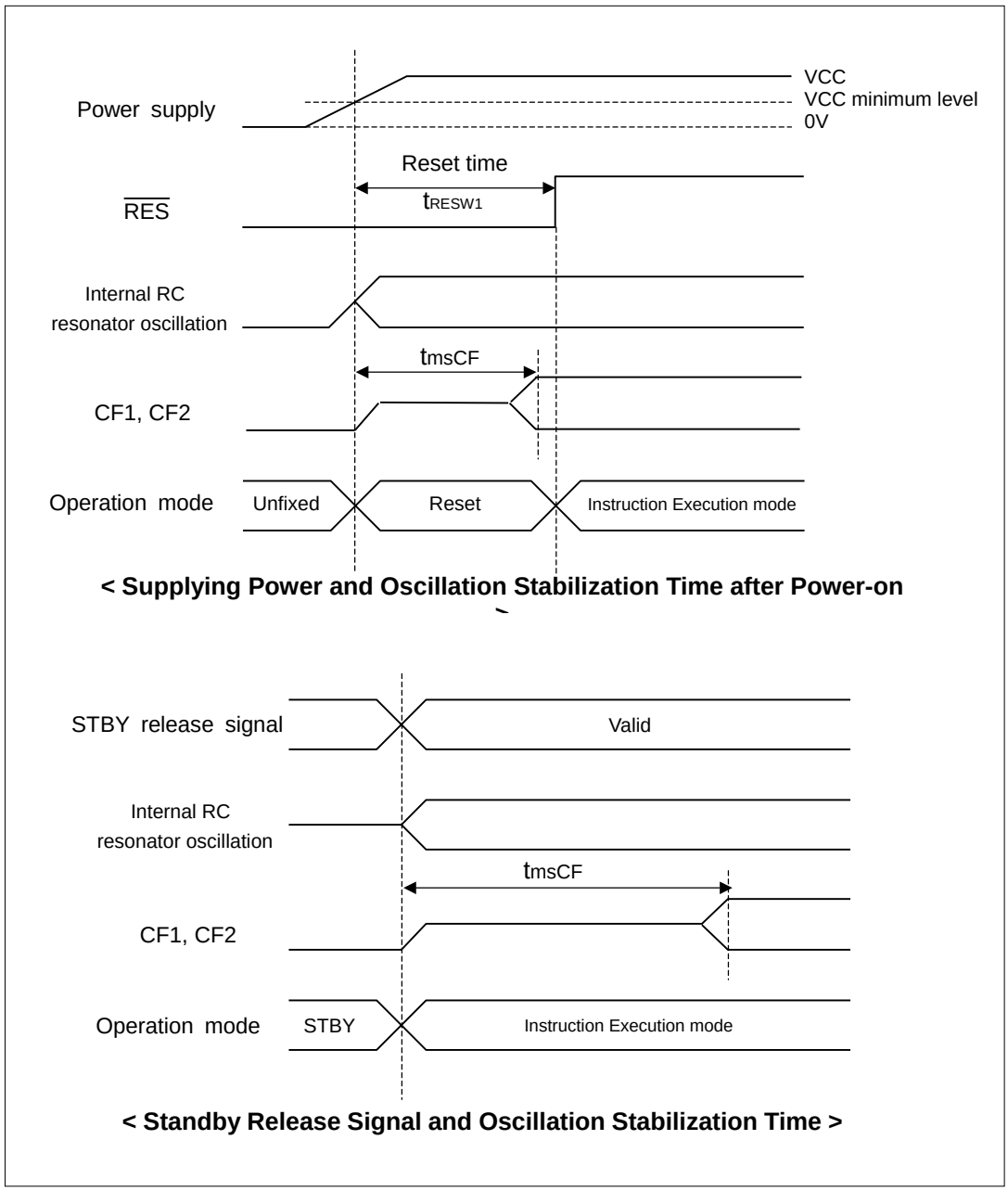


Figure 3 Oscillation Stabilization Time

NOTE: 10ms or more is required for the reset time at power-on.

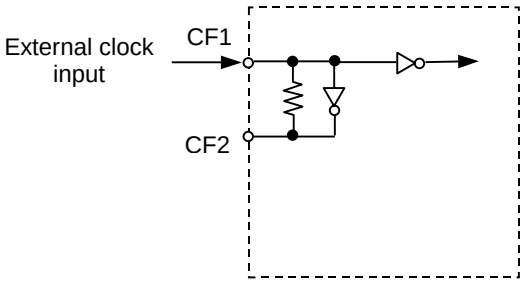


Figure 4 External clock input

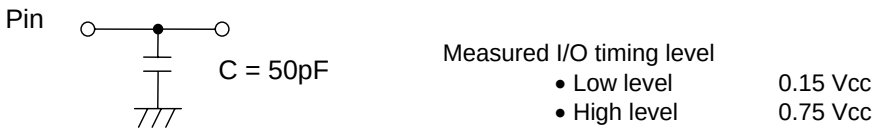


Figure 5 AC Timing loading

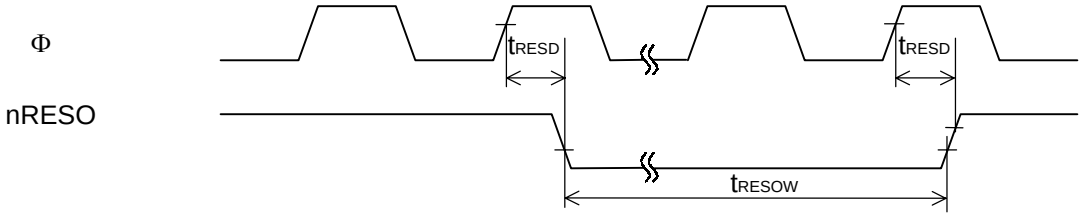


Figure 6a Reset output timing

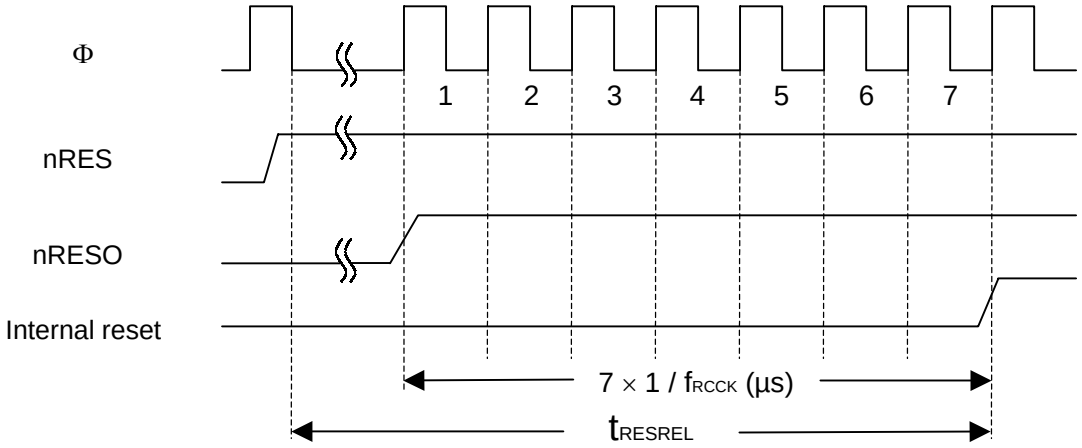


Figure 6b Reset release timing

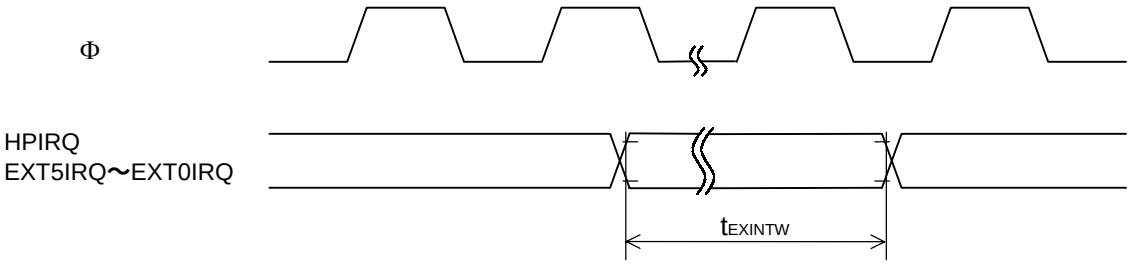


Figure 7 Interrupt input timing

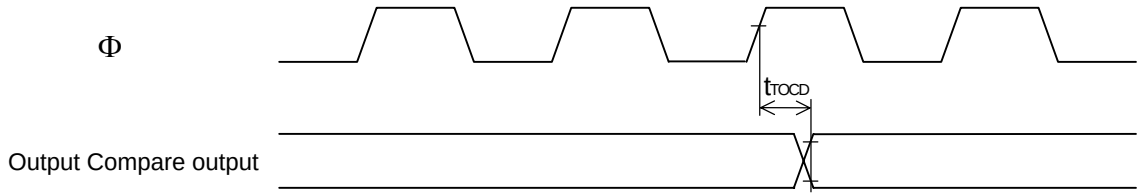


Figure 8 MTM output timing

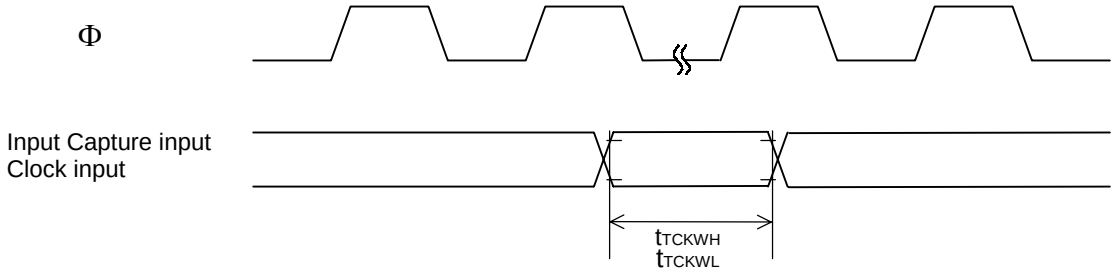
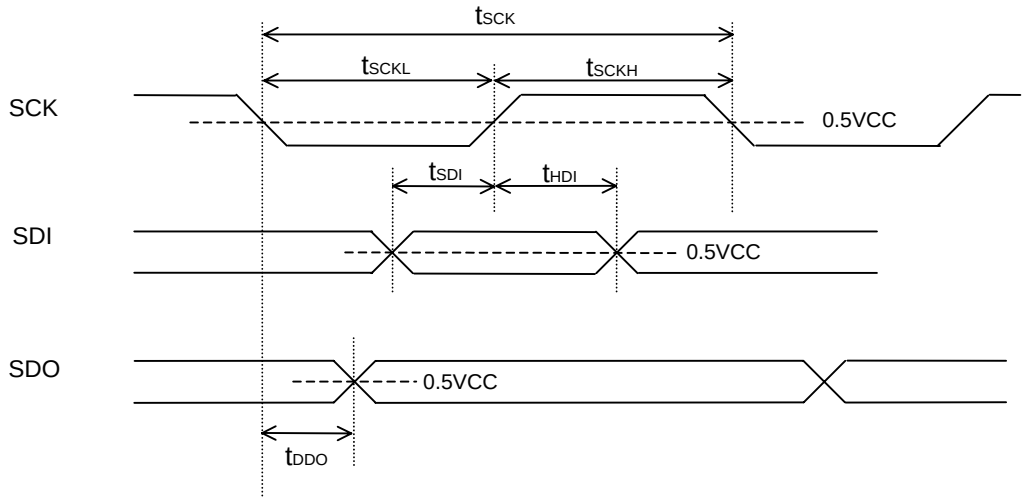


Figure 9 MTM input timing



NOTE: If the polarity of SCK is inverted, the SCK waveform (shown above) turns upside down.

Figure 10 Serial I/O timing

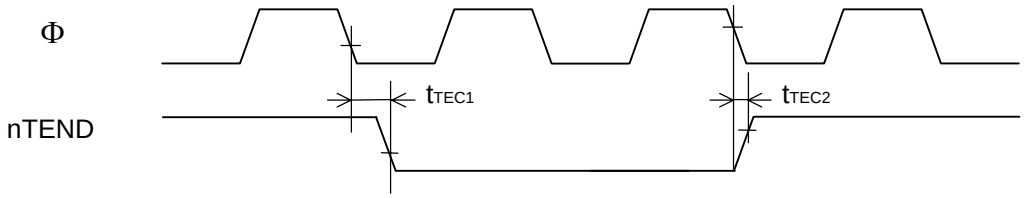


Figure 11　nTEND output timing of DMAC

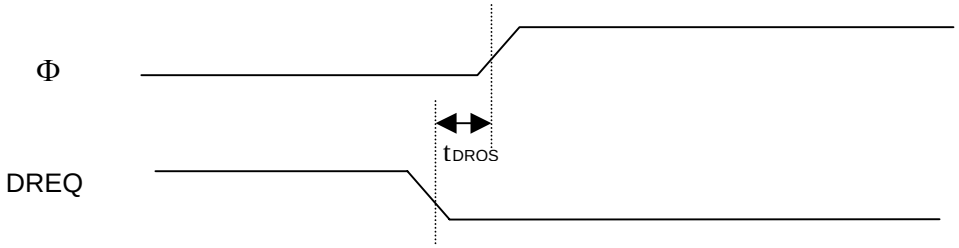


Figure 12　DREQ input timing of DMAC

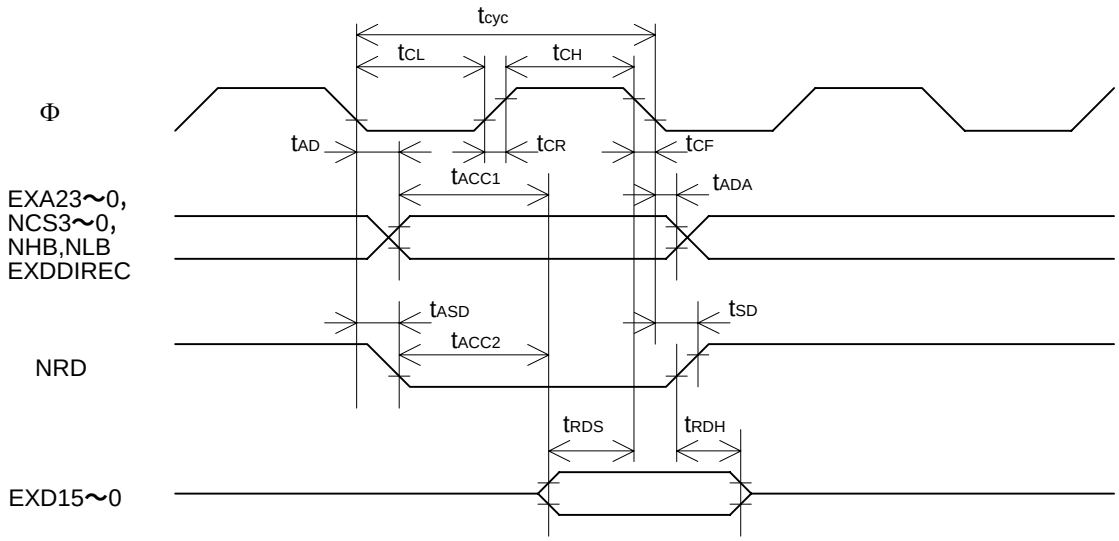


Figure 13a　Read timing of the external bus (No wait, RTCR=0)

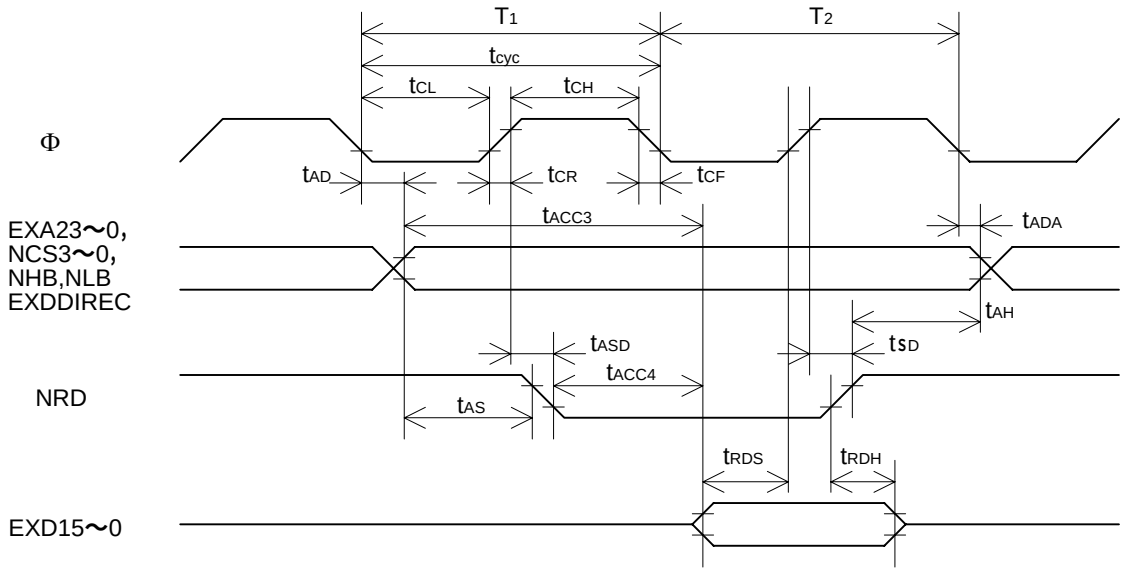


Figure 13b Read timing of the external bus (1 wait, RTCR=1)

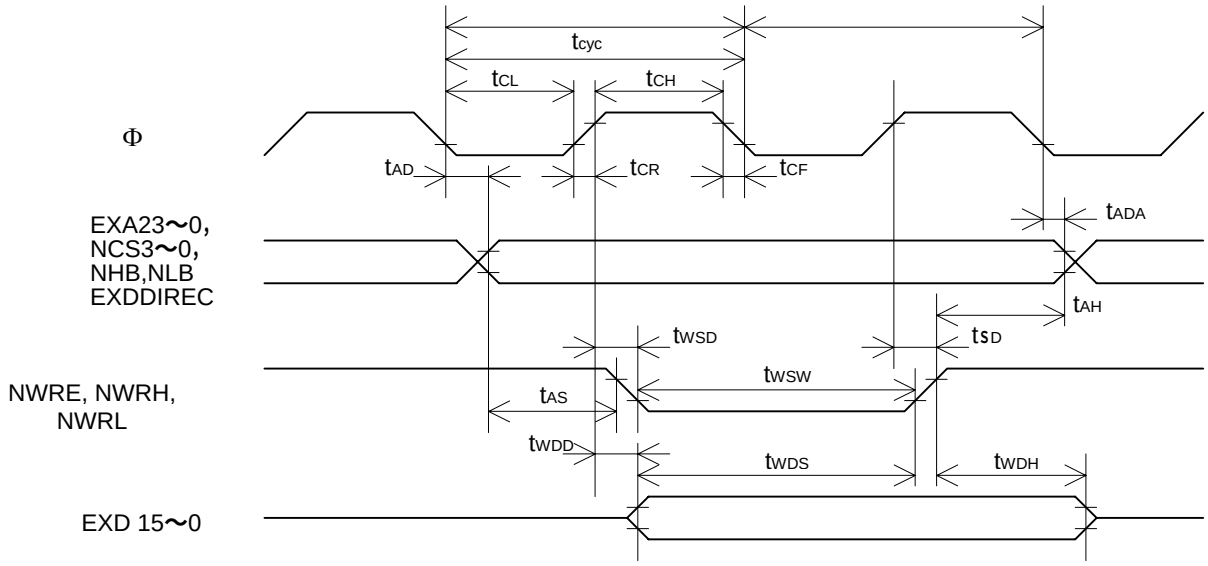


Figure 13c Write timing of the external bus (1 wait)

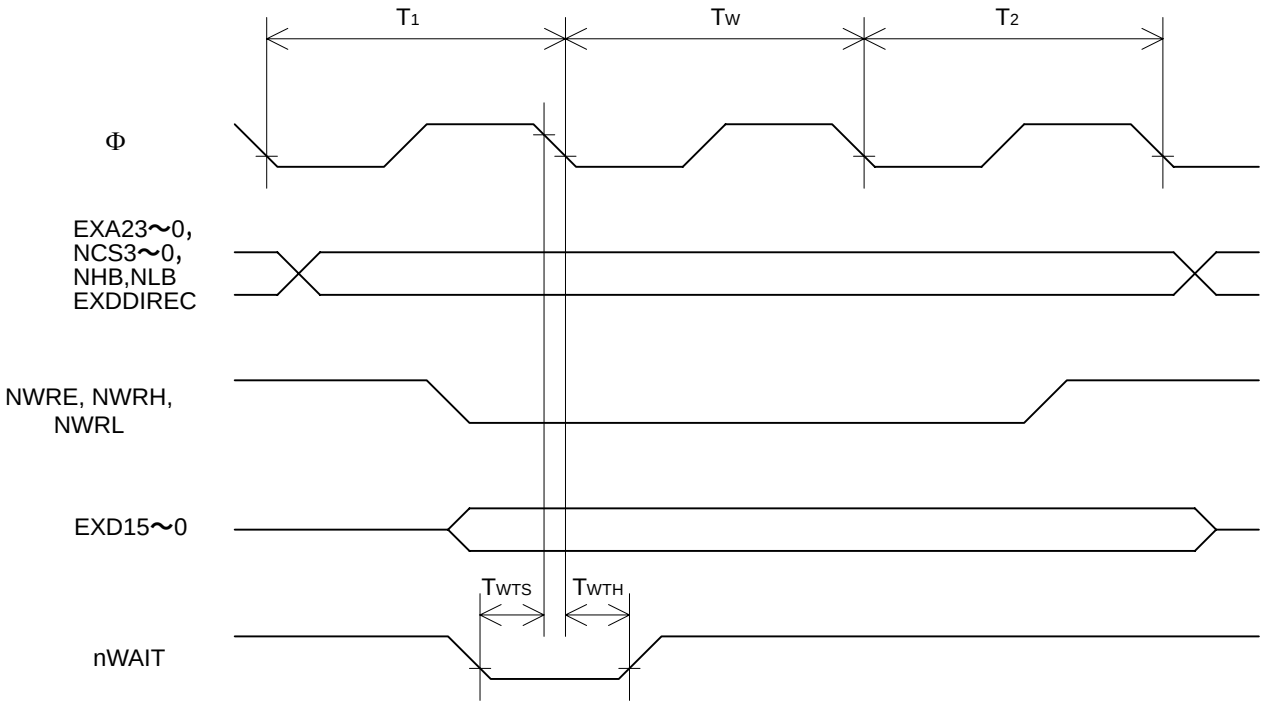


Figure 13d　Wait timing of the external bus (external 1 wait)

Points to take into consideration when designing your system

Points to be aware of in the design of systems (which use this microcontroller) and measures that can be taken to reduce noise are outlined below. These are useful in avoiding operation failure due to noise such as erroneous operation or system crashes.

1. VDD,VSS: power supply pins

The capacitors should be connected in accordance with the following design rules.

- The distances from the VDD, VSS pins to the capacitors C1 and C2 should be as similar (to each other) (L1=L1', L2=L2') and as short as possible.
- C1 (having a large capacitance) and C2 (having a small capacitance) should be connected in parallel.
  *C2 should have a capacitance of at least 4400pf.
- The VDD and VSS patterns should be wider than those of others.

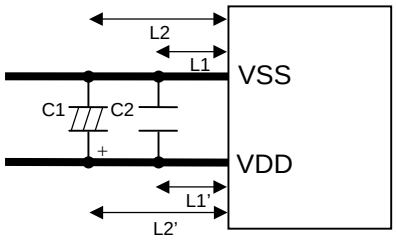


Figure 15 Sample power supply circuit

2. CF1,CF2: clock input/output pins

Oscillation by a ceramic resonator (Refer to figure 16)

- The distance between the clock I/O pins (C1 is for input and C2 for output) and external parts (Losc) should be as short as possible. (1cm maximum)
- The distance between the VSS side of the capacitors connected to the ceramic oscillator and the microcontroller's VSS pin (Lvss+L1[L2]) should be as short as possible.
- The VSS of the oscillation circuit (and other VSSs) should be placed away from the terminals.
- The values for the oscillation parameters such as capacitors C1, C2 and resistor Rd recommended in this document may need to be changed depending on the amount of wiring in your system board in order to attain the desired clock frequency. For further information, please contact your oscillator manufacturer.

External Oscillation (Refer to figure 17)

- The distance between the clock input pin (CF1) and the external oscillator (Losc) should be as short as possible.
- Please leave the clock output pin open (CF2).
- The distance between the external oscillator and its VDD, VSS (Losc) should also be as short as possible.

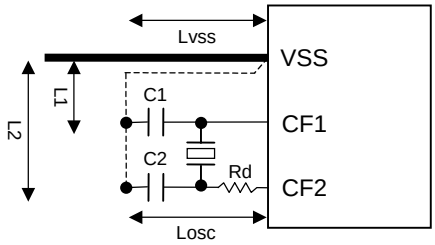


Figure 16 Sample oscillation circuit 1 (using a ceramic resonator)

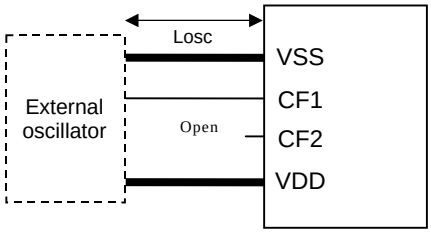


Figure 17 Sample oscillation circuit 2 (using an external oscillator)

Additional notes

Signal lines with rapid state changes, large amplitude or through which large current flows should be allocated away from the oscillation circuit and should not cross over any lines which are related to the clock.

3. nRES: Reset pin
   - The distance between the nRES pin and the external circuit (Lres) should be as short as possible.
   - The capacitor connected between VSS and nRES (Cres) should be as close as possible to the VSS and nRES pins.

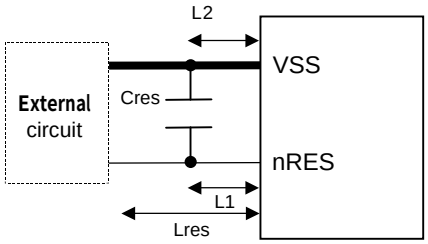


Figure 18 Sample of the nRES pin wiring

4. TEST: Test pin
   - The distance between the TEST pin and VSS line (L) should be as short as possible.
   - The line connecting the TEST pin and VSS pin should be connected as close as possible to the VSS pin.

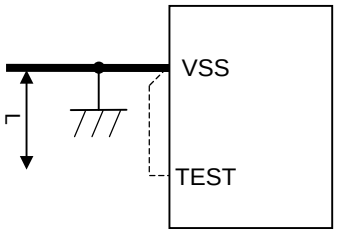


Figure 19 Sample of the TEST pin wiring

5. AN0 to AN7: Analog input pins

   The wiring of analog input pins such as the AD converter input pins should be conducted with respect to the following design rules.
   - The distance between the limiting resistor (R1) and the analog input pins (L1) should be as short as possible.
   - The capacitor between the analog input pins and AVSS pin (C) should be connected as close as possible to the AVSS pin. ((L1 + L2) should be as short as possible.)

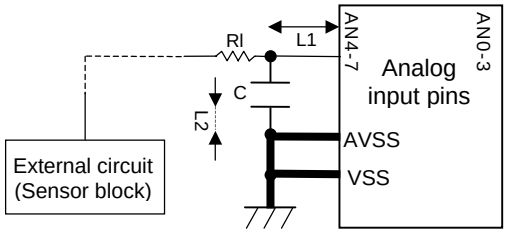


Figure 20 Sample of the analog pins wiring

6. Input and I/O pins

   If a pin is to be used for input, a limiting resistor should be connected to it and the distance between the pin and resistor should be made as short as possible.

   [Supplement**]** Aside from the hardware design rules, so as to prevent the microcontroller from behaving unpredictably, we also recommend that the following design rules be implemented with respect to the software:
   - When an external signal is input from a pin, debouncing of the signal should be performed.
   - When outputting data from a pin, the data should be re-output periodically.

7. Unused pins

   For details, please refer to the relevant user's manual or the “Pin Descriptions” section of this document.