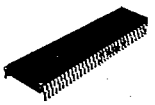
LC67216A



T-49-19-04

3071

CMOS LSI

4-Bit Single Chip Microcomputer

On-Chip FLT Controller, A/D Converter, Remote Control Signal Detector, 16K-Byte ROM

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TENTATIVE

Overview

The LC67216A is a 4-bit single chip microcomputer fabricated with CMOS technology. It includes CPU (operational speed: 0.92 μs), ROM (16K bytes), RAM (608 words), AD converter, DA converter (PWM type), Remote control signal receiver, FLT display controller/driver, and horizontal synchronization detect counter in a 64-pin package.

Applications:

- VCR timer, audio timer, DSP amp controller

Features:

(1) Dedicated hardware: Simpler program and more additional values
- FLT display controller/driver → Total 28 lines (max.): 20 segments and 16 digits (max.), Various display modes (dimmer, static, and so on), and automatic scanner function (no interrupt processing required)
- Remote control signal receiver → Continuous pulse (L, H) detection by remote control detection timer and internal high-frequency band noise elimination filter. Recommended for use in products with the 'Association of home electronic appliances' standards.
- Tone output → Beep sound and melody tone outputs
- Horizontal synchronization detect counter → Tuner synchronization detectable by an independent 9-bit counter
- PWM type DA converter → 14-bit DAC output, voltage synthesizer tuner and electronic volume control

(2) AD converter: Lower cost, more additional values and higher functionality
- Direct input of various analog signals → AD conversion for level meter and display, S curve detect → no dedicated IC required.
- key matrix input by resistance division → Better economical space layout, less pins count, reduced harness and improved radiation immunity

(3) Protection against noise radiation
- Improved protection against noises from oscillation circuit or FLT driving circuit → Shortened noise protection design process and parts reduction in noise protection mechanism

(4) Clock standby function
- Two types of oscillation circuits (4MHz band and 32KHz band) → Battery-backed-up clock application

Hardware Configuration

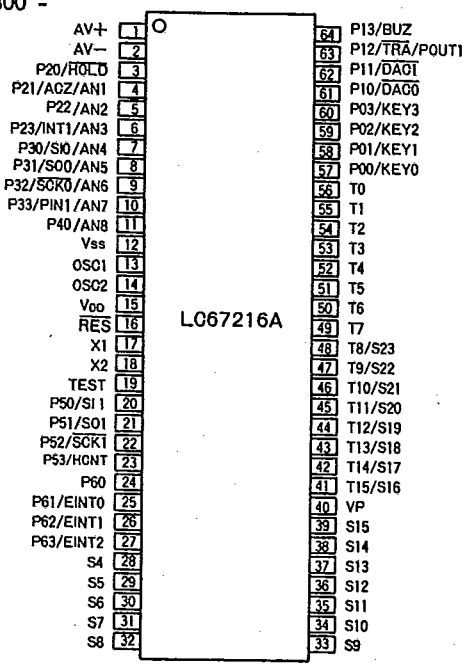
Applicable to: LC66000 series/LC67000 series microcomputers

Model name	LC66506B/508B/512B/516B	LC66304A/306A/308A	LC67216A
ROM capacity	6K/8K/12K/16K bytes	4K/6K/8K bytes	16K bytes
RAM capacity	512×4	512×4	608×4 (96 x 4 for display)
Packaging	DIP64S, QIP64	DIP42S	DIP64S
High withstand voltage port	Not provided.	Not provided.	Provided (28 lines)
Analog input	Comparator (4 channels) Tri-state input (2 channels)	Comparator (4 channels) Tri-state input (2 channels)	AD converter with an accuracy of 4 bits (8 channels)
Evaluation chip	LC66599	LC66599	LC67999
Remarks	Currently on the market	Currently under development	Currently on the market

Functions:

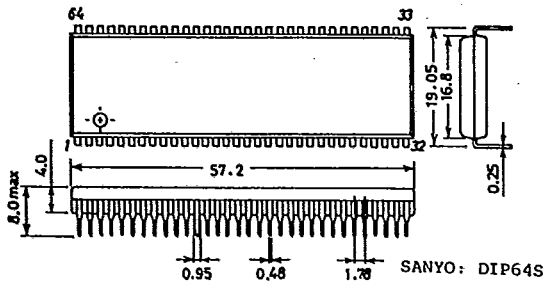
(1) Instructions: 116 (upwards compatible with the LC66000 series microcomputers)
(2) ROM capacity: 16K bytes. RAM capacity: 608x 4 words (of the capacity, 96 x 4 words used as the display RAM)
(3) Minimum cycle time: 0.92 µs at 4.5V to 6.0V. 7.6 µs at 3.0V to 6.0V
(4) System clock selectable by a software → Less power dissipation
- In case of main system clock = 4.19MHz: 0.95, 7.6 or 30.6 µs
- In case of sub system clock = 32.768KHz: 61 µs
(5) Input/output ports: Total = 53 lines
- Output ports: 28 lines → FLT controller directly drivable
- Input/output ports: 24 lines → LED directly drivable
- Input port: 1 line
(6) Interrupt: 11 sources (external interrupt = 4 lines, AC zero cross interrupt = 1 line , timer interrupt = 3 lines, serial input/output interrupt = 2 lines, and key scan interrupt = 1 line). 6 vector addresses.
(7) Timer: 3-channel multiple-functional timer
- Timer 1: Remote control signal receiver/8-bit interval + tone generator
- Timer 2: PWM type DA converter(14 bits or 8 bits + 6 bits)/tone generator
- Time base timer: Clock counter(also used as a watchdog timer)/14-bit event counter
(8) Serial input/output: 8 bits x 2 channels. One of them can be used as the LSB-first or the MSB-first serial transfer port.
(9) 4-bit 8-channel AD converter: AD conversion mode/comparator mode
(10) FLT display controller
- Segments: 8 to 20. Digits: 8 to 16 → Selectable by software.
- 8-level dimmer function
- Pull-down resistor option available
- Static display mode available
(11) On-chip 9-bit counter for detecting horizontal sync.
(12) On-chip AC zero cross detector
(13) On-chip triac driver
(14) Standby function
- Count operation continues while the CPU operation stops.
- All of the operations stop. Oscillation stabilization at the restart is internally supported.
(15) Oscillation circuits: 2
- Main clock: 4.19MHz crystal oscillator or 4.0MHz ceramic resonator
- Sub clock: 32.768kHz crystal oscillator
(16) Packaging: DIP64S
(17) Evaluation LSI: LC67999(evaluation chip) + EVA850/800 + TB67216(evaluation chip board). LC67PG216 (piggyback type)

DIP64S

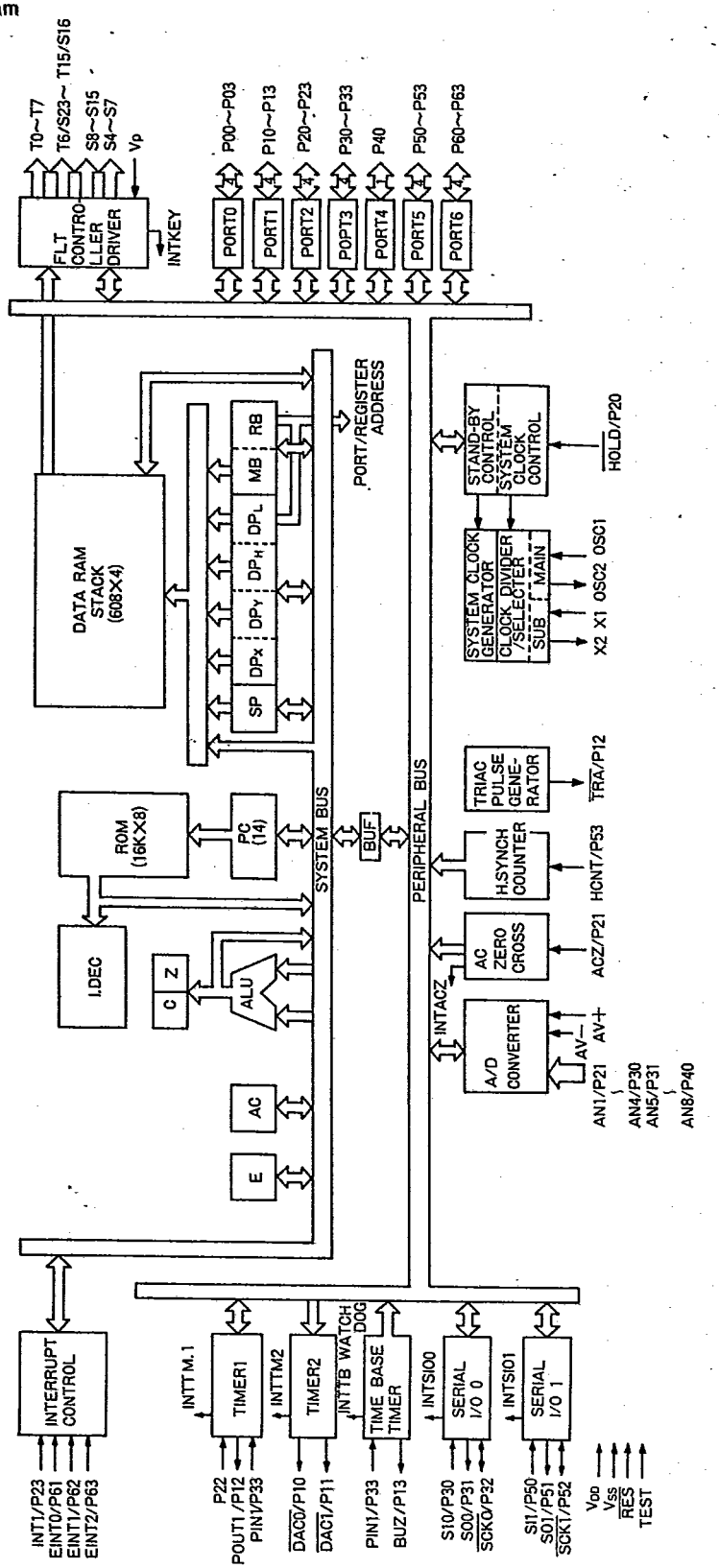


Pin Assignment

Case Outline 3071-D64IC
(unit:mm)



System Block Diagram



LC67216A Block Diagram

Development Support System

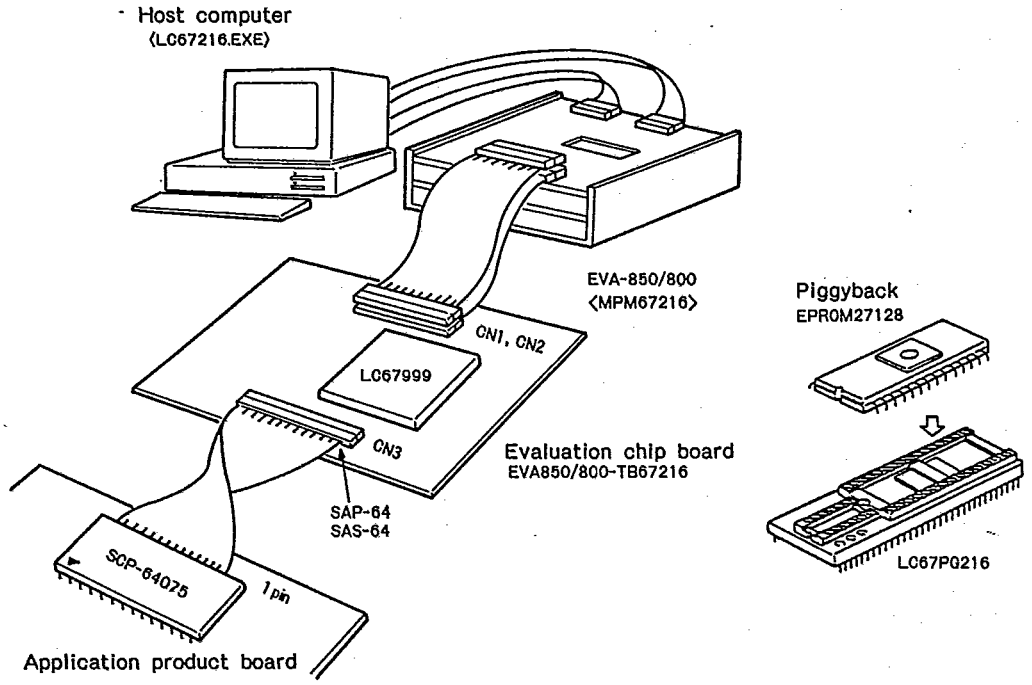
The following development support tools are provided to develop application programs for the LC67216A microcomputer.

(1) User's Manual
LC67216A User's Manual

(2) Development Tool Manual
EVA850/800-LC67216 Development Tool Manual

(3) Development Support Tools
1 Tools for developing application programs
i. Host computer --- Sanyo MS-DOS machine compatible with IBM PC/XT or IBM PC/AT.
ii. Cross Assembler ---MS-DOS based cross assembler (LC67216.EXE)
2 Tools for evaluating application programs
i. Emulator --- EVA-850 main unit or EVA-800 main unit (monitor ROM: MPM67216) and EVA chip board (EVA850/800-TB67216)
ii. Evaluation chip --- LC67999
iii. Simulation chip --- LC67PG216

Outline of the development support system



Note 1: IBM PC/XT and IBM PC/AT are products of IBM Corporation. MS-DOS is a registered trademark of Microsoft Corporation.

Note 2: The suffixes of the EVA-850 and EVA-800 change like A to B, B to C, and so on as some improvements are made on them.
Please check the suffix before starting program evaluation.

Pin Description

Pin No	Pin name	I/O	Function(s)
1	AV+	—	AD conversion reference voltage input (+)
2	AV−	—	AD conversion reference voltage input (-)
3	P20/$\overline{\text{HOLD}}$	I	Input/HOLD control input
4	P21/ACZ/AN1	I/O	Input/output, also used as AC zero cross input/AD input
5	P22/AN2	I/O	Input/output, also used as AD input.
6	P23/INT1/AN3	I/O	Input/output, also used as interrupt input/AD input
7	P30/SI1/AN4	I/O	Input/output, also used as serial input/AD input.
8	P31/SO0/AN5	I/O	Input/output, also used as serial output/AD input.
9	P32/$\overline{\text{SCK0}}$/AN6	I/O	Input/output, also used as serial clock input/output or AD input.
10	P33/PIN1/AN7	I/O	Input/output, also used as remote control signal input/AD input.
11	P40/AN8	I/O	Input/output, also used as AD input.
12	Vss	—	Power supply (-)
13	OSC1	I	Main clock oscillation input
14	OSC2	O	Main clock oscillation output
15	VDD	—	Power supply (+)
16	$\overline{\text{RES}}$	I	Reset input
17	X1	I	Sub clock oscillation input
18	X2	O	Sub clock oscillation output
19	TEST	I	Test input
20	P50/SI1	I/O	Nch medium withstand voltage input/output, also used as serial input.
21	P51/SO1	I/O	Nch medium withstand voltage input/output, also used as serial output.
22	P52/$\overline{\text{SCK1}}$	I/O	Nch medium withstand voltage input/output, also used as serial clock input/output
23	P53/HCNT	I/O	Nch medium withstand voltage input/output, also used as H counter input.
24	P60	I/O	Nch medium withstand voltage input/output
25	P61/EINT0	I/O	Nch medium withstand voltage input/output, also used as interrupt input
26	P62/EINT1	I/O	Same as above
27	P63/EINT2	I/O	Same as above
28	S4	O	Pch high withstand voltage output (for segment)
29	S5	O	Same as above.
30	S6	O	Same as above.
31	S7	O	Same as above.
32	S8	O	Same as above.
33	S9	O	Pch high withstand voltage output (for segment)
34	S10	O	Same as above.
35	S11	O	Same as above.
36	S12	O	Same as above.
37	S13	O	Same as above.
38	S14	O	Same as above.
39	S15	O	Same as above.
40	Vp	—	Power supply for pull- down resistors
41	T15/S16	O	Pch high withstand voltage output (for digit/segment)
42	T14/S17	O	Same as above.
43	T13/S18	O	Same as above.
44	T12/S19	O	Same as above.
45	T11/S20	O	Same as above.
46	T10/S21	O	Same as above.
47	T9/S22	O	Same as above.
48	T8/S23	O	Same as above.
49	T7	O	Pch high withstand voltage output (for digit)
50	T6	O	Same as above.
51	T5	O	Same as above.
52	T4	O	Same as above.
53	T3	O	Same as above.
54	T2	O	Same as above.
55	T1	O	Same as above.
56	T0	O	Same as above.
57	P00/KEY0	I/O	Nch medium withstand voltage input/output, also used as key scan input.
58	P01/KEY1	I/O	Same as above.
59	P02/KEY2	I/O	Same as above.
60	P03/KEY3	I/O	Same as above.
61	P10/$\overline{\text{DAC0}}$	I/O	Nch medium withstand voltage input/output, also used DA output.
62	P11/$\overline{\text{DAC1}}$	I/O	Nch medium withstand voltage input/output, also used DA output.
63	P12/$\overline{\text{TRA}}$ /POUT1	I/O	Nch medium withstand voltage input/output, also used triac output/pulse output.
64	P13/BUZ	I/O	Nch medium withstand voltage input/output, also used as buzzer sound output.

Pin Function

Pin name	#	I/O	Option(s)	Functional description	Logic and mode at reset	Unused pin handling
V_{DD}	1	—	—	Power supply	—	—
V_{SS}	1	—				
Vp	1	—	—	Power supply for high withstand voltage pin load	—	Connected to V_{DD}.
AV+	1	—	—	AD converter reference voltage input	—	Connected to V_{SS}.
AV−	1	—				
TEST	1	I	—	LSI test input. Be sure to connect this with V_{SS}.	—	Always connected to V_{SS}.
$\overline{RES}$	1	I	—	System reset input. With $\overline{HOLD}$ = 'H' and $\overline{RES}$ = 'L', the system will be initialized (initial system reset).	—	—
OSC1	1	I	• CF • X'tal • External input	Main system clock oscillation circuit pin. If external clock input is selected, leave the OSC2 pin open and use the OSC1 input pin.	—	—
OSC2	1	O				
X1	1	I	—	Sub clock oscillation circuit pin. If external clock input is selected, leave the X2 pin open and use the X1 input pin. With on-chip feedback resistor and damping resistor.	—	Connect X1 to V_{DD} while leave X2 open.
X2	1	O				
P00/KEY0 P01/KEY1 P02/KEY2 P03/KEY3	4	I/O	• Pull-up/open drain output (in bit units) • Pull-down resistor (in-bit units)	Input/output in bit units or 4-bit units. Output circuit type can be selected for each pin from open drain (OD) and pull-up MOS output (PU) types. If OD is selected, the withstand voltage level will be +15V. Low threshold level input for key scan input. Automatic key data storage into RAM	'H' in output mode	Connect OD pin to V_{SS} while leave the PU pin open.
P10/$\overline{DAC0}$ P11/$\overline{DAC1}$ P12/$\overline{TRA}$ /POUT1 P13/BUZ	4	I/O	• Pull-up/open drain output (in bit units)	Input/output in bit units or 4-bit units. Output circuit type can be selected for each pin from open drain (OD) and pull-up MOS output (PU) types. If OD is selected, the withstand voltage level will be +15V. Alternative pin function(s) $\overline{DAC0}$ PWM DAC0 output from timer 2 $\overline{DAC1}$ PWM DAC1 output from timer 2, and program pulse output [$\overline{TRA}$ /POUT1 Triac control pulse output, or program pulse output from timer 1 BUZ Buzzer output from time base timer	'H' in output mode	Connect OD pin to V_{SS} while leave the PU pin open.
P20/$\overline{HOLD}$	4	I	—	Input/output in bit units or 4-bit units. A direction register is provided to set an operation mode (input mode or output mode) for each port bit. The P20/$\overline{HOLD}$ pin is used only as the input pin. Alternative pin function(s) $\overline{HOLD}$ HOLD control input and reset inhibit input ACZ AC zero cross detect input INT1 Interrupt input AN1 AD converter channel 1 input AN2 AD converter channel 2 input AN3 AD converter channel 3 input	Input mode	Connected to V_{DD}. The pins already connected to V_{DD} should not be set to the output mode by software.
P21/ACZ/AN1		I/O				
P22/AN2		I/O				
P23/INT1/AN3		I/O				
P30/SI0/AN4 P31/SO0/AN5 P32/$\overline{SCK0}$ /AN6 P33/PIN1/AN7	4	I/O	—	Input/output in bit units or 4-bits units. A direction register is provided to set an operation mode (input mode or output mode) for each port bit. Alternative pin function(s) SI0 Serial I/O channel 0 → Serial data input SO0 Serial I/O channel 0 → Serial data output $\overline{SCK0}$ Serial I/O channel 0 → Serial clock input/output PIN1 External interrupt source input (timer 1 and time base timer) AN4 AD converter channel 4 input AN5 AD converter channel 5 input AN6 AD converter channel 6 input AN7 AD converter channel 7 input	Input mode	Connected to V_{DD}. Note that the pins already connected to V_{DD} should not be set to the output mode by software.

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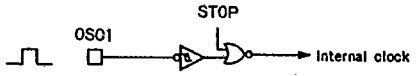
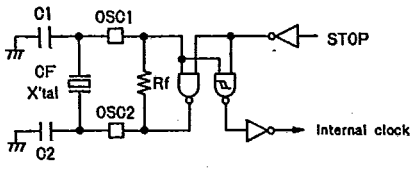
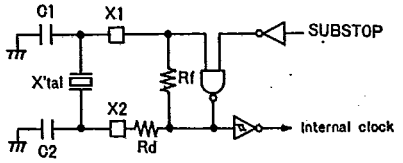
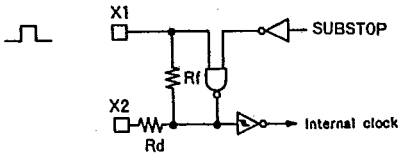
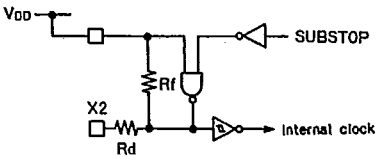
Pin name	No.	I/O	Option(s)	Functional description	Logic and mode at reset	Unused pin handling
P40/AN8	1	I/O	—	Input/output in bit units. A direction register is provided to set an operation mode (input mode or output mode) for each port bit. Alternative pin function AN8 AD converter channel 8 input	Input mode	Connected to V_{DD}. Note that the pins already connected to V_{DD} should not be set to the output mode by software.
P50/SI1 P51/SO1 P52/$\overline{SCK1}$ P53/HCNT	4	I/O	• Pull-up/open drain output (in bit units)	Input/output in bit units or 4-bit units. Output circuit type can be selected for each pin from open drain (OD) and pull-up MOS output (PU) types. If OD is selected, the withstand voltage level will be +15V. A port control register is provided to set an operation mode (input mode or output mode) for all the four port pins at the same time. Alternative pin function(s) SI1 Serial I/O channel 1 → Serial data input SO1 Serial I/O channel 1 → Serial data output $\overline{SCK1}$ Serial I/O channel 1 → Serial clock input/output HCNT H counter count input	Input mode	Connect the OD pin to V_{SS} while leave the PU pin open.
P60 P61/EINT0 P62/EINT1 P63/EINT2	4	I/O	• Pull-up/open drain output (in bit units)	Input/output in bit units or 4-bit units. Output circuit type can be selected for each pin from open drain (OD) and pull-up MOS output (PU) types. If OD is selected, the withstand voltage level will be +15V. Alternative pin function(s) EINT0 Extended interrupt input EINT0 EINT1 Extended interrupt input EINT1 EINT2 Extended interrupt input EINT2	'H' in output mode	Same as above.
S4~S7	4	O	Pull-down resistor (in bit units)	Segment outputs from an FLT controller (S4 to S7). If static display mode is selected, these output pins are used to output data to an external circuit from a fixed RAM address (general discrete output).	'L' in output mode	Leave the pull-down type pins open while connect the OD type pins to V_{DD}.
S8~S15	8	O	Pull-down resistor (in bit units)	Segment outputs from an FLT controller (S8 to S15). If static display mode is selected, these output pins are used to output data to an external circuit from fixed RAM addresses (general discrete output).	'L' in output mode	Same as above.
T0~T7	8	O	Pull-down resistor (in bit units)	Timing signal outputs from an FLT controller (T0 to T7). If static display mode is selected, these output pins are used to output data to an external circuit from fixed RAM addresses (general discrete output).	'L' in output mode	Same as above.
T8/S23~ T15/S16	8	O	Pull-down resistor (in bit units)	Timing signal/segment outputs from an FLT controller (alternate output pins). If static display mode is selected, these output pins are used to output data to an external circuit from fixed RAM addresses (general discrete output). In addition, unused pins are used for the same purpose.	'L' in output mode	Same as above.

User Options

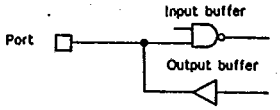
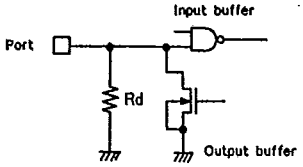
① Options for main clock oscillation circuits

Option name	Related pins	Oscillation circuit type	Circuit conditions
External clock option	OSC1, OSC2		- Internal clock input with Schmitt specification - Leave the OSC2 pin open.
Ceramic (CF) resonator oscillation option Crystal (X'tal) oscillation option			- Rf is a feedback resistor. - Internal clock input with Schmitt specification

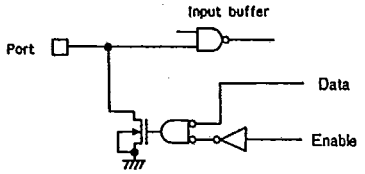
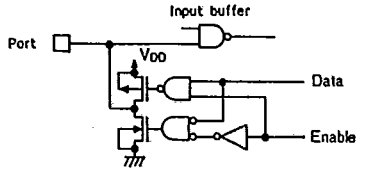
② Options for sub clock oscillation circuits

Option name	Related pins	Oscillation circuit type	Circuit conditions
Crystal (X'tal) oscillation option	X1, X2		- Rf is a feedback resistor. - Rd is a damping resistor.
External clock option			- Leave the X2 pin open.
No sub clock oscillation circuit			- Connect the X1 pin to VDD. - Leave the X2 pin open.

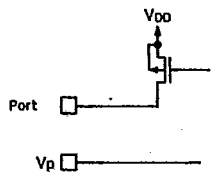
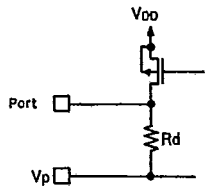
③ Options for port 0 input pull-down resistor (in 4-bit units)

Option name	Related pins	Oscillation circuit type	Circuit conditions
No pull-down resistor selected	P00~P03		
Pull-down resistor selected			- The pull-down resistor has been selected. Note that the pull-down resistor option can be used independently of the pull-up (PU) transistor output option.

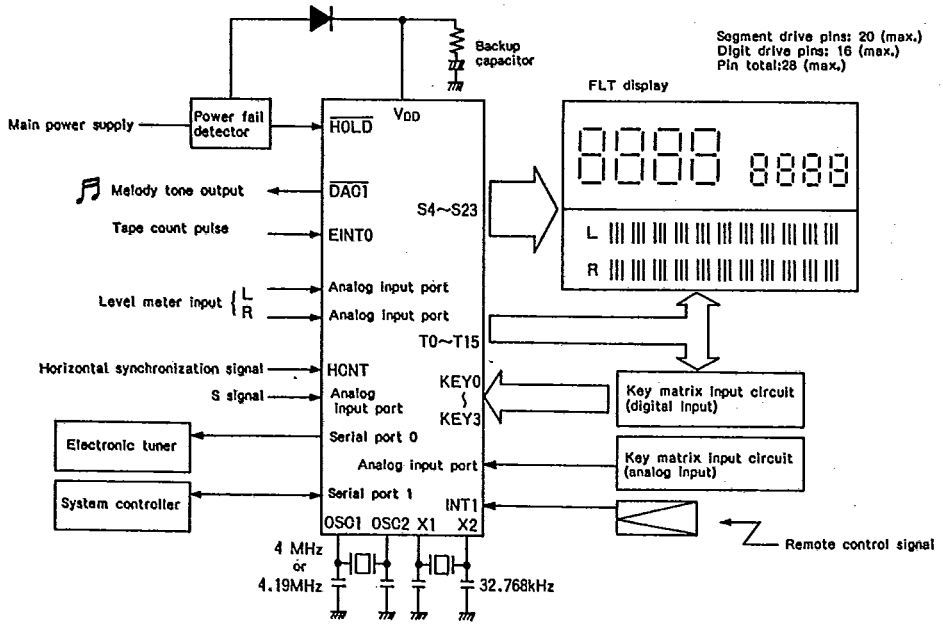
④ Options for output circuit types of medium withstand voltage ports (in bit units)

Option name	Related pins	Oscillation circuit type	Circuit conditions
Nch open drain output (OD)	P00~P03 P10~P13 P50~P53 P60~P63		Input/output withstand voltage level = +15V
Pull- up transistor output (PU)			Input/output withstand voltage level = V_{DD} + 0.3V. The output types can be divided into two according to Pch transistor driving capability: CMOS output (P1 and P5) and PU MOS output (P0 and P6).

⑤ Options for the output types of high withstand voltage ports (in bit units)

Option name	Related pins	Oscillation circuit type	Circuit conditions
Pch open drain output (OD)	T0~T7 T8/S23~T15/S16 S4~S15		
Output with a pull-down resistor (PD)			

Example application



Example application: VCR channel select timer, level meter, tape counter, and remote control signal receiver

T-49-19-04

Main Specifications for the LC67216A

1. Absolute Maximum Ratings/Ta = 25°C, V_{SS} = 0V

Parameter	Symbol	Related Pins	Conditions		Limits	Units
Power supply voltage	V_{DD} max	V_{DD}			−0.3~+7.0	V
	V_P max	V_P			V_{DD}−45~V_{DD}+0.3	
	AV+max	AV+			−0.3~V_{DD}+0.3	
	AV−max	AV−			−0.3~V_{DD}+0.3	
Input voltage	V_I(1)	OSC1, X1	Self oscillation		Up to produced voltage.	V
	V_I(2)	TEST, $\overline{RES}$, OSC1 P20/$\overline{HOLD}$	OSC1: External clock input		−0.3~V_{DD}+0.3	
	V_I(3)	P00~P03	Input pull-down resistor selected. Nch output transistor OFF.		−0.3~V_{DD}+0.3	
Output voltage	V_O(1)	OSC2, X2	Self oscillation		Up to produced voltage.	V
	V_O(2)	S4~S15 T0~T7 T8/S23~T15/S16			V_{DD}−45~V_{DD}+0.3	
Input/ output voltage	V_{IO}(1)	P21~P23 P30~P33 P40			−0.3~V_{DD}+0.3	V
		P00~P03 P10~P13 P50~P53 P60~P63	Pull-up option selected.			
	V_{IO}(2)	P00~P03 P10~P13 P50~P53 P60~P63	Open drain option selected. P00-P03; Without input pull-down resistor		−0.3~+15	V
Output current	I_{OP}(1)	P00~P03 P60~P63	Pull-up option selected	Per pin	−2~0	mA
		P21~P23	Output enable mode			
	I_{OP}(2)	P10~P13 P50~P53	Pull-up option selected	Per pin	−4~0	mA
		P30~P33 P40	Output enable mode			
	I_{OP}(3)	S4~S15	Per pin		−15~0	mA
	I_{OP}(4)	T0~T7 T8/S23~T15/S16	Per pin		−30~0	mA
	I_{ON}(1)	P00~P03 P21~P23 P40 P60~P63	Per pin		0~15	mA
	I_{ON}(2)	P30~P33 P50~P53			0~20	
	I_{ON}(3)	P10~P13			0~50	
	ΣI_{OP}(1)	P00~P03 P10~P13	Pull-up option selected	Pin total	−15~0	
		P21~P23 P30~P33 P40	Output enable mode			
	ΣI_{OP}(2)	P50~P53 P60~P63	Pull-up option selected	Pin total	−120~0	
		S4~S15 T0~T7 T8/S23~T15/S16				

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Parameter	Symbol	Related Pins	Conditions		Limits	Units
Output current	$\Sigma I_{ON}(1)$	P00~P03 P10~P13 P21~P23 P30~P33 P40	Pin total	Average value for 100 msec	0~55	mA
	$\Sigma I_{ON}(2)$	P50~P53 P60~P63	Pin total	Average value for 100 msec	0~30	mA
Allowable power dissipation	Pd max	DIP-64S	Ta=−30~+70℃		600	mW
Operating temperature range	Topg				−30~+70	℃
Storage temperature range	Tstg				−55~+125	℃

2. Recommended Operating Conditions/ Ta=−30to+70℃, Vss=0 V

Parameter	Symbol	Related Pins	Conditions		V_{DD}(V)	Limits min	Limits typ	Limits max	Units
Operating power supply	$V_{DD}(1)$	V_{DD}	0.92μs≦ Tcyc≦67μs	Main clock operation mode		4.5		6.0	V
	$V_{DD}(2)$		7.36μs≦ Tcyc≦67μs			3.0		6.0	
	$V_{DD}(3)$		40μs Tcyc≦67μs	Sub clock operation mode		3.0		6.0	
	Vp	Vp				−35		V_{DD}	V
	AV+	AV+				AV−		V_{DD}	
	AV−	AV−				Vss		AV+	
Power supply for RAM backed-up mode	V_{ST}	V_{DD}	HOLD mode			1.8		6.0	V
Input High voltage	$V_{IH}(1)$ (Schmitt)	$\overline{RES}$			4.5~6.0	0.75V_{DD}		V_{DD}	V
					3.0~4.5	0.8V_{DD}		V_{DD}	
					1.8~3.0	0.85V_{DD}		V_{DD}	
	$V_{IH}(2)$ (Schmitt)	P20/$\overline{HOLD}$			4.5~6.0	0.75V_{DD}		V_{DD}	
					3.0~4.5	0.8V_{DD}		V_{DD}	
	$V_{IH}(3)$ (Schmitt)	P22,P23 P30~P33 OSC1 and X1: External clock input	P22, P23, P30 to P33: Output disabled		4.5~6.0	0.75V_{DD}		V_{DD}	
					3.0~4.5	0.8V_{DD}		V_{DD}	
	$V_{IH}(4)$ (Schmitt)	Output option: OD P50~P53 P61~P63	Nch output transistor OFF		4.5~6.0	0.75V_{DD}		+13.5	
					3.0~4.5	0.8V_{DD}		+13.5	
	$V_{IH}(5)$ (Schmitt)	Output option: PU P50~P53 P61~P63	Nch output transistor OFF		4.5~6.0	0.75V_{DD}		V_{DD}	
					3.0~4.5	0.8V_{DD}		V_{DD}	
	$V_{IH}(6)$ (Low threshold input voltage)	Output option: OD P00~P03	Nch output transistor OFF		3.0~6.0	1.9		+13.5	
	$V_{IH}(7)$ (Low threshold input voltage)	Output option: PU P00~P03	Nch output transistor OFF		3.0~6.0	1.9		V_{DD}	
	$V_{IH}(8)$	P21,P40 P60 with PU output specification	P21 and P40: Output disabled. P60: Nch output transistor OFF		4.5~6.0	0.7V_{DD}		V_{DD}	
					3.0~4.5	0.75V_{DD}		V_{DD}	
	$V_{IH}(9)$	P10 to P13 and P60 with OD output specification	Nch output transistor OFF		4.5~6.0	0.7V_{DD}		+13.5	
					3.0~4.5	0.75V_{DD}		+13.5	

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Parameter		Symbol	Related Pins	Conditions		Limits (Ta=−30to+70℃)			Units
					VDD(V)	min	typ	max	
Input Low voltage		VIL(1) (Schmitt)	RES P20/HOLD		4.5~6.0	Vss		0.25VDD	V
					3.0~4.5	Vss		0.2VDD	
					1.8~3.0	Vss		0.15VDD	
		VIL(2) (Schmitt)	P22, P23 P30~P33 P61~P63 P50 to P53: Output with OD specification. OSC1: External clock input	P22, P23, P30 to P33: Output disabled P50 to P53, P61 to P63: Nch output transistor OFF	4.5~6.0	Vss		0.25VDD	V
					3.0~4.5	Vss		0.2VDD	
		VIL(3) (Low threshold input voltage)	P00~P03	Nch output transistor OFF	4.5~6.0	Vss		0.5	V
					3.0~4.5	Vss		0.35	
		VIL(4)	P10 to P13, P40, P60, and P21: output with OD specification. TEST X1: External clock input	P10 to P13, P60: Nch output transistor OFF P21 and P40: Output disabled	4.5~6.0	Vss		0.3VDD	V
					3.0~4.5	Vss		0.25VDD	
Instruction cycle time		Tcyc		The instruction cycle times vary depending on the operating power supply range. References to VDD(1) to VDD(3) are also required.		0.92		67	μsec
External main clock input mode	Frequency	fmosc(1)	OSC1	See Figure 1.	3.0~6.0	2.0		4.33	MHz
	Pulse width	fmextH fmextL		Same as above.	4.5~6.0	70			nsec
					3.0~6.0	140			
	Rise time and fall time	tmextR tmextF		Same as above.	4.5~6.0			30	nsec
					3.0~6.0			60	
External sub clock input mode	Frequency	tsosc	X1	See Figure 1.	3.0~6.0	30		50	kHz
	Pulse width	tsextH tsextL		Same as above.	3.0~6.0	6		34	μsec
	Rise time and fall time	tsextR tsextF		Same as above.	3.0~6.0			0.2	μsec
Self main clock oscillation Crystal oscillation	Oscillation frequency	fmxtal	OSC1, OSC2	See Figure 2.	4.19MHz	3.0~6.0		4.194304	MHz
	Oscillation stable period	tmsxtat		See Figure 5.				20	msec
Self main clock oscillation Ceramic resonator oscillation	Oscillation frequency	fmCF		See Figure 3.	4 MHz	3.0~6.0		4.0	MHz
	Oscillation stable period	tmsCF		See Figure 5.	4 MHz	3.0~6.0		20	msec
Self sub clock oscillation Crystal oscillation	Oscillation frequency	fsxtal	X1, X2	See Figure 4.	32kHz	3.0~6.0		32.768	kHz
	Oscillation stable period	fssxtal		See Figure 5.				10	sec

3. Electrical Characteristics
3-1. DC Characteristics/Ta=−30 to+70℃, Vss=0 V

Parameter	Symbol	Related Pins	Conditions		Limits				Units
					VDD(V)	min	typ	max	
Input High current	IIH(1)	Output option: OD specification P00~P03, P10~P13, P50~P53, P60~P63	VIN= +13.5V	Nch output transistor OFF (including output-OFF leakage current). P00 to P03: Without input pull-down resistor.	3.0~6.0			+5.0	μA
	IIH(2)	$\overline{RES}$, P20/$\overline{HOLD}$ OSC1: External clock input	VIN=VDD		3.0~6.0			+1.0	μA
	IIH(3)	P21~P23, P30~P33, P40	VIN=VDD	Output disabled (including output-OFF leakage current). P21 or ACZ: Self bias OFF.	3.0~6.0			+1.0	μA
	IIH(4)	P00 to P03: PD output specification	VIN=VDD	Nch output transistor OFF	3.0~6.0	+2.5		+200	μA
					4.5~6.0	+13		+200	
Input Low current	IIL(1)	Output option: OD specification P00~P03, P10~P13, P50~P53, P60~P63, P20/$\overline{HOLD}$, $\overline{RES}$ OSC1: External clock input	VIN=VSS	Nch output transistor OFF (including output-OFF leakage current)	3.0~6.0	−1.0			μA
	IIL(2)	P21~P23, P30~P33, P40	VIN=VSS	Output disabled (including output-OFF leakage current). P21 or ACZ: Self bias OFF.	3.0~6.0	−1.0			μA
	IIL(3) (Pull-up MOS output current)	P00~P03, P21~P23, P60~P63	VIN=VSS	H output. Output enabled (including output-OFF leakage current). P22 or ACZ: Self bias OFF.	6.0	−1.6			mA
Output High voltage	VOH(1) (Pull-up MOS output voltage)	P21~P23 Output option: PU specification P00~P03, P60~P63	IOH= −200μA	P21 to P23: Output disabled. P22 or ACZ: Self bias OFF.	4.5	2.4			V
			IOH= −10μA		4.5	4.0			
	VOH(2) (CMOS output voltage)	P30~P33, P40 Output option: PU specification P10~P13, P50~P53	IOH= −1 mA	P30 to P33 and P40: Output disabled. The other ports mean the ports to which VOH(1) and VOH(2) apply. However, the IOH total should not exceed the absolute maximum rating.	4.5~6.0	VDD −1.0			V
			IOH= −0.1mA (IOH of each pin of other ports must be less than -1mA.)		3.0~6.0	VDD −0.5			

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Parameter	Symbol	Related Pins	Conditions		VDD(V)	Limits min	typ	max	Units
Output High voltage	VOH(3)	S4~S15	IOH= −5 mA	The other ports mean the ports to which VOH(3) and VOH (4) apply. However, the IOH total should not exceed the absolute maximum rating.	4.5~6.0	VDD −1.8			V
			IOH= −1 mA (IOH of each pin of other ports must be less than -1mA.)		3.0~6.0	VDD −1.0			
	VOH(4)	T0~T7 T8/S23~T15/S16	IOH= −20mA	The other ports mean the ports to which VOH (3) and VOH (4) apply. However, the IOH total should not exceed the absolute maximum rating.	4.5~6.0	VDD −2.1			V
			IOH= −1 mA (IOH of each pin of other ports must be less than -1mA.)		3.0~6.0	VDD −1.0			
Output Low voltage	VOL(1)	P00~P03 P21~P23 P40 P60~P63	IOL=10mA	P21/ACZ: Self bias OFF. P21 to P23, and P40: Output enable mode	4.5~6.0			2.0	V
			IOL= 5 mA		3.0~6.0			2.0	
	VOL(2)	P30~P33 P50~P53	IOL=15mA	Output enable mode. The other ports mean the ports to which VOH(1), VOH(2), VOH(3) and VOH(4) apply. However, the IOL total should not exceed the absolute maximum rating.	4.5~6.0			2.0	V
			IOL=1.6mA		4.5~6.0			0.4	
			IOL=0.5mA (IOL of each pin of other ports must be less than 1mA.)		3.0~6.0			0.5	
	VOL(3)	P10~P13	IOL=30mA	The other ports mean the ports to which VOH(1), VOH(2), VOH(3) and VOH(4) apply. However, the IOL total should not exceed the absolute maximum rating.	4.5~6.0			2.0	V
			IOL= 2 mA (IOL of each pin of other ports must be less than 1mA.)		3.0~6.0			1.0	
	VOL(4)	Output option: PD specification S4~S15 T0~T7 T8/S23~T15/S16	VP=−35V See Figure 9.	Pch output transistor OFF.	4.5~6.0			−33	V
Output-OFF leakage current	IOFF(1)	Output option: OD specification S4~S15 T0~T7 T8/S23~T15/S16	VOUT=VDD	Pch output transistor OFF	3.0~6.0			+30	μA
			VOUT= VDD−40V		3.0~6.0	−30			
Output Low current (current which flows into a pull-down resistor)	IOL(1)	Output option: PD specification S4~S15 T0~T17 T8/S23~T15/S16	VOUT= +3.0V VP=−35V	Pch output transistor OFF	5.0	190	362	830	μA

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Parameter	Symbol	Related Pins	Conditions		Limits				Units
					VDD(V)	min	typ	max	
Hysteresis voltage	VHYS(1)	P20/$\overline{\text{HOLD}}$,P22,P23 P30~P33 P50 to P53 and P61 to P63: OD output specification. OSC1: External clock input $\overline{\text{RES}}$.	P20, P22 and P23, and P30 to P33: Output disabled. P50 to P53, and P60 to P63: Nch output transistor OFF		3.0~6.0		0.1VDD		V
Operating current dissipation	IDDOP(1)	VDD	Main crystal oscillation fosc = 4.19MHz. Sub crystal oscillation fosc = 32kHz. Tcyc = 0.95 µsec. Internal operation at a maximum mode.	Not including the amount of current dissipated by output drivers and pull-down resistors.	4.5~6.0		4	12	mA
	IDDOP(2)		Main crystal oscillation fosc = 4.19MHz. Sub crystal oscillation fosc = 32kHz. Tcyc = 30.4 µsec. Internal operation at a maximum mode.		3.0		0.35	1	mA
					6.0		1.4	3.6	
	IDDOP(3)		Main crystal oscillation fosc = Stop mode. Sub crystal oscillation = 32kHz. Tcyc = 61 µsec. Internal operation at a maximum mode.		3.0		0.04	0.15	mA
					6.0		0.25	0.8	
Current dissipation at HALT mode	IDDHALT (1)	VDD	Internal operation at a maximum mode. Main crystal oscillation fosc = 4.19MHz. Sub crystal oscillation fosc = 32kHz. HALT mode.	Not including the amount of current dissipated by output drivers and pull-down resistors.	4.5~6.0		1.5	4	mA
	IDDHALT (2)		Main crystal oscillation = Stop. Sub crystal oscillation fosc = 32kHz. Only internal time base timer being operated.		3.0		15	50	µA
					6.0		150	500	
Current dissipation at HOLD mode	IDDHOLD	VDD	HOLD mode	Not including the amount of current dissipated by output drivers and pull-down resistors. In addition, the input current to each pin and output-OFF leakage current are not included.	6.0		0.05	10	µA
					1.8		0.02	2	

3-2. AC Characteristics/Ta=−30to+70℃, Vss=0V

Parameter			Symbol	Related Pins	Conditions	Limits				Units
						VDD(V)	min	typ	max	
Serial clock	Cycle time	Input	tCKCY	SCK0, SCK1	See Figure 6. OD output specification requires a 1kΩ of pull-up resistance to be externally added.	4.5~6.0	0.8			μsec
		Output				3.0~6.0	3.2			
						3.0~6.0	2Tcyc			
	Low level pulse width, High level pulse width.	Input	tCKL tCKH		Same as above.	4.5~6.0	0.3			μsec
						3.0~6.0	1.2			
		Output				3.0~6.0	1Tcyc			
Serial input	Data setup time		tICK	SI0, SI1	Same as above.	4.5~6.0	0.15			μsec
						3.0~6.0	0.6			
	Data hold time		tCKI			4.5~6.0	0.15			
						3.0~6.0	0.6			
Serial output	Output delay time		tCKO	SO0, SO1	Same as above.	4.5~6.0			0.25	μsec
						3.0~6.0			1.0	
Pulse input conditions	High level/ Low level pulse width		tPIH(1) tPIL(1)	INT1 EINT0 EINT1 EINT2 HCNT RES PIN1	INT1 ·Conditions required by each interrupt source. EINT1 EINT2 · See Figure 7. HCNT · H counter operational conditions required by clock detect mode. RES · Reset conditions required by a reset operation.	3.0~6.0	2Tcyc			μsec
			tPIH(2) tPIL(2)	PIN1	See Figure 7. Timer 1 pulse counter operational conditions required by a remote control signal receive mode.	3.0~6.0	61			μsec
			tPIH(3) tPIL(3)	PIN1 HCNT	PIN1 ·Time base timer pulse count conditions required by an external clock input mode. HCNT ·H counter pulse count conditions required by an immediate input mode. See Figure 7.	3.0~6.0	0.5			μsec

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	Parameter	Symbol	Related Pins	Conditions		Limits				Units
						V_{DD}(V)	min	typ	max	
AC zero cross detect input characteristics	Input frequency	f_{ZIN}	ACZ/P21		See Figure 8. Self bias ON at open drain output.	4.5~6.0	40		1000	Hz
	Input voltage	V_{ZIN}		Coupling capacitor C=1 μF			1.0		2.4	Vp-p
	Detection error	V_{ZA}		60Hz Sine wave input					±100	mV
	Input current	I_{IHZ}		$V_{IN}=V_{DD}$				+20	+60	μA
		I_{ILZ}		$V_{IN}=V_{SS}$			−60	−20		
	H level input threshold voltage	Vt^*_{ACH}						Vt^*_{ACM} +0.2		V
	M level input threshold voltage	Vt^*_{ACM}					0.3V_{DD}		0.7V_{DD}	
	L level input threshold voltage	Vt^*_{ACL}						Vt^*_{ACM} −0.2		

3-3. A/D conversion characteristics /Ta=−30to+70℃, V_{SS}=0 V (A/D conversion is used in A/D mode.)

Parameter	Symbol	Related Pins	Conditions		Limits				Units
					V_{DD}(V)	min	typ	max	
Resolution					5.0~6.0		8		Bit
Absolute accuracy			AV+=V_{DD} AV−=V_{SS} AN1: ACZ self bias OFF					±16	LSB
Conversion time	T_{CAD}		AD conversion time: 51 Tcyc period			47 (Tcyc=0.92μs)		204 (Tcyc=4μs)	μsec
Reference input voltage	AV+	AV+				AV−		V_{DD}	V
	AV−	AV−				V_{SS}		AV+	
Reference input current	I_{AV} I_{REF}	AV+ AV−	AV+=V_{DD} AV−=V_{SS}			75	150	300	μA
Analog input voltage	V_{AIN}	AN1~AN8	• AN1/ACZ: Self bias OFF			AV−		AV+	V
Analog port input current	I_{AIN}	AN1~AN8	V_{AIN}=AV+	AN1: Self bias OFF. Including output-OFF leakage current. AV+=V_{DD} AV−=V_{SS}				1	μA
			V_{AIN}=AV−			−1			

3-4 Comparator characteristics /Ta=−30to+70℃, V_{SS}= 0 V (A/D conversion is used in comparator mode.)

Parameter	Symbol	Related Pins	Conditions	V_{DD}(V)	Limits min	typ	max	Units
Comparison accuracy	V_{CECON}	AN1~AN8	AV+=V_{DD} P21/ACZ: Self bias OFF. AV−=V_{SS} AN1: ACZ self bias OFF	5.0~6.0			±16	LSB
Threshold voltage	V_{THCON}	AN1~AN8			AV−		AV+	V
Input voltage	V_{INCON}				AV−		AV+	V
Reference input voltage	AV+	AV+			AV−		V_{DD}	V
	AV−	AV−			V_{SS}		AV+	
Conversion time	Tcc		Comparator conversion time: 23 Tcyc period		21 (Tcyc= 0.92μs)		92 (Tcyc= 4μs)	μs

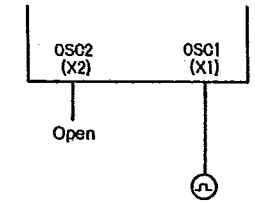
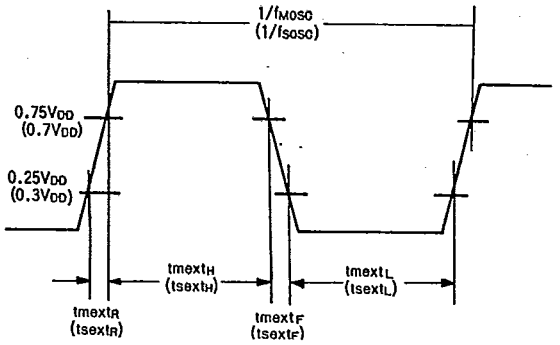
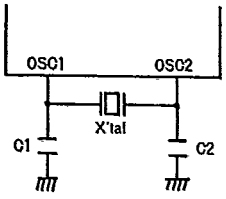


Figure 1 External clock input conditions



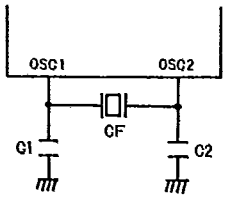
The values in parentheses are the parameters for sub clock oscillation mode.



Frequency	Maker name	X'tal oscillation	C 1	C 2
4.194304kHz	Tokyo Denpa	HC-49/U C_L=18pF	22pF	22pF
	Kinseki	HC-49/U C_L=16pF	15pF	15pF

C1 and C2 error: Less than 10% (including wire capacitance).
C_L = Load capacitance

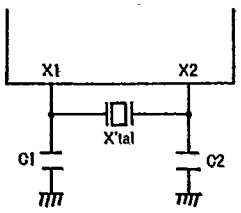
Figure 2 Main clock X'tal oscillation conditions



Frequency	Maker name	Ceramic resonator	C 1	C 2
4 MHz	Murata	CSA4.00MG	33pF	33pF
		CST4.00MGW *1	Not required	Not required
	Kyocera	KBR4.0MS	33pF	33pF
		KBR4.0MES *1	Not required	Not required

C1 and C2 error: Less than 10% (including wire capacitance).
*1 : 3-terminal ceramic resonator (with internal C)

Figure 3 Main clock ceramic resonator (CF) oscillation conditions



Frequency	Maker name	X'tal oscillation	C 1	C 2
32.768kHz	Kyocera	KF-38G-13200 C_L=13pF	22pF	22pF
	Daiwa Shinku	DT-38 C_L=12.5pF	15pF	15pF

C1 and C2 error: Less than 10% (including wire capacitance).
C_L = Load capacitance.

Figure 4 Sub clock crystal oscillation conditions

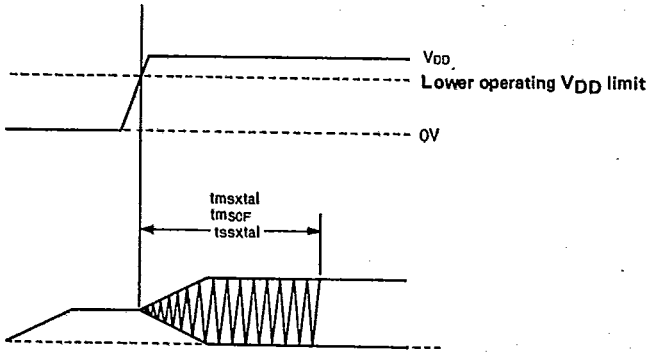


Figure 5 Oscillation stabilization time

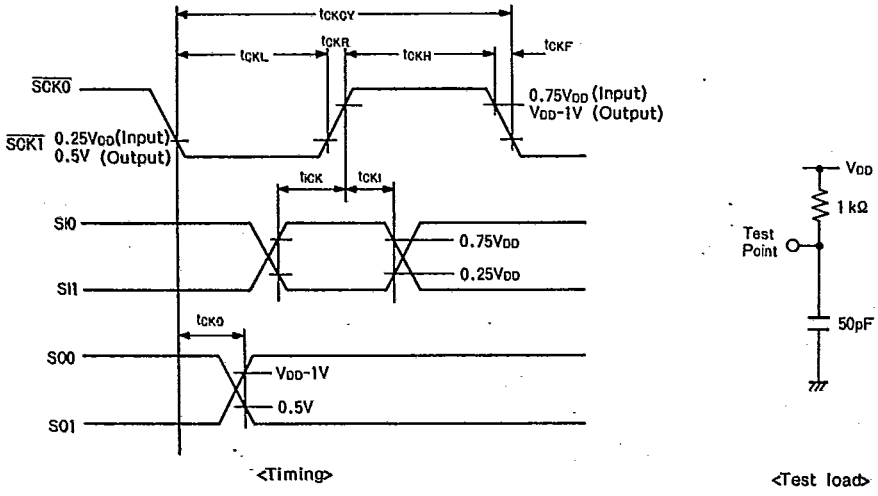


Figure 6 Serial input/output test conditions

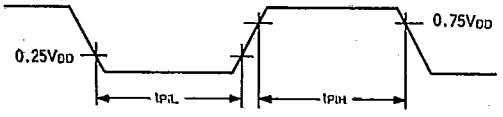
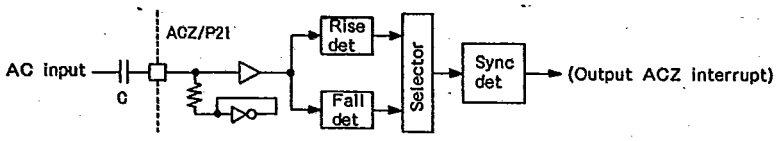
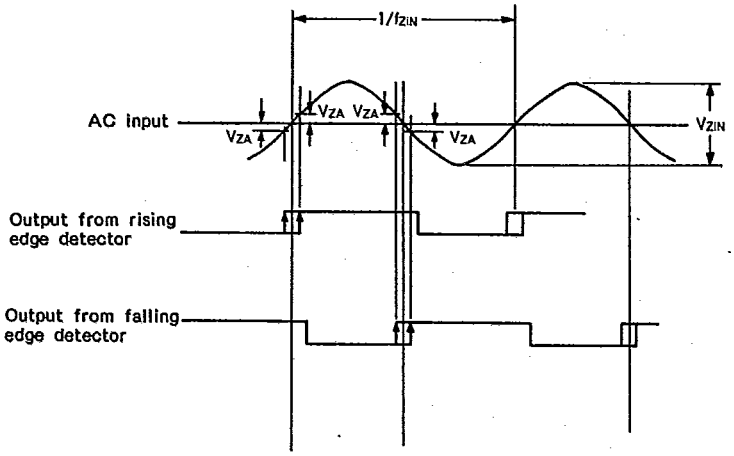


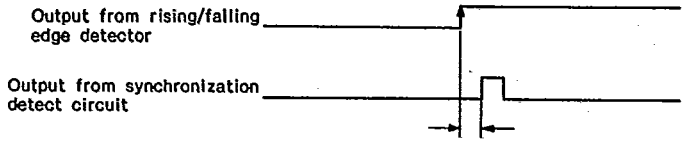
Figure 7 Pulse input timing conditions



<AC zero cross detection>



<Timing>



Synchronization delay = 0 to 1 Tcyc period

Figure 8 AC zero cross detection

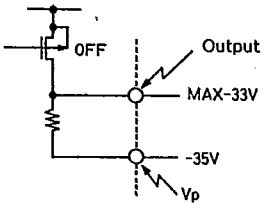


Figure 9 Leakage current at high withstand voltage output

Insturuction Set

Instruction group	Mnemonic		Op code		Bytes	Cycles	Operations	Operations description	Affected flag(s)	Remarks
			$D_7D_6D_5D_4$	$D_3D_2D_1D_0$						
Accumulator Manipulation Instructions	CLA	Clear AC	1 0 0 0	0 0 0 0	1	1	AC←0 (same as LAI 0)	Clear the AC.	ZF	Note 1
	DAA	Decimal adjust AC in addition	1 1 0 0 0 0 1 0	1 1 1 1 0 1 1 0	2	2	AC←(AC)+6 (same as ADI 6)	Add 6 to the AC.	ZF	
	DAS	Decimal adjust AC in subtraction	1 1 0 0 0 0 1 0	1 1 1 1 1 0 1 0	2	2	AC←(AC)+10 (same as ADI 0AH)	Add 10 to the AC.	ZF	
	CLC	Clear CF	0 0 0 1	1 1 1 0	1	1	CF←0	Clear the CF (Carry Flag).	CF	
	STC	Set CF	0 0 0 1	1 1 1 1	1	1	CF←1	Set the CF.	CF	
	CMA	Complement AC	0 0 0 1	1 0 0 0	1	1	AC←$\overline{(AC)}$	Complement the AC.	ZF	
	IA	Increment AC	0 0 0 1	0 1 0 0	1	1	AC←(AC)+1	Increment the AC by 1.	ZF, CF	
	DA	Decrement AC	0 0 1 0	0 1 0 0	1	1	AC←(AC)−1	Decrement the AC by 1.	ZF, CF	
	RAR	Rotate AC right through CF	0 0 0 1	0 0 0 0	1	1	AC_3←(CF), ACn←(ACn+1), CF←(AC_0)	Rotate the AC right through the CF.	CF	
	RAL	Rotate AC left through CF	0 0 0 0	0 0 0 1	1	1	AC_0←(CF), ACn+1←(ACn), CF←(AC_3)	Rotate the AC left through the CF.	CF, ZF	
	TAE	Transfer AC to E	0 1 0 0	0 1 0 1	1	1	E←(AC)	Transfer the AC content to the E register.		
	TEA	Transfer E to AC	0 1 0 0	0 1 1 0	1	1	AC←(E)	Transfer the E register content to the AC.	ZF	
	XAE	Exchange AC with E	0 1 0 0	0 1 0 0	1	1	(AC)↔(E)	Exchange the AC content with the E register content.		
Memory Manipulation Instructions	IM	Increment M	0 0 0 1	0 0 1 0	1	1	M(MBR,HL)←(M(MBR,HL))+1	Increment the content of M(MBR, HL) by 1.	ZF, CF	
	DM	Decrement M	0 0 1 0	0 0 1 0	1	1	M(MBR,HL)←(M(MBR,HL))−1	Decrement the content of M(MBR,HL) by 1.	ZF, CF	
	IMDR i8	Increment M direct	1 1 0 0 I_7 I_6 I_5 I_4	0 1 1 1 I_3 I_2 I_1 I_0	2	2	M(MBR,i8)←(M(MBR,i8))+1	Increment the content of M(MBR,i8) by 1. i8 is 8-bit immediate data.	ZF, CF	
	DMDR i8	Decrement M direct	1 1 0 0 I_7 I_6 I_5 I_4	0 0 1 1 I_3 I_2 I_1 I_0	2	2	M(MBR,i8)←(M(MBR,i8))−1	Decrement the content of M(MBR,i8) by 1. i8 is 8-bit immediate data.	ZF, CF	
	SMB i2	Set M data bit	0 0 0 0	1 1 i_1 i_0	1	1	(M(MBR,HL),i2)←1	Set a specified bit of the content of M(MBR, HL). Note that the two LSBs are used to specify the bit.		
	RMB i2	Reset M data bit	0 0 1 0	1 1 i_1 i_0	1	1	(M(MBR,HL),i2)←0	Reset a specified bit of the content of M(MBR, HL). Note that the two LSBs are used to specify the bit.	ZF	
Operations and Comparison Instructions	AD	Add M to AC	0 0 0 0	0 1 1 0	1	1	AC←(AC)+(M(MBR,HL))	Add the AC content and that of the M(MBR, HL) together in binary and then store the resulted sum into the AC.	ZF, CF	
	ADDR i8	Add M direct to AC	1 1 0 0 I_7 I_6 I_5 I_4	1 0 0 1 I_3 I_2 I_1 I_0	2	2	AC←(AC)+(M(MBR,i8))	Add the AC content and that of the M(MBR, i8) together in binary and then store the resulted sum into the AC. i8 is 8-bit immediate data.	ZF, CF	
	ADC	Add M to AC with CF	0 0 0 0	0 0 1 0	1	1	AC←(AC)+(M(MBR,HL))+(CF)	Add the AC content and those of the M(MBR, HL) and the carry flag (CF) together in binary and then store the resulted sum into the AC.	ZF, CF	
	ADI i4	Add immediate data to AC	1 1 0 0 0 0 1 0	1 1 1 1 I_3 I_2 I_1 I_0	2	2	AC←(AC)+I_3,I_2,I_1,I_0	Add the AC content and immediate data in binary and then store the resulted sum into the AC.	ZF	
	SUBC	Subtract AC from M with CF	0 0 0 1	0 1 1 1	1	1	AC←(M(MBR,HL))−(AC)−$\overline{(CF)}$	Subtract the AC content plus the inverted CF content from the M(MBR, HL) content in binary and then store resulted difference into the AC.	ZF, CF	If there has been a borrow, the carry flag (CF) is set to '0'. Otherwise, the flag is set to '1'.
	ANDA	And M with AC then store AC	0 0 0 0	0 1 1 1	1	1	AC←(AC)∧(M(MBR,HL))	Logically AND the M(MBR,HL) content with the AC content and then store the resulted logical product into the AC.	ZF	
	ORA	Or M with AC then store AC	0 0 0 0	0 1 0 1	1	1	AC←(AC)∨(M(MBR,HL))	Logically OR the M(MBR,HL) content with the AC content and then store the resulted logical sum into the AC.	ZF	
	EXL	Exclusive or M with AC then store AC	0 0 0 1	0 1 0 1	1	1	AC←(AC)∀(M(MBR,HL))	Logically X-AND the M(MBR,HL) content with the AC content and then store the resulted logical product into the AC.	ZF	
	ANDM	And M with AC then store M	0 0 0 0	0 0 1 1	1	1	M(MBR,HL)←(AC)∧(M(MBR,HL))	Logically AND the M(MBR,HL) content with the AC content and then store the resulted logical product into the M(MBR,HL).	ZF	
	ORM	Or M with AC then store M	0 0 0 0	0 1 0 0	1	1	M(MBR,HL)←(AC)∨(M(MBR,HL))	Logically OR the M(MBR,HL) content with the AC content and then store the resulted logical sum into the M(MBR,HL).	ZF	

Note 1: If multiple CLA instructions are used in a row, only the execution of the instructions following the first CLA can be skipped.

Instruction group	Mnemonic		Op code $D_7D_6D_5D_4$	Op code $D_3D_2D_1D_0$	Bytes	Cycles	Operations	Operations description	Affected flag(s)	Remarks
Operations and Comparison Instructions	CM	Compare AC with M	0 0 0 1	0 1 1 0	1	1	$\overline{(M(MBR,HL))}+(AC)+1$	Compare the AC content with that of M(MBR,HL) and set or reset the carry flag (CF) and the zero flag (ZF). Compare operations: $(M(MBR,HL))>(AC)$ CF=0 ZF=0; $(M(MBR,HL))=(AC)$ CF=1 ZF=1; $(M(MBR,HL))<(AC)$ CF=1 ZF=0	ZF, CF	
	CI i4	Compare AC with immediate data	1 1 0 0 1 0 1 0	1 1 1 1 $I_3 I_2 I_1 I_0$	2	2	$\overline{I_3 I_2 I_1 I_0}+(AC)+1$	Compare the AC content with immediate data $I_3I_2I_1I_0$ and set or reset the carry flag (CF) and the zero flag (ZF). Compare operations: $I_3I_2I_1I_0>(AC)$ CF=0 ZF=0; $I_3I_2I_1I_0=(AC)$ CF=1 ZF=1; $I_3I_2I_1I_0<(AC)$ CF=1 ZF=0	ZF, CF	
	CLI i4	Compare DP_L with immediate data	1 1 0 0 1 0 1 1	1 1 1 1 $I_3 I_2 I_1 I_0$	2	2	ZF←1 if $(DP_L)=I_3I_2I_1I_0$ ZF←0 if $(DP_L)\neq I_3I_2I_1I_0$	Compare the DP_L content with immediate data $I_3I_2I_1I_0$. If they are equal to each other, the zero flag (ZF) will be set. Otherwise, the flag will be reset.	ZF	
	CMB t2	Compare AC bit with M data bit	1 1 0 0 1 1 0 1	1 1 1 1 0 0 t_1 t_0	2	2	ZF←1 if $(AC,t2)=(M(MBR,HL),t2)$ ZF←0 if $(AC,t2)\neq(M(MBR,HL),t2)$	Compare the AC content with the content of a bit of M(MBR,HL), specified by the two LSBs (t_1t_0). If they are equal to each other, the zero flag (ZF) will be set. Otherwise, it will be reset.	ZF	
Load and Store Instructions	LAE	Load AC and E from M2 (MBR,HL)	0 1 0 1	1 1 0 0	1	1	AC←M(MBR,HL) E←M(MBR,HL+1)	Load the content of M(MBR,HL) into the AC and the E register.		
	LAI i4	Load AC with immediate data	1 0 0 0	$I_3 I_2 I_1 I_0$	1	1	AC←$I_3I_2I_1I_0$	Load immediate data into the AC.	ZF	Note 1
	LADR i8	Load AC from M direct	1 1 0 0 $I_7 I_6 I_5 I_4$	0 0 0 1 $I_3 I_2 I_1 I_0$	2	2	AC←(M(MBR,i8))	Load the content of M(MBR,i8) into the AC. Note that i8 means 8-bit immediate data.	ZF	
	S	Store AC to M	0 1 0 0	0 1 1 1	1	1	M(MBR,HL)←(AC)	Store the AC content into M(MBR,HL).		
	SAE	Store AC and E to M2 (MBR,HL)	0 1 0 1	1 1 1 0	1	1	M(MBR,HL)←(AC) M(MBR,HL+1)←(E)	Store the content of M2(MBR,HL) into the AC and the E register.		
	LA reg	Load AC from M (MBR,reg)	0 1 0 0	1 0 t_0 0	1	1	AC←(M(MBR,reg))	Load the content of M(MBR,reg) into the AC. Note that 'reg' indicates the HL or XY. reg: HL → t0 = 0; XY → t0 = 1	ZF	
	LA reg,I	Load AC from M (MBR,reg) then increment reg	0 1 0 0	1 0 t_0 1	1	2	AC←(M(MBR,reg)) DP_L←$(DP_L)+1$ Or if DP_Y←$(DP_Y)+1$	Load the content of M(MBR,reg) into the AC. Note that 'reg' indicates the HL or XY. After loading, the content of DP_L or DPy will be incremented by 1. The relationship between reg and t0 is the same as that shown in the LA reg instruction.	ZF	The zero flag (ZF) will be set or reset accordingly after the content of the DP_L or the DPy is incremented by 1.
	LA reg, D	Load AC from M (MBR,reg) then decrement reg	0 1 0 1	1 0 t_0 1	1	2	AC←(M(MBR,reg)) DP_L←$(DP_L)-1$ Or DP_Y←$(DP_Y)-1$	Load the content of M(MBR,reg) into the AC. Note that 'reg' indicates the HL or XY. After loading, the content of DP_L or DPy will be decremented by 1. The relationship between reg and t0 is the same as that shown in the LA reg instruction.	ZF	The zero flag (ZF) will be set or reset accordingly after the content of the DP_L or the DPy is decremented by 1.
	XA reg	Exchange AC with M(MBR,reg)	0 1 0 0	1 1 t_0 0	1	1	(AC)↔(M(MBR,reg))	Exchange the AC content with that of M(MBR,reg). Note that 'reg' indicates the HL or XY. reg: HL → t0 = 0; XY → t0 = 1		
	XA reg,I	Exchange AC with M (MBR,reg) then increment reg	0 1 0 0	1 1 t_0 1	1	2	(AC)↔(M(MBR,reg)) DP_L←$(DP_L)+1$ Or if DP_Y←$(DP_Y)+1$	Exchange the AC content with that of M(MBR,reg). Note that 'reg' indicates the HL or XY. After exchange, the content of the DP_L or the DPy will be incremented by 1. The relationship between reg and t0 is the same as that shown in the LA reg instruction.	ZF	The zero flag (ZF) will be set or reset accordingly after the content of the DP_L or the DPy is incremented by 1.
	XA reg, D	Exchange AC with M (MBR,reg) then decrement reg	0 1 0 1	1 1 t_0 1	1	2	(AC)↔(M(MBR,reg)) DP_L←$(DP_L)-1$ Or DP_Y←$(DP_Y)-1$	Exchange the AC content with that of M(MBR,reg). Note that 'reg' indicates the HL or XY. After exchange, the content of the DP_L or the DPy will be decremented by 1. The relationship between reg and t0 is the same as that shown in the LA reg instruction.	ZF	The zero flag (ZF) will be set or reset accordingly after the content of the DP_L or the DPy is decremented by 1.
	XADR i8	Exchange AC with M direct	1 1 0 0 $I_7 I_6 I_5 I_4$	1 0 0 0 $I_3 I_2 I_1 I_0$	2	2	(AC)↔(M(MBR,i8))	Exchange the AC content with the that of M(MBR,i8). Note that i8 means 8-bit immediate data.		

Note 1: If multiple LAI i4 instructions are used in a row, the execution of the instructions following the first LAI instruction can be skipped.

Instruction group	Mnemonic		Op code $D_7D_6D_5D_4$	Op code $D_3D_2D_1D_0$	Bytes	Cycles	Operations	Operations description	Affected flag(s)	Remarks
Load and Store Instructions	LEAI i8	Load E & AC with immediate data	1 1 0 0 I_7 I_6 I_5 I_4	0 1 1 0 I_3 I_2 I_1 I_0	2	2	E ← I_7 I_6 I_5 I_4 AC ← I_3 I_2 I_1 I_0	Load immediate data I8 into the AC and the E register.		
	RTBL	Read table data from program ROM	0 1 0 1	1 0 1 0	1	2	E, AC ← (ROM(PCh, E, AC))	Replace the lower PC 8 bits with the E and AC contents. Then load the content of a ROM address specified by the PC content into the AC and the E register.		
Data Pointer Manipulation Instructions	LDZ i4	Load DP_H with zero and DP_L with immediate data respectively	0 1 1 0	I_3 I_2 I_1 I_0	1	1	DP_H ← 0 DP_L ← I_3 I_2 I_1 I_0	Load '0' into the DP_H and immediate data I4 into the DP_L.		
	LHI i4	Load DP_H with immediate data	1 1 0 0 0 0 0 0	1 1 1 1 I_3 I_2 I_1 I_0	2	2	DP_H ← I_3 I_2 I_1 I_0	Load immediate data I4 into the DP_H.		
	LLI i4	Load DP_L with immediate data	1 1 0 0 0 0 0 1	1 1 1 1 I_3 I_2 I_1 I_0	2	2	DP_L ← I_3 I_2 I_1 I_0	Load immediate data I4 into the DP_L.		
	LHLI i8	Load DP_H, DP_L with immediate data	1 1 0 0 I_7 I_6 I_5 I_4	0 0 0 0 I_3 I_2 I_1 I_0	2	2	DP_H ← I_7 I_6 I_5 I_4 DP_L ← I_3 I_2 I_1 I_0	Load immediate data into the DP_H and the DP_L.		
	LXYI i8	Load DP_X, DP_Y with immediate data	1 1 0 0 I_7 I_6 I_5 I_4	0 0 1 0 I_3 I_2 I_1 I_0	2	2	DP_X ← I_7 I_6 I_5 I_4 DP_Y ← I_3 I_2 I_1 I_0	Load immediate data into the DPX and the DPY.		
	IL	Increment DP_L	0 0 0 1	0 0 0 1	1	1	DP_L ← (DP_L) + 1	Increment the DP_L by 1.	ZF	
	DL	Decrement DP_L	0 0 1 0	0 0 0 1	1	1	DP_L ← (DP_L) − 1	Decrement the DP_L by 1.	ZF	
	IY	Increment DP_Y	0 0 0 1	0 0 1 1	1	1	DP_Y ← (DP_Y) + 1	Increment the DPY by 1.	ZF	
	DY	Decrement DP_Y	0 0 1 0	0 0 1 1	1	1	DP_Y ← (DP_Y) − 1	Decrement the DPY by 1.	ZF	
	TAH	Transfer AC to DP_H	1 1 0 0 1 1 1 1	1 1 1 1 0 0 0 0	2	2	DP_H ← (AC)	Transfer the AC content into the DP_H.		
	THA	Transfer DP_H to AC	1 1 0 0 1 1 1 0	1 1 1 1 0 0 0 0	2	2	AC ← (DP_H)	Transfer the DP_H content into the AC.	ZF	
	XAH	Exchange AC with DP_H	0 1 0 0	0 0 0 0	1	1	(AC) ↔ (DP_H)	Exchange AC content with that of the DP_H.		
	TAL	Transfer AC to DP_L	1 1 0 0 1 1 1 1	1 1 1 1 0 0 0 1	2	2	DP_L ← (AC)	Transfer the AC content into the DP_L.		
	TLA	Transfer DP_L to AC	1 1 0 0 1 1 1 0	1 1 1 1 0 0 0 1	2	2	AC ← (DP_L)	Transfer the DP_L content into the AC.	ZF	
	XAL	Exchange AC with DP_L	0 1 0 0	0 0 0 1	1	1	(AC) ↔ (DP_L)	Exchange the AC content with that of the DP_L.		
	TAX	Transfer AC to DP_X	1 1 0 0 1 1 1 1	1 1 1 1 0 0 1 0	2	2	DP_X ← (AC)	Transfer the AC content into the DP_X.		
	TXA	Transfer DP_X to AC	1 1 0 0 1 1 1 0	1 1 1 1 0 0 1 0	2	2	AC ← (DP_X)	Transfer the DP_X content into the AC.	ZF	
	XAX	Exchange AC with DP_X	0 1 0 0	0 0 1 0	1	1	(AC) ↔ (DP_X)	Exchange the AC content with that of the DP_X.		
	TAY	Transfer AC to DP_Y	1 1 0 0 1 1 1 1	1 1 1 1 0 0 1 1	2	2	DP_Y ← (AC)	Transfer the AC content into the DP_Y.		
	TYA	Transfer DP_Y to AC	1 1 0 0 1 1 1 0	1 1 1 1 0 0 1 1	2	2	AC ← (DP_Y)	Transfer the DP_Y content into the AC.	ZF	
	XAY	Exchange AC with DP_Y	0 1 0 0	0 0 1 1	1	1	(AC) ↔ (DP_Y)	Exchange the AC content with that of the DP_Y.		
Flag Manipulation Instructions	SFB n4	Set flag bit	0 1 1 1	$n_3n_2n_1n_0$	1	1	Fn ← 1	Set the flag specified by immediate data n4.		
	RFB n4	Reset flag bit	0 0 1 1	$n_3n_2n_1n_0$	1	1	Fn ← 0	Reset the flag specified by immediate data n4.	ZF	
Jump and Subroutine Instructions	JMP addr	Jump in the current bank	1 1 1 0 $P_7P_6P_5P_4$	$P_{11}P_{10}P_9P_8$ $P_3P_2P_1P_0$	2	2	PC13 ← PC13 PC11~0 ← P_{11}~P_0	Program jump to an address within the same bank area, specified by immediate data P_{11} to P_0.		If this instruction is executed immediately after the SB instruction, the upper two PC bits (P_{13} and P_{12}) are replaced by immediate data I1|0. See the SB instruction for more details.
	JPEA	Jump to the address stored at E and AC in the current page	0 0 1 0	0 1 1 1	1	1	PC13~PC8 ← PC13~PC8 PC7~4 ← (E) PC3~0 ← (AC)	Replace the lower 8 PC bits with the AC and the E register contents and jump to an address pointed to by the new program counter (PC) value.		

Instruction area	Mnemonic		Op code		Bytes	Cycles	Operations	Operations description	Affected flag(s)	Remarks
			$D_7D_6D_5D_4$	$D_3D_2D_1D_0$						
Jump and Subroutine Instructions	CAL addr	Call subroutine	1 0 1 0 $P_7P_6P_5P_4$	$P_{11}P_{10}P_9P_8$ $P_3P_2P_1P_0$	2	2	PC13, 12←0 PC11~0←P_{11}~P_0 M4(SP)←(CF, ZF, PC13~0) SP←(SP)-4	Call a subroutine.		
	PUSH reg	Push reg on M2(SP)	1 1 0 0 1 1 1 1	1 1 1 1 1 i_1 i_0 0	2	2	M2(SP)←(reg) SP←(SP)-2	Store the 'reg' content into the M2(SP) and then decrement the SP content by 2. reg: HL (i_1 i_0 = 0 0); XY (0 1); AE (1 0); BR (1 1)		
	POP reg	Pop reg off M2(SP)	1 1 0 0 1 1 1 0	1 1 1 1 1 i_1 i_0 0	2	2	SP←(SP)+2 reg←(M2(SP))	Increment the SP content by 2 and then load the content of M2(SP) into the 'reg'. The relationship between the i_1i_0 and 'reg' is the same as that shown in PUSH reg instruction.		
	RT	Return from subroutine	0 0 0 1	1 1 0 0	1	2	SP←(SP)+4 PC←(M4(SP))	Return to a main routine from a subroutine or interrupt servicing routine. The zero flag (ZF) and the carry flag (CF) are not affected by this instruction.		
	RTI	Return from interrupt routine	0 0 0 1	1 1 0 1	1	2	SP←(SP)+4 PC←(M4(SP)) CF, ZF←(M4(SP))	Return to a main routine from a subroutine or interrupt servicing routine. The previous contents of the ZF and CF are restored.	ZF; CF	
Branch Instructions	BAt2 addr	Branch on AC bit	1 1 0 1 $P_7P_6P_5P_4$	0 0 t_1 t_0 $P_3P_2P_1P_0$	2	2	PC7~0←$P_7P_6P_5P_4$ $P_3P_2P_1P_0$ if(AC, t2) = 1	Check an AC bit specified by immediate data t_1t_0 to see if it has been set to '1'. If set to '1', program execution is passed to an address within the same page. Note the address is specified by the lower 8 PC bits (P_7 to P_0).		
	BNAt2 addr	Branch on no AC bit	1 0 0 1 $P_7P_6P_5P_4$	0 0 t_1 t_0 $P_3P_2P_1P_0$	2	2	PC7~0←$P_7P_6P_5P_4$ $P_3P_2P_1P_0$ if(AC, t2) = 0	Check an AC bit specified by immediate data t_1t_0 to see if it has been set to '0'. If set to '0', program execution is passed to an address within the same page. Note the address is specified by the lower 8 PC bits (P_7 to P_0).		
	BMt2 addr	Branch on M bit	1 1 0 1 $P_7P_6P_5P_4$	0 1 t_1 t_0 $P_3P_2P_1P_0$	2	2	PC7~0←$P_7P_6P_5P_4$ $P_3P_2P_1P_0$ if(M(MBR, HL), t2)=1	Check an M(MBR,HL) bit specified by immediate data t_1t_0 to see if it has been set to '1'. If set to '1', program execution is passed to an address within the same page. Note the address is specified by the lower 8 PC bits (P_7 to P_0).		
	BNMt2 addr	Branch on no M bit	1 0 0 1 $P_7P_6P_5P_4$	0 1 t_1 t_0 $P_3P_2P_1P_0$	2	2	PC7~0←$P_7P_6P_5P_4$ $P_3P_2P_1P_0$ if(M(MBR, HL), t2)=0	Check an M(MBR,HL) bit specified by immediate data t_1t_0 to see if it has been set to '0'. If set to '0', program execution is passed to an address within the same page. Note the address is specified by the lower 8 PC bits (P_7 to P_0).		
	BPt2 addr	Branch on Port bit	1 1 0 1 $P_7P_6P_5P_4$	1 0 t_1 t_0 $P_3P_2P_1P_0$	2	2	PC7~0←$P_7P_6P_5P_4$ $P_3P_2P_1P_0$ if(P(RBR, DP_L),t2)=1	Check a port or register P(RBR,DP_L) bit specified by immediate data t_1t_0 to see if it has been set to '1'. If set to '1', program execution is passed to an address within the same page. Note the address is specified by the lower 8 PC bits (P_7 to P_0).		
	BNPt2 addr	Branch on no Port bit	1 0 0 1 $P_7P_6P_5P_4$	1 0 t_1 t_0 $P_3P_2P_1P_0$	2	2	PC7~0←$P_7P_6P_5P_4$ $P_3P_2P_1P_0$ if(P(RBR, DP_L),t2)=0	Check a port or register P(RBR,DP_L) bit specified by immediate data t_1t_0 to see if it has been set to '0'. If set to '0', program execution is passed to an address within the same page. Note the address is specified by the lower 8 PC bits (P_7 to P_0).		
	BC addr	Branch on CF	1 1 0 1 $P_7P_6P_5P_4$	1 1 0 0 $P_3P_2P_1P_0$	2	2	PC7~0←$P_7P_6P_5P_4$ $P_3P_2P_1P_0$ if(CF)=1	Check the carry flag (CF) to see if it has been set to '1'. If set to '1', program execution is passed to an address within the same page. Note that the address is specified by the lower 8 PC bits (P_7 to P_0).		
	BNC addr	Branch on no CF	1 0 0 1 $P_7P_6P_5P_4$	1 1 0 0 $P_3P_2P_1P_0$	2	2	PC7~0←$P_7P_6P_5P_4$ $P_3P_2P_1P_0$ if(CF)=0	Check the carry flag (CF) to see if it has been set to '0'. If set to '0', program execution is passed to an address within the same page. Note that the address is specified by the lower 8 PC bits (P_7 to P_0).		
	BZ addr	Branch on ZF	1 1 0 1 $P_7P_6P_5P_4$	1 1 0 1 $P_3P_2P_1P_0$	2	2	PC7~0←$P_7P_6P_5P_4$ $P_3P_2P_1P_0$ if(ZF)=1	Check the zero flag (ZF) to see if it has been set to '1'. If set to '1', program execution is passed to an address within the same page. Note that the address is specified by the lower 8 PC bits (P_7 to P_0).		
	BNZ addr	Branch on no ZF	1 0 0 1 $P_7P_6P_5P_4$	1 1 0 1 $P_3P_2P_1P_0$	2	2	PC7~0←$P_7P_6P_5P_4$ $P_3P_2P_1P_0$ if(ZF)=0	Check the zero flag (ZF) to see if it has been set to '0'. If set to '0', program execution is passed to an address within the same page. Note that the address is specified by the lower 8 PC bits (P_7 to P_0).		

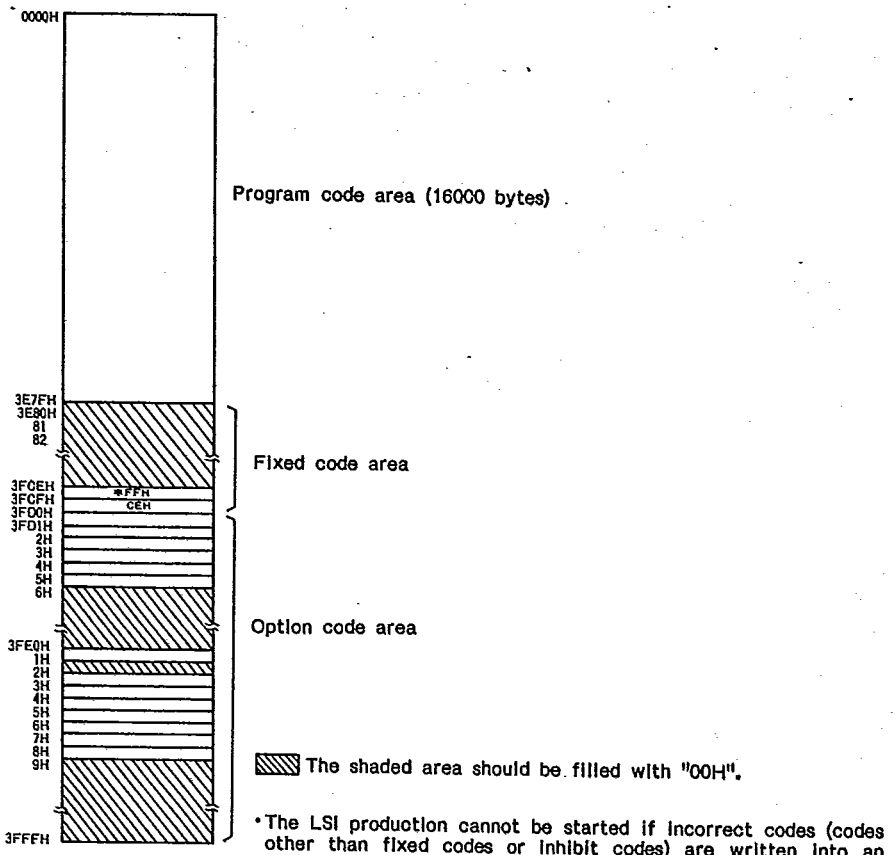
Instruction group	Mnemonic		Op code		Bytes	Cycles	Operations	Operations description	Affected flag(s)	Remarks
			$D_7D_6D_5D_4$	$D_3D_2D_1D_0$						
Branch instructions	BFn4 addr	Branch on flag bit	1 1 1 1 $P_7P_6P_5P_4$	$n_3n_2n_1n_0$ $P_3P_2P_1P_0$	2	2	PC7~0←$P_7P_6P_5P_4$ $P_3P_2P_1P_0$ if(Fn)=1	Check a flag specified by n3n2n1n0 to see if it has been set to '1'. If set to '1', program execution is passed to an address within the same page. Note that the total number of specifiable flags is 16 and that the address is specified by the lower 8 PC bits (P_7 to P_0).		
	BNFn4 addr	Branch on no flag bit	1 0 1 1 $P_7P_6P_5P_4$	$n_3n_2n_1n_0$ $P_3P_2P_1P_0$	2	2	PC7~0←$P_7P_6P_5P_4$ $P_3P_2P_1P_0$ if(Fn)=0	Check a flag specified by n3n2n1n0 to see if it has been set to '0'. If set to '0', program execution is passed to an address within the same page. Note that the total number of specifiable flags is 16 and that the address is specified by the lower 8 PC bits (P_7 to P_0).		
Input/output instructions	IP0	Input port 0 to AC	0 0 1 0	0 0 0 0	1	1	AC←(P(RBR,0))	Input the content of port or register P(RBR,0) to the AC.	ZF	
	IP	Input port to AC	0 0 1 0	0 1 1 0	1	1	AC←(P(RBR,DP_L))	Input the content of port or register P(RBR,DP_L) to the AC.	ZF	
	IPM	Input port to M	0 0 0 1	1 0 0 1	1	1	M(HL)←(P(RBR,DP_L))	Input the content of port or register P(RBR,DP_L) to M(MBR,HL).		
	IPDRP4	Input port to AC direct	1 1 0 0 0 1 1 0	1 1 1 1 $P_3P_2P_1P_0$	2	2	AC←(P(RBR,DP_L))	Input the content of P(RBR,P4) to the AC.	ZF	
	OP	Output AC to port	0 0 1 0	0 1 0 1	1	1	P(RBR,DP_L)←(AC)	Output the AC content to port or register P(RBR,DP_L).		
	OPM	Output M to port	0 0 0 1	1 0 1 0	1	1	P(RBR,DP_L)←(M(MBR,HL))	Output the content of M(MBR,HL) to port P(RBR,DP_L).		
	OPDRP4	Output AC to port direct	1 1 0 0 0 1 1 1	1 1 1 1 $P_3P_2P_1P_0$	2	2	P(RBR,P4)←(AC)	Output the AC content to P(RBR,P4).		
	SPB t2	Set port bit	0 0 0 0	1 0 t_1 t_0	1	1	(P(RBR,DP_L), t2)←1	Set a specified bit of port or register P(RBR,DP_L). Note that the bit is specified by immediate data t_1t_0.		
	RPB t2	Reset port bit	0 0 1 0	1 0 t_1 t_0	1	1	(P(RBR,DP_L), t2)←0	Reset a specified bit of port or register P(RBR,DP_L). Note that the bit is specified by immediate data t_1t_0.	ZF	
	ANDPDR i4, p4	And port with immediate data then output	1 1 0 0 I_3 I_2 I_1 I_0	0 1 0 1 $P_3P_2P_1P_0$	2	2	P(RBR,P_3~P_0)←(P(RBR,P_3~0))∧ I_3~0	Logically AND the content of P(RBR,P_3 to P_0) with immediate data $I_3I_2I_1I_0$ and then output the resulted logical product to P(RBR,P_3 to P_0).	ZF	
	ORPDR i4, p4	Or port with immediate data then output	1 1 0 0 I_3 I_2 I_1 I_0	0 1 0 0 $P_3P_2P_1P_0$	2	2	P(RBR,P_3~P_0)←(P(RBR,P_3~0))∨ I_3~0	Logically OR the content of P(RBR,P_3 to P_0) with immediate data $I_3I_2I_1I_0$ and then output the resulted logical product to P(RBR,P_3 to P_0).	ZF	
	IP8	Input 8bit date to E and AC	1 1 0 0 1 1 0 1	1 1 1 1 1 0 0 0	2	2	AC←(P(RBR,DP_L))	Input 8- bit data to the AC and E register from a port or register P(RBR,DP_L).		
	OP8	Output 8bit E and AC to Port	1 1 0 0 1 1 0 1	1 1 1 1 1 0 0 1	2	2	P(RBR,DP_L)←(AC), (E)	Output 8-bit data to a port or register P(RBR,DP_L) from the AC and the E register.		

Instruction group	Mnemonic		Op code		Bytes	Cycles	Operations	Operations description	Affected flag(s)	Remarks
			$D_7D_6D_5D_4$	$D_3D_2D_1D_0$						
Interrupt control instructions	MSET	Set Interrupt Master Enable Flag	1 1 0 0 0 1 0 1	1 1 0 1 0 0 0 0	2	2	MSE←1	Set the interrupt master enable flag.		
	MRESET	Reset Interrupt Master Enable Flag	1 1 0 0 1 0 0 1	1 1 0 1 0 0 0 0	2	2	MSE←0	Reset the interrupt master enable flag.	ZF	
	EIH i4	Enable interrupt high	1 1 0 0 0 1 0 1	1 1 0 1 I_3 I_2 I_1 I_0	2	2	EDIH←(EDIH)∨i4	Set the interrupt enable flag.		
	EIL i4	Enable interrupt low	1 1 0 0 0 1 0 0	1 1 0 1 I_3 I_2 I_1 I_0	2	2	EDIL←(EDIL)∨i4	Set the interrupt enable flag.		
	DIH i4	Disable interrupt high	1 1 0 0 1 0 0 1	1 1 0 1 I_3 I_2 I_1 I_0	2	2	EDIH←(EDIH)∧$\overline{i4}$	Reset the interrupt enable flag.	ZF	
	DIL i4	Disable interrupt low	1 1 0 0 1 0 0 0	1 1 0 1 I_3 I_2 I_1 I_0	2	2	EDIL←(EDIL)∧$\overline{i4}$	Reset the interrupt enable flag.	ZF	
	WTSP	Write SP	1 1 0 0 1 1 0 1	1 1 1 1 1 0 1 0	2	2	SP←(E), (AC)	Transfer the contents of the AC and the E register to the SP.		
	RSP	Read SP	1 1 0 0 1 1 0 1	1 1 1 1 1 0 1 1	2	2	E, AC←(SP)	Transfer the SP content to the AC and the E register.		
Standby control instructions	HALT	HALT	1 1 0 0 1 1 0 1 0 0 0 0	1 1 1 1 1 1 1 0 0 0 0 0	3	3	HALT	Start the HALT mode.		
	HOLD	HOLD	1 1 0 0 1 1 0 1 0 0 0 0	1 1 1 1 1 1 1 1 0 0 0 0	3	3	HOLD	Start the HOLD mode.		
Other instructions	NOP	No operation	0 0 0 0	0 0 0 0	1	1	No operation	Nothing will be done during 1 machine cycle.		
	SB i3	Select bank	0 1 0 1	D_1 I_2 I_1 I_0	1	1	PC13, PC12←I_1 I_0	SB + JMP: The two PC MSBs (P_{13} and P_{12}) are replaced with immediate data I_1I_0. SB + SRBA: Immediate data $I_2I_1I_0$ will be set in the RBR. SB + SMBA: Immediate data $I_2I_1I_0$ will be set in the MBR.		
	SRBA	Set Register Bank Address	1 1 0 0	1 0 1 1	1	1	RBR←I_2 I_1 I_0	SB + SRBA: Immediate data $I_2I_1I_0$ will be set in the RBR.		
	SMBA	Set Memory Bank Address	1 1 0 0	1 0 1 0	1	1	MBR←I_2 I_1 I_0	SB + SMBA: Immediate data $I_2I_1I_0$ will be set in the MBR.		

Option code specification for the LC67216A microcomputer

The EPROM which is to be sent to Sanyo should contain various mask option codes and program codes for the LC67216A microcomputer.
In order to write option codes into the EPROM, we provide the LC67216A cross assembler. This cross assembler would enable the user to enter the option codes in interactive operation mode.
In case where the cross assembler provided by Sanyo is not used for the above purpose, the required option codes should be entered in the following manner. If you enter the codes in the manner, the same option codes as those generated by the LC67216A cross assembler can be set in the EPROM.
When placing your order, please provide us with an option code list and the EPROM (27128) containing program codes and option codes.
For detailed information on the option codes, please refer to section 9."Specifying User Options" of the manual, 'EVA850/800-LC67216 Development Tool Manual'. However, the main clock oscillation circuit option for the RC (resistor- capacitor) oscillation is not provided for the LC67216A microcomputer. Please keep it in mind.

EPROM address map



•The LSI production cannot be started if incorrect codes (codes other than fixed codes or inhibit codes) are written into an EPROM. Please keep it in mind.

Notes on the evaluation of user programs for the LC67216A microcomputer

If the user programs for the LC67216A microcomputer are evaluated on the evaluation chip (LC67999 or LC67PG216), please read carefully section 5.3 "considerations in Program Evaluation" of the 'LC67216A User's Manual'. In addition, please keep in mind the following cautions.
Notes on program code area: The program code area of the production chip is 16000 bytes in size. That is, its address starts from address 0000H, ending at address 3E7FH. However, the accessible area of an evaluation chip is in the range between address 0000H and address 3FFFH. That is, it can be said that the program code area of the evaluation chip is 16383 bytes in size. As a result, the code area after address 3E80H should not be used for storing program codes. Please keep the following two points in mind.

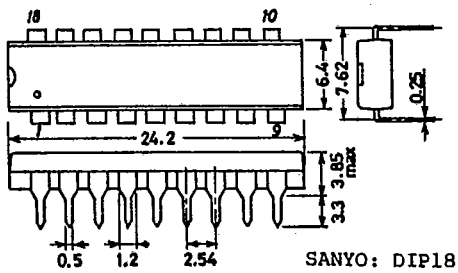
(1) No program codes in the area after address 3E80H.
(2) No program jump to the area after address 3E80H.

T-90-20

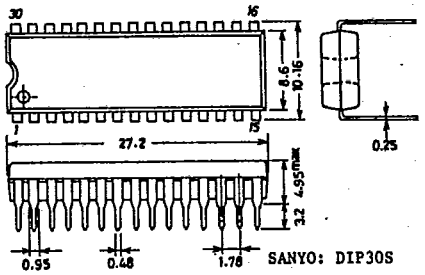
CASE OUTLINES OF 8/4-BIT MICROCOMPUTERS, GATE ARRAYS

- All of Sanyo microcomputer case outlines are illustrated below.
- All dimensions are in mm, and dimensions which are not followed by min. or max. are represented by typical values.
- No marking is indicated.

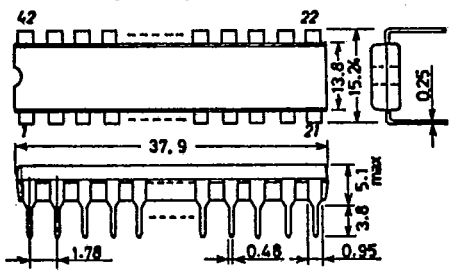
Case Outline—[3007A] unit: mm



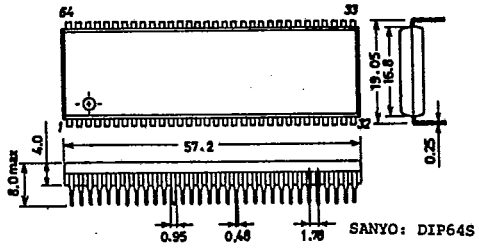
Case Outline—[3061] unit: mm



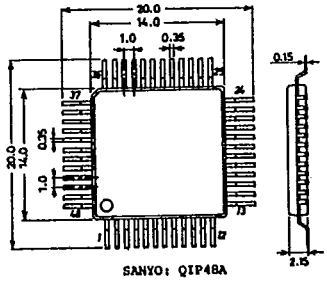
Case Outline—[3025B] unit: mm



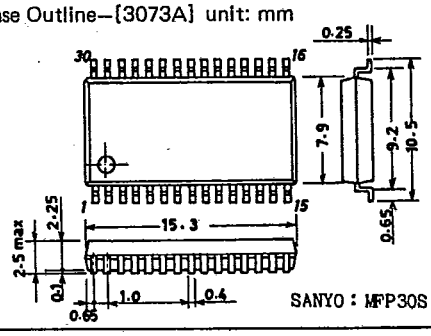
Case Outline—[3071] unit: mm



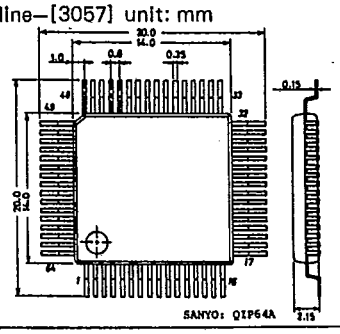
Case Outline—[3052A] unit: mm



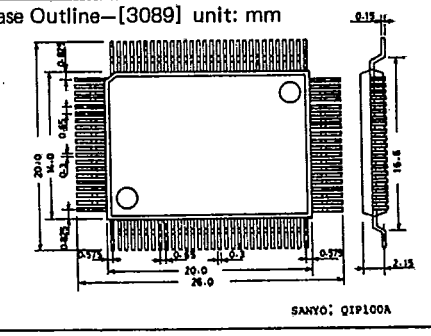
Case Outline—[3073A] unit: mm



Case Outline—[3057] unit: mm

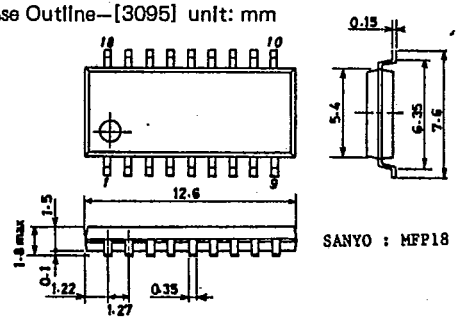


Case Outline—[3089] unit: mm



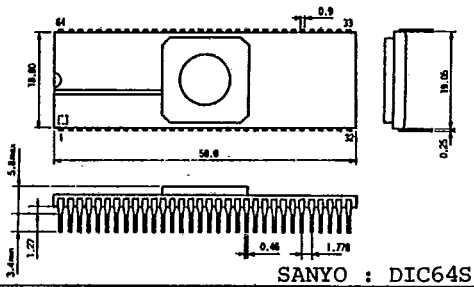
T-90-20

Case Outline—[3095] unit: mm



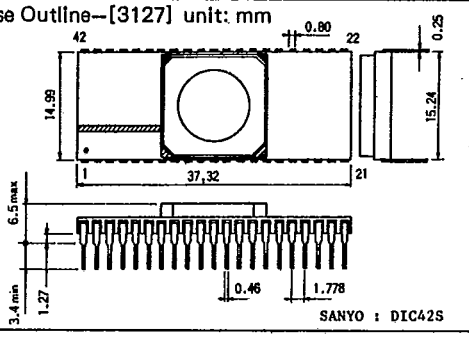
SANYO : MFP18

Case Outline—[3126] unit: mm



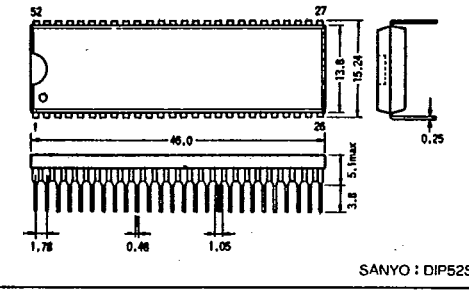
SANYO : DIC64S

Case Outline—[3127] unit: mm



SANYO : DIC42S

Case Outline—[3128] unit: mm



SANYO : DIP52S