Ordering number:ENN2648

CMOS IC

LC66PG5XX

EPROM-Mountable Type 4-bit Microcomputer Evaluation Chip for The LC665XX Series Microcomputers

Overview

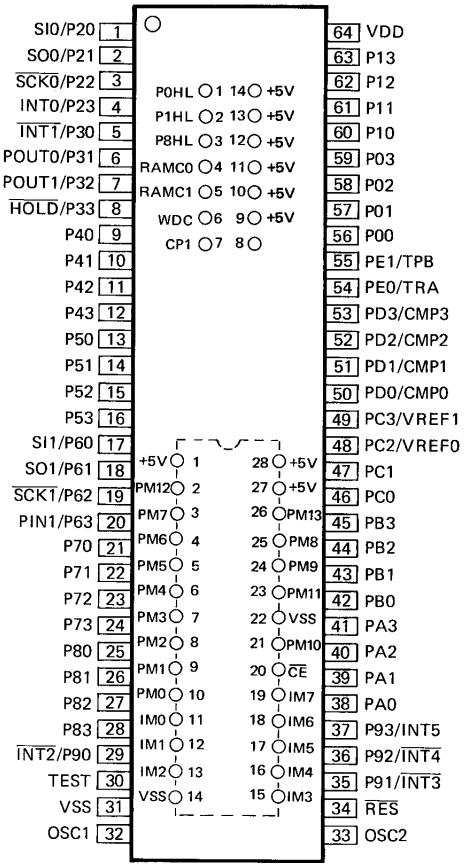
The LC66PG5XX is an EPROM-mountable type 4-bit microcomputer for developing and evaluating programs written for the CMOS 4-bit single-chip LC665XX series microcomputers. Either 2764 or 27128 type EPROM can be mounted on the LC66PG5XX. The LC66PG5XX with the EPROM mounted can carry out the same functions as those of the LC665XX series microcomputers. Therefore, you can evaluate programs developed for application products controlled by the LC665XX series microcomputers by incorporating the LC66PG5XX into the applications before the programs are masked in the ROMs.

Features

- Either 2764 or 27128 type EPROM can be mounted.
- Shrink type 64-pin configuration compatible with the LC665XX series microcomputers. Note that pull-up resistors need to be externally added.
- Options provided for selecting functions.
  Options allowing the user to select output signal level for ports 0, 1 and 8 at the initial reset or to specify whether the watchdog timer function is employed by setting external pin levels
- Instruction cycle time 0.92 to 10 microseconds.
- +5V single power source.

The LC66PG5XX has the 28-pin soket and 14-pin soket on the top face of the package. It also has the shrink type 64-pin terminals on the bottom face of the package. The 28-pin soket is used for mounting the EPROM containing the programs and 14-pin soket for selecting functions by options (input/output options not included). The shrink type 64-pin terminals are compatible with the LC665XX series microcomputers.

Pin assignment



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Configurations of the LC665XX series microcomputers

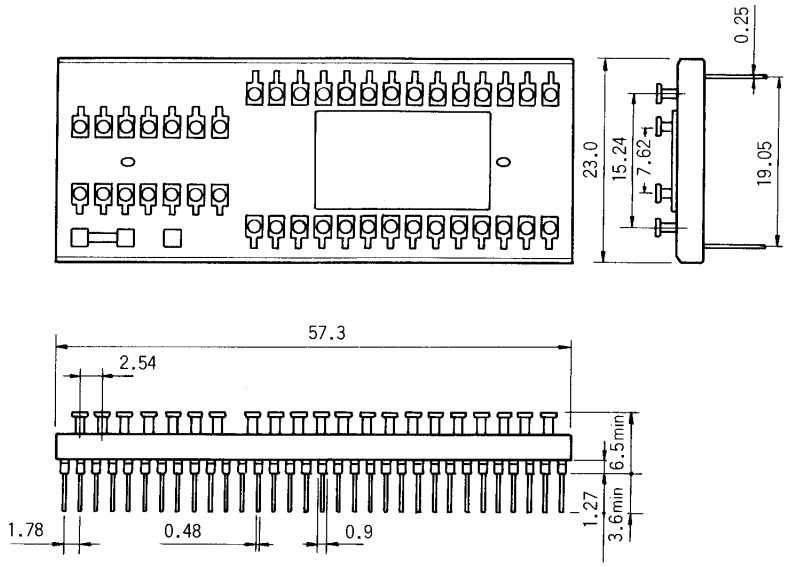
Model name	LC66506A	LC66508A	LC66512A	LC66516A	LC66PG5XX	LC66599
ROM capacity	6KB	8KB	12KB	16KB	16K bytes. Externally added	16K bytes. Externally added
RAM capacity	512×4	512×4	512×4	512×4	512×4	512×4
Package	DIP64S FLP64	←	←	←	DIC64S	PGA120
Remarks	Available	←	←	←	Piggyback	EVA chip

Notes on use

The LC66PG5XX is a product for developing and evaluating programs for the LC665XX series microcomputers. Keep always in mind the following considerations when using the LC66PG5XX.

1. The operating conditions are different from those of the production mask ROM . It is not recommended that the LC66PG5XX is used under the environmental conditions including high temperature and terrible humidity.
2. The electric characteristics are not the same as those of the production mask ROM. To evaluate strictly the electric characteristics at the interface with external circuits, use the recommended electric characteristics values of the production mask ROM.
3. The discrepancy in internal circuit pattern configuration between the LC66PG5XX and the production mask ROM results in the following differences between them.
   - •Different initial values are set in RAMs at power ON.
   - •Different noise figures (NF) are recorded. That is, the static noise intensity of the LC66PG5XX is different from that of the production mask ROM. Keep it always in mind.

External dimension



Overview of terminal function

Terminal name	Input/ output	Function	LC66PG5XX output format	Option (production chip)	At initial reset
P00 P01 P02 P03	I/O	Input/output port P00 to P03 •Data input and output in 4-bit units or in 1-bit units. •P00 to P03 used for controlling HALT mode.	•Nch OD output	•Pull-up MOS or Nch OD (open drain) output •Output level at initial reset	H or L (optional)
P10 P11 P12 P13	I/O	Input/output port P10 to P13 •Data input and output in 4-bit units or in 1-bit units.	•Nch OD output	•Pull-up MOS or Nch OD output •Output level at initial reset	H or L (optional)
P20/SI0 P21/SO0 P22/$\overline{SCK0}$ P23/INT0	I/O	Input/output port P20 to P23 •Data input and output in 4-bit units or in 1-bit units. •P20 also used as SI0 terminal for serial input. •P21 also used as SO0 for serial output. •P22 also used as $\overline{SCK0}$ for serial clock signal input/output. •P23 also used as INT0 terminal for INT0 interrupt request input . In addition, it is used for timer 0 event count input and pulse width measurement input.	•Nch OD output	•CMOS or Nch OD output	H
P30/$\overline{INT1}$ P31/POUT0 P32/POUT1	I/O	Input/output port P30 to P32 •Data input and output in 3-bit units or in 1-bit units. •P30 also used as $\overline{INT1}$ terminal for $\overline{INT1}$ interrupt request signal. •P31 also used for burst pulse signal output from timer 0. •P32 also used for burst pulse signal output from timer 1 and PWM signal output.	•Nch OD output	•CMOS or Nch OD output	H
P33/$\overline{HOLD}$	I	HOLD mode control input. •When $\overline{HOLD}$=L, HOLD mode to be set by the HOLD instruction. •During HOLD mode "ON", restart up to the CPU by applying "H"-level signal to the $\overline{HOLD}$ terminal. •Also used as input port P33 if used together with port P30 to P32. •CPU not to be reset even if "L"-level signal is applied to the $\overline{RES}$ terminal with the P33/$\overline{HOLD}$ set to "L". The output level of the P33/$\overline{HOLD}$ terminal at power ON must not be set "L"on your application products.	–	–	–
P40 P41 P42 P43	I/O	Input/output port P40 to P43 •Data input and output in 4-bit units and 1-bit units. •Also used for data input/output in 8-bit units if jointly used with port P50 to P53. •Used for ROM data output in 8-bit units if jointly used with port P50 to P53.	•Nch OD output	•Pull-up MOS or Nch OD output	H

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Terminal name	Input/ output	Function	LC66PG5XX output format	Option (production chip)	At initial reset
P50 P51 P52 P53	I/O	Input/output port P50 to P53 •Data input/output in 4-bit units and 1-bit unit. •Used for input/output in 8-bit units if jointly used with port P40 to P43. •Used for ROM data output in 8-bit units if jointly used with port P40 to P43.	•Nch OD output	•Pull-up MOS or Nch OD output	H
P60/SI1 P61/SO1 P62/$\overline{SCK1}$ P63/PIN1	I/O	Input/output port P60 to P63 •Data input/output in 4-bit units and 1-bit units. •P60 terminal also used as terminal SI1 for serial input. •P61 terminal also used as terminal SO1 for serial output. •P62 terminal also used as terminal $\overline{SCK1}$ for serial clock signal input/output. •P63 terminal also used for event count input to timer 1.	•Nch OD output	•CMOS or Nch OD output	H
P70 P71 P72 P73	O	Output port P70 to P73 •Data output in 4-bit units and in 1-bit units. •The contents of output latch circuit to be input with input-related instructions.	•Nch OD output	•Pull-up MOS or Nch OD output	H
P80 P81 P82 P83	O	Output port P80 to P83 •Data output in 4-bit units and in 1-bit units. •The contents of output latch circuit to be input with input-related instructions. •Pch OD output option available.	•Pch OD output	•CMOS or Pch OD output •Output level at the initial reset	H or L (optional)
P90/$\overline{INT2}$ P91/$\overline{INT3}$ P92/$\overline{INT4}$ P93/INT5	I/O	Input/output port P90 to P93 •Data input and output in 4-bit units and in 1-bit units. •P90 also used as the $\overline{INT2}$ terminal for $\overline{INT2}$ interrupt request input. •P91 also used as the $\overline{INT3}$ terminal for $\overline{INT3}$ interrupt request input. •P92 also used as the $\overline{INT4}$ terminal for $\overline{INT4}$ interrupt request input. •P93 also used as the INT5 terminal for INT5 interrupt request input.	•Nch OD output	•CMOS or Nch OD output	H
PA0 PA1 PA2 PA3	O	Output port PA0 to PA3 •Data output in 4-bit units and in 1-bit units. •The contents of output latch circuit to be input with input-related instructions.	•Nch OD output	•Pull-up MOS or Nch OD output	H
PB0 PB1 PB2 PB3	O	Output port PB0 to PB3 •Data output output in 4-bit units and in 1-bit units. •The contents of output latch circuit to be input with input-related instructions.	•Nch OD output	•Pull-up MOS or Nch OD output	H

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Terminal name	Input/ output	Function	LC66PG5XX output format	Option (production chip)	At initial reset
PC0 PC1 PC2/VREF0 PC3/VREF1	I/O	Input/output port PC0 to PC3 •Data input and output in 4-bit units and in 1-bit units. •PC2 also used as the VREF0 terminal for reference voltage input. •PC3 also used as the VREF1 terminal for reference voltage input.	•Nch OD output	•CMOS or Nch OD output	H
PD0/CMP0 PD1/CMP1 PD2/CMP2 PD3/CMP3	I	Input port PD0 to PD3 •Can be selected as comparator input terminals on programs. PD0 : reference voltage input (VREF0). PD1 to PD3 : reference voltage input (VREF1) •PD0, PD1 (PD2 to PD3) selectable as comparator input ports on programs in this unit.	–	–	Normal input
PE0/TRA PE1/TRB	I	Input port •Selectable as three-state input port on programs.	–	–	Normal input
OSC1 OSC2	I O	Terminals for system clock oscillator externally added. •Leave OSC2 open and close OSC1 for external clock signal input when external clock mode is selected.	–	•Ceramic resonator oscillation, RC (resistor and capacitor) or external clock selection.	–
$\overline{RES}$	I	Terminal for system reset signal input. •CPU to be initialized when P33/$\overline{HOLD}$="H" plus "L" level voltage is applied to the $\overline{RES}$ terminal.	–	–	–
TEST	I	Terminal for CPU test signal input. •Always connected to V_{SS} during operation.	–	–	–
V_{DD} V_{SS}	–	Power source terminal	–	–	–

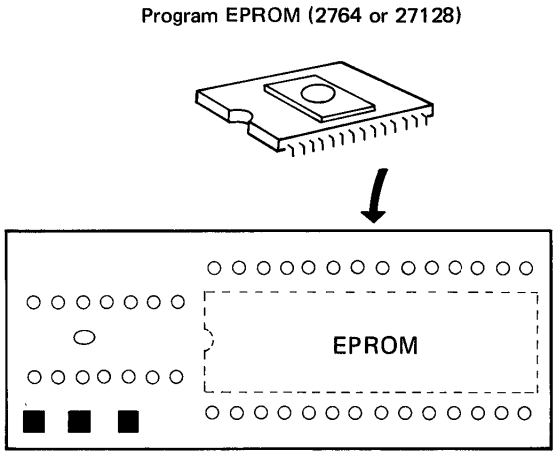
LC66PG5XX special terminals

Terminal name	Input/ output	Output type	Function
P0HL P1HL P8HL	I	–	Terminals for signal input to select output level at ports 0, 1 and 8 at the reset. "H" level output to be selected if "H" level signal is input to the terminals.
RAMC0 RAMC1	I	–	Terminal for signal input to control RAM capacity.
WDC	I	–	Terminal for signal input to contorol whether the watchdog timer function is used. The watchdog timer function to be selected if "H" level signal is input.
CP1	O	Pu MOS output	Terminal for signal output to select clock signal edge for output latch of extended ports.
IM0 to IM7	I	–	Terminals for instruction input from external circuits.
PM0 to PM13	O	Pu MOS output	Terminals for PC output to external circuits.
$\overline{CE}$	O	Pu MOS output	Terminal for signal output to contorol the $\overline{CE}$ terminal of memory externally added.

Remarks : Pu MOS output ..... Pull-up MOS transistor output.
CMOS output ..... Complementary MOS output.
OD output..... Open drain output.

How to mount and use EPROM on the LC66PG5XX

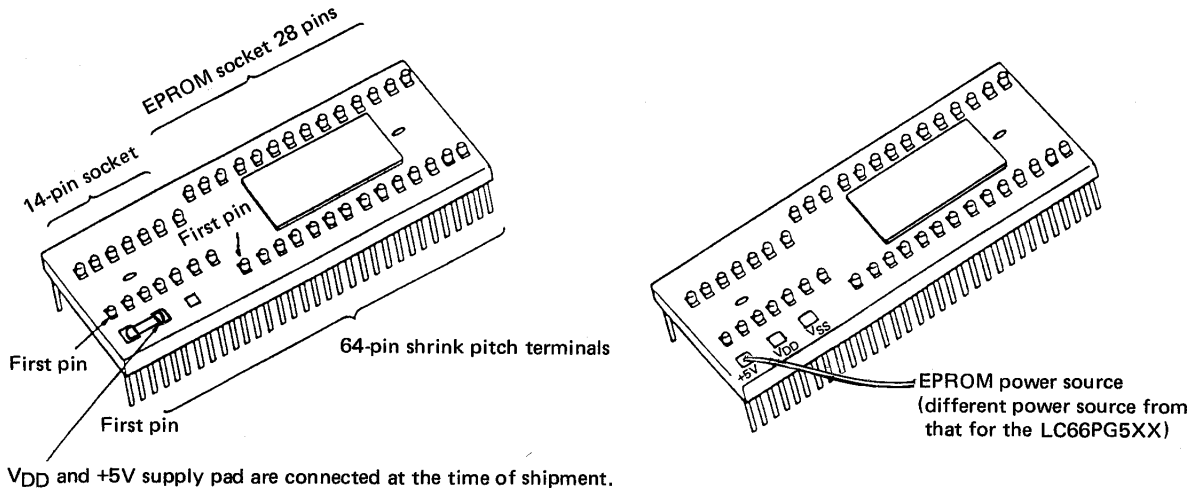
You write assembled program data into an EPROM and mount it on the LC66PG5XX. To write data into the EPROM, you can use the EPROM writer function of the EVA-800.



▲ First pin location of the 2764 or 27128 type EPROM

Power source for EPROM

Normal current drain per EPROM is in the range of 50mA and 100mA. When power capacity of an application product is not sufficient, power can be supplied to the EPROM from external independent power source. That is, the power source which is different from that on the application system can be selected.
At the factory shipment, the +5V pin and V_{DD} pin are connected on the LC66PG5XX. Therefore, power is supplied to the EPROM from the LC66PG5XX power source terminal (pin64).
Of the power source pads on the package surface, +5V pad is used to supply power to the EPROM.



Note

The LC66PG5XX is a CMOS type IC. This reminds us that latch-up may be caused by input voltage level below the V_{SS} level or above the V_{DD} level. The latch-up is specific to this type of IC and destroys IC device structure or adversely affects operating functions. You should be careful about the voltage level range of the LC66PG5XX and EPROM. To start the LC66PG5XX and EPROM operation, first turn on the LC66PG5XX and then the EPROM. To stop the LC66PG5XX and EPROM operation, first turn off the EPROM and then the LC66PG5XX.

Function selection by options

Select the port 0, port 1 or port 8 output level at the reset, watchdog timer function and internal RAM capacity according to the options and functions of the microcomputer to be evaluated. Set as below pins 1 to 6 of the 14-pin socket on the package surface.

Function type	Pin No.	Pin name	Pin setting		Function mode
Port 0, port 1 and Port 8 output level at reset	1 2 3	P0HL P1HL P8HL	ON		Port output level "H"
			OFF		Port output level "L"
Watchdog timer	6	WDC	ON		Operation
			OFF		Stop
Internal RAM capacity	4 5	RAMC0 RAMC1	Pin setting		RAM capacity
			RAMC1	RAMC0	
			OFF	OFF	No setting for the LC665XX series microcomputers
			OFF	ON	
			ON	OFF	512W
			ON	ON	

ON : +5V voltage input, OFF : Open.

Pins 14, 13, 12, 11, 10 and 9 of the 14-pin socket are assigned as the +5V terminals. These terminals can be used only for supplying +5V voltage to the pins 1, 2, 3, 4, 5, and 6.
Note that pin 8 is reserved for future use and should be left open.

Notes on use

1. The port output format for the LC66PG5XX is as follows : The Pch OD format is employed only for port 8. The Nch OD format is employed for the rest. Add resistors to each port according to the port output formats employed for production chips.
   - When optional pull-up resistors are selected for ports P0, P1, P4, P5, P7, PA and PB, add resistors of about 10kΩ to them and connect the port to the V_{DD} terminal.
   - When the optional CMOS output format is selected for port P8, add the resistor of about 1kΩ to it and connect the port to the V_{SS} terminal. Select the resistor in the range of 0.5kΩ to 10kΩ according to load balance.
   - When the optional CMOS output format is selected for ports P2, P3 (P33 not included), P6, P9 and PC, add the resistors of about 10 kΩ to them and connect them to the V_{DD} terminal. (add the resistors of more than 1 kΩ if sink current is used.)
2. The LC66PG5XX has no feedback resistors. Add the external feedback resistor of about 1 MΩ to the LC66PG5XX when the ceramic resonator oscillation is selected. The external capacitance is the same as that of production chips.
3. The constants and oscillation characteristics of the RC (resistor and capacitor) oscillation circuit are different from those of production chips. Set them to the oscillation frequency of production chips by making adjustments to volume resistor.
4. The operating voltage level of the LC66PG5XX must be within the range of the operating voltage of the EPROM and other ICs.
   That is, the level is : V_{DD}=5Vwith 5% margin.
5. The operating environment temperature is in the range of 10°C to 40°C.

Absolute maximum ratings at Ta = 25˚C, V_{SS} = 0V

Parameter	Symbol	Terminal and note	Condition	Ratings	Unit	Note
Maximum voltage level	V_{DD} max	V_{DD}		–0.3 to +7.0	V	
Input voltage	$V_{IN}1$	P2, P3(P33/$\overline{HOLD}$ not included), P6		–0.3 to +15.0	V	1
	$V_{IN}2$	Other inputs		–0.3 to V_{DD}+3.0	V	2
Output voltage	$V_{OUT}1$	P2, P3(P33/$\overline{HOLD}$ not included), P6, P7 and PA		–0.3 to +15.0	V	1
	$V_{OUT}2$	Other outputs		–0.3 to V_{DD}+3.0	V	2
Output current per terminal	$I_{ON}1$	P0, P1, P2, P3(P33/$\overline{HOLD}$ not included), P4, P5, P6, P8, P9 and PC		4	mA	3
	$I_{ON}2$	P7, PA, PB		20	mA	3
	$-I_{OP}2$	P8		4	mA	4
Total terminal current	$\Sigma I_{ON}1$	P2, P3(P33/$\overline{HOLD}$ not included), P4, P5, P6, P7 and P8		75	mA	3
	$\Sigma I_{ON}2$	P0, P1, P9, PA, PB, PC		75	mA	3
	$-\Sigma I_{DP}1$	8		25	mA	4
Allowable power dissipation	Pd max	Ta=10 to 40° C	DIC-64S	600	mW	
Operating temperature	Topr			+10 to +40	°C	
Storage tempurature	Tstg			+55 to +125	°C	

Note 1: Applicable only when open drain output format is selected. If the format is not selected, another standard value is used.

Note 2: The self oscillation voltage level can be included in the standard value range as far as oscillation input/output is concerned.

Note 3: Sink current (applicable to P8 only when CMOS output format is selected).

Note 4: Source current (applicable to terminals other than P8 only when pull-up output format or CMOS output format is selected).

Recomemended operating conditions at Ta = 10˚C to 40˚C, V_{SS} = 0V, unless otherwise specified

Parameter		Symbol	Terminal	Codnitions		Ratings			Unit	Note
					V_{DD}(V)	min	typ	max		
Operating power voltage		V_{DD}	V_{DD}			4.0	5.0	6.0	V	
Memory hold voltage		$V_{DD}H$	V_{DD}	HOLD mode		1.8		6.0	V	
High-level input voltage		$V_{IH}1$	P2, P3 (33/$\overline{HOLD}$ not included),P6	Output Nch Tr OFF	4.0 to 6.0	0.75V_{DD}		+13.5	V	1
		$V_{IH}2$	P33/$\overline{HOLD}$ P9, $\overline{RES}$, OSC1	Output Nch Tr OFF	4.0 to 6.0	0.75V_{DD}		V_{DD}	V	2
		$V_{IH}3$	P0, P1, P4, P5, PC, PD, PE	Output Nch Tr OFF	4.0 to 6.0	0.7V_{DD}		V_{DD}	V	3
		$V_{IH}4$	PE	3-state input format	4.0 to 6.0	0.8V_{DD}		V_{DD}	V	
Medium-level input voltage		V_{IM}	PE	3-state input format	4.0 to 6.0	0.4V_{DD}		0.6V_{DD}	V	
In-phase input voltage range		V_{CMM}	PD, PC2, PC3	Comparator input mode	4.0 to 6.0	1.0		V_{DD}–1.5	V	
Low-level input voltage		$V_{IL}1$	P2, P3 (33/$\overline{HOLD}$ not included),P6, P9, $\overline{RES}$, OSC1	Output Nch Tr OFF	4.0 to 6.0	V_{SS}		0.25V_{DD}	V	2
		$V_{IL}2$	P33/$\overline{HOLD}$		1.8 to 6.0	V_{SS}		0.25V_{DD}	V	
		$V_{IL}3$	P0, P1, P4, P5, PC, PD, PE, TEST	Output Nch Tr OFF	4.0 to 6.0	V_{SS}		0.3V_{DD}	V	3
		$V_{IL}4$	PE	3-state input format	4.0 to 6.0	V_{SS}		0.2V_{DD}	V	
Operating frequency (instruction cycle time)		fop (Tcyc)			4.0 to 6.0	0.4 (10)		4.35 (0.92)	MHz (µs)	
Externanl clock pulse input condition	Frequency	f_{ext}	OSC1	See Figure 1. Input to the OSC1 terminal. OSC2 terminal left open.	4.0 to 6.0	0.4		4.35	MHz	
	Pulse width	textH textL		Same as sbove.	4.0 to 6.0	7.0			ns	
	Fall/rise time	textR textF		Same as sbove.	4.0 to 6.0			30	ns	
Self osillation conditions	Frequency	f_{CF}	OSC1, OSC2	See Figure 2. 4MHz	4.0 to 6.0		4.0		MHz	
	Ceramic resonator oscillation: Oscillation stabilization time	f_{CFS}		See Figure 3. 4MHz	4.0 to 6.0			10	ms	
	External RC oscillation constants	Cext Rext	OSC1, OSC2	See FIgure 4.	4.0 to 6.0		100 2.2		pF kΩ	

Note 1: Applicable to terminals with open drain output format. $V_{IH}2$ applied to P33/$\overline{HOLD}$ terminal.
Note 2: Applicable to terminals with open drain output format.
Note 3: $V_{IH}4$, V_{IM} and $V_{IL}4$ applied when PE is used for 3-state input operation.

Electric characteristics at Ta = 10˚C to 40˚C, V_{SS} = 0, unless otherwise specified

Parameter			Symbol	Terminal	Codnitions	Ratings			Unit	Note
					V_{DD}(V)	min	typ	max		
High-level input current			$I_{IH}1$	P2, P3 (33/HOLD not included),P6	V_{IN} =13.5V Output Nch Tr OFF	4.0 to 6.0			+5.0	µA	1
			$I_{IH}2$	P0, P1, P4, P5, P9 PC, OSC1, $\overline{RES}$, P33/$\overline{HOLD}$ (PD, PE, PC2 and PC3, not included)	V_{IN} =V_{DD} Output Nch Tr OFF	4.0 to 6.0			+1.0	µA	1
			$I_{IH}3$	PD, PE, PC2, PC3	V_{IN}=V_{DD} Output Nch Tr OFF	4.0 to 6.0			+1.0	µA	1
Low-level input current			$I_{IL}1$	Input level to terminals other than PD, PE, PC2 and PC3	V_{IN}=V_{SS} Output Nch Tr OFF	4.0 to 6.0	–1.0			µA	2
			$I_{IL}2$	PC2, PC3, PD, PE	V_{IN}=V_{SS} Output Nch Tr OFF	4.0 to 6.0	–1.0			µA	2
High-level output voltage			$V_{OH}1$	P8	I_{OH}= –1mA	4.0 to 6.0	V_{DD}–1.0			V	
					I_{OH}= –0.1mA	4.0 to 6.0	V_{DD}–0.5				
Low-level output voltage			$V_{OL}1$	P0, P1, P2, P3, P4, P5, P6, P9, and PC (P33/$\overline{HOLD}$ not included)	I_{OL}= 1.6mA	4.0 to 6.0			0.4	V	
			$V_{OL}2$	P7, PA, PB	I_{OL}= 10mA	4.0 to 6.0			1.5	V	
Output off leak current			$I_{OFF}1$	P2, P3, P6, P7, PA	V_{IN}=13.5V	4.0 to 6.0			5.0	µA	6
			$I_{OFF}2$	(P2, P3, P6, P7, P8 and PA not included)	V_{IN}=V_{DD}	4.0 to 6.0			1.0	µA	6
			$I_{OFF}3$	P8	V_{IN}=V_{SS}	4.0 to 6.0	–1.0			µA	7
Comparator offset voltage			V_{OFF}	PD	V_{IN}=1.0V to V_{DD}–1.5V	4.0 to 6.0		±50	±300	mV	
Schmidt characteristics	Hysteresis voltage		V_{HYS}	P2, P3, $\overline{RES}$, P6, P9 and OSC1. OSC1 for external clock signal input.		4.0 to 6.0		0.1V_{DD}		V	
	High-level threshold voltage		VtH				0.5V_{DD}		0.75V_{DD}		
	Low-level threshold voltage		VtL				0.25V_{DD}		0.5V_{DD}		
RC (resistor and capacitor) oscillation frequency)			f_{RC}	OSC1, OSC2	See Figure 4. Cext=100pF±5% Rext=2.2kΩ±1%	4.0 to 6.0	2.0	3.0	4.0	MHz	
Serial clock	Cycle time	Input	t_{CKCY}	$\overline{SCK0}$, $\overline{SCK1}$	See the timing shown in Figure 5 and the test load in Figure 6.	4.0 to 6.0	0.92			µs	
		Outnput				4.0 to 6.0	2.0			Tcyc	
	Low-level/ high-level/ pulse width	Input	t_{CKL}			4.0 to 6.0	0.4			µs	
		Outnput	t_{CKH}			4.0 to 6.0	1.0			Tcyc	
	Fall/rise time	Input	t_{CKR}			4.0 to 6.0			3.0	µs	
		Outnput	t_{CKF}			4.0 to 6.0			0.1		

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Parameter		Symbol	Terminal		Codnitions	Ratings			Unit	Note
					V_{DD}(V)	min	typ	max		
Serial input	Data setup time	t_{ICK}	SI0, SI1		See Figure 5 "Serial input/output timing" Synchronized with the rise (↑) of the $\overline{SCK0}$ and $\overline{SCK1}$ signals.	4.0 to 6.0	0.3			µs	
	Data hold time	t_{CKI}				4.0 to 6.0	0.3			µs	
Serial output	Output delay time	t_{CKO}	SO0, SO1		See Figure 5 "Serial input/output timing" and Figure 6 "Timing load". Synchronized with the fall (↓) of the $\overline{SCK0}$ and $\overline{SCK1}$ signals.	4.0 to 6.0			0.3	µs	
Pulse input conditions	INT0 high-level/ low-level/pulse width	t_{I0H} t_{I0L}	INT0	See Figure 7.	•When INT0 interrupt is accepted. •When timer 0 event counter/pulse width measure input is accepted.	4.0 to 6.0	2			Tcyc	
	Interrupt input to terminals other than INT0. High-level/low-level/ pulse width.	t_{I1H} t_{I1L}	$\overline{INT1}$, $\overline{INT2}$ $\overline{INT3}$, $\overline{INT4}$ $\overline{INT5}$		•When each interrupt is accepted.		2			Tcyc	
	PIN1 high-level/ low-level/pulse width	t_{PINH} t_{PINL}	PIN1		•When timer 1 event counter input is accepted.		2			Tcyc	
	$\overline{RES}$ high-level/ low-level/pulse width	t_{RSH} t_{RSL}	$\overline{RES}$		•When reset signai is accepted.		3			Tcyc	
Comparator response speed		T_{RS}	PD	See Figure 8.		4.0 to 6.0			30	µs	
Operating mode current drain		I_{DDop}	V_{DD}		4MHz ceramic resonator oscillation	4.0 to 6.0		4.5	8	mA	8
					4MHz external clock			6.5	11		
					RC oscillation			4.0	8		
HALT mode current drain		I_{DDHALT}	V_{DD}		4MHz ceramic resonator oscillation	4.0 to 6.0		1.0	2.5	mA	9
					4MHz external clock			2	3.5		
					RC oscillation			1.2	2.5		
HOLD mode current drain		I_{DDHOLD}	V_{DD}			1.8 to 6.0		0.01	10	µA	9

Note 1: Open drain output format and output Nch Tr OFF for input/output common ports.
Note 2: Open drain output format and output Nch Tr OFF for input/output common ports.
Note 6: Open drain output format and output Nch Tr OFF.
Note 7: Open drain output format and output Pch Tr OFF.
Note 8: Reset status. EPROM current drain not included.
Note 9: EPROM current drain not included.

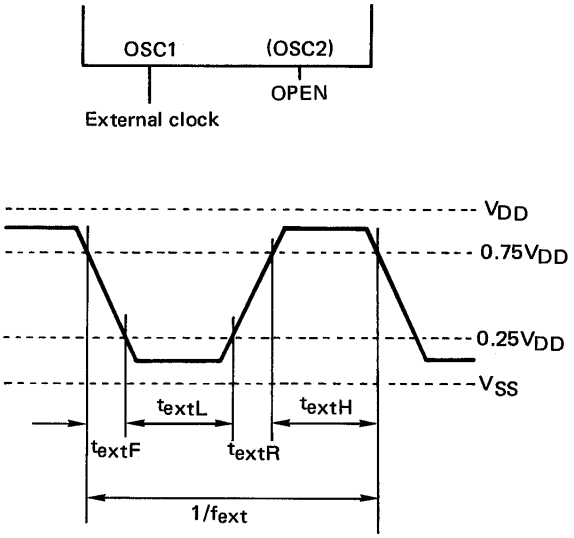
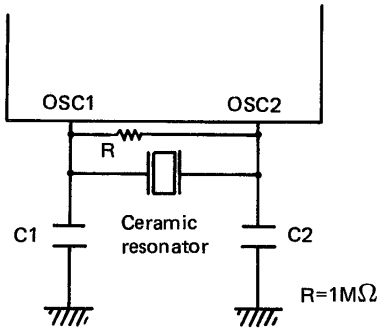


Fig. 1 External clock input waveform

(1) Capacitor externally connected type



(2) Capacitor contained type

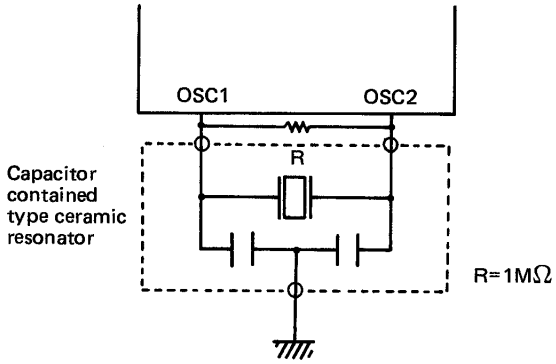


Fig. 2 Ceramic resonator oscillation circuit

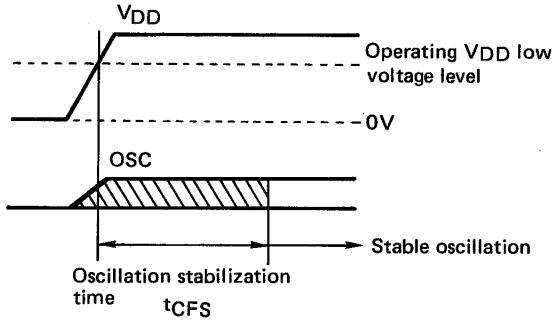


Fig. 3 Oscillation stable time

Capacitor externally connected type	4MHz (Murata) CSA4.00MG	C1	33pF±10%
		C2	33pF±10%
	4MHz (Kyocera) KBR4.0MS	C1	33pF±10%
		C2	33pF±10%
Capacitor contained type	4MHz CST4.00MG (Murata)		
	4MHz KBR-4.0MES (Kyocera)		

Table1 : Recommended ceramic resonator constants

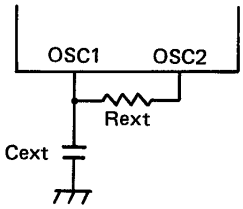


Fig. 4 RC oscillation

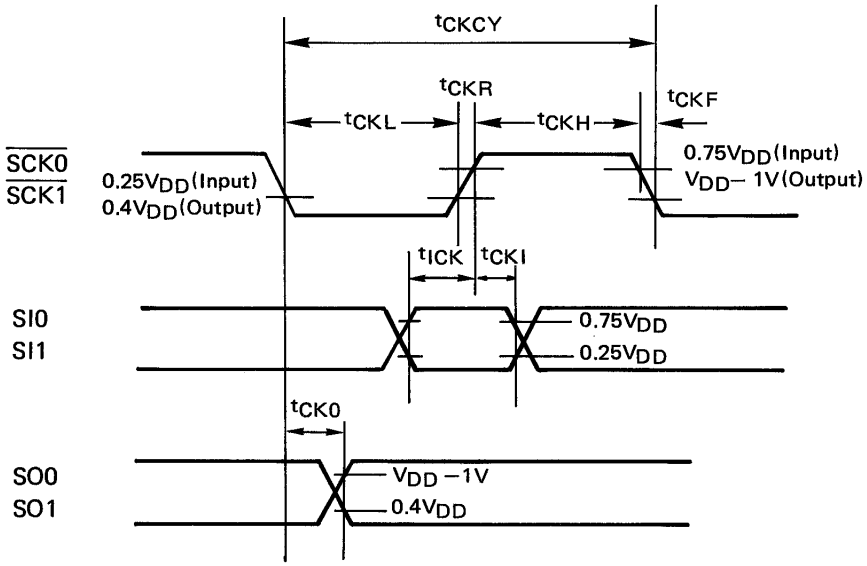


Fig. 5 Serial input/output timing

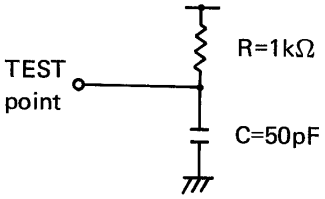


Fig. 6 Test Loads

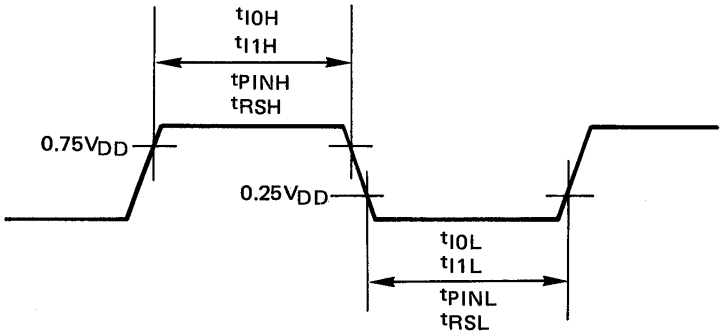


Fig. 7 INT0, $\overline{\text{INT1}}$, $\overline{\text{INT2}}$, $\overline{\text{INT3}}$, $\overline{\text{INT4}}$, INT5, PIN1, $\overline{\text{RES}}$ input timing

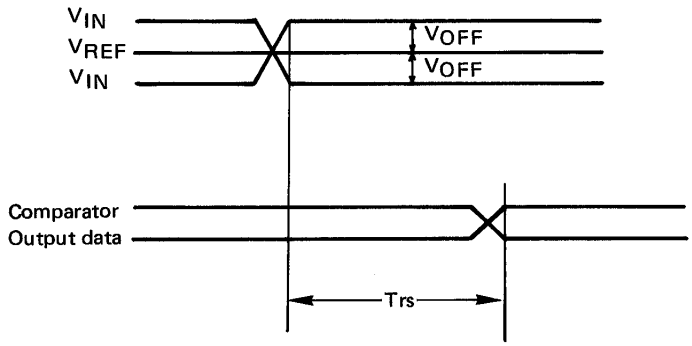


Fig. 8 Comparator response Trs timing