Ordering number : EN*4434

CMOS IC

# LC58E76

## On-Chip EPROM Microcomputer 4-Bit Single Chip Microprocessor with LCD Driver, 12 Kbytes of EPROM and 1 Kbit of RAM On-Chip

## Overview

The LC58E76 is an on-chip EPROM microcontroller in the LC587X series of CMOS 4-bit single chip microcontrollers.

The LC58E76 provides the same functionality as the LC5876 mask ROM version, and has the same pin layout. The LC58E76 has a 16-kbyte EPROM capacity, and corresponds to the LC5872, LC5873, LC58E74 and LC5876.

The LC58E76 is provided in an 80-pin ceramic window package, and programs can be written and erased repeatedly. Thus it is optimal for use during program development.

## Applications

The LC58E76 can be used for program and function evaluation in the following applications.

- System control of consumer products that use LCD displays, such as cameras, CD players and tuners
- Remote controllers for products such as VCRs or tuners
- System control of instruments that use LCD displays, such as miniature test equipment and medical equipment.
- The LC58E76 is optimal for products that use LCD displays, in particular, battery operated products.

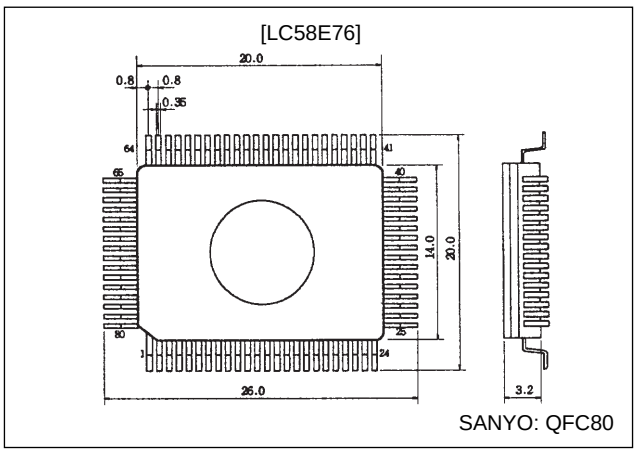
## Features

- Optional functions can be switched by EPROM data settings.
  The LC58E76 includes both program and option selection EPROM on-chip. The option selection EPROM can be used to specify almost all of the LC587X options, including crystal/ceramic oscillator specifications, port hold transistor selection and segment PLA specifications. These option specifications allow functional and operational testing in the actual PC board used in the mass-produced end product.
- On-chip 16 kbyte program EPROM
  The on-chip 16 kbyte program EPROM allows the LC58E76 to be used to evaluate all four members of the LC587X series. (See the series structure table on the next page.)
- Program and option data read/write
  The program and option data can be read and written with a standard commercial EPROM writer by using a dedicated EPROM writing board. (256K equivalent)
  (Either a Sanyo or an Advanced EPROM writer should be used.)
- Pin correspondence
  The LC58E76 is pin compatible with the mask ROM versions. (There is no chip correspondence.)

## Package Dimensions

unit: mm

**3152A-QFC80**






**SANYO Electric Co.,Ltd. Semiconductor Bussiness Headquarters**
TOKYO OFFICE Tokyo Bldg., 1-10, 1 Chome, Ueno, Taito-ku, TOKYO, 110-8534 JAPAN

## Series Structure

| Item \ Type No. | LC5872 | LC5873 | LC5874 | LC5876 | LC58E76 |
|---|---|---|---|---|---|
| ROM capacity | 2 k × 16 bits | 3 k × 16 bits | 4 k × 16 bits | 6 k × 16 bits | EPROM: 16 kbytes |
| RAM capacity | 256 × 4 bits | 256 × 4 bits | 256× 4 bits | 256 × 4 bits | 256 × 4 bits |
| Package | QIP80 | QIP80 | QIP80 | QIP80 | QFC80 ceramic window package |
| Notes | Available in quantity | Available in quantity | Available in quantity | Available in quantity | The on-chip EPROM window version will be available shortly. |

## Usage Notes

The LC58E76 is designed for use in developing and evaluating programs for the microprocessors in the LC587X series. However, there are differences between the LC58E76 and the mask ROM versions. Keep the following points in mind when using the LC58E76.

1. Notes on Reset
   When the RES pin input changes from high to low, the reset state is cleared after the prescribed oscillator stabilization period has elapsed. The options and the segment PLA are set up during the first 256 cycles following the clearing of the reset state. Instructions are executed starting at location 0 after this setup phase has completed. (The options are undefined and the segment outputs are held at the $V_{SS}$ level when the RES pin is high and during the first 256 cycles following the clearing of the reset state.)

2. Cover the LC58E76's window with an opaque seal when writing data to EPROM.

3. The LC58E76 and the mask ROM versions differ in the following points.

| Item | LC58E76 | Mask ROM versions (LC587X) | Note |
|---|---|---|---|
| Operating temperature | 10 to 40°C | –30 to 70°C | |
| Operating supply voltage | 2.8 to 5.5 V | 2.0 to 6.0 V | |
| Operating supply currents | 5 µA typ. (3 V, 32 kHz crystal)<br>20 µA typ. (5 V, 32 kHz crystal)<br>400 µA typ. (5 V, 400 kHz ceramic)<br>500 µA typ. (5 V, 2 MHz ceramic)<br>700 µA typ. (5 V, 4 MHz ceramic) | 4 µA typ. (3 V, 32 kHz crystal)<br>15 µA typ. (5 V, 32 kHz crystal)<br>400 µA typ. (5 V, 400 kHz ceramic)<br>500 µA typ. (5 V, 2 MHz ceramic)<br>700 µA typ. (5 V, 4 MHz ceramic) | Hold mode |
| Common segment output states at reset | Segment pins: VSS level (CMOS output)<br>Common pins: N-channel open drain | Static operation<br>(LCD drive output) | • Option switching in the EPROM version is performed by writing data to the option EPROM.<br>• Option switching in mask ROM versions is performed by specifying mask options. |
| Segment output states after the reset state is cleared | Off state | Off state/lit state | |
| Oscillator circuit specifications | CF/Xtal/CF + Xtal | CF/Xtal/CF + Xtal<br>RC/RC+Xtal/EXT/EXT+Xtal | |
| Crystal oscillator circuit | 32K/38K/65K (Note that this is 65K in the reset state) | 32K/38K/65K | |
| RES pin specifications | Open (reset on high) | Open (reset on high)<br>Open (reset on low)<br>Pull-up (reset on low)<br>Pull-down (reset on high) | |
| N ports | Open drain output | Open drain output/CMOS output | |
| LCD drive specifications | Static<br>1/2 bias, 1/2 duty<br>1/2 bias, 1/3 duty<br>1/2 bias, 1/4 duty<br>1/3 bias, 1/3 duty<br>1/3 bias, 1/4 duty<br>(Substitute static when the LCD driver is not used.) | Static<br>1/2 bias, 1/2 duty<br>1/2 bias, 1/3 duty<br>1/2 bias, 1/4 duty<br>1/3 bias, 1/3 duty<br>1/3 bias, 1/4 duty<br>(Substitute static when the LCD driver is not used.) | |
| Number of specifiable strobes | 00 – 1E<br>However, 0E and 0F cannot be used with the 4 MHz specifications. | 00 – 1E<br>However, 0E and 0F cannot be used with the 4 MHz specifications. | |

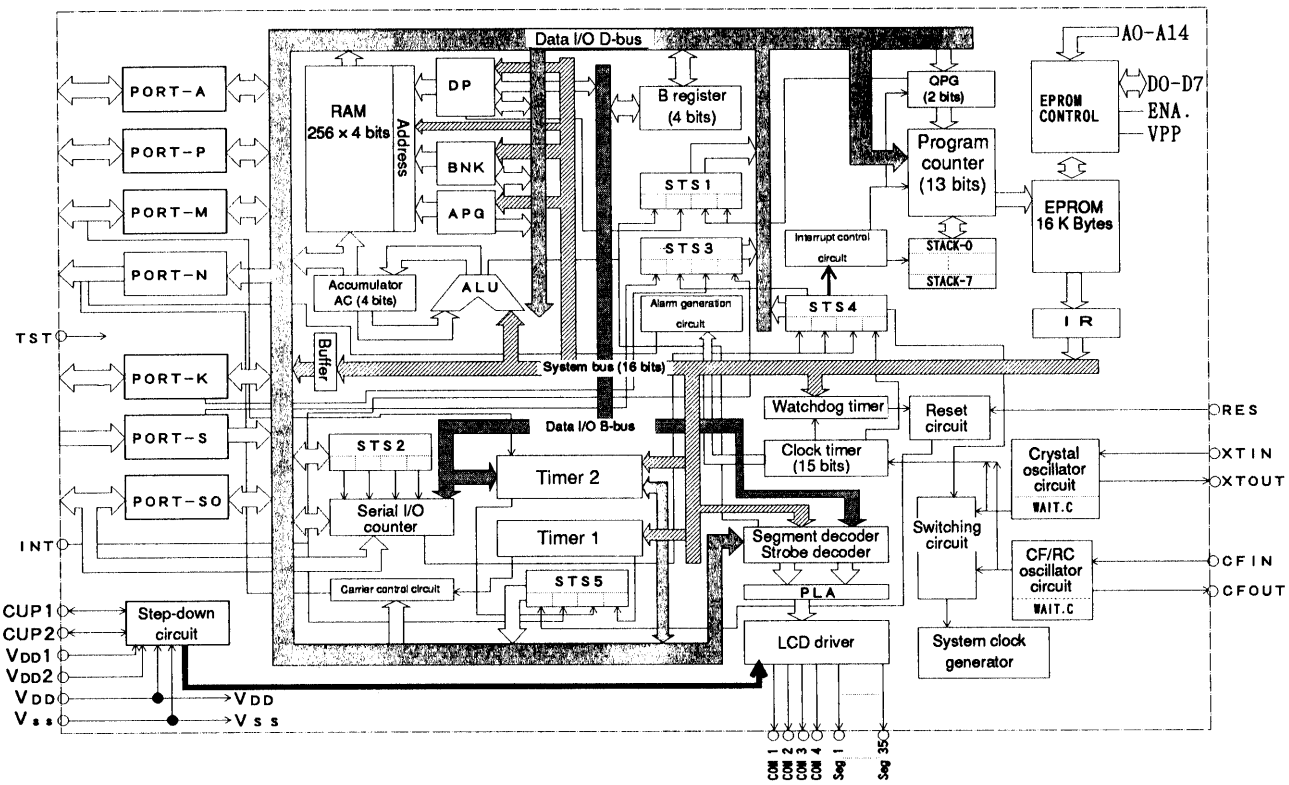
Note: Although the strobes number 00 to 1E can be used with CF 2 MHz and lower specifications, strobes number 0E, 0F and 1E cannot be used with the CF 4 MHz specifications.

## Pin Assignments

| PIn No. | Symbol | PIn No. | Symbol | PIn No. | Symbol | PIn No. | Symbol |
|---|---|---|---|---|---|---|---|
| 1 | COM2 | 21 | $V_{DD}2$ | 41 | N3 (Output ports) | 61 | Seg18 |
| 2 | COM1 | 22 | $V_{DD}1$ | 42 | N4 (Output ports) | 62 | Seg19 |
| 3 | CUP1 | 23 | $V_{SS}$ | 43 | TST | 63 | Seg20 |
| 4 | CUP2 | 24 | $V_{DD}$ | 44 | Seg1 | 64 | Seg21 |
| 5 | RES | 25 | CFIN | 45 | Seg2 | 65 | Seg22 |
| 6 | INT | 26 | CFOUT | 46 | Seg3 | 66 | Seg23 |
| 7 | SO1 (I/O, serial I/O ports) | 27 | S1 (Input ports) | 47 | Seg4 | 67 | Seg24 |
| 8 | SO2 (I/O, serial I/O ports) | 28 | S2 (Input ports) | 48 | Seg5 | 68 | Seg25 |
| 9 | SO3 (I/O, serial I/O ports) | 29 | S3 (Input ports) | 49 | Seg6 | 69 | Seg26 |
| 10 | SO4 (I/O, serial I/O ports) | 30 | S4 (Input ports) | 50 | Seg7 | 70 | Seg27 |
| 11 | A1 (I/O ports) | 31 | K1 (I/O ports) | 51 | Seg8 | 71 | Seg28 |
| 12 | A2 (I/O ports) | 32 | K2 (I/O ports) | 52 | Seg9 | 72 | Seg29 |
| 13 | A3 (I/O ports) | 33 | K3 (I/O ports) | 53 | Seg10 | 73 | Seg30 |
| 14 | A4 (I/O ports) | 34 | K4 (I/O ports) | 54 | Seg11 | 74 | Seg31 |
| 15 | P1 (I/O ports) | 35 | M1 (I/O ports) | 55 | Seg12 | 75 | Seg32 |
| 16 | P2 (I/O ports) | 36 | M2 (I/O ports) | 56 | Seg13 | 76 | Seg33 |
| 17 | P3 (I/O ports) | 37 | M3 (I/O ports) | 57 | Seg14 | 77 | Seg34 |
| 18 | P4 (I/O ports) | 38 | M4 (I/O ports) | 58 | Seg15 | 78 | Seg35 |
| 19 | XTOUT | 39 | N1 (Output ports) | 59 | Seg16 | 79 | COM4 |
| 20 | XTIN | 40 | N2 (Output ports) | 60 | Seg17 | 80 | COM3 |

Note: 1. The TST pin must be connected to $V_{SS}$ in normal operation.
2. When mounting the LC58E76, do not use solder dip techniques.

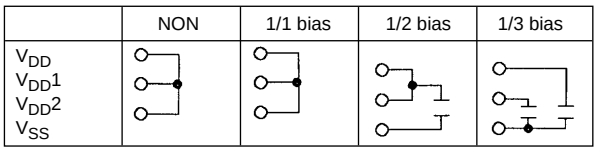
## System Block Diagram




**LC58E76 System Block Diagram**

| | | | | | |
|---|---|---|---|---|---|
| RAM | : Data memory | B | : B register | STS4 | : Status register 4 |
| ROM | : Program memory | OPG | : ROM page flag | STS5 | : Status register 5 |
| DP | : Data pointer register | PC | : Program counter | PLA | : Program logic for segment data and strobes |
| BNK | : Bank register | IR | : Instruction register | | |
| APG | : RAM page flag | STS1 | : Status register 1 | WAIT.C | : Wait time counter |
| AC | : Accumulator | STS2 | : Status register 2 | | |
| ALU | : Arithmetic and logic unit | STS3 | : Status register 3 | | |

## Pin Functions

| Pin | I/O | QFC-80 Pin No. | Function | Option | At reset |
|---|---|---|---|---|---|
| $V_{DD}$<br>$V_{SS}$ | —<br>— | 24<br>23 | Power supply | | |
| $V_{DD}1$<br>$V_{DD}2$ | —<br>— | 22<br>21 | LCD drive power supply<br>  | | |
| CUP1<br>CUP2 | —<br>— | 3<br>4 | Switching pin used to supply the LCD drive voltage to the VDD1 and VDD2 pins<br>• Connect a nonpolar capacitor between CUP1 and CUP2 when 1/2 or 1/3 bias is used.<br>• Leave open when a bias other than 1/2 or 1/3 is used. | | |
| CFIN<br>CFOUT | Input<br>Output | 25<br>26 | System clock oscillator connections<br>• Ceramic resonator connection (CF specifications)<br>• RC component connection (RC specifications)<br>• External signal input pin (CFOUT is left open)<br>This oscillator is stopped by the execution of a STOP or SLOW instruction. | • CF specifications<br>• Not used | |
| XTIN<br>XTOUT | Input<br>Output | 20<br>19 | Reference calculation (clock specifications, LCD alternation frequency), system clock oscillator<br>• 32 kHz crystal resonator connection<br>• 65 kHz crystal resonator connection<br>This oscillator is stopped by the execution of a STOP instruction. | • 32k specifications<br>• 65k specifications<br>• 38k specifications<br>• Not used | |
| S1<br>S2<br>S3<br>S4 | Input | 27<br>28<br>29<br>30 | Input-only ports<br>• Input pins used to read data into RAM<br>• Built-in 7.8 ms and 1.95 ms chatter exclusion circuits<br>• Built-in pull-up/pull-down resistors<br>Note: The 7.8 ms and 1.95 ms times are the times when ø0 is 32.768 kHz. | • Transistors to hold a low or high level<br>• Selection of either pull-up or pull-down resistors | • The pull-up or pull-down resistors are on.<br>Note: These pins go to the floating state when reset is cleared. |
| K1<br>K2<br>K3<br>K4 | I/O | 31<br>32<br>33<br>34 | I/O ports<br>• Input pins used to read data into RAM<br>• Output pins used to output data from RAM<br>• Built-in 7.8 ms and 1.95 ms input-mode chatter exclusion circuits. The selection of 7.8 or 1.95 ms is linked to that for the S ports.<br>Note: The 7.8 ms and 1.95 ms times are the times when ø0 is 32.768 kHz. | • Transistors to hold a low or high level<br>• Selection of either pull-up or pull-down resistors | • The pull-up or pull-down resistors are on.<br>Note: These pins go to the floating state when reset is cleared.<br>• Input mode<br>• Output latch data is set high. |
| M1<br>M2<br>M3<br>M4 | I/O | 35<br>36<br>37<br>38 | I/O ports<br>• Input pins used to read data into RAM<br>• Output pins used to output data from RAM<br>• M4 is used as the external clock input pin in TM2 mode 3.<br>* The minimum period for the external clock is twice the cycle time.<br>• Built-in pull-up/pull-down resistors | The same as K1 to K4 | The same as K1 to K4 |
| A1<br>A2<br>A3<br>A4 | I/O | 11<br>12<br>13<br>14 | I/O ports<br>• Input pins used to read data into RAM<br>• Output pins used to output data from RAM<br>• Built-in pull-up/pull-down resistors | The same as K1 to K4 | The same as K1 to K4 |
| P1<br>P2<br>P3<br>P4 | I/O | 15<br>16<br>17<br>18 | I/O ports<br>Function: The same as pins A1 to A4 | The same as K1 to K4 | The same as K1 to K4 |

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| Pin | I/O | QFC-80 Pin No. | Function | Option | At reset |
|---|---|---|---|---|---|
| SO1<br>SO2<br>SO3<br>SO4 | I/O | 7<br>8<br>9<br>10 | I/O ports<br>Function: The same as pins A1 to A4<br>Pins SO1 to SO3 area also used for the serial interface.<br>• Use of these pins in serial mode can be selected under program control.<br>• Pin functions: SO1: Serial input pin<br>SO2: Serial output pin<br>SO3: Serial clock pin<br>The serial clock pin can be switched between internal and external, and between rising edge output and falling edge output. | • Transistors to hold a low or high level<br>• Selection of either pull-up or pull-down resistors<br>• Internal serial clock divisor selection<br>I 1/1<br>II 1/2<br>III 1/4 | The same as K1 to K4 |
| N1<br>N2<br>N3<br>N4 | Output | 39<br>40<br>41<br>42 | Output-only ports<br>• Output pins used to output data from RAM<br>• An alarm signal can be output from pin N4. (Note that this is only when the N4 output latch is low.)<br>• An alarm signal modulated at 1, 2 or 4 kHz can be output. (These frequencies are output when ø0 is 32.768 kHz.)<br>• A carrier signal can be output from N3. (Note that this is only when the N3 output latch is low.) | • Pin N1 to N4 output circuit type:<br>I N-channel open drain<br>• Pin N1 to N4 output level<br>I High level<br>II Low level | The output levels on pins N1 to N4 can be specified as an option. |
| INT | Input | 6 | Input ports<br>• External interrupt request inputs<br>• Input pins used to read data into RAM<br>• Input detection can be performed on either rising or falling edges.<br>• Built-in pull-up/pull-down resistors | • Transistors to hold a low or high level<br>• Selection of either pull-up or pull-down resistors<br>• Signal conversion (rising/falling) selection | |
| RES | Input | 5 | LSI reset input<br>• The LC58E7008 resets on a high level input<br>Note: • An external resistor is required.<br>• The reset pulse must be at least 200 µs. | * Only when the input resistor open specification is selected | |
| TST | Input | 43 | Test input<br>Connect to $V_{SS}$ in normal operation. | | |
| Seg1,<br>Seg2 to<br>Seg35 | Output | 44,<br>45 to<br>78 | • LCD panel drive/general-purpose output<br>— LCD panel drive<br>I STATIC<br>II 1/2 bias – 1/2 duty<br>III 1/2 bias – 1/3 duty<br>IV 1/2 bias – 1/4 duty<br>V 1/3 bias – 1/3 duty<br>VI 1/3 bias – 1/4 duty<br>Types I to V can be specified as mask options.<br>— General-purpose output mode<br>I CMOS<br>II P-channel open drain<br>III N-channel open drain<br>Types I to III can be specified as mask options.<br>• LCD/general-purpose output control is handled by the segment PLA, and thus program control is not required.<br>• These pins support output latch control on reset and in standby states when the oscillators are stopped.<br>• Arbitrary combinations of LCD drive and general-purpose outputs can be used. | • LCD driver/general-purpose output switching<br>• LCD drive type switching<br>— STATIC<br>— 1/2 bias – 1/2 duty<br>— 1/2 bias – 1/3 duty<br>— 1/2 bias – 1/4 duty<br>— 1/3 bias – 1/3 duty<br>— 1/3 bias – 1/4 duty<br>• General-purpose output circuit switching<br>— CMOS<br>— P-channel open drain<br>— N-channel open drain<br>• Output latch control in standby modes | • LCD drive<br>All segments off<br>• General-purpose outputs<br>Low level<br>Note: When a combination of LCD drive and general- purpose outputs, the output state is either all segments off or low level.<br>• These pins go to the $V_{SS}$ level during the reset period. |

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<table>
<tr><th>Pin</th><th>I/O</th><th>QFC-80<br>Pin No.</th><th>Function</th><th>Option</th><th>At reset</th></tr>
<tr><td>COM1<br>COM2<br>COM3<br>COM4</td><td>Output</td><td>2<br>1<br>80<br>79</td><td>LCD panel drive common polarity outputs<br>The table below shows how these pins are used depending on the duty used. (Values for alternation frequency reflect a typical specification of 32.768 MHz for ø0)
<table>
<tr><th></th><th>Static duty</th><th>1/2 duty</th><th>1/3 duty</th><th>1/4 duty</th></tr>
<tr><td>COM1<br>COM2<br>COM3<br>COM4</td><td>❍<br>×<br>×<br>×</td><td>❍<br>❍<br>×<br>×</td><td>❍<br>❍<br>❍<br>×</td><td>❍<br>❍<br>❍<br>❍</td></tr>
<tr><td>Alternation frequency</td><td>32 Hz</td><td>32 Hz</td><td>42.7 Hz</td><td>32 Hz</td></tr>
</table>
Note: A cross ( × ) indicates that the pin is not used with that duty type.</td><td></td><td>These pins are n-channel open-drain outputs during the reset period.</td></tr>
</table>

## Usage Notes

The following tools and software are required when the LC58E76 is used.

The LC5870 Series Software Development Tools: For creating programs and option data.
Note that only MS-DOS machines are supported as the development host machine. See the LC5870 Series Software Development Tools manuals for details on the use of these tools.

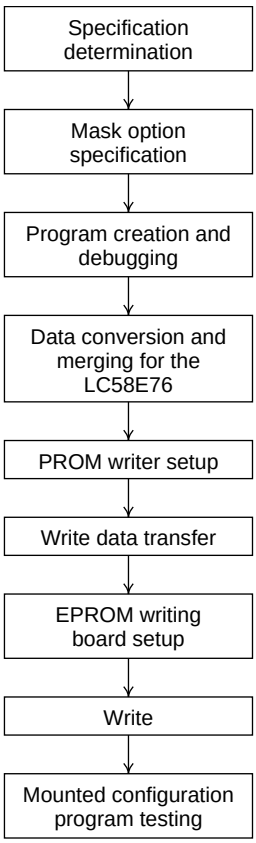
EC5876.EXE: This is a program that converts and merges program and option data for the LC5870 series so that it can be written to the LC58E76 EPROM.

EPROM writing board (adapter socket: W58E68Q): This is a socket adapter that allows a general-purpose PROM writer to be used to write program data to the LC58E76.

General-purpose PROM writer: The EVA-520 programmer that comes with the LC5870 Series Software Development Tools cannot be used. A general-purpose PROM writer must be used.

This section describes the procedures used with the LC58E76 and the EC5876.EXE program, which is one of the tools mentioned above. More details on LC5870 Series program development are available in LC5870 Series Users Manual and the manuals for the LC5870 Series Development Tools and the general-purpose PROM writer.

1. Procedure (This flowchart describes the procedure used.)




Use the SU5870.EXE program to create the option specification data.

Use the LC5870S.EXE cross assembler to create the program. Use the dedicated development tools for debugging.

Use the EC5876.EXE program to convert and merge the program and option data. This creates the data to be written to the LC58E76 EPROM. (See “Using the EC5876.EXE Program”.)

Setup the PROM writer ROM type, the start and stop addresses, and other states.
(See “Use of the EPROM Writing Board”.)

Transfer the LC58E76 EPROM data created with the EC5876.EXE program to the PROM writer.

Mount the PROM writer in the LC58E76 EPROM writing board.

Mount the LC58E76 in the EPROM writing board, and write the data.
Apply an opaque seal to the LC58E76 window at the point that the data is written.

Mount the LC58E76 in the socket in the application circuit, and check that the program functions correctly.

Note: There are differences in function and characteristics between the LC58E76 and the LC5870 series mask ROM versions. Be sure to take these differences into account when testing the programmed LC58E76. See the “Usage Notes” section for details on the differences.

2. Using the EC5876.EXE Program (Operation)
   As shown in the figures below, the data to be written to the LC58E76 consists of a program data area (instruction code area) and an option data area. The EC5876.EXE program applies a special conversion process to the option specification data to create the option data area data.

   The EC5876.EXE program converts and merges program data and option data to create the data to be written to the LC58E76.

   • Start-up procedure

```
A:>EC5876 ROMSAMP.HEX PLASAMP.HEX EP-SAMP.HEX<ENT>
Or:
A:>EC5876<ENT>
  ******************************************************
  * LC58E76 PROGRAM & MASK OPTION CONVERSION Ver XXXXXX *
  ******************************************************
  ROM PROGRAM NAME : ROMSAMP.HEX<ENT>
  PLA PROGRAM NAME : PLASAMP.HEX<ENT>
  EP ROM WRITE NAME: EP–SAMP.HEX<ENT>
Program complete..........Program termination message
```

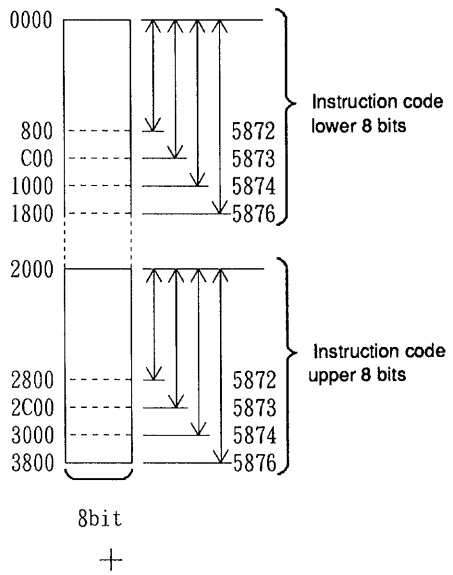
- Error messages

```
Error ON filename.HEX, FILE NOT FOUND.....The file “filename.HEX” was not found.
                                          The filename “filename.HEX” was incorrect.
Error ON MAKE LC5876, 5874, 5873, 5872.....The ROM data and the option data object
                                           microprocessor type did not agree. The ROM data
                                           must be created with a cross assembler and option
                                           specification software designed for the same
                                           microprocessor type.
Error ON filename.HEX, EOF NOT DETECTED.....A hexadecimal record end marker was not found
                                            in the file “filename.HEX”.
Error ON filename.HEX, ILLEGAL CHARACTER.....A character other than 0 to 9 or A to F was found
                                             in a hexadecimal context while reading the file
                                             “filename.HEX”.
Error ON filename.HEX, ADDRESS OVER.....An address in the file “filename.HEX” exceeded
                                        the allowed range.
Error ON filename.HEX, ILLEGAL FILEHDR.....The header in the file “filename.HEX” is not for
                                           the LC5870 series.
                                           There was an error in the hexadecimal file
                                           specification.
Error ON command line input,
         INVALID NUMBER OF PARAMETERS.....The number of parameters in the command line
                                          was inappropriate.
Error ON ILLEGAL, MASK OPTION DATA.....There was an error in the mask option data.
```

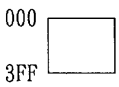
- EPROM data structure

Cross assembler and mask option data

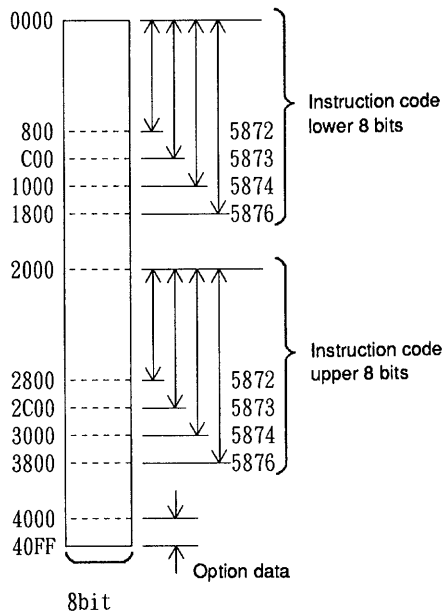
(1) Cross assembler data




(2) Mask option data

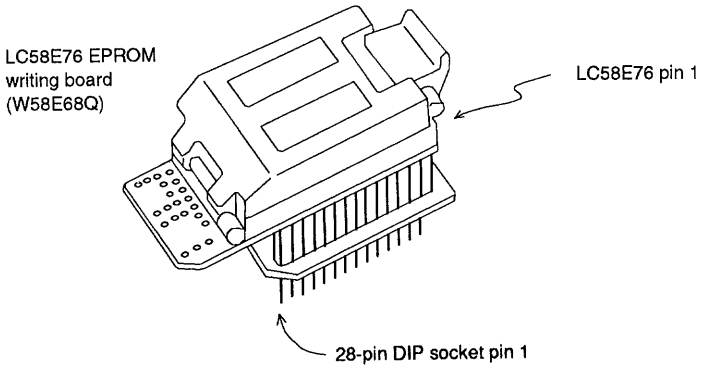



EPROM Data



3. Use of the W58E68Q EPROM Writing Board (Board used with both the LC58E68 and the LC58E76)
   The EPROM writing board is a socket adapter that fits the LC58E76 to the device socket in a general-purpose PROM writer.

   • EPROM Writing Board Appearance




   • PROM writer settings

   — ROM type: 256 K, VPP = 21 V mode
   — Start and stop addresses: Set these to 0000H and 40FFH.

4. Erasing LC58E76 EPROM Data
   Use a general-purpose EPROM eraser to erase data written to an LC58E76.

5. Notes On Order Mask ROM

   • The following methods cannot be used to order LC5870 Series mask ROM products.

   — Use of ".HEX" files that were converted and merged for use in an LC58E76
   — Use of an LC58E76 itself

   • Ordering mask ROM
   — Use the program hexadecimal data generated by the cross assembler.
   — Use the option hexadecimal data generated by the option specification software.
   — Provide three EPROMs to which the program hexadecimal data has been written using a general-purpose EPROM writer.
   — Provide three EPROMs to which the option hexadecimal data has been written using a general-purpose EPROM writer.

# Specifications

The electrical characteristics listed here are provisional values and are subject to change.

## Absolute Maximum Ratings at $V_{SS}$ = 0 V, TA = 25°C

| Parameter | Symbol | Conditions/Pin | | Ratings min | Ratings typ | Ratings max | Unit |
|---|---|---|---|---|---|---|---|
| Maximum supply voltage | $V_{DD}$ | | | –0.3 | | +6.0 | V |
| | $V_{DD}1$ | | | –0.3 | | $V_{DD}$ | V |
| | $V_{DD}2$ | | | –0.3 | | $V_{DD}$ | V |
| Maximum input voltage | $V_I$ (1) | As allowed in the specified circuit (Figure 1) XTIN, CFIN | | Allowed up to the voltage that appears | | | |
| | $V_I$ (2) | S1 – 4, K1 – 4, P1 – 4, SO1 – 4, A1 – 4, RES, INT, TST (K, P, M, SO and A ports in input mode) | | –0.3 | | $V_{DD}$ +0.3 | V |
| Maximum output voltage | $V_O$ (1) | As allowed in the specified circuit (Figure 1) XTOUT, CFOUT | | Allowed up to the voltage that appears | | | |
| | $V_O$ (2) | K1 –4, P1 – 4, SO1 – 4, A1 – 4, N1 – 4, CUP1, CUP2, Seg1 – 35, COM1 – 4, (K, P, M, SO and A ports in output mode) | | –0.3 | | $V_{DD}$ +0.3 | V |
| | $V_O$ (3) | Open drain specifications | N1 to N4 (n-channel) | –0.3 | | +13 | V |
| Output pin current | $I_O$ (1) | Per pin | N1 – 4 | 0 | | 15 | mA |
| | $I_O$ (2) | Per pin | N1 – 4 | –10 | | 0 | mA |
| | $I_O$ (3) | Per pin | K1 – 4, P1 – 4, M1 – 4, SO1 – 4, A1 – 4 | 0 | | 5 | mA |
| | $I_O$ (4) | Per pin | K1 – 4, P1 – 4, M1 – 4, SO1 – 4, A1 – 4 | –5 | | 0 | mA |
| | Σ $I_O$ (1) | Total (summed) pin current | K1 – 4, P1 – 4, M1 – 4, SO1 – 4, A1 –4, N1 – 4, Seg1 – 35 | | | 70 | mA |
| | Σ $I_O$ (2) | Total (summed) pin current | K1 – 4, P1 – 4, M1 – 4, SO1 – 4, A1 –4, N1 – 4, Seg1 – 35 | –70 | | | mA |
| Allowable power dissipation | Pdmax | For the QFC80 window ceramic flat package | | | | 500 | mW |
| Operating temperature | Topr | | | 10 | | 40 | °C |
| Storage temperature | Tstg | | | –55 | | +125 | °C |

## Allowable Operating Ranges at $V_{SS}$ = 0 V, Ta = 25°C

| Parameter | Symbol | Conditions/Pin | | Ratings min | Ratings typ | Ratings max | Unit |
|---|---|---|---|---|---|---|---|
| Supply voltage | $V_{DD}$ | No LCD specifications: $V_{DD}1 = V_{DD}2 = V_{DD}$ | | 2.8 | | 5.5 | V |
| | | Static drive specifications: $V_{DD}1 = V_{DD}2 = V_{DD}$ | | 2.8 | | 5.5 | V |
| | | 1/2 bias specifications: $V_{DD}1 = V_{DD}2 \cong 1/2V_{DD}$ | | 2.8 | | 5.5 | V |
| | | 1/3 bias specifications: $V_{DD}1 \cong 2 \times 1/3V_{DD}$<br>$V_{DD}2 \cong 1/3V_{DD}$ | | 2.8 | | 5.5 | V |
| Data retention supply voltage | $V_{HD}$ | RAM and register contents retention voltage* | | 2.8 | | $V_{DD}$ | V |
| Input high-level voltage | $V_{IH}1$ | S1 – 4, K1 – 4, P1 – 4, M1 – 4, SO1 – 4, A1 – 4, INT<br>(K, P, M, SO and A ports in input mode) | | 0.7 $V_{DD}$ | | $V_{DD}$ | V |
| Input low-level voltage | $V_{IL}1$ | | | 0 | | 0.3 $V_{DD}$ | V |
| Input high-level voltage | $V_{IH}2$ | RES pin | | 0.75 $V_{DD}$ | | $V_{DD}$ | V |
| Input low-level voltage | $V_{IL}2$ | | | 0 | | 0.25 $V_{DD}$ | V |
| Input high-level voltage | $V_{IH}3$ | CFIN pin | | 0.75 $V_{DD}$ | | $V_{DD}$ | V |
| Input low-level voltage | $V_{IL}3$ | | | 0 | | 0.25 $V_{DD}$ | V |
| Operating frequency 1 | fopg1 | $V_{DD}$ = 2.8 to 5.5 V, 32 kHz | XTIN/XTOUT crystal oscillator | 32 | | 33 | kHz |
| Operating frequency 2 | fopg2 | $V_{DD}$ = 2.8 to 5.5 V, 38 kHz | | 37 | | 39 | kHz |
| Operating frequency 3 | fopg3 | $V_{DD}$ = 2.8 to 5.5 V, 65 kHz | | 60 | | 70 | kHz |
| Operating frequency 4 | fopg4 | $V_{DD}$ = 2.8 to 5.5 V | CFIN/CFOUT CF specifications | 190 | | 1200 | kHz |
| Operating frequency 5 | fopg5 | $V_{DD}$ = 3.0 to 5.5 V | | 190 | | 2300 | kHz |
| Operating frequency 6 | fopg6 | $V_{DD}$ = 4.5 to 5.5 V | | 190 | | 4200 | kHz |
| Operating frequency 7 | fopg7 | $V_{DD}$ = 3.0 to 5.5 V | Pins SO1 and SO3 (in serial mode)<br>The rising and falling edges of input signal and clock waveforms must be ≤ 10 µs. | DC | | 200 | kHz |

Note: * In a state with the CF/RC oscillator and the crystal oscillator completely stopped, and all internal circuits stopped

## Electrical Characteristics at $V_{DD}$ = 2.8 to 3.2 V, $V_{SS}$ = 0 V, Ta = 25°C

| Parameter | Symbol | Conditions/Pin | | Ratings min | Ratings typ | Ratings max | Unit |
|---|---|---|---|---|---|---|---|
| Input resistance | $R_{IN}1$ A | VIN = 0.2 $V_{DD}$,<br>Low-level hold transistor *, Figure 2 | | 60 | 300 | 1200 | kΩ |
| | $R_{IN}1$ B | VIN = $V_{DD}$, Pull-down resistor *, Figure 2 | | 30 | 150 | 500 | kΩ |
| | $R_{IN}1$ C | VIN = 0.8 $V_{DD}$,<br>High-level hold transistor *, Figure 2 | | 60 | 300 | 1200 | kΩ |
| | $R_{IN}1$ D | VIN = $V_{SS}$, Pull-up resistor *, Figure 2 | | 30 | 150 | 500 | kΩ |
| | $R_{IN}2$ A | VIN = 0.2 $V_{DD}$, INT low-level hold transistor | | 60 | 300 | 1200 | kΩ |
| | $R_{IN}2$ B | VIN = $V_{DD}$, INT pull-down resistor | | 300 | 1500 | 5000 | kΩ |
| | $R_{IN}2$ C | VIN = 0.8 $V_{DD}$, INT high-level hold transistor | | 60 | 300 | 1200 | kΩ |
| | $R_{IN}2$ D | VIN = $V_{SS}$, INT pull-up resistor | | 300 | 1500 | 5000 | kΩ |
| | $R_{IN}3$ | VIN = $V_{DD}$,<br>With a pull-down resistor on the TST pin | | 20 | 70 | 300 | kΩ |
| Output low-level voltage | $V_{OL}$ (1) | IOL = 1.0 mA | N1 – 4 | | | 0.5 | V |
| Output high-level voltage | $V_{OH}$ (2) | IOH = –400 µA | K1 – 4, P1 – 4, M1 – 4, SO1 – 4, A1 – 4<br>(K, P, M, SO and A ports in output mode) | $V_{DD}$ – 0.5 | | | V |
| Output low-level voltage | $V_{OL}$ (2) | IOL = 400 µA | | | | 0.5 | V |
| Output off leakage current | $\lvert I_{OFF} \rvert$ | VOH = 10.5 V | N1 – 4, Figure 10 | | | 1.0 | µA |
| Segment port output impedance<br>• When CMOS output ports are used | | | | | | | |
| Output high-level voltage | $V_{OH}$ (3) | IOH = –100 µA | Seg 1 to 35 | $V_{DD}$ – 0.5 | | | V |
| Output low-level voltage | $V_{OL}$ (3) | IOL = 100 µA | | | | 0.5 | V |

Note: * The 24 pins S1 to S4, K1 to K4, P1 to P4, M1 to M4, SO1 to SO4 and A1 to A4.

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| Parameter | Symbol | Conditions/Pin | | Ratings min | Ratings typ | Ratings max | Unit |
|---|---|---|---|---|---|---|---|
| • When p-channel open-drain output ports are used (See Figure 11.) | | | | | | | |
| Output high-level voltage | $V_{OH}$ (3) | $I_{OH}$ = –100 µA | Seg 1 to 35 | $V_{DD}$ – 0.5 | | | V |
| Output off leakage current | $\|I_{OFF}\|$ | $V_{OL} = V_{SS}$ | | | | 1.0 | µA |
| • When n-channel open-drain output ports are used (See Figure 11.) | | | | | | | |
| Output low-level voltage | $V_{OL}$ (3) | $I_{OL}$ = 100 µA | Seg 1 to 35 | | | 0.5 | V |
| Output off leakage current | $\|I_{OFF}\|$ | $V_{OH} = V_{DD}$ | | | | 1.0 | µA |
| • Static drive | | | | | | | |
| Output high-level voltage | $V_{OH}$ (4) | $I_{OH}$ = –20 µA | Seg 1 to 35 | $V_{DD}$ – 0.2 | | | V |
| Output low-level voltage | $V_{OL}$ (4) | $I_{OL}$ = 20 µA | | | | 0.2 | V |
| Output high-level voltage | $V_{OH}$ (5) | $I_{OH}$ = –100 µA | COM1 | $V_{DD}$ – 0.2 | | | V |
| Output low-level voltage | $V_{OL}$ (5) | $I_{OL}$ = 100 µA | | | | 0.2 | V |
| • 1/2 bias | | | | | | | |
| Output high-level voltage | $V_{OH}$ (4) | $I_{OH}$ = –20 µA | Seg 1 to 35 | $V_{DD}$ – 0.2 | | | V |
| Output low-level voltage | $V_{OL}$ (4) | $I_{OL}$ = 20 µA | | | | 0.2 | V |
| Output high-level voltage | $V_{OH}$ (6) | $I_{OH}$ = –100 µA | COM1 – 4 | $V_{DD}$ – 0.2 | | | V |
| Output middle-level voltage | $V_{OM}2$–1 | $I_{OH}$ = –100 µA<br>$I_{OL}$ = 100 µA | | $V_{DD}/2$ – 0.2 | | $V_{DD}/2$ + 0.2 | V |
| Output low-level voltage | $V_{OL}$ (6) | $I_{OL}$ = 100 µA | | | | 0.2 | V |
| • 1/3 bias | | | | | | | |
| Output high-level voltage | $V_{OH}$ (4) | $I_{OH}$ = –20 µA | Seg 1 to 35 | $V_{DD}$ – 0.2 | | | V |
| Output middle-level voltage | $V_{OM}$1–1 | $I_{OH}$ = –20 µA<br>$I_{OL}$ = 20 µA | | $2V_{DD}/3$ – 0.2 | | $2V_{DD}/3$ + 0.2 | V |
| | $V_{OM}$1–2 | | | $V_{DD}/3$ – 0.2 | | $V_{DD}/3$ + 0.2 | V |
| Output low-level voltage | $V_{OL}$ (4) | $I_{OL}$ = 20 µA | | | | 0.2 | V |
| Supply leakage current | $I_{LEK}$ (1) | $V_{DD}$ = 3.0 V | Ta = 25°C, STOP mode, Figure 3 | | 1.0 | | µA |
| Input leakage current | $I_{OFF}$ | $V_{DD}$ = 3.0 V | S1 – 4, K1 – 4, P1 – 4, M1 – 4, SO1 – 4, A1 – 4, INT, RES (K, P, M, SO and A ports in input mode, INT and RES pin open specifications) | | | | |
| | | $V_{IN} = V_{DD}$ | | | | 1.0 | µA |
| | | $V_{IN} = V_{SS}$ | | –1.0 | | | µA |
| Output voltage 1 | $V_{DD}$1–(1) | $V_{DD}$ = 3.0 V, C1 = C2 = 0.1 µF 1/2 bias, fopg = 32.768 kHz, Figure 4 | $V_{DD}1 = V0$ | | 1.5 | | V |
| Output voltage 2 | $V_{DD}$2–(1) | $V_{DD}$ = 3.0 V, C1 = C2 = 0.1 µF 1/3 bias, fopg = 32.768 kHz, Figure 4 | $V_{DD}1 = V0$<br>$V_{DD}2 = V0$ | | 2.0 | | V |
| | $V_{DD}$2–(2) | | | | 1.0 | | V |
| Supply current 1 | $\|I_{DD}\|$ 1 | $V_{DD}$ = 3.0 V | Ta = 25°C, Crystal oscillator specifications, Crystal: 32 kHz, Cg = 20 pF, CI = 25 kΩ Halt mode, LCD at 1/3 bias, Figure 6 | | 5.0 | | µA |
| Supply current 2 | $\|I_{DD}\|$ 2 | $V_{DD}$ = 3.0 V | Ta = 25°C, Crystal oscillator specifications, Crystal: 38 kHz or 65 kHz, Cg = 10 pF, CI = 25 kΩ, Halt mode, LCD at 1/3 bias, Figure 6 | | 10.0 | | µA |
| Supply current 3 | $\|I_{DD}\|$ 3 | $V_{DD}$ = 3.0 V | Ta = 25°C, CF oscillator specifications, CF: 400 kHz, Ccg = Ccd = 330 pF Halt mode, LCD at 1/3 bias, Figure 8 | | 150 | | µA |
| Supply current 4 | $\|I_{DD}\|$ 4 | $V_{DD}$ = 3.0 V | Ta = 25°C, CF oscillator specifications, CF: 1 MHz, Ccg = Ccd = 100 pF, Halt mode, LCD at 1/3 bias, Figure 8 | | 200 | | µA |

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| Parameter | Symbol | Conditions/Pin | | Ratings min | Ratings typ | Ratings max | Unit |
|---|---|---|---|---|---|---|---|
| Oscillator start time | \| TSTT \| | $V_{DD}$ = 2.8 V | Crystal oscillator specifications, with a 32 kHz crystal CI ≤ 25 kΩ, Cg = 20 pF | | | 5 | s |
| Oscillator stabilization degree | Δf | $V_{DD}$ = 2.95 to 3.05 V | Figure 6 | | | 3 | ppm |
| Oscillator start time | \| TSTT \| | $V_{DD}$ = 2.8 V | Crystal oscillator specifications, with a 38 or 65 kHz crystal XCg = 10 pF, CI ≤ 25 kΩ Figure 6 | | | 5 | s |
| Oscillator start time | \| TSTT \| | $V_{DD}$ = 2.8 V | CF oscillator specifications, with a 400 kHz CF used Ccg = Ccd = 330 pF, Figure 7 | | | 30 | ms |
| Oscillator start time | \| TSTT \| | $V_{DD}$ = 2.8 V | CF oscillator specifications, with an 800 kHz CF used Ccg = Ccd = 220 pF or 100 pF Figure 7 | | | 30 | ms |
| Oscillator compensation capacitance | Cd | $V_{DD}$ = 3.0 V | XTOUT pin (built-in) | | 20 | | pF |

## Electrical Characteristics at $V_{DD}$ = 4.5 to 5.5 V, $V_{SS}$ = 0 V, Ta = 25°C

| Parameter | Symbol | Conditions/Pin | | Ratings min | Ratings typ | Ratings max | Unit |
|---|---|---|---|---|---|---|---|
| Input resistance | $R_{IN}$1 A | VIN = 0.2 $V_{DD}$, Low-level hold transistor *, Figure 2 | | 30 | 120 | 500 | kΩ |
| | $R_{IN}$1 B | VIN = $V_{DD}$, Pull-down resistor *, Figure 2 | | 10 | 50 | 200 | kΩ |
| | $R_{IN}$1 C | VIN = 0.8 $V_{DD}$, High-level hold transistor *, Figure 2 | | 30 | 120 | 500 | kΩ |
| | $R_{IN}$1 D | VIN = $V_{SS}$, Pull-up resistor *, Figure 2 | | 10 | 50 | 200 | kΩ |
| | $R_{IN}$2 A | VIN = 0.2 $V_{DD}$, INT low-level hold transistor | | 30 | 120 | 500 | kΩ |
| | $R_{IN}$2 B | VIN = $V_{DD}$, INT pull-down resistor | | 100 | 500 | 2000 | kΩ |
| | $R_{IN}$2 C | VIN = 0.8 $V_{DD}$, INT high-level hold transistor | | 30 | 120 | 500 | kΩ |
| | $R_{IN}$2 D | VIN = $V_{SS}$, INT pull-up resistor | | 100 | 500 | 2000 | kΩ |
| | $R_{IN}$3 | VIN = $V_{DD}$, With a pull-down resistor on the TST pin | | 20 | 70 | 300 | kΩ |
| Output low-level voltage | $V_{OL}$ (1) | IOL = 10.0 mA | N1 – 4 | | | 0.5 | V |
| Output high-level voltage | $V_{OH}$ (2) | IOH = –1.0 mA | K1 – 4, P1 – 4, M1 – 4, SO1 – 4, A1 – 4 (K, P, M, SO and A ports in output mode) | $V_{DD}$ – 0.5 | $V_{DD}$ – 0.2 | | V |
| Output low-level voltage | $V_{OL}$ (2) | IOL = 2.0 mA | | | 0.2 | 0.5 | V |
| Output off leakage current | \| $I_{OFF}$ \| | VOH = 10.5 V | N1 – 4, Figure 10 | | | 1.0 | μA |
| Segment port output impedance • When CMOS output ports are used | | | | | | | |
| Output high-level voltage | $V_{OH}$ (3) | IOH = –500 μA | Seg 1 to 35 | $V_{DD}$ – 0.5 | $V_{DD}$ – 0.2 | | V |
| Output low-level voltage | $V_{OL}$ (3) | IOL = 500 μA | | | | 0.5 | V |
| • When p-channel open drain output ports are used (See Figure 11.) | | | | | | | |
| Output high-level voltage | $V_{OH}$ (4) | IOH = –500 μA | Seg 1 to 35 | $V_{DD}$ – 0.5 | $V_{DD}$ – 0.2 | | V |
| Output off leakage current | \| $I_{OFF}$ \| | VOL = $V_{SS}$ | | | | 1.0 | μA |
| • When n-channel open-drain output ports are used (See Figure 11.) | | | | | | | |
| Output low-level voltage | $V_{OL}$ (4) | IOL = 500 μA | Seg 1 to 35 | | 0.2 | 0.5 | V |
| Output off leakage current | \| $I_{OFF}$ \| | VOH = $V_{DD}$ | | | | 1.0 | μA |
| • Static drive | | | | | | | |
| Output high-level voltage | $V_{OH}$ (4) | IOH = –40 μA | Seg 1 to 35 | $V_{DD}$ – 0.2 | | | V |
| Output low-level voltage | $V_{OL}$ (4) | IOL = 40 μA | | | | 0.2 | V |
| Output high-level voltage | $V_{OH}$ (6) | IOH = –400 μA | COM1 | $V_{DD}$ – 0.2 | | | V |
| Output low-level voltage | $V_{OL}$ (6) | IOL = 400 μA | | | | 0.2 | V |

Note: * The 24 pins S1 to S4, K1 to K4, P1 to P4, M1 to M4, SO1 to SO4 and A1 to A4.

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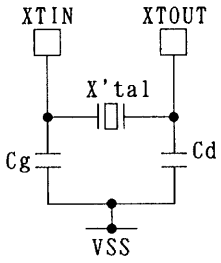
| Parameter | Symbol | Conditions/Pin | | Ratings min | Ratings typ | Ratings max | Unit |
|---|---|---|---|---|---|---|---|
| • 1/2 bias | | | | | | | |
| Output high-level voltage | $V_{OH}$ (4) | $I_{OH}$ = –40 µA | Seg 1 to 35 | $V_{DD}$ – 0.2 | | | V |
| Output low-level voltage | $V_{OL}$ (4) | $I_{OL}$ = 40 µA | | | | 0.2 | V |
| Output high-level voltage | $V_{OH}$ (6) | $I_{OH}$ = –400 µA | COM1 – 4 | $V_{DD}$ – 0.2 | | | V |
| Output middle-level voltage | $V_{OM}2$–1 | $I_{OH}$ = –400 µA<br>$I_{OL}$ = 400 µA | | $V_{DD}/2$ – 0.2 | | $V_{DD}/2$ + 0.2 | V |
| Output low-level voltage | $V_{OL}$ (6) | $I_{OL}$ = 400 µA | | | | 0.2 | V |
| • 1/3 bias | | | | | | | |
| Output high-level voltage | $V_{OH}$ (4) | $I_{OH}$ = –40 µA | Seg 1 to 35 | $V_{DD}$ – 0.2 | | | V |
| Output middle-level voltage | $V_{OM}1$–1 | $I_{OH}$ = –40 µA | | $2V_{DD}/3$ – 0.2 | | $2V_{DD}/3$ + 0.2 | V |
| | $V_{OM}1$–2 | $I_{OL}$ = 40 µA | | $V_{DD}/3$ – 0.2 | | $V_{DD}/3$ + 0.2 | V |
| Output low-level voltage | $V_{OL}$ (4) | $I_{OL}$ = 40 µA | | | | 0.2 | V |
| Output high-level voltage | $V_{OH}$ (6) | $I_{OH}$ = –400 µA | COM1 – 4 | $V_{DD}$ – 0.2 | | | V |
| Output middle-level voltage | $V_{OM}2$–1 | $I_{OH}$ = –400 µA | | $2V_{DD}/3$ – 0.2 | | $2V_{DD}/3$ + 0.2 | V |
| | $V_{OM}2$–2 | $I_{OL}$ = 400 µA | | $V_{DD}/3$ – 0.2 | | $V_{DD}/3$ + 0.2 | V |
| Output low-level voltage | $V_{OL}$ (6) | $I_{OL}$ = 400 µA | | | | 0.2 | V |
| Supply leakage current | $I_{LEK}$ (1) | $V_{DD}$ = 5.5 V | Ta = 25°C, Stop mode, Figure 3 | | 1.0 | | µA |
| Input leakage current | $I_{OFF}$ | $V_{DD}$ = 5.5 V | S1 – 4, K1 – 4, M1 – 4, SO1 – 4, A1 – 4, INT, RES (K, P, M, SO and A ports in input mode, INT and RES pin open specifications) | | | | |
| | | $V_{IN}$ = $V_{DD}$ | | | | 1.0 | µA |
| | | $V_{IN}$ = $V_{SS}$ | | –1.0 | | | µA |
| Output voltage 1 | $V_{DD}1$–(1) | $V_{DD}$ = 5.0 V, C1 = C2 = 0.1 µF, 1/2 bias, fopg = 32.768 kHz | $V_{DD}1$ = V0 Figure 4 | | 2.5 | | V |
| Output voltage 2 | $V_{DD}2$–(1) | $V_{DD}$ = 5.0 V, C1 = C2 = 0.1 µF, 1/3 bias, fopg = 32.768 kHz | $V_{DD}1$ = V0<br>$V_{DD}2$ = V0<br>Figure 4 | | 3.33 | | V |
| | $V_{DD}2$–(2) | | | | 1.67 | | V |
| Supply current 1 | \| $I_{DD}$ \| 1 | $V_{DD}$ = 5.0 V | Ta = 25°C, Crystal oscillator specifications, Crystal: 32 kHz, Cg = 20 pF, CI = 25 kΩ Halt mode, LCD at 1/3 bias, Figure 6 | | 20 | | µA |
| Supply current 2 | \| $I_{DD}$ \| 2 | $V_{DD}$ = 5.0 V | Ta = 25°C, Crystal oscillator specifications, Crystal: 38 kHz or 65 kHz, Cg = 10 pF, CI = 25 kΩ, Halt mode, LCD at 1/3 bias, Figure 6 | | 30 | | µA |
| Supply current 3 | \| $I_{DD}$ \| 3 | $V_{DD}$ = 5.0 V | Ta = 25°C, CF oscillator specifications, CF: 400 kHz, Ccg = Ccd = 330 pF Halt mode, LCD at 1/3 bias, Figure 7 | | 400 | | µA |
| Supply current 4 | \| $I_{DD}$ \| 4 | $V_{DD}$ = 5.0 V | Ta = 25°C, CF oscillator specifications, CF: 1 MHz, Ccg = Ccd = 100 pF, Halt mode, LCD at 1/3 bias, Figure 8 | | 450 | | µA |
| Supply current 5 | \| $I_{DD}$ \| 5-1 | $V_{DD}$ = 5.0 V | Ta = 25°C, CF oscillator specifications, CF: 2 MHZ, Ccg = Ccd = 33 pF, Halt mode, LCD at 1/3 bias, Figure 8 | | 500 | | µA |
| Supply current 6 | \| $I_{DD}$ \| 6-1 | $V_{DD}$ = 5.0 V | Ta = 25°C, CF oscillator specifications, CF: 4 MHz, Ccg = Ccd = 33 pF, Halt mode, LCD at 1/3 bias, Figure 8 | | 700 | | µA |
| Oscillator compensation capacitance | Cd | $V_{DD}$ = 5.0 V | XTOUT pin (built-in) | | 20 | | pF |




Xtal
32 k: 32.768 kHz
65 k: 65.536 kHz
38 k: 38.2293 kHz

**Figure 1-(1) Specified Oscillator Circuit (XT pin)**

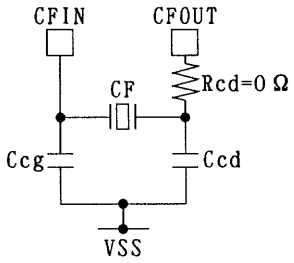



**Figure 1-(2) Specified Oscillator Circuit (CF pin)**

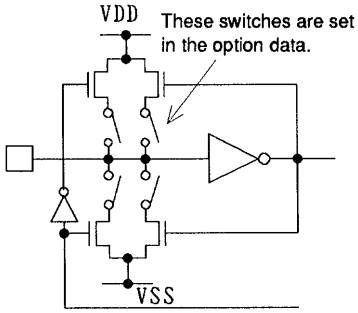
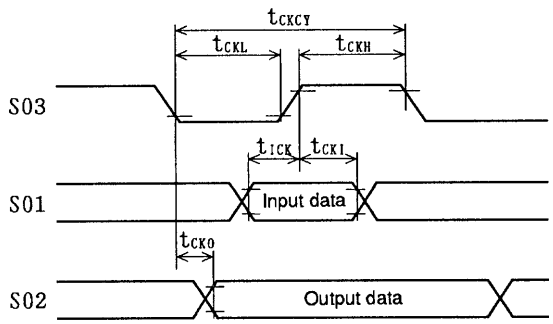



**Figure 2 S, K, P, M, SO and A Port Input Circuit**

## (Reference)
## Recommended Ceramic Resonators for Mask ROM Versions

| Manufacturer | Murata Mfg. Co., Ltd. | | | Kyocera Corporation | | |
|---|---|---|---|---|---|---|
| Item / Frequency | Type No. | Ccg (pF) | Ccd (pF) | Type No. | Ccg (pF) | Ccd (pF) |
| 400 kHz | CSB400P | 330 | 330 | KBR-400B | 330 | 330 |
| 800 kHZ | CSB800J | 220 | 220 | KBR-800H | 100 | 100 |
| 1 MHz | CSB1000J | 220 | 220 | KBR-1000H | 100 | 100 |
| 2 MHz | CSA2.00MG, CST2.00MG | 33 | 33 | KBR-2.00MS | 33 | 33 |
| 4 MHz | CSA4.00MG, CST4.00MG | 33 | 33 | KBR-4.00MS | 33 | 33 |




$t_{CKCY}$ ····· 5 μs MIN
$t_{CKL}$=$t_{CKH}$ ····· 2.4 μs MIN
$t_{ICK}$ ····· 1 μs MIN
$t_{CKI}$ ····· 1 μs MIN
$t_{CKO}$ ····· 1 μs MAX
VDD=3.0 to 5.5V

**Figure 13 Serial I/O Timing (in external clock mode)**

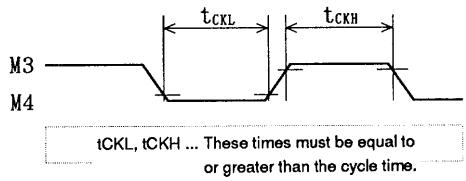



**Figure 14 Timer 2 External Clock Input Timing (in external clock mode: pin M4)**

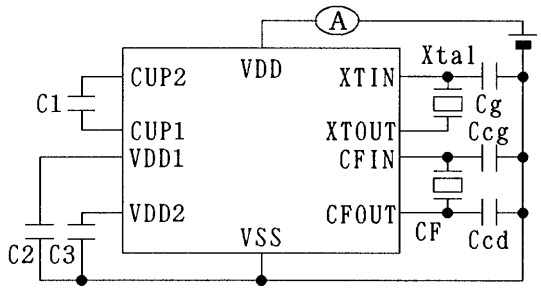



**Figure 3 Supply Leakage Current Test Circuit**

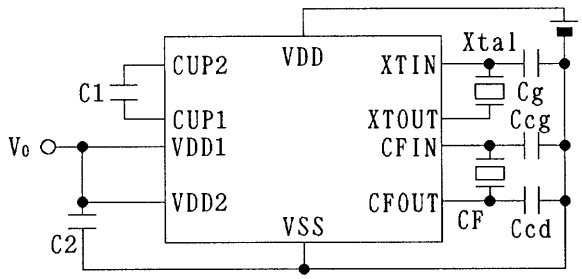
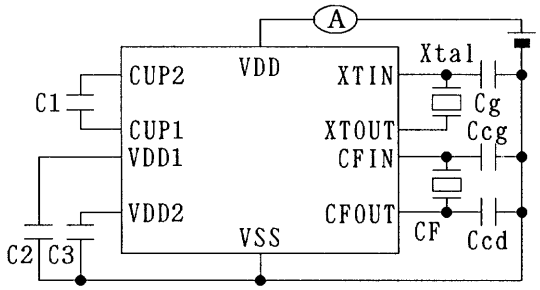
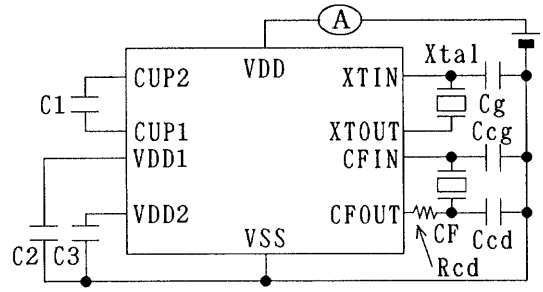



**Figure 4 Output Voltage Test Circuit**




Note: With the CF oscillator stopped
With a 32, 38, or 65 kHz crystal
C1, C2, C3: 0.1 µF

**Figure 6: Supply Current Test Circuit**




Note: The crystal is in the oscillator stopped state

**Figure 8 Supply Current Test Circuit**

Figure 3
- In the stop state
- With the S-port input resistors on
- With the I/O ports in output mode with high-level data values
- With the INT pin built-in resistor connected and in the open state
- With an external pull-down resistor on the RES pin
- The LCD-port values do not include the external component currents.
- With a crystal frequency between 32 and 65 kHz
- With CF between 200 kHz and 4 MHz

Figures 4 and 5
- With a crystal frequency of 32 kHz
- C1, C2, and C3 are 0.1 µF capacitors.
- With the LCD ports open
- With CD between 200 kHz and 4 MHz

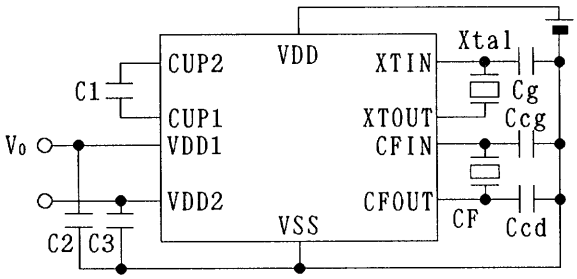



**Figure 5 Output Voltage Test Circuit**

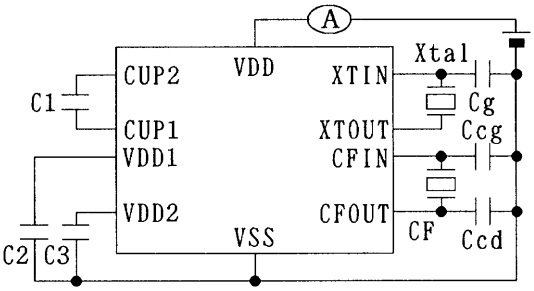



**Figure 7: Supply Current Test Circuit**

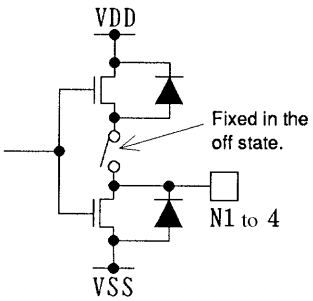



**Figure 10 Pin N1 to Pin N4 Circuits**

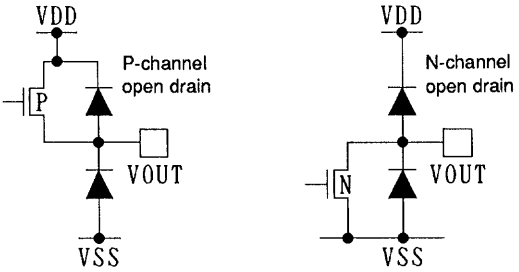



**Figure 11: Segment Pin Open-Drain Circuits**