Ordering number: EN 3410C

CMOS LSI

No. 3410C

LC58E68

4-bit Microprocessor with Built-in EPROM and LCD Drivers

Overview

The LC58E68 is a 4-bit microprocessor with built-in 16 Kbytes of EPROM, 1 Kbit of RAM and LCD drivers. It can perform most of the functions of the LC586X series single-chip microprocessors, making it ideal for prototyping systems based on these devices.

The LC58E68 features an additional 224 bytes of EPROM containing the configuration option data. Configuration options include input and output configurations and oscillator selection. Input configuration options are LOW-level hold transistor, HIGH-level hold transistor and no hold transistor enabled, and pull-up and pull-down input transistors. Output configuration options are LCD driver and CMOS, p-channel open-drain and n-channel open-drain general-purpose outputs. The oscillator options are ceramic filter, crystal, and both ceramic filter and crystal.

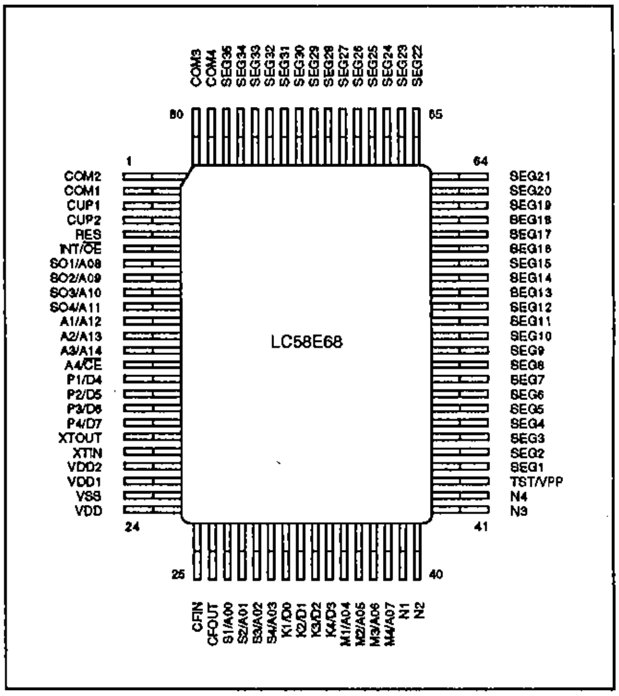
The LC58E68's UV-erasable EPROM can be reprogrammed using a general-purpose PROM programmer and an adapter board.

The LC58E68 operates from a 3 or 5 V supply and is available in 80-pin QIPs.

Features

- Compatible with the LC586X series mask ROM devices
- 16-Kbyte program EPROM
- 224-byte configuration EPROM
- 1-Kbit RAM
- LCD drivers
- 3 or 5 V supply
- 80-pin QIP

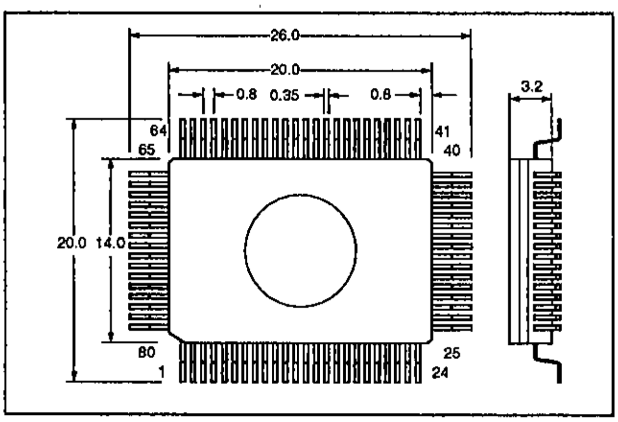
Pin Assignment



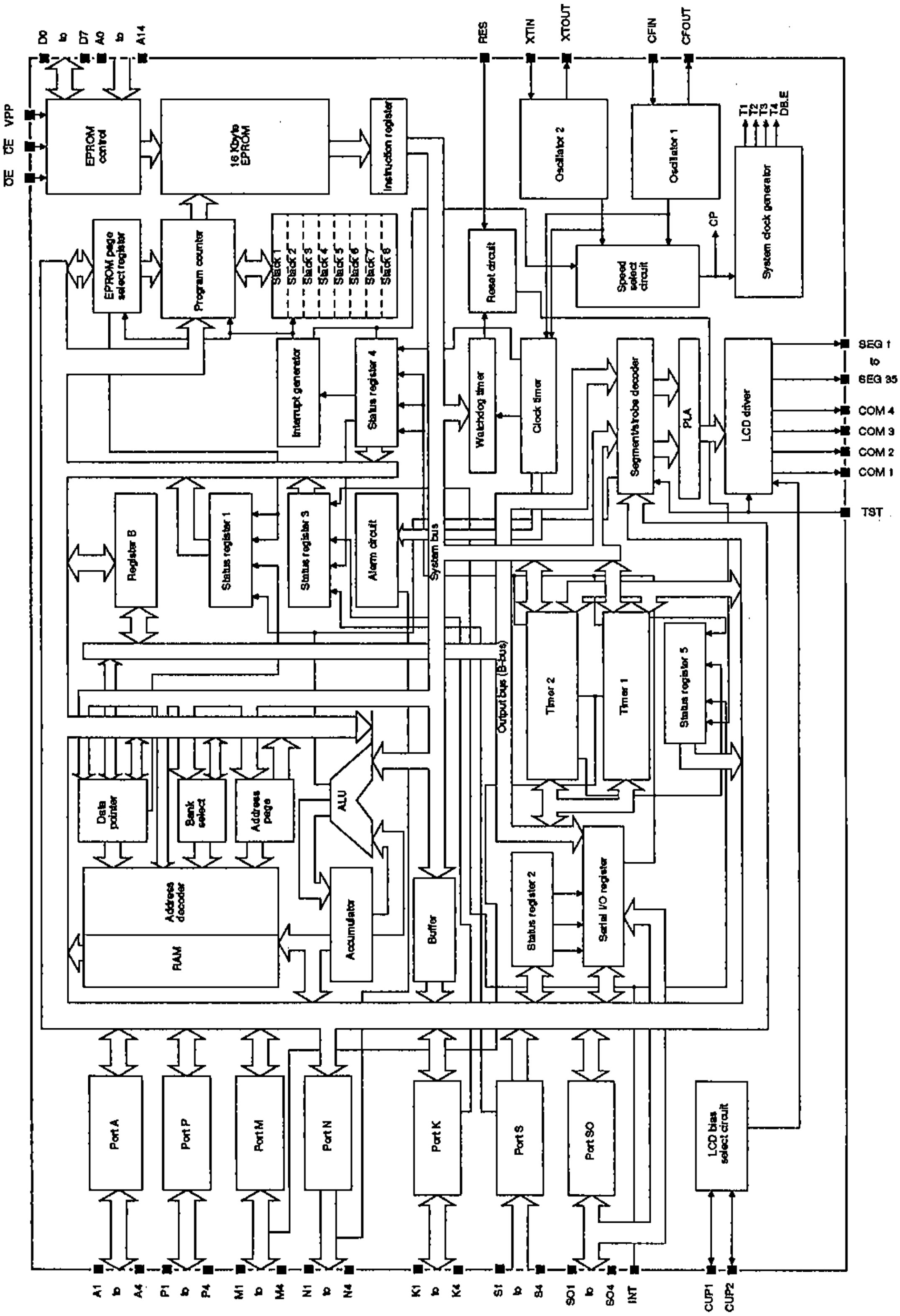
Package Dimensions

Unit: mm

3152A-QFC80C



Block Diagram



Pin Functions

Number	Name	Function
1	COM2	LCD common outputs
2	COM1	
3	CUP1	LCD drive bias circuit capacitor connections
4	CUP2	
5	RES	Active-HIGH reset input
6	INT/$\overline{OE}$	Multiplexed interrupt request (INT) and EPROM output enable ($\overline{OE}$) input
7	SO1/A08	Multiplexed 4-bit input/output port SO (SO1 to SO4), serial port (SO1 to SO3) and EPROM address inputs (A08 to A11)
8	SO2/A09	
9	SO3/A10	
10	SO4/A11	
11	A1/A12	Multiplexed 4-bit input/output port A (A1 to A4), EPROM address inputs (A12 to A14) and chip enable input ($\overline{CE}$)
12	A2/A13	
13	A3/A14	
14	A4/$\overline{CE}$	
15	P1/D4	Multiplexed 4-bit input/output port P (P1 to P4) and EPROM data bus lines (D4 to D7)
16	P2/D5	
17	P3/D6	
18	P4/D7	
19	XTOUT	Crystal oscillator connections
20	XTIN	
21	VDD2	LCD drive bias supply capacitor connections
22	VDD1	
23	VSS	Ground
24	VDD	Voltage supply
25	CFIN	Ceramic filter oscillator connections
26	CFOUT	
27	S1/A00	Multiplexed 4-bit input port S (S1 to S4) and EPROM address inputs (A00 to A03)
28	S2/A01	
29	S3/A02	
30	S4/A03	
31	K1/D0	Multiplexed 4-bit input/output port K (K1 to K4) and EPROM data bus lines (D0 to D3)
32	K2/D1	
33	K3/D2	
34	K4/D3	

Number	Name	Function
35	M1/A04	Multiplexed 4-bit input/output port M (M1 to M4), EPROM address inputs (A04 to A07) and timer 1 and 2 external clock inputs (M3 and M4)
36	M2/A05	
37	M3/A06	
38	M4/A07	
39	N1	Multiplexed 4-bit, open-drain output port N (N1 to N4) and alarm signal output (N4)
40	N2	
41	N3	
42	N4	
43	TST/VPP	Multiplexed test input (TST) and EPROM V_{PP} supply (VPP)
44 to 78	SEG1 to SEG35	LCD segment drivers or general-purpose outputs
79	COM4	LCD common outputs
80	COM3	

Specifications

Absolute Maximum Ratings

Parameter	Symbol	Ratings	Unit
Supply voltage range	V_{DD} max	–0.3 to +6.0	V
LCD supply voltage 1 range	V_{DD1}	–0.3 to V_{DD}	V
LCD supply voltage 2 range	V_{DD2}	–0.3 to V_{DD}	V
XTIN and CFIN input voltage range	V_{I1}	0 to maximum generated voltage	V
Ports S, K, P, SO and A, and RES, INT and TST input voltage range	V_{I2}	–0.3 to V_{DD} + 0.3	V
XTOUT and CFOUT output voltage range	V_{O1}	0 to maximum generated voltage	V
Ports K, P, SO and A, and CUP1, CUP2, SEG1 to SEG 35 and COM1 to COM4 output voltage range	V_{O2}	–0.3 to V_{DD} + 0.3	V
Port N open-drain output voltage range	V_{O3}	–0.3 to +13	V
Port N output current range	I_{O1}	–10 to +15	mA
Ports K, P, M, SO and A output current range	I_{O2}	–5 to +5	mA
Ports K, P, M, SO, A and N, and SEG1 to SEG 35 total output current range	ΣI_O	–70 to 70	mA
Power dissipation	P_D	500	mW
Operating temperature range	Topr	10 to 40	°C
Storage temperature range	T_{stg}	–55 to +125	°C

Allowable Operating Ranges

T_a = 25 °C

Parameter	Symbol	Ratings	Unit
Supply voltage range with LCD disabled. See note 1.	V_{DD}	2.8 to 5.5	V
Supply voltage range with static bias. See note 1.	V_{DD}	2.8 to 5.5	V
Supply voltage range with ½-bias. See note 2.	V_{DD}	2.8 to 5.5	V
Supply voltage range with ⅓-bias. See note 3.	V_{DD}	2.8 to 5.5	V
Minimum data retention voltage. See note 4.	V_{DR}	2.8 to V_{DD}	V

Notes

1. $V_{DD1} = V_{DD2} = V_{DD}$
2. $V_{DD1} = V_{DD2} \approx 1/2 \times V_{DD}$
3. $V_{DD1} \approx 2/3 \times V_{DD}$, $V_{DD2} \approx 1/3 \times V_{DD}$
4. Oscillator and all internal circuits halted

Electrical Characteristics

V_{DD} = 2.8 to 3.2 V

T_a = 25 °C

Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
LCD supply voltage 1	V_{DD1}	V_{DD} = 3 V, C1 = C2 = 0.1 μF, ½-bias, f_{xtal} = 32.768 kHz. See figure 2.	–	1.5	–	V
		V_{DD} = 3 V, C1 = C2 = 0.1 μF, ⅓-bias, f_{xtal} = 32.768 kHz. See figure 3.	–	1.0	–	
LCD supply voltage 2	V_{DD2}	V_{DD} = 3 V, C1 = C2 = 0.1 μF, ⅓-bias, f_{xtal} = 32.768 kHz. See figure 3.	–	2.0	–	V
Supply current	I_{DD}	V_{DD} = 3 V, f_{xtal} = 32 kHz, C_g = 20 pF, Z_c = 25 kΩ, halt mode, ⅓-bias. See figure 4.	–	5	–	μA
		V_{DD} = 3 V, f_{xtal} = 38 or 65 kHz, C_g = 10 pF, Z_c = 25 kΩ, halt mode, ⅓-bias. See figure 4.	–	10	–	
		V_{DD} = 3 V, f_{cer} = 400 kHz, C_{cg} = C_{cd} = 330 pF, halt mode. See figure 5.	–	150	–	

Parameter	Symbol	Conditions	Ratings min	Ratings typ	Ratings max	Unit
Supply current	I_{DD}	V_{DD} = 3 V, f_{osc} = 1 MHz, C_{cg} = C_{cd} = 100 pF, halt mode. See figure 6.	–	200	–	µA
Supply leakage current	I_{DD}	V_{DD} = 3 V, standby mode. See figure 1.	–	1	–	µA
Ports S, K, P, M, SO and A, and INT LOW-level input voltage	V_{IL1}		0	–	$0.3V_{DD}$	V
Ports S, K, P, M, SO and A, and INT HIGH-level input voltage	V_{IH1}		$0.7V_{DD}$	–	V_{DD}	V
RES and CFIN LOW-level input voltage	V_{IL2}		0	–	$0.25V_{DD}$	V
RES and CFIN HIGH-level input voltage	V_{IH2}		$0.75V_{DD}$	–	V_{DD}	V
Ports K, P, M, SO and A LOW-level output voltage	V_{OL2}	I_{OL} = 400 µA	–	0.2	0.5	V
Ports K, P, M, SO and A HIGH-level output voltage	V_{OH1}	I_{OH} = –400 µA	V_{DD} – 0.5	V_{DD} – 0.2	–	V
Ports S, K, M, SO and A, and INT input leakage current	I_{leak1}	V_{DD} = 3 V, V_I = V_{SS}	–1	–	–	µA
		V_{DD} = 3 V, V_I = V_{DD}	–	–	1	µA
Port N LOW-level output voltage	V_{OL1}	I_{OL} = 10 mA	–	–	0.5	V
Port N output leakage current	I_{leak2}	V_{OH} = 10.5 V	–	–	1	µA
SEG1 to SEG35 CMOS LOW-level output voltage	V_{OL3}	I_{OL} = 100 µA	–	–	0.5	V
SEG1 to SEG35 CMOS HIGH-level output voltage	V_{OH2}	I_{OH} = –100 µA	V_{DD} – 0.5	–	–	V
SEG1 to SEG35 p-channel HIGH-level output voltage	V_{OH3}	I_{OH} = –100 µA	V_{DD} – 0.5	–	–	V
SEG1 to SEG35 p-channel output leakage current	I_{leak3}	V_{OL} = 0 V	–	–	1	µA
SEG1 to SEG35 n-channel LOW-level output voltage	V_{OL4}	I_{OL} = 100 µA	–	–	0.5	V
SEG1 to SEG35 n-channel output leakage current	I_{leak4}	V_{OH} = V_{DD}	–	–	1	µA
Static-bias SEG1 to SEG35 LOW-level output voltage	V_{OL5}	I_{OL} = 20 µA	–	–	0.2	V
Static-bias SEG1 to SEG35 HIGH-level output voltage	V_{OH4}	I_{OH} = –20 µA	V_{DD} – 0.2	–	–	V
Static-bias COM1 LOW-level output voltage	V_{OL6}	I_{OL} = 100 µA	–	–	0.2	V
Static-bias COM1 HIGH-level output voltage	V_{OH5}	I_{OH} = –100 µA	V_{DD} – 0.2	–	–	V
½-bias SEG1 to SEG35 LOW-level output voltage	V_{OL7}	I_{OL} = 20 µA	–	–	0.2	V
½-bias SEG1 to SEG35 HIGH-level output voltage	V_{OH6}	I_{OH} = –20 µA	V_{DD} – 0.2	–	–	V

Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
½-bias COM1 to COM4 LOW-level output voltage	V_{OL8}	I_{OL} = 100 µA	–	–	0.2	V
½-bias COM1 to COM4 MID-level output voltage	V_{OM1}	I_{OL} = 100 µA or I_{OH} = –100 µA	(V_{DD} ÷ 2) – 0.2	–	(V_{DD} ÷ 2) + 0.2	V
½-bias COM1 to COM4 HIGH-level output voltage	V_{OH7}	I_{OH} = –100 µA	V_{DD} – 0.2	–	–	V
⅓-bias SEG1 to SEG35 LOW-level output voltage	V_{OL9}	I_{OL} = 20 µA	–	–	0.2	V
⅓-bias SEG1 to SEG35 MID-level output voltage	V_{OM2}	I_{OL} = 20 µA or I_{OH} = –20 µA	(V_{DD} ÷ 3) – 0.2	–	(V_{DD} ÷ 3) + 0.2	V
		I_{OL} = 20 µA or I_{OH} = –20 µA	(2V_{DD} ÷ 3) – 0.2	–	(2V_{DD} ÷ 3) + 0.2	V
⅓-bias SEG1 to SEG35 HIGH-level output voltage	V_{OH8}	I_{OH} = –20 µA	V_{DD} – 0.2	–	–	V
⅓-bias COM1 to COM4 LOW-level output voltage	V_{OL10}	I_{OL} = 100 µA	–	–	0.2	V
⅓-bias COM1 to COM4 MID-level output voltage	V_{OM3}	I_{OL} = 100 µA or I_{OH} = –100 µA	(V_{DD} ÷ 3) – 0.2	–	(V_{DD} ÷ 3) + 0.2	V
		I_{OL} = 100 µA or I_{OH} = –100 µA	(2V_{DD} ÷ 3) – 0.2	–	(2V_{DD} ÷ 3) + 0.2	V
⅓-bias COM1 to COM4 HIGH-level output voltage	V_{OH9}	I_{OH} = –100 µA	V_{DD} – 0.2	–	–	V
Ports S, K, P, M, SO and A LOW-level hold transistor input resistance	R_{IL1}	V_I = 0.2V_{DD}	60	300	1200	kΩ
Ports S, K, P, M, SO and A HIGH-level hold transistor input resistance	R_{IH1}	V_I = 0.8V_{DD}	60	300	1200	kΩ
Ports S, K, P, M, SO and A pull-up transistor input resistance	R_{PU1}	V_I = V_{SS}	30	150	500	kΩ
Ports S, K, P, M, SO and A pull-down transistor input resistance	R_{PD1}	V_I = V_{DD}	30	150	500	kΩ
INT LOW-level hold transistor input resistance	R_{IL2}	V_I = 0.2V_{DD}	60	300	1200	kΩ
INT HIGH-level hold transistor input resistance	R_{IH2}	V_I = 0.8V_{DD}	60	300	1200	kΩ
INT pull-up transistor resistance	R_{PU2}	V_I = V_{SS}	300	1500	5000	kΩ
INT pull-down transistor resistance	R_{PD2}	V_I = V_{DD}	300	1500	5000	kΩ
TST pull-down transistor resistance	R_{PD3}	V_I = V_{DD}	20	70	300	kΩ
XTOUT oscillation compensating capacitance	C_d	V_{DD} = 3 V	–	20	–	pF
Crystal oscillator operating frequency	f_{xtal}	32 kHz range	32	–	33	kHz
		38 kHz range	37	–	39	
		65 kHz range	60	–	70	
Ceramic filter oscillator operating frequency	f_{cer}		190	–	1200	kHz
Serial interface clock frequency	f_{ser}	Rise/fall time ≤ 10 µs	0	–	200	kHz

V_{DD} = 4.5 to 5.5 V

T_a = 25 °C

Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
LCD supply voltage 1	V_{DD1}	V_{DD} = 5 V, C1 = C2 = 0.1 µF, ½-bias, f_{xtal} = 32.768 kHz. See figure 2.	–	2.5	–	V
		V_{DD} = 5 V, C1 = C2 = 0.1 µF, ⅓-bias, f_{xtal} = 32.768 kHz. See figure 3.	–	1.67	–	
LCD supply voltage 2	V_{DD2}	V_{DD} = 5 V, C1 = C2 = 0.1 µF, ⅓-bias, f_{xtal} = 32.768 kHz. See figure 3.	–	3.33	–	V
Supply current	I_{DD}	V_{DD} = 5 V, f_{xtal} = 32 kHz, C_g = 20 pF, Z_c = 25 kΩ, halt mode, ⅓-bias. See figure 4.	–	20	–	µA
		V_{DD} = 5 V, f_{xtal} = 38 or 65 kHz, C_g = 10 pF, Z_c = 25 kΩ, halt mode, ⅓-bias. See figure 4.	–	30	–	
		V_{DD} = 5 V, f_{cer} = 400 kHz, C_{cg} = C_{cd} = 330 pF, halt mode. See figure 5.	–	400	–	
		V_{DD} = 5 V, f_{cer} = 1 MHz, C_{cg} = C_{cd} = 100 pF, halt mode. See figure 6.	–	450	–	
		V_{DD} = 5 V, f_{cer} = 2 MHz, C_{cg} = C_{cd} = 33 pF, halt mode. See figure 6.	–	500	–	
		V_{DD} = 5 V, f_{cer} = 4 MHz, C_{cg} = C_{cd} = 33 pF, halt mode. See figure 6.	–	700	–	
Supply leakage current	I_{DD}	V_{DD} = 5.5 V, standby mode. See figure 1.	–	1	–	µA
Ports S, K, P, M, SO and A, and INT. LOW-level input voltage	V_{IL1}		0	–	$0.3V_{DD}$	V

Parameter	Symbol	Conditions		Ratings			Unit
				min	typ	max	
Ports S, K, P, M, SO and A, and INT HIGH-level input voltage	V_{IH1}			$0.7V_{DD}$	–	V_{DD}	V
RES and CFIN LOW-level input voltage	V_{IL2}			0	–	$0.25V_{DD}$	V
RES and CFIN HIGH-level input voltage	V_{IH2}			$0.75V_{DD}$	–	V_{DD}	V
Ports K, P, M, SO and A LOW-level output voltage	V_{OL2}	I_{OL} = 2 mA		–	0.2	0.5	V
Ports K, P, M, SO and A HIGH-level output voltage	V_{OH1}	I_{OH} = –1 mA		V_{DD} – 0.5	V_{DD} – 0.2	–	V
Ports S, K, M, SO and A, and INT input leakage current	I_{leak1}	V_{DD} = 5.5 V	$V_I = V_{SS}$	–1	–	–	µA
			$V_I = V_{DD}$	–	–	1	
Port N LOW-level output voltage	V_{OL1}	I_{OL} = 10 mA		–	–	0.5	V
Port N output leakage current	I_{leak2}	V_{OH} = 10.5 V		–	–	1	µA
SEG1 to SEG35 CMOS LOW-level output voltage	V_{OL3}	I_{OL} = 250 µA		–	–	0.5	V
SEG1 to SEG35 CMOS HIGH-level output voltage	V_{OH2}	I_{OH} = –250 µA		V_{DD} – 0.5	–	–	V
SEG1 to SEG35 p-channel HIGH-level output voltage	V_{OH3}	I_{OH} = –250 µA		V_{DD} – 0.5	–	–	V
SEG1 to SEG35 p-channel output leakage current	I_{leak3}	V_{OL} = 0 V		–	–	1	µA
SEG1 to SEG35 n-channel LOW-level output voltage	V_{OL4}	I_{OL} = 250 µA		–	–	0.5	V
SEG1 to SEG35 n-channel output leakage current	I_{leak4}	$V_{OH} = V_{DD}$		–	–	1	µA
Static-bias SEG1 to SEG35 LOW-level output voltage	V_{OL5}	I_{OL} = 20 µA		–	–	0.2	V
Static-bias SEG1 to SEG35 HIGH-level output voltage	V_{OH4}	I_{OH} = –20 µA		V_{DD} – 0.2	–	–	V
Static-bias COM1 LOW-level output voltage	V_{OL6}	I_{OL} = 200 µA		–	–	0.2	V
Static-bias COM1 HIGH-level output voltage	V_{OH5}	I_{OH} = –200 µA		V_{DD} – 0.2	–	–	V
½-bias SEG1 to SEG35 LOW-level output voltage	V_{OL7}	I_{OL} = 20 µA		–	–	0.2	V
½-bias SEG1 to SEG35 HIGH-level output voltage	V_{OH6}	I_{OH} = –20 µA		V_{DD} – 0.2	–	–	V
½-bias COM1 to COM4 LOW-level output voltage	V_{OL8}	I_{OL} = 200 µA		–	–	0.2	V
½-bias COM1 to COM4 MID-level output voltage	V_{OM1}	I_{OL} = 200 µA or I_{OH} = –200 µA		(V_{DD} ÷ 2) – 0.2	–	(V_{DD} ÷ 2) + 0.2	V
½-bias COM1 to COM4 HIGH-level output voltage	V_{OH7}	I_{OH} = –200 µA		V_{DD} – 0.2	–	–	V

Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
1/3-bias SEG1 to SEG35 LOW-level output voltage	V_{OL9}	I_{OL} = 20 µA	–	–	0.2	V
1/3-bias SEG1 to SEG35 MID-level output voltage	V_{OM2}	I_{OL} = 20 µA or I_{OH} = –20 µA	(V_{DD} + 3) – 0.2	–	(V_{DD} + 3) + 0.2	V
		I_{OL} = 20 µA or I_{OH} = –20 µA	(2V_{DD} + 3) – 0.2	–	(2V_{DD} + 3) + 0.2	V
1/3-bias SEG1 to SEG35 HIGH-level output voltage	V_{OH8}	I_{OH} = –20 µA	V_{DD} – 0.2	–	–	V
1/3-bias COM1 to COM4 LOW-level output voltage	V_{OL10}	I_{OL} = 200 µA	–	–	0.2	V
1/3-bias COM1 to COM4 MID-level output voltage	V_{OM3}	I_{OL} = 200 µA or I_{OH} = –200 µA	(V_{DD} + 3) – 0.2	–	(V_{DD} + 3) + 0.2	V
		I_{OL} = 200 µA or I_{OH} = –200 µA	(2V_{DD} + 3) – 0.2	–	(2V_{DD} + 3) + 0.2	V
1/3-bias COM1 to COM4 HIGH-level output voltage	V_{OH9}	I_{OH} = –200 µA	V_{DD} – 0.2	–	–	V
Ports S, K, P, M, SO and A LOW-level hold transistor input resistance	R_{IL1}	V_I = 0.2V_{DD}	30	120	500	kΩ
Ports S, K, P, M, SO and A HIGH-level hold transistor input resistance	R_{IH1}	V_I = 0.8V_{DD}	30	120	500	kΩ
Ports S, K, P, M, SO and A pull-up transistor input resistance	R_{PU1}	V_I = V_{SS}	10	50	200	kΩ
Ports S, K, P, M, SO and A pull-down transistor input resistance	R_{PD1}	V_I = V_{DD}	10	50	200	kΩ
INT LOW-level hold transistor input resistance	R_{IL2}	V_I = 0.2V_{DD}	30	120	500	kΩ
INT HIGH-level hold transistor input resistance	R_{IH2}	V_I = 0.8V_{DD}	30	120	500	kΩ
INT pull-up transistor resistance	R_{PU2}	V_I = V_{SS}	100	500	2000	kΩ
INT pull-down transistor resistance	R_{PD2}	V_I = V_{DD}	100	500	2000	kΩ
TST pull-down transistor resistance	R_{PD3}	V_I = V_{DD}	20	70	300	kΩ
XTOUT oscillation compensating capacitance	C_d	V_{DD} = 5 V	–	20	–	pF
Crystal oscillator operating frequency	f_{xtal}	32 kHz range	32	–	33	kHz
		38 kHz range	37	–	39	
		65 kHz range	60	–	70	
Ceramic filter oscillator operating frequency	f_{cer}		190	–	1200	kHz
Serial interface clock frequency	f_{ser}	Rise/fall time ≤ 10 µs	0	–	200	kHz

Measurement Circuits

The following conditions apply to figure 1.

- Standby mode
- Port S input resistors enabled
- I/O ports in output mode, all outputs HIGH
- INT open and internal input transistors enabled
- External pull-down resistor connected to RES.
- Current flow through components connected to LCD ports is not included.
- f_{xtal} = 32 to 65 kHz
- f_{ccr} = 200 kHz to 4 MHz

The following conditions apply to figures 2 and 3.

- f_{xtal} = 32 kHz
- C1 = C2 = C3 = 0.1 μF
- LCD ports are open.
- f_{ccr} = 200 kHz to 4 MHz

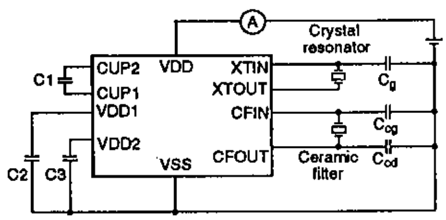


Figure 1. Supply leakage measurement

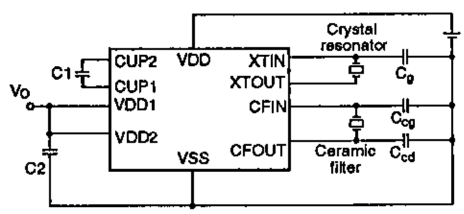


Figure 2. Output voltage measurement 1

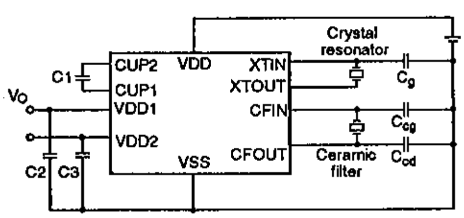


Figure 3. Output voltage measurement 2

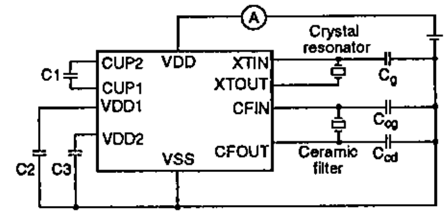


Figure 4. Supply current measurement 1

Notes

1. Ceramic filter oscillator stopped
2. f_{xtal} = 32, 38 or 65 kHz

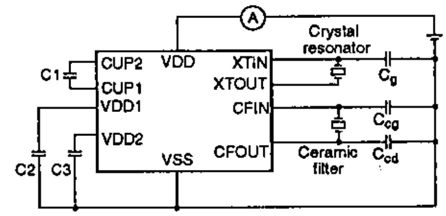


Figure 5. Supply current measurement 2

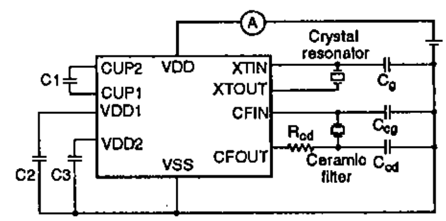
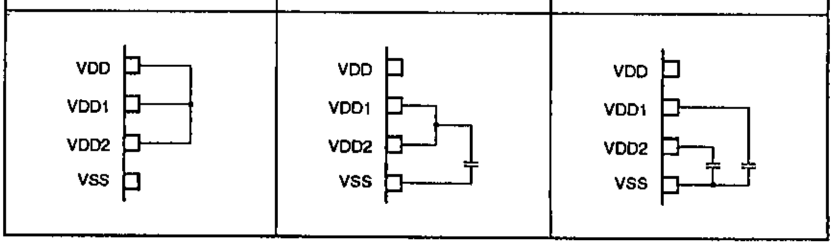


Figure 6. Supply current measurement 3

Note

Crystal oscillator stopped

Pin Functions

<table>
<tr><th>Name</th><th>Function</th></tr>
<tr><td>COM1</td><td rowspan="4">COM1 to COM4 function as LCD common driver outputs. The active outputs and frame frequency for each duty cycle are shown in the table below.
<table>
<tr><th>Duty cycle</th><th>COM1</th><th>COM2</th><th>COM3</th><th>COM4</th><th>Frame frequency (Hz)</th></tr>
<tr><td>Static</td><td>✓</td><td>–</td><td>–</td><td>–</td><td>32</td></tr>
<tr><td>1/2</td><td>✓</td><td>✓</td><td>–</td><td>–</td><td>32</td></tr>
<tr><td>1/3</td><td>✓</td><td>✓</td><td>✓</td><td>–</td><td>42.7</td></tr>
<tr><td>1/4</td><td>✓</td><td>✓</td><td>✓</td><td>✓</td><td>32</td></tr>
</table>
Note
ϕ_0 = 32.768 kHz</td></tr>
<tr><td>COM2</td></tr>
<tr><td>COM3</td></tr>
<tr><td>COM4</td></tr>
<tr><td>CUP1</td><td rowspan="2">CUP1 and CUP2 are part of the LCD-drive voltage divider circuit. When using 1/2- or 1/3-bias, connect a bipolar capacitor between these pins, otherwise leave them open.</td></tr>
<tr><td>CUP2</td></tr>
<tr><td>RES</td><td>RES pulsewidths greater than 200 µs reset the microprocessor. RES requires an external input resistor.</td></tr>
<tr><td>INT/$\overline{OE}$</td><td>INT functions as the output enable input when the EPROM is addressed.</td></tr>
<tr><td>SO1/A08</td><td rowspan="4">Port SO functions as address bus inputs when the EPROM is addressed. SO1 also functions as the serial data input, SO2 as the serial data output and SO3 as the serial data clock input or output. Clock direction and polarity are determined by software.</td></tr>
<tr><td>SO2/A09</td></tr>
<tr><td>SO3/A10</td></tr>
<tr><td>SO4/A11</td></tr>
<tr><td>A1/A12</td><td rowspan="4">Port A functions as address bus inputs and the chip enable input when the EPROM is addressed.</td></tr>
<tr><td>A2/A13</td></tr>
<tr><td>A3/A14</td></tr>
<tr><td>A4/$\overline{CE}$</td></tr>
<tr><td>P1/D4</td><td rowspan="4">Port P functions as data bus lines when the EPROM is addressed.</td></tr>
<tr><td>P2/D5</td></tr>
<tr><td>P3/D6</td></tr>
<tr><td>P4/D7</td></tr>
<tr><td>XTIN</td><td rowspan="2">XTIN and XTOUT function as the crystal oscillator connections, otherwise they are left open. The crystal frequency is a configuration option. The oscillator halts after a HOLD instruction.</td></tr>
<tr><td>XTOUT</td></tr>
<tr><td>VDD1</td><td rowspan="2">VDD1 and VDD2 function as LCD drive bias circuit capacitor connections. For each bias drive, connect these pins as shown below.
<table>
<tr><th>Static bias</th><th>1/2-bias</th><th>1/3-bias</th></tr>
</table>

</td></tr>
<tr><td>VDD2</td></tr>
<tr><td>CFIN</td><td rowspan="2">CFIN and CFOUT function as the ceramic filter connections, otherwise they are left open. The oscillator halts after a HOLD or SLOW instruction.</td></tr>
<tr><td>CFOUT</td></tr>
</table>

Name	Function
S1/A00	Port S functions as address bus inputs when the EPROM is addressed. Port S pins have internal key-debounce circuits. The 1.95 or 7.8 ms (at ϕ_0 = 32.768 kHz) debounce delay period is selected by software.
S2/A01	
S3/A02	
S4/A03	
K1/D0	Port K functions as data bus lines when the EPROM is addressed. Port K pins have internal input key-debounce circuits. The delay period is the same as the port S debounce delay.
K2/D1	
K3/D2	
K4/D3	
M1/A04	Port M functions as address bus inputs when the EPROM is addressed. M3 also functions as timer 1, and M4 as timer 2 external clock inputs when the timers are in mode 3. The minimum external clock period is double the cycle time.
M2/A05	
M3/A06	
M4/A07	
N1	N4 functions as the 1, 2, or 4 kHz (at ϕ_0 = 32.768 kHz) alarm signal output (when the N4 output latch is LOW).
N2	
N3	
N4	
TST/VPP	TST functions as the VPP input when the EPROM is addressed. It is normally connected to ground.
SEG1 to SEG35	SEG1 to SEG35 function as LCD segment drivers or general-purpose outputs. The function of individual outputs are set as configuration options.

Configuration Options

Oscillator

The oscillator options are ceramic filter, crystal, and both ceramic filter and crystal. When the crystal oscillator is used, the oscillator frequency options are 32, 38 or 65 kHz. The ceramic filter and crystal oscillator options are shown in figures 7 and 8, respectively.

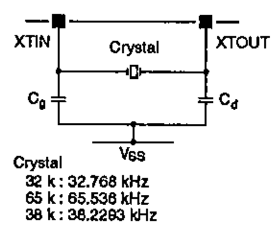


Figure 8. Crystal oscillator

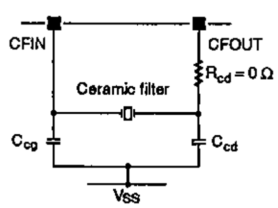


Figure 7. Ceramic filter oscillator

Input Ports

Ports S, K, P, SO and A input options are hold transistor and input transistor configurations as shown in figure 9. The hold transistor options are LOW-level hold transistor, HIGH-level hold transistor and no hold transistor enabled. The input options are pull-up and pull-down transistors enabled.

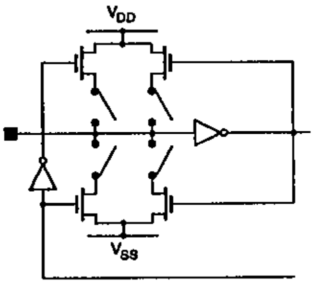


Figure 9. Ports S, K, P, SO and A input circuit

Note
Configuration data determines switch settings.

Outputs

SEG1 to SEG35

The SEG1 to SEG35 options are LCD driver or general-purpose outputs, LCD driver bias and duty configuration, general-purpose output configuration and output latch state in STOP mode. The LCD driver and general-purpose output function selection is hard coded in the PLA and, therefore, cannot be selected by software.

The LCD driver bias and duty configuration is set for all LCD drivers. The configuration options are as follows.

- Static
- 1/2-bias and 1/2-duty
- 1/2-bias and 1/3-duty
- 1/2-bias and 1/4-duty
- 1/3-bias and 1/3-duty
- 1/3-bias and 1/4-duty

The general-purpose output configuration is set for individual outputs. The options are CMOS, p-channel open-drain and n-channel open-drain. The p-channel and n-channel output equivalent circuits are shown in figures 10 and 11, respectively.

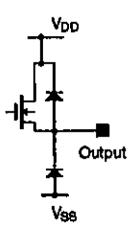


Figure 10. p-channel output

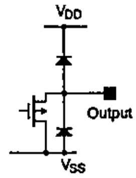


Figure 11. n-channel output

The output latch state of all LCD drivers and general-purpose outputs can be reset in standby mode. The options are reset and no change.

Port N

Port N outputs are n-channel open-drain as shown in figure 12.

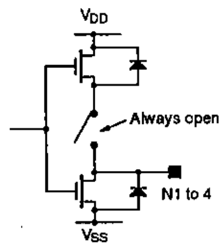


Figure 12. Port N open-drain outputs

Serial Data Clock

The SO3 clock divider ratio options are 1/1, 1/2 and 1/4.

Interrupt Request

The interrupt request input options are hold transistor, input transistor and interrupt request trigger configurations. The input hold transistor and input transistor options are the same as for the port inputs. The interrupt request trigger options are rising-edge and falling-edge triggering.

Design Information

Development Process

The LC5860 series software development tools, EC5868.EXE software and a general-purpose PROM programmer with a W58E68Q adapter board are required for LC58E68 program development. The development flowchart is shown in figure 13.

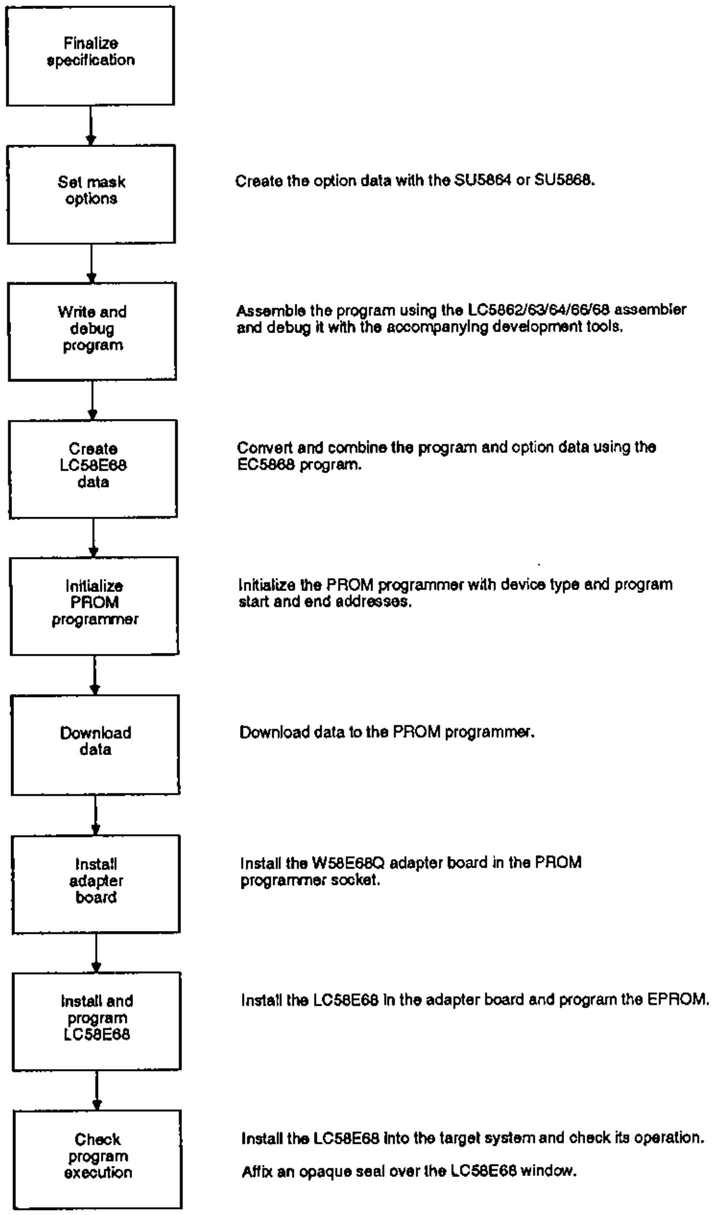


Figure 13. Development flowchart

LC586X series software development tools

These tools are used on an MS-DOS computer to create programs and option data. See the LC586X series development tools manual for further information.

EC5868.EXE

This program combines an LC586X series program with the configuration option data generated by the option data software and converts the result to LC58E68 EPROM downloading format as shown in figure 14.

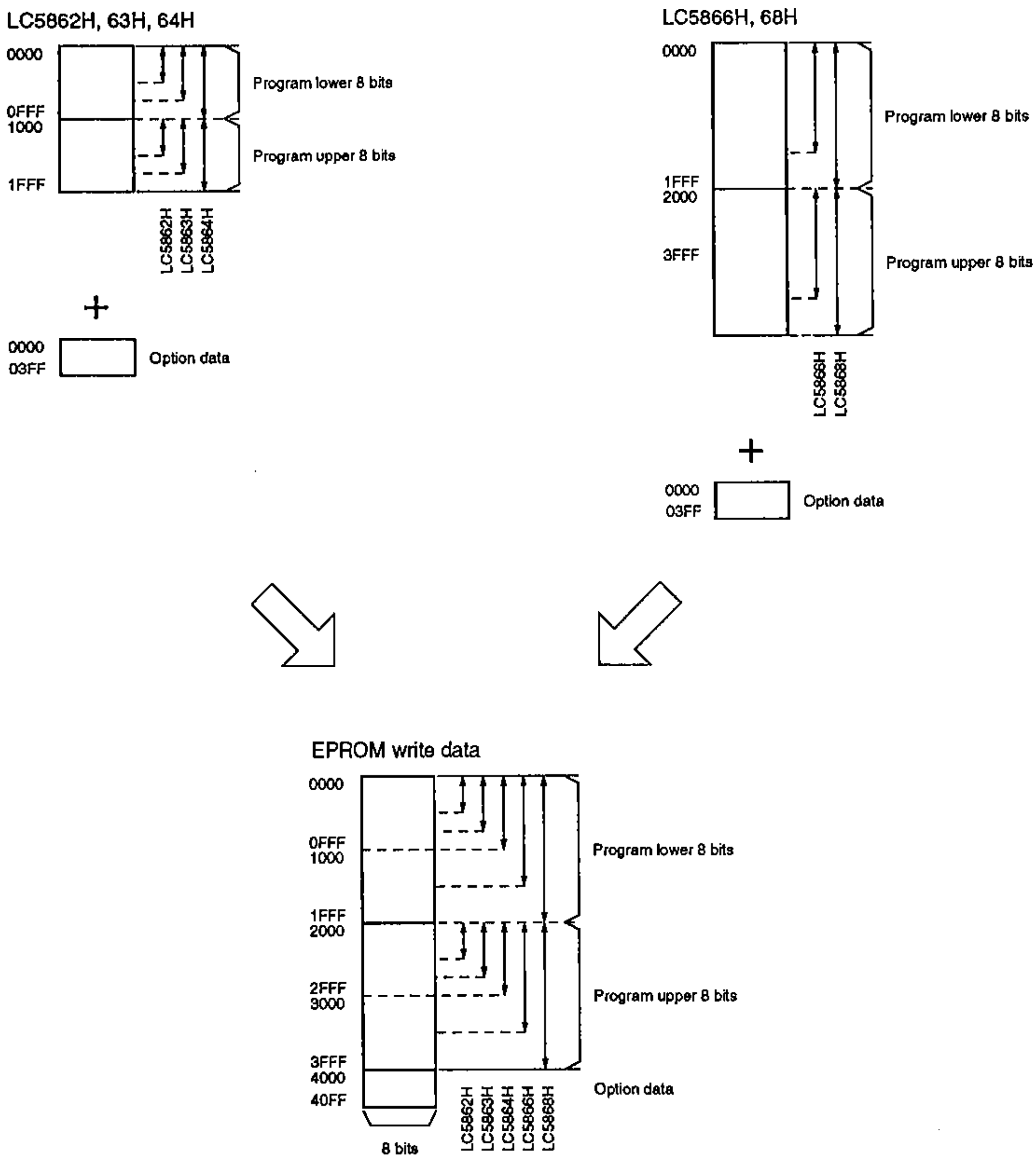


Figure 14. Conversion to EPROM format

For example, to convert the ROMSAMP.HEX program file and the PLASAMP.HEX option data file into the EP-SAMP.HEX download-format file, enter one of the following commands at the command line:

```
A:> EC5868 ROMSAMP.HEX PLASAMP.HEX EP-SAMP.HEX ↵
or
A:> EC5868 B:ROMSAMP.HEX B:PLASAMP.HEX C:EP-SAMP.HEX ↵
or
A:> EC5868 ↵
*****************************************************
* LC58E68 PROGRAM & MASK OPTION CONVERSION Ver XXXX *
*****************************************************
A: ROM PROGRAM NAME : B:ROMSAMP.HEX ↵
A: PLA PROGRAM NAME : B:PLASAMP.HEX ↵
A: EP ROM WRITE NAME : B:EP-SAMP.HEX ↵
```

A program completion message is output at the end of conversion.

If an error occurs, the program will issue one of the following error messages.

- `Error ON filename.HEX, FILE NOT FOUND`
  The file filename.HEX was not found or the file name was incorrect.
- `Error ON, MAKE LC5864H, 63H, 62H`
  The ROM data and option data are not consistent. The cross assembler and option data software used should be for the same device.
- `Error ON filename.HEX, EOF NOT DETECTED`
  The file filename.HEX does not have a record end marker or the file is corrupted.
- `Error ON filename.HEX, ILLEGAL CHARACTER`
  The file filename.HEX contains a non-hexadecimal character.
- `Error ON filename.HEX, ADDRESS OVER`
  An address in the file filename.HEX exceeds the address limit.
- `Error ON filename.HEX, ILLEGAL FILE HDR.`
  The file filename.HEX does not have the correct LC586X series header or there is an error in the hex file.
- `Error ON command line input, INVALID NUMBER OF PARAMETERS`
  The number of parameters entered on the command line is incorrect.
- `Error ON ILLEGAL, MASK OPTION DATA`
  The mask option data is incorrect.

PROM programmer and W58E68Q adapter board

Programming the LC58E68 requires a general-purpose PROM programmer and a W58E68Q adapter board. Note that the programmer provided with the EVA-520 and EVA-850 development tools cannot be used. Set the programmer for a 256 Kbyte PROM, V_{P-P} = 21 V and program addresses 0000H to 40FFH.

The W58E68Q adapter board, shown in figure 15, is placed in the PROM programmer socket and the LC58E68 to be programmed, in the W58E68Q adapter.

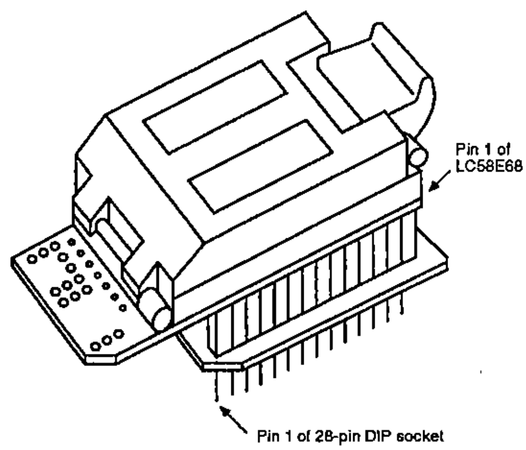


Figure 15. W58E68Q adapter board

Affix an opaque seal to the window of the programmed LC58E68 when not programming the EPROM.

Erasing the EPROM

The EPROM data can be erased with a standard UV EPROM eraser.

Soldering

Do not use the solder-dip process for soldering the LC58E68.

Reset Timing

The reset state is released following a HIGH-to-LOW transition on RES. Configuration options and the segment output control PLA are initialized during the next 256 clock cycles. The program counter is then reset and program execution begins. Configuration options are invalid and segment outputs are held at V_{SS} from when RES goes HIGH until the options are initialized.

Ordering Information

Typically, a mask ROM LC586X series device is ordered after a system has been prototyped with the LC58E68. However, a programmed LC58E68 or an LC58E68-format hex file cannot be used to specify the mask ROM device.

When ordering, provide three EPROMs each containing the mask ROM program generated using a standard assembler and another three EPROMs each containing the option data generated using the option specification tool.

A comparison of LC58E68 characteristics with those of LC586X series mask ROM devices is shown in tables 1 and 2.

Table 1. Electrical characteristics comparison

Parameter	Symbol	Conditions	LC58E68	LC586X series	Unit
Operating temperature range	Topr		10 to 40	–30 to 70	°C
Supply voltage range	V_{DD}		2.8 to 5.5	2.0 to 6.0	V
Typical halt-mode supply current	I_{DD}	V_{DD} = 3 V, f_{xtal} = 32 kHz	5	4	µA
		V_{DD} = 5 V, f_{xtal} = 32 kHz	20	15	
		V_{DD} = 5 V, f_{cer} = 400 kHz	400	400	
		V_{DD} = 5 V, f_{cer} = 2 MHz	500	500	
		V_{DD} = 5 V, f_{cer} = 4 MHz	700	700	

Table 2. Configuration comparison

Parameter	LC58E68	LC586X devices
LCD segment and common outputs during reset	Segment outputs are CMOS and are held at V_{SS}. Common outputs are n-channel and open-drain.	Static operation
Segment output state after reset	Not displayed	Displayed or not displayed
Oscillator circuit type	Ceramic filter, crystal, or ceramic filter and crystal	Ceramic filter, crystal, ceramic filter and crystal, RC circuit, RC circuit and crystal, external oscillator or external oscillator and crystal
Crystal frequency	32, 38 or 65 kHz (65 kHz during reset)	32, 38 or 65 kHz
RES reset input	Active-HIGH	Active-LOW, active-LOW with pull-up, active-HIGH or active-HIGH with pull-up
Port N outputs	Open-drain	Open-drain or CMOS
LCD drive type	Static, ½-bias and ½-duty, ½-bias and ⅓-duty, ½-bias and ¼-duty, ⅓-bias and ⅓-duty or ⅓-bias and ¼-duty (See note 1.)	Static, ½-bias and ½-duty, ½-bias and ⅓-duty, ½-bias and ¼-duty, ⅓-bias and ⅓-duty, ⅓-bias and ¼-duty or unused
'Strobe No.' range	00H to 1EH (See note 2.)	00H to 1EH

Notes

1. Configure as static drive if not used.
2. Strobe numbers 00 to 1EH can be used in applications that use a 2 MHz ceramic resonator. Strobe numbers 0E, 0F and 1EH cannot be used in applications that use a 4 MHz ceramic resonator.

The LC586X series devices, including the LC58E68, are shown in table 3.

Table 3. LC586X series devices

Device	ROM capacity (Kbytes)	RAM capacity (bits)	Package type
LC5862H	4	256 × 4	QIP80
LC5863H	6	256 × 4	QIP80
LC5864H	8	256 × 4	QIP80
LC5866H	12	256 × 4	QIP80
LC5868H	16	256 × 4	QIP80
LC58E68	16 (EPROM)	256 × 4	QFC80

Table 4. Recommended ceramic resonators for LC5862H/63H/64H/66H/68H mask ROMs

Resonator frequency	Manufacturer					
	Murata			Kyocera		
	Part number	C_{cg} (pF)	C_{cd} (pF)	Part number	C_{cg} (pF)	C_{cd} (pF)
400 kHz	CSB400P	330	330	KBR-400B	330	330
800 kHz	CSB800J	220	220	KBR-800H	100	100
1 MHz	CSB1000J	220	220	KBR-1000H	100	100
2 MHz	CSA2.00MG CST2.00MG	33	33	KBR-2.0MS	33	33
4 MHz	CSA4.00MG CST4.00MG	33	33	KBR-4.0MS	33	33