CMOS LSI

LC1707PLF — FM multiple tuner IC

Application Note

ON Semiconductor®
http://onsemi.com

Overview:

LC01707PLF is a vehicle-mounted FM multiple tuner IC with FM-FE, IF, IF-Filter, PLL, FM-DEMO and LPF incorporated. An FM multiple tuner can be developed with this one chip. It makes up a small-sized FM multiple tuners which can be mounted on PND.

Functions:

- It is the FM tuner IC exclusively for the FM multiple.
- LNA is incorporated
- Image reduction complex BPF is incorporated
- Wide / Narrow Band RF AGC is incorporated
- Narrow Band IF AGC is incorporated
- Image rejection is adopted
- DLL detection method is adopted for the FM detection circuit, and it is not necessary to adjust.
- LPF for the carrier removal is incorporated.
- IC requires fewer external components.
- It is a BUS control tuner IC which can be controlled by controlled by I^2C BUS.

Typical Applications:

- DARC tuner for AVN, PND and Car Audio System
- SCA tuner for AVN, PND and Car Audio System
- RDS tuner for AVN, PND and Car Audio System

Specifications:

Maximum Ratings at Ta = 25°C

Parameter	Symbol	Conditions	Ratings	Unit
Supply voltage	V_{DD} max		4.3	V
Maximum input voltage	V_{DD} H		4.3	V
Maximum output voltage	V_{DD} L		4.3	V
Power dissipation	Pd max	Ta = 85°C *1	700	mW
Operating ambient	Topr		-40 to 85	°C
Storage temperature	Tstg		-55 to 150	°C
Maximum junction	Tj max		150	°C

*1: Board size: 80mm × 70mm × 1.6mm Glass epoxy double-sided board

Recommended Operating Conditions at Ta = 25°C

Parameter	Symbol	Conditions	Ratings	Unit
Supply voltage range	V_{DD}		3.0 to 3.6	V
Recommended supply temperature	V_{DD}		3.3	V

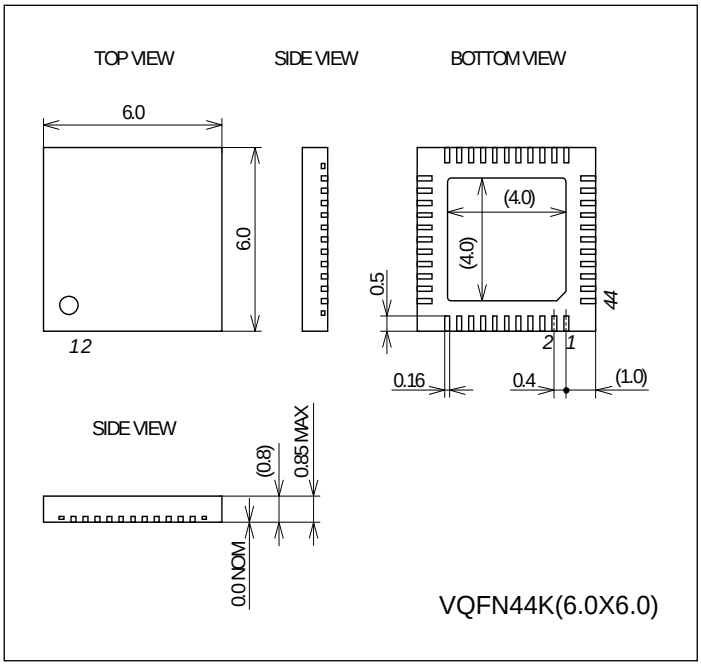
Electrical Characteristics at Ta = 25°C, V_{DD} = 3.3V,
fc = 83MHz, VIN=60dBμVEMF, fm=1kHz, Audio filter: HPF=100Hz, LPF=15kHz
Resister setting: IF AGC (02h) =6(110), RF AGC (00h) =0(0000)
DLL demodulator loop gain setting (09h) =1(01), Mono multi center setting (09h) =7(0111)

Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
Practical sensitivity 1 (S/N30dB)	SN30	22.5kHz dev, fm=1kHz, S/N=30dB input level		12	20	dBμEMF
Practical sensitivity 2 (S/N10dB)	SN10	7.5kHz dev, fm=76kHz, S/N=10dB input level *1		27		dBμEMF
S/N1	SN1	22.5kHz dev, fm=1kHz	34	44		dB
S/N2	SN2	7.5kHz dev, fm=76kHz *1		21		dB
Total harmonic distortion rate 1	THD_1	22.5kHz dev, fm=1kHz		0.5		%
Total harmonic distortion rate 2	THD_2	75.0kHz dev, fm=1kHz		0.5		%
AM suppression ratio	AMR	AM 30% mod	34	44		dB
Image rejection ratio	IMR	22.5kHz dev, fm=1kHz		32		dB
Audio output level 1	AD01	7.5kHz dev, fm=1kHz *1	26	39	70	mVrms
Audio output level 2	AD02	7.5kHz dev, fm=76kHz *1	15	23	41	mVrms
Consumption current	IDD	No signal input		106	170	mA

*1: Audio filter: HPF=100Hz, LPF=OFF

Package Dimensions:

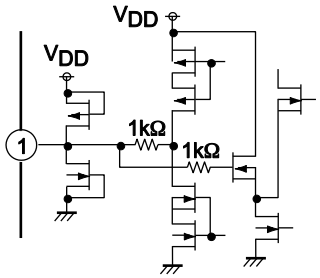
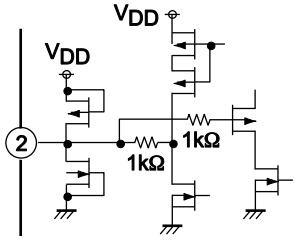
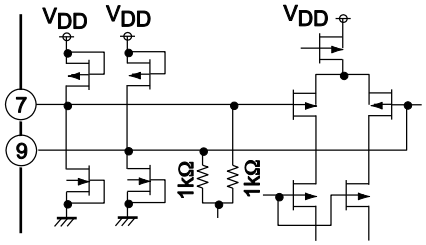
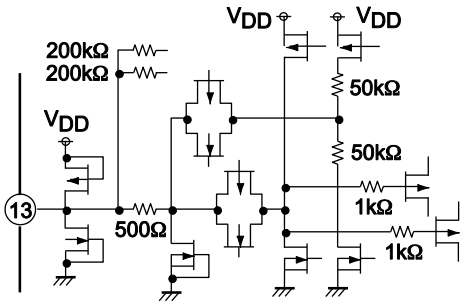
unit : mm (typ)
3408



Pin Description:

Pin No.	Pin name	I/O	Function
1	NAGC	O	Narrow band AGC detection capacitance connecting pin
2	WAGC	O	Wide band AGC detection capacitance connecting pin
3	V_{SS}	P	GND pin for IF
4	NC	-	
5	NC	-	
6	V_{DD}	P	Supply pin for LNA
7	LNA_A	I	LNA +input pin
8	V_{SS}	P	GND pin for LNA
9	LNA_N	I	LNA -input pin
10	NC	-	
11	NC	-	
12	V_{SS}	P	GND pin for 1st Mixer
13	CP	O	PLL charge pump capacitance connecting pin
14	V_{DD}	P	Supply pin 1st Mixer
15	V_{DD}	P	Supply pin for local oscillation
16	LO_1	O	Inductor connecting pin for local oscillation
17	V_{SS}	P	GND pin for local oscillation
18	LO_2	O	Inductor connecting pin for local oscillation
19	NC	-	
20	NC	-	
21	NC	-	
22	NC	-	
23	DEVER	I	Device address setting pin
24	V_{SS}	P	GND pin for PLL and logic
25	XTAL	I	Crystal resonator connecting pin (Clock input pin)
26	SD	O	Station detector pin
27	NC	-	
28	NC	-	
29	NC	-	
30	INT	O	Test pin
31	SCL	I	Serial data clock input
32	SDA	I	serial data input-output
33	V_{DD}	P	Supply pin for PLL and logic
34	SMETER	O	S-meter output
35	V_{DD}	P	Supply pin for IF
36	LPFO	O	Demodulation output (after band limitation)
37	DEMOO	O	Demodulation output
38	LPFI	I	Demodulation signal input pin
39	DEMOC	O	Capacitance connecting pin for demodulation detection
40	NC	-	
41	NC	-	
42	NC	-	
43	NC	-	
44	GND	P	GND pin

Pin Function:

Pin No.	Pin name	Function	Equivalent circuit
1	NAGC	Narrow band AGC detection capacitor connection pin.	
2	WAGC	Wide band AGC detection capacitor connection pin.	
3	V_{SS}	GND pin for IF.	
4	NC	No connection.	
5	NC	No connection.	
6	V_{DD}	Supply pin for LNA.	
7 8 9	LNA_P V_{SS} LNA_N	Pin 7 is + input pin for LNA. Pin 8 is GND pin for LNA. Pin 9 is - input pin for LNA.	
10	NC	No connection.	
11	NC	No connection.	
12	V_{SS}	GND pin 1st mixer for the 1st mixer.	
13	CP	PLL charge pump capacitor connection pin.	
14	V_{DD}	Supply pin for the 1st mixer.	
15	V_{DD}	Supply pin for local oscillator.	

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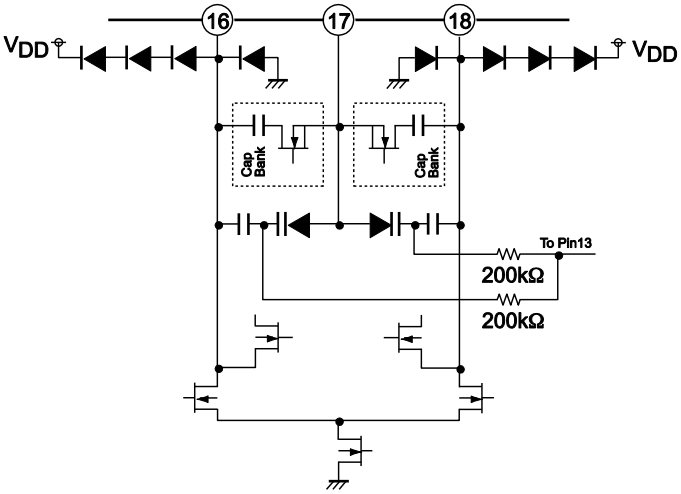
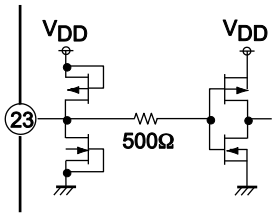
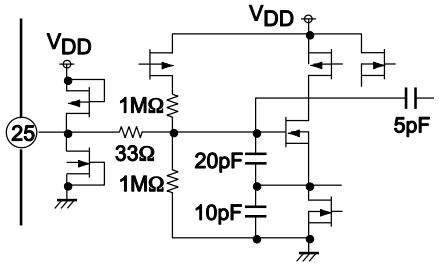
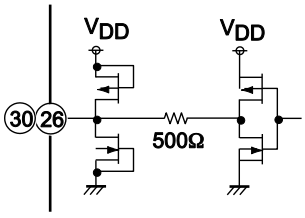
Pin No.	Pin name	Function	Equivalent circuit
16 17 18	LO_1 V_{SS} LO_2	Pin 16 is inductor connection pin for local oscillator. Pin 17 is GND pin for local oscillator. Pin 18 is inductor connection pin for local oscillator.	
19	NC	No connection.	
20	NC	No connection.	
21	NC	No connection.	
22	NC	No connection.	
23	DEVAR	Device address setting pin.	
24	V_{SS}	PLL_logic GND pin.	
25	XTAL	Crystal oscillator connection pin (clock input pin).	
26 30	SD INT	Station detector pin. Test monitor pin.	
27	NC	No connection.	
28	NC	No connection.	
29	NC	No connection.	

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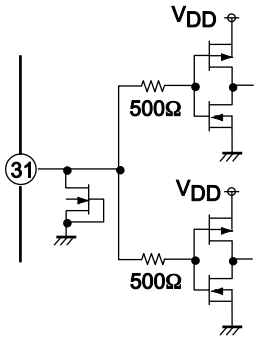
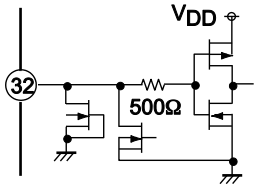
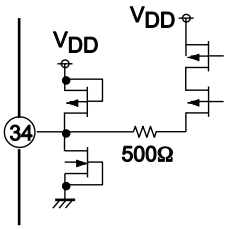
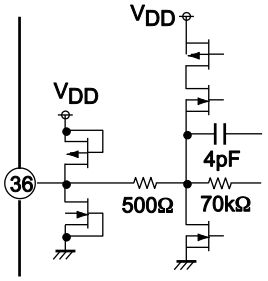
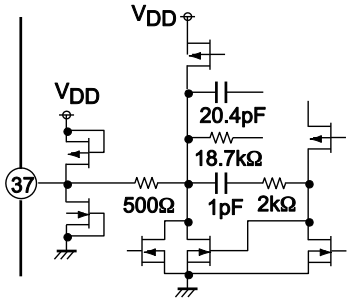
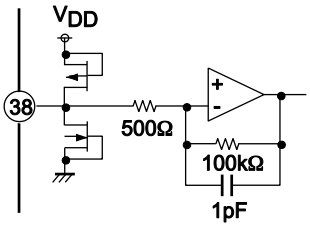
Pin No.	Pin name	Function	Equivalent circuit
31	SCL	Serial data clock input.	
32	SDA	Serial data input/ output.	
33	V_{DD}	PLL_logic supply voltage pin.	
34	SMETER	S-meter output.	
35	V_{DD}	IF supply voltage pin	
36	LPFO	Demodulator output (After band limit).	
37	DEMOO	Demodulator output.	
38	LPFI	Demodulator signal input pin.	

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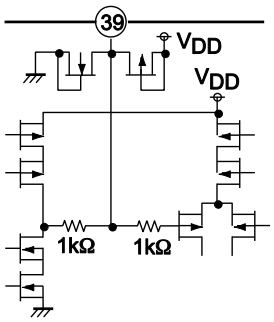
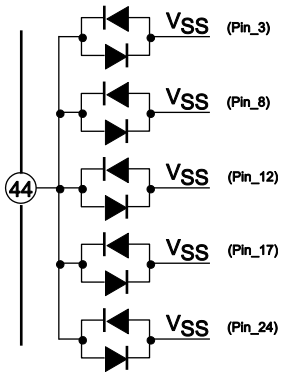
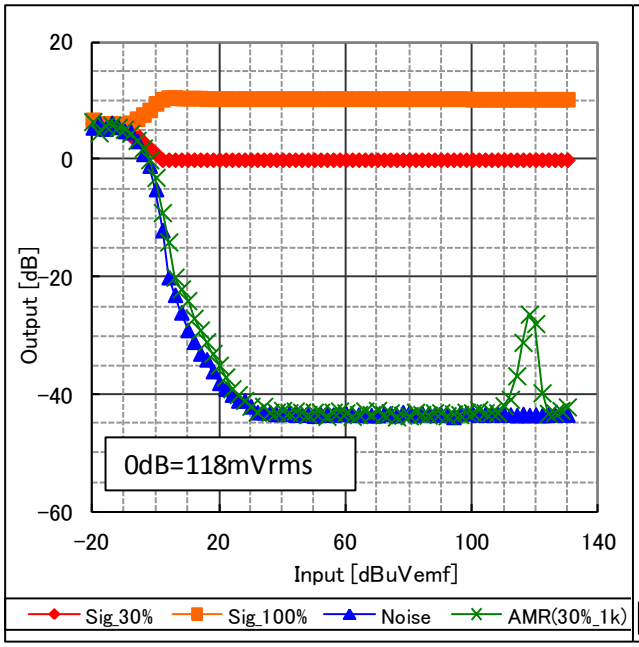
Pin No.	Pin name	Function	Equivalent circuit
39	DEMOC	Capacitor connection pin for demodulator detection.	
40	NC	No connection.	
41	NC	No connection.	
42	NC	No connection.	
43	NC	No connection.	
44	GND	GND pin.	

TYPICAL PERFORMANC CURVES

Input/output characteristics

fm=1kHz, 30% HPF=100Hz, LPF=15kHz

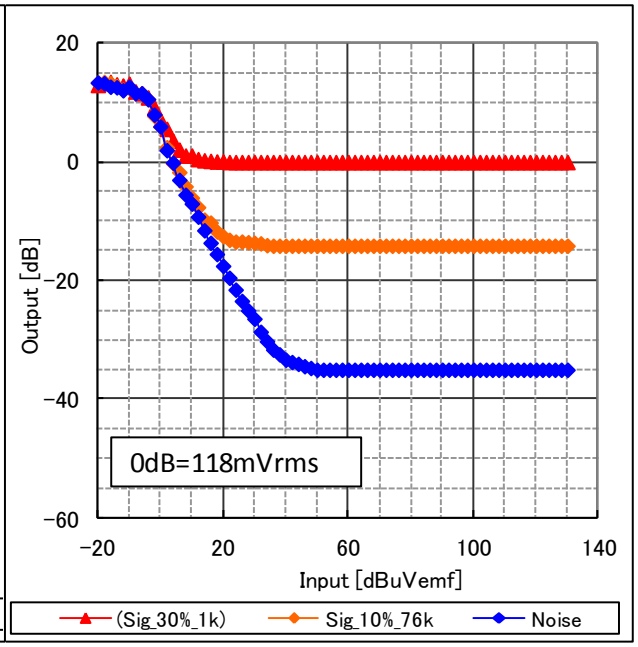
RF AGC(00h)=0(0000) IF AGC(02h)=6(110)



Input/output characteristics

fm=76kHz, 4%,10%, HPF=100Hz, LPF=OFF

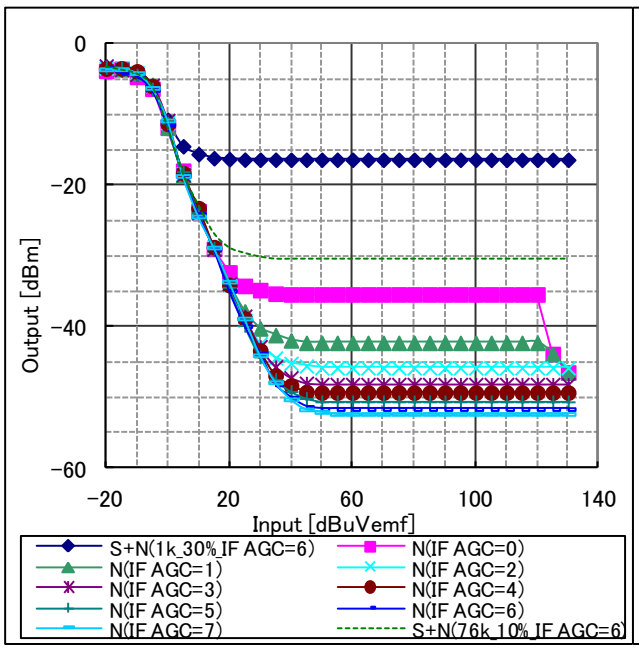
RF AGC(00h)=0(0000) IF AGC(02h)=6(110)



IF AGC bit vs. S/N

fm=1kHz,30% HPF=100Hz, LPF=OFF

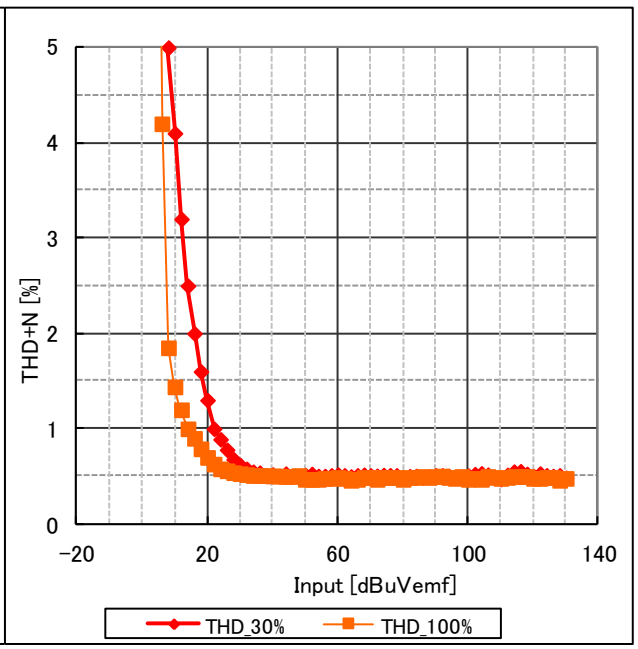
RF AGC(00h)=0(0000), IF AGC(02h)=variable



THD input/output characteristics

fm=1kHz, 30%, 100% HPF=100Hz, LPF=15kHz

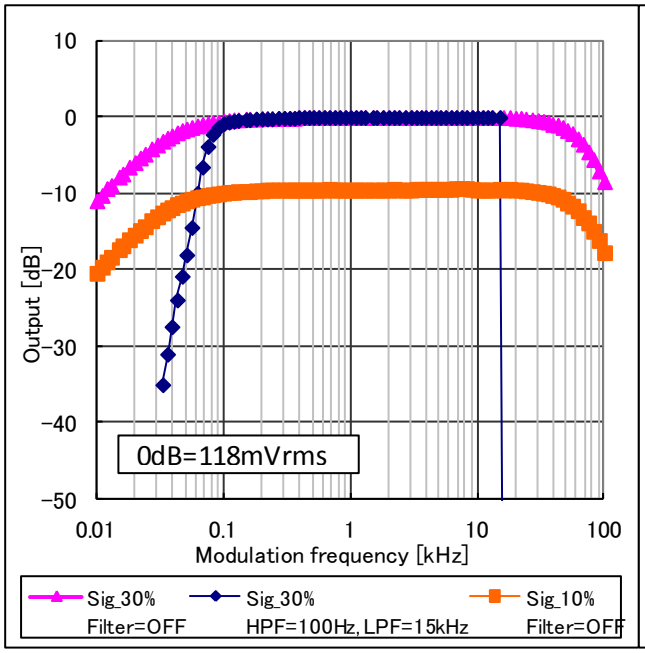
RF AGC(00h)=0(0000), IF AGC(02h)=6(110)



composite output vs. mod frequency

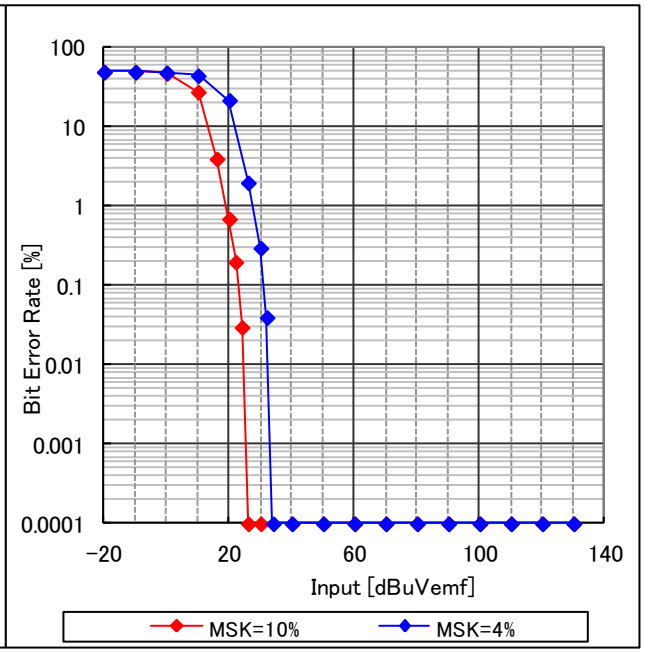
fm=1kHz, 30%, 100% HPF=variable, LPF variable

RF AGC(00h)=0(0000), IF AGC(02h)=6(110)



BER input/output characteristics

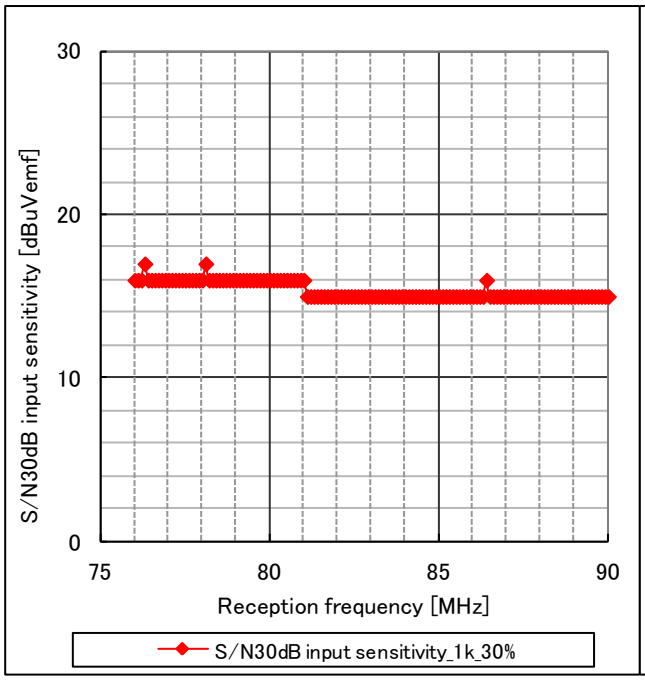
RF AGC(00h)=0(0000), IF AGC(02h)=6(110)



S/N30dB sens vs. frequency

fm=1kHz, 30% filter=DIN AUDIO

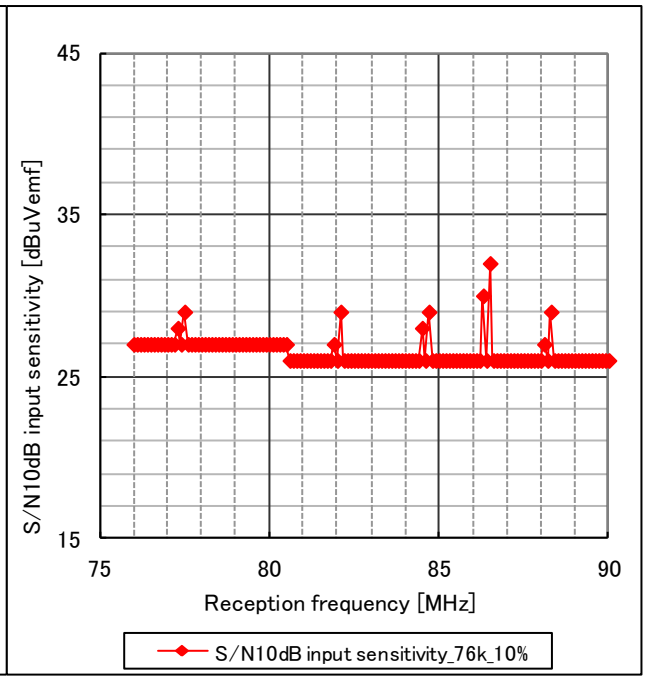
RF AGC(00h)=0(0000), IF AGC(02h)=6(110)



S/N10dB sens vs.frequency

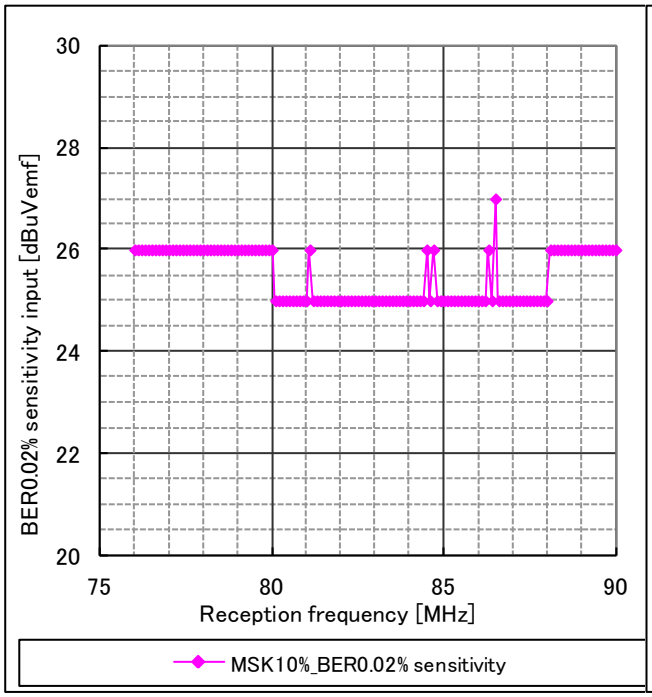
fm=76kHz, 10% filter=FLAT

RF AGC(00h)=0(0000), IF AGC(02h)=6(110)



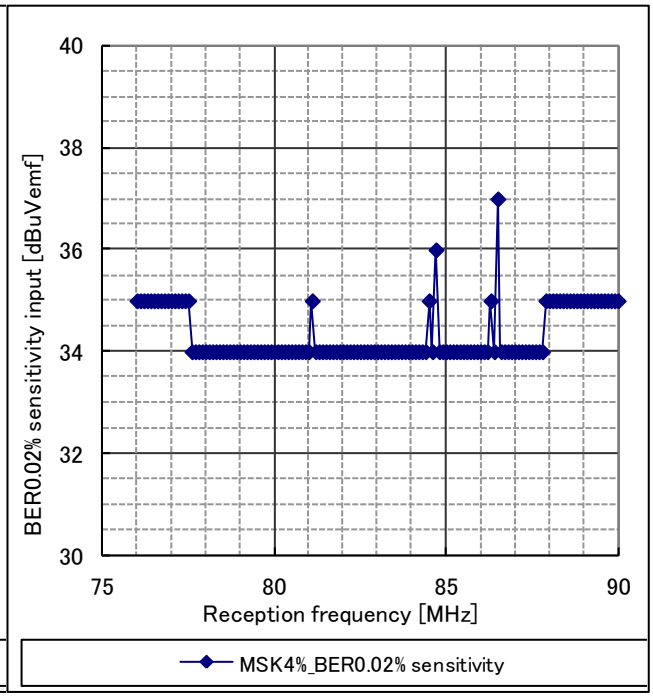
BER0.02% sens vs. frequency

MSK=10%



BER0.02% sens vs. frequency

MSK=4%

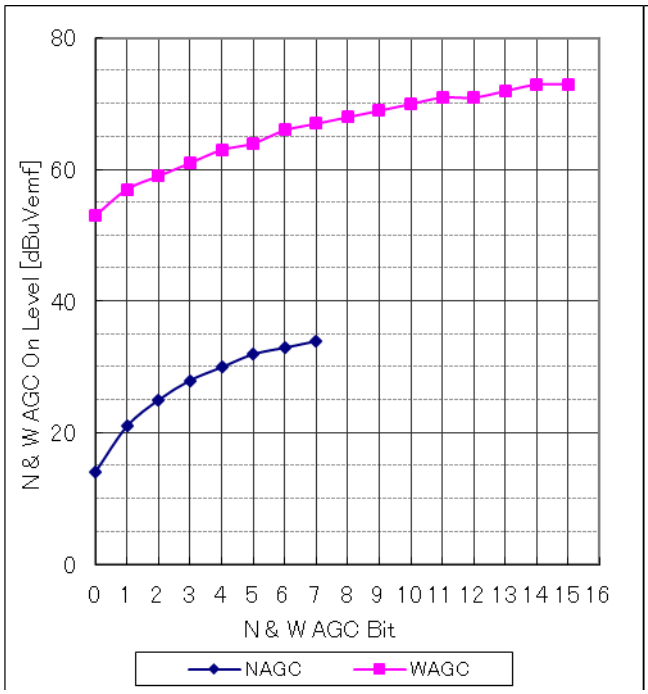


N & W AGC bit vs. on level

on level: AGC pin voltage >0.3V

WAGC:NB chk off

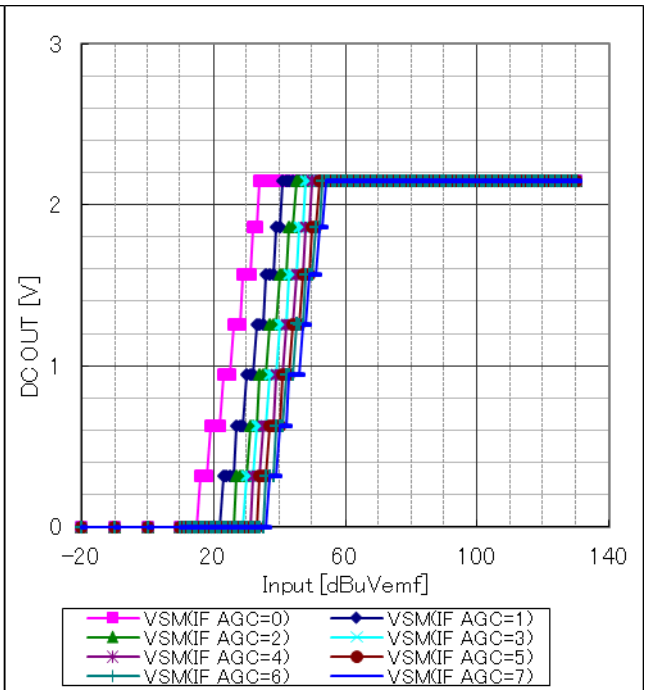
NAGC:WB chk off



S-meter input/output characteristics

mod-off WB:chk off

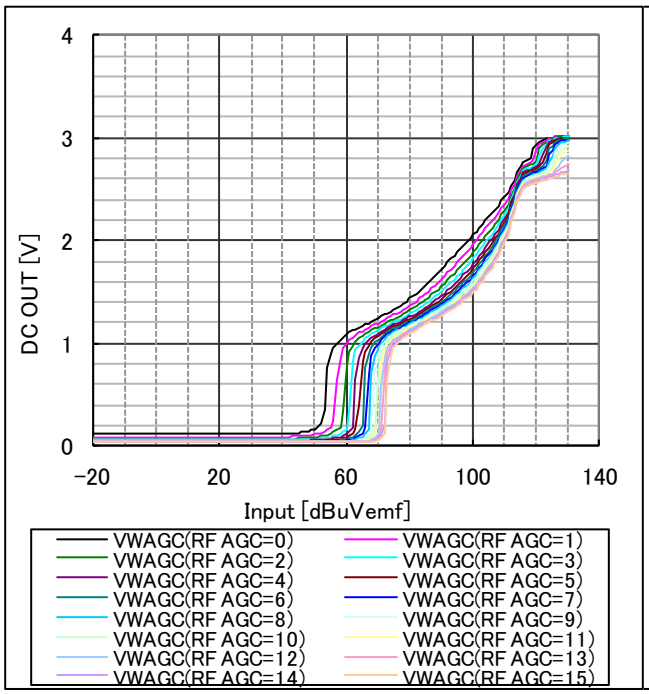
RF AGC(00h)=0(0000), IF AGC(02h)=variable



WAGC input/output characteristics

RF AGC(00h)=variable, IF AGC(02h)=6(110)

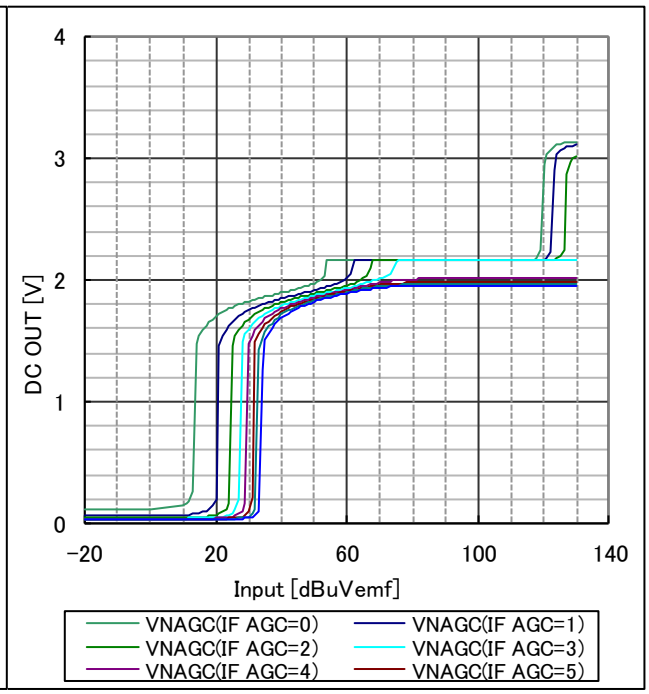
mod-off NB:chk off



NAGC input/output characteristics

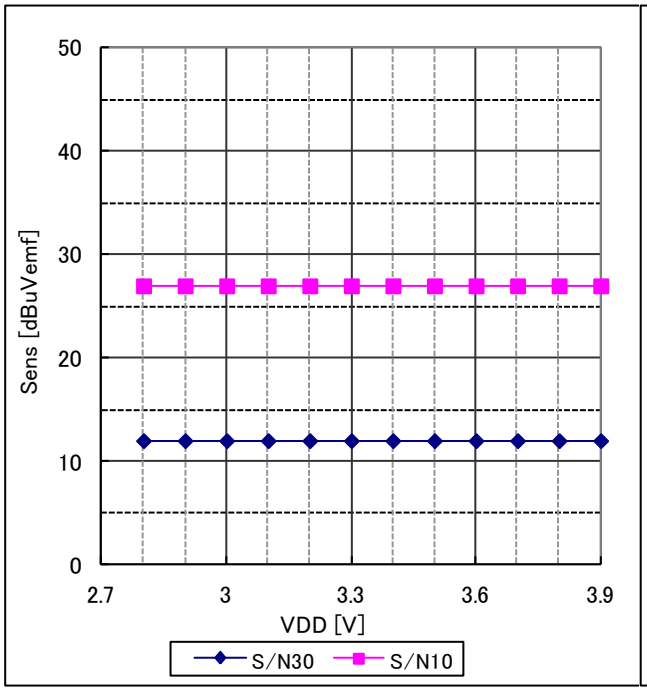
RF AGC(00h)=0(0000), IF AGC(02h)=variable

mod-off WB:chk off

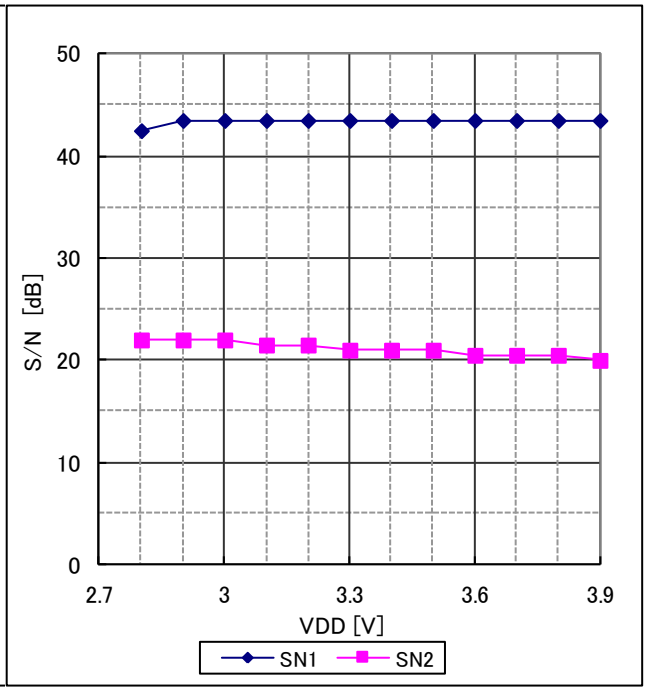


Supply Voltage Characteristics

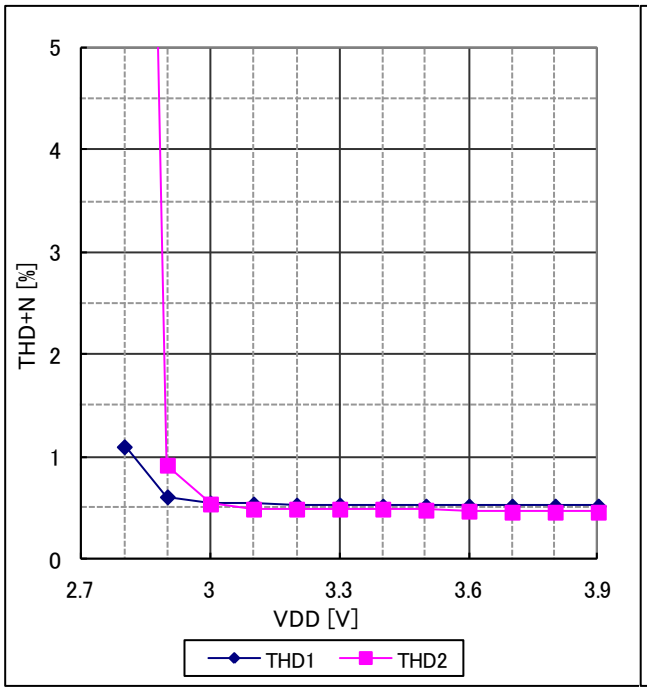
Sens



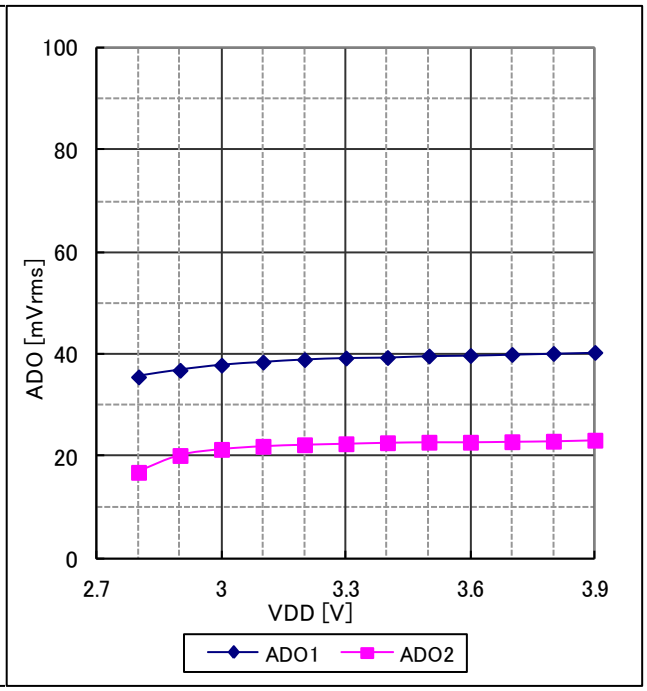
S/N



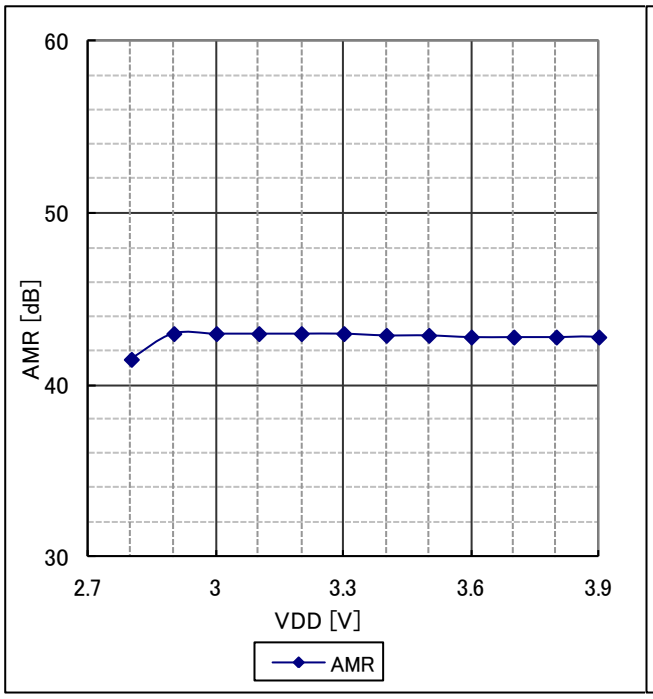
THD



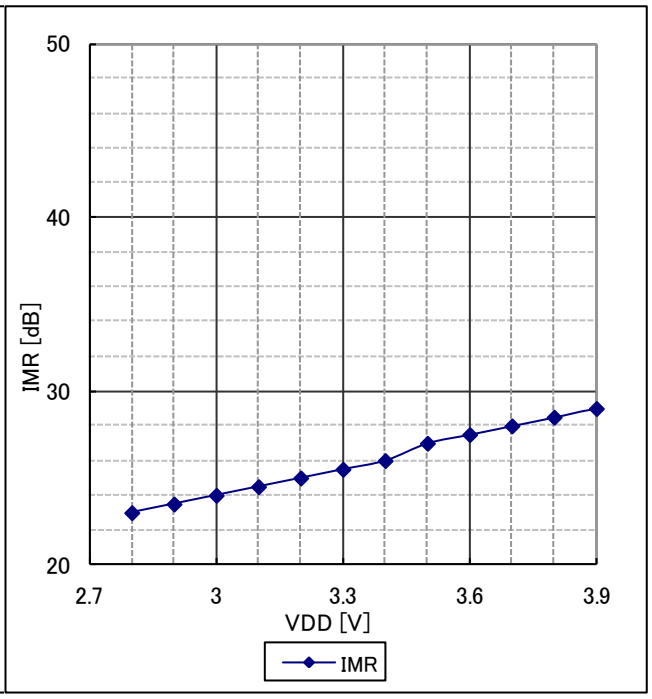
ADO



AMR

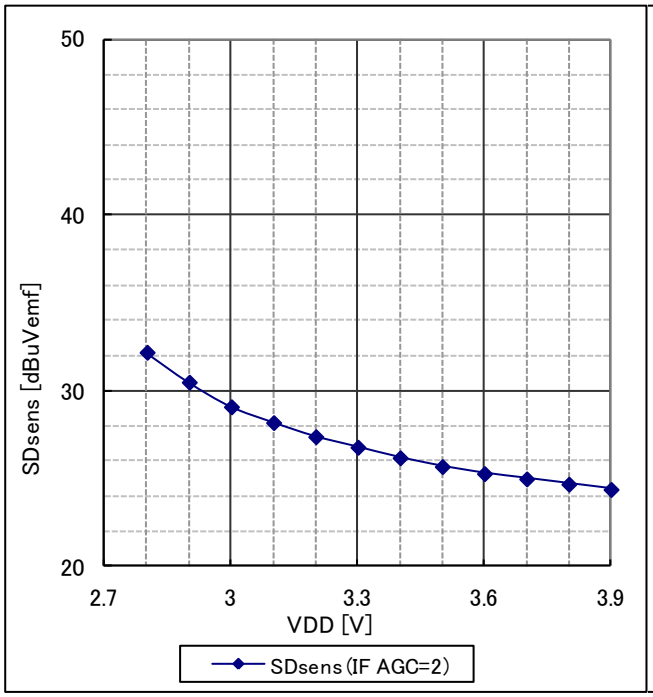


IMR

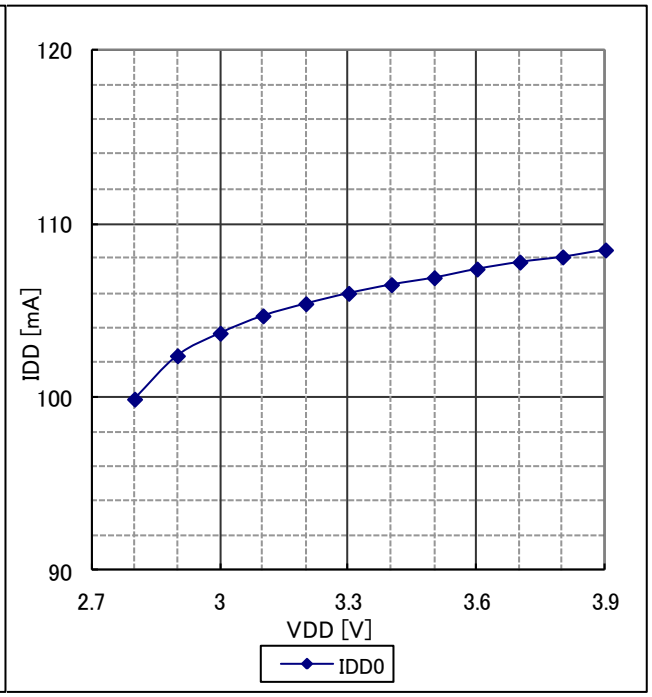


SD sens

IF AGC(02h)=2(010) SD=0

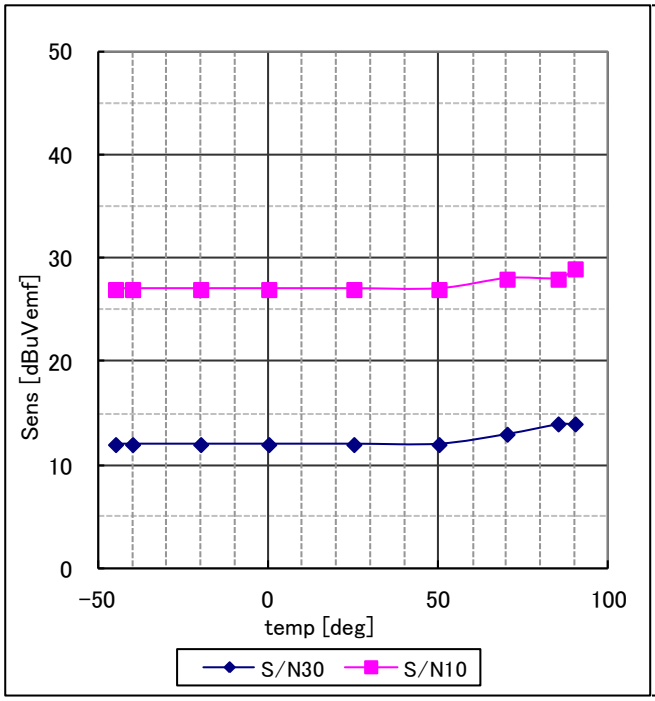


IDDO

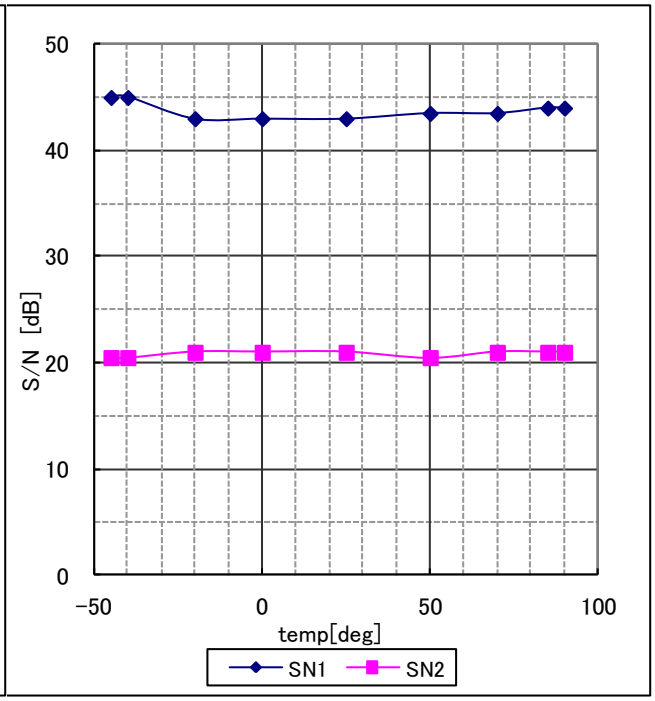


Temperature Characteristics

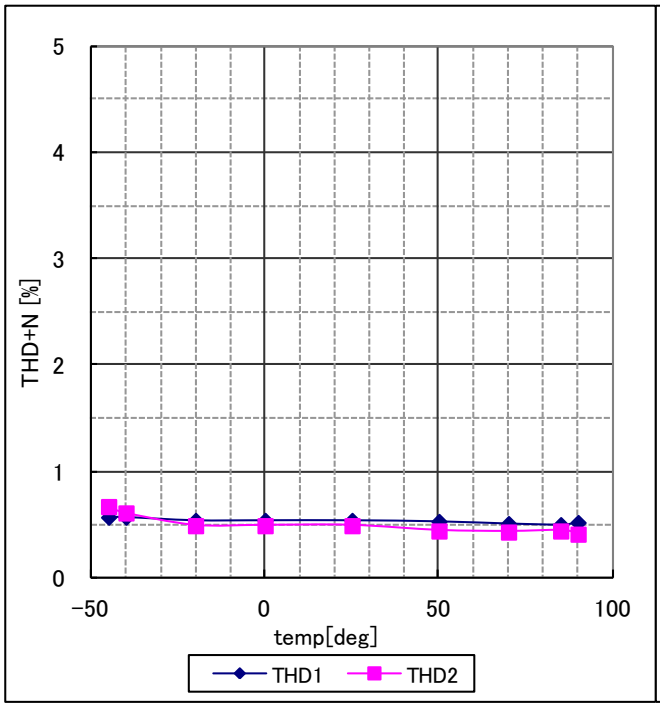
Sens



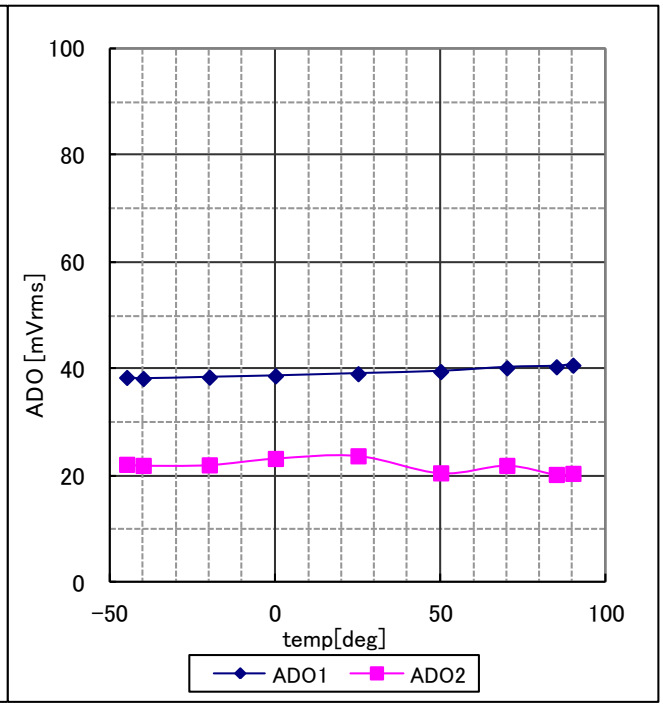
S/N



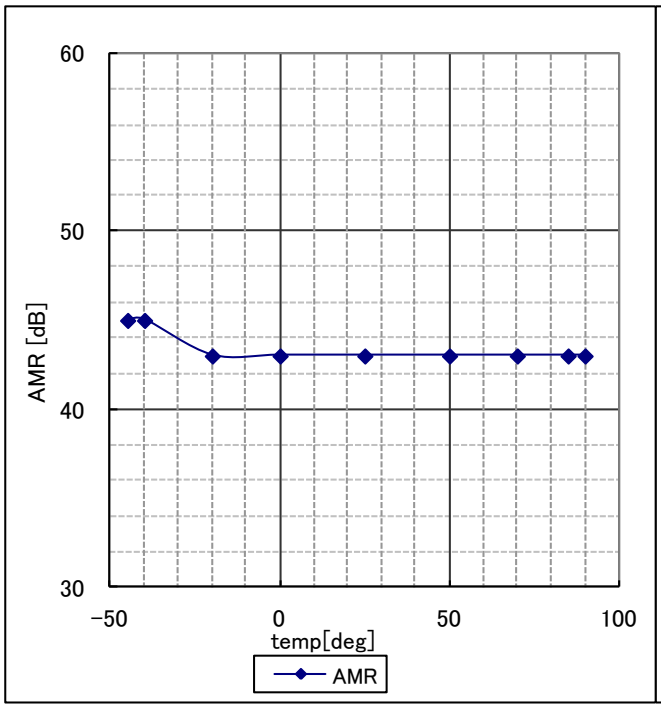
THD



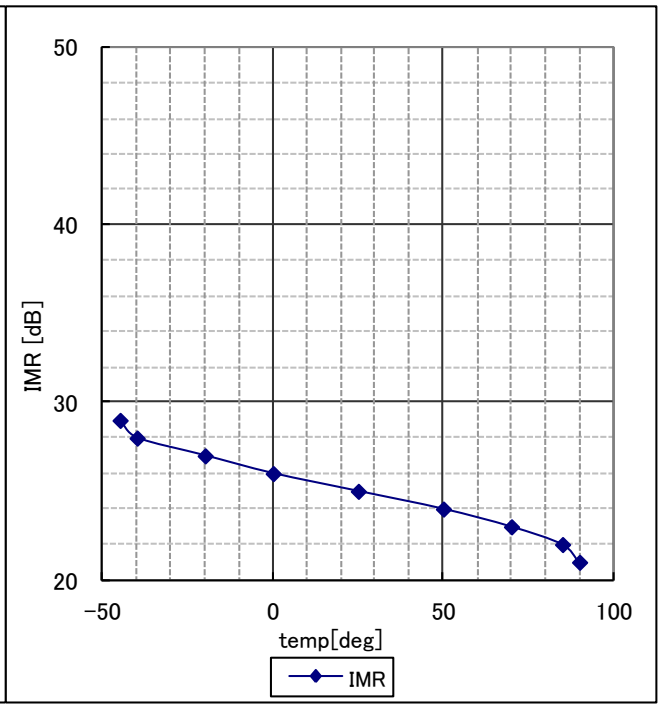
ADO



AMR

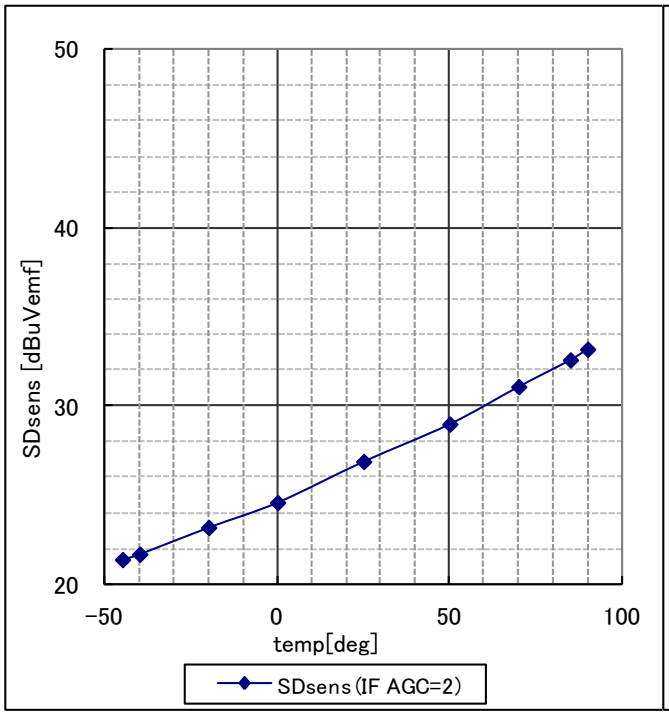


IMR

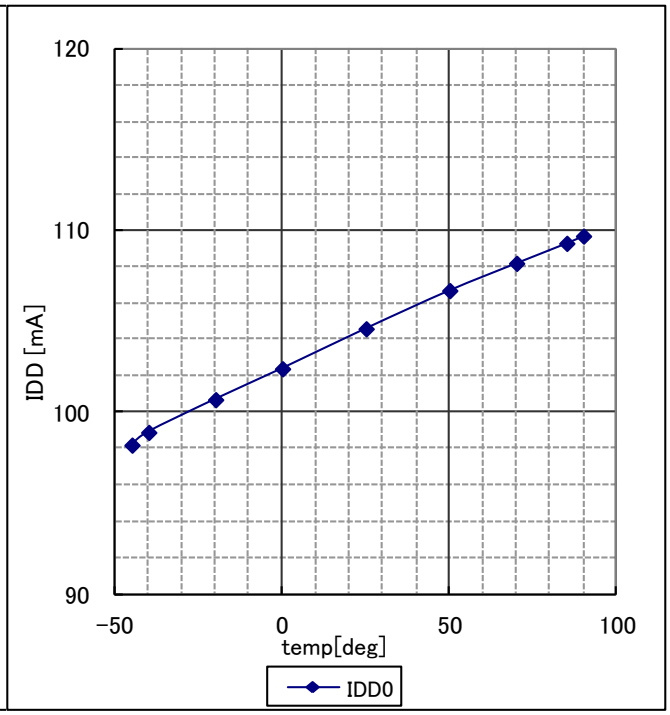


SD sens

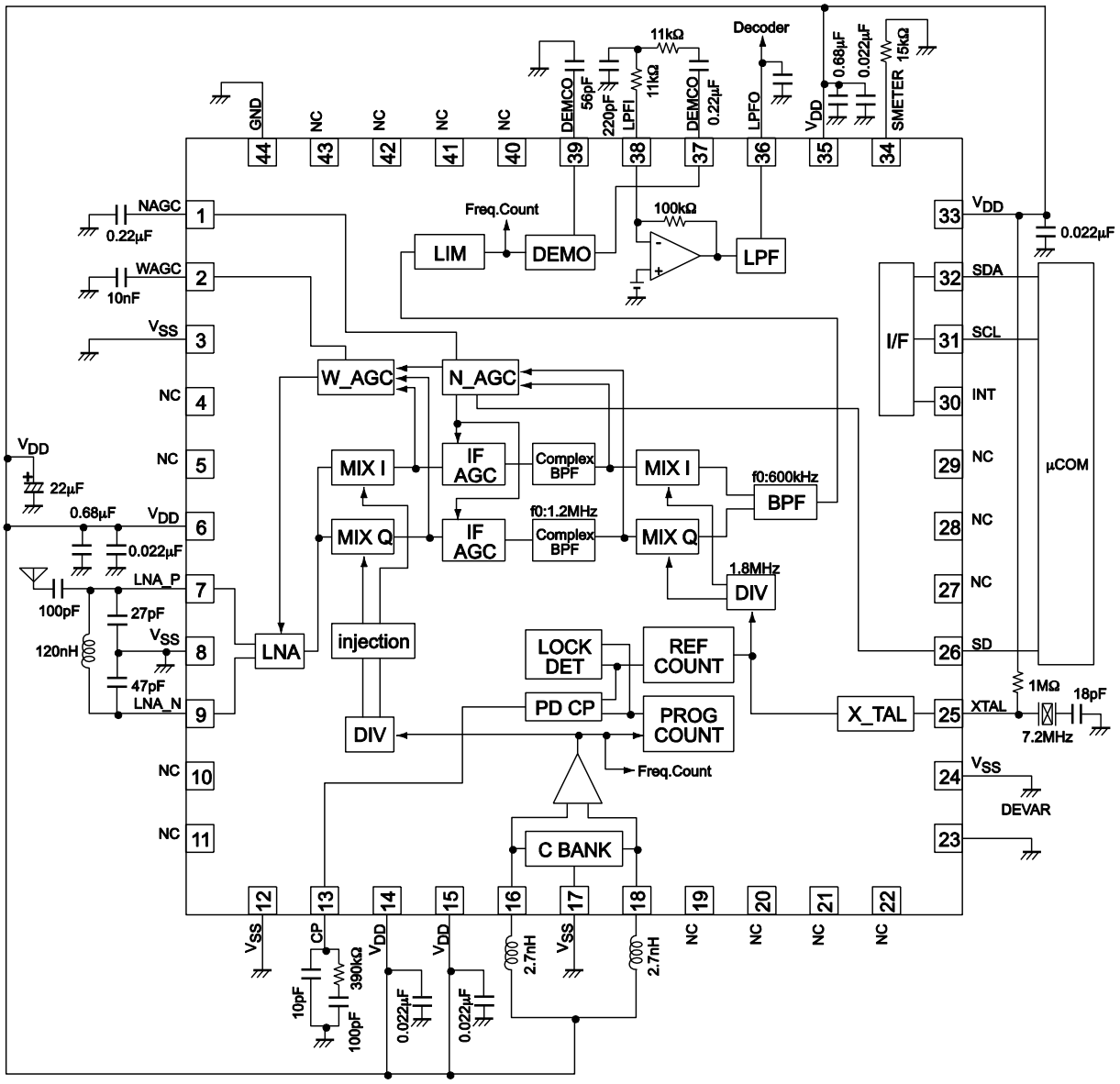
IF AGC(02h)=2(010) SD=0



IDDO



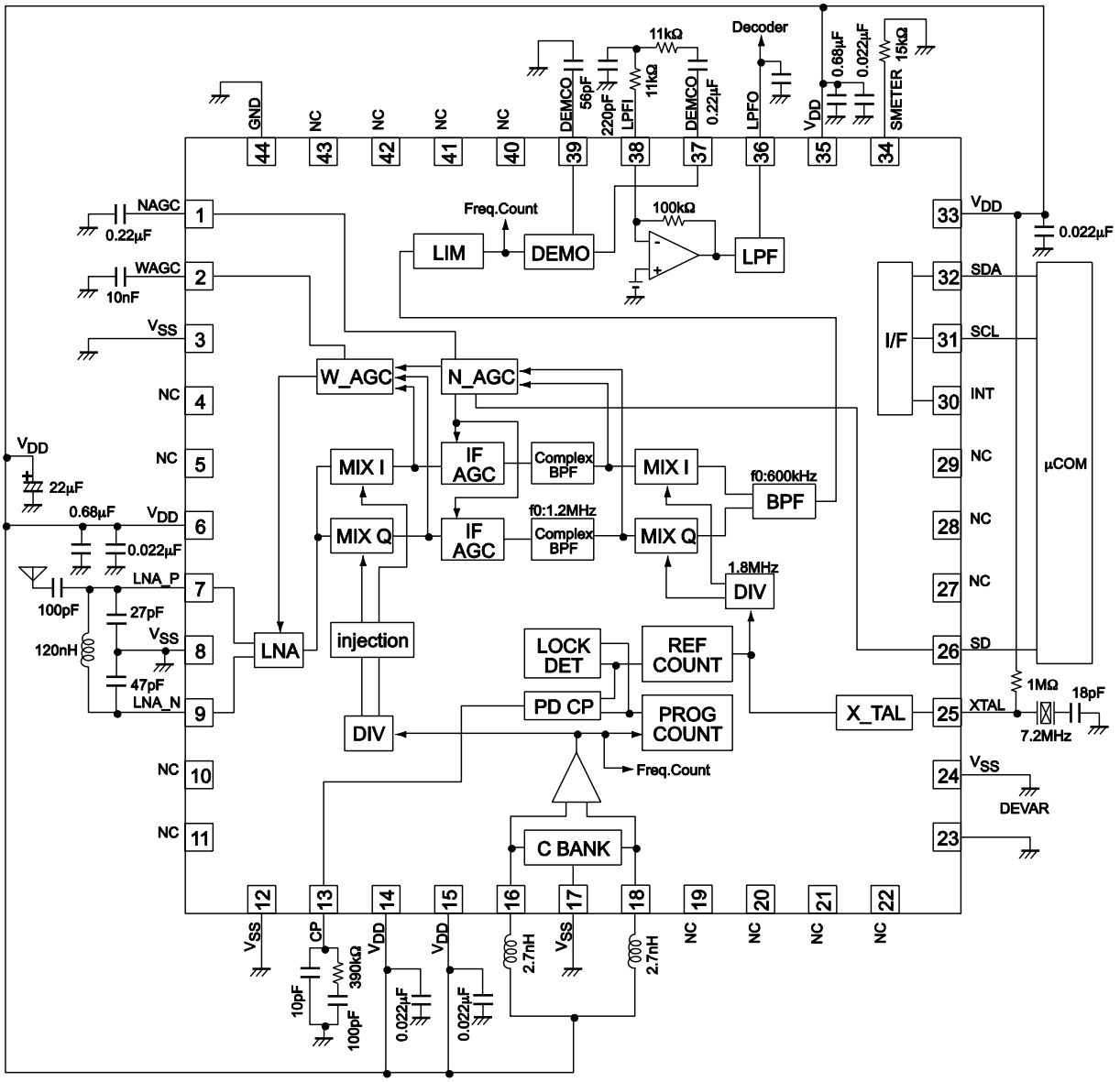
Example of applied circuit 1(constant is tentative):



* Culprits oscillation circuit is used in this IC as a crystal oscillation circuit. Caution is required for layout of the board because oscillation between pin25 and power source and GND line.
* The margin of crystal oscillation changes due to the combination of the IC, a crystal oscillator and a board layout. This independent IC does not quarantine the oscillation operation.
* This IC uses the signal of FM band frequency (VCO divided into 1/4) which leaks into ANT pin. If the VCO leakage affects the performance of the system, make sure to connect an isolator on ANT pin path.

Component	Parameter	Value	Type	Supplier
L1/L2	Local OSC coil	2.7nH	C2012H-2N7D-RD	SAGAMI
L3	Differential input coil	120nH	C2012H-R12G-RC	SAGAMI
X1	Crystal	7.2MHz	SMD-49	KDS
			AT-49	KDS
			EXS00A-A01145	NDK
			EXS00A-A01146	NDK

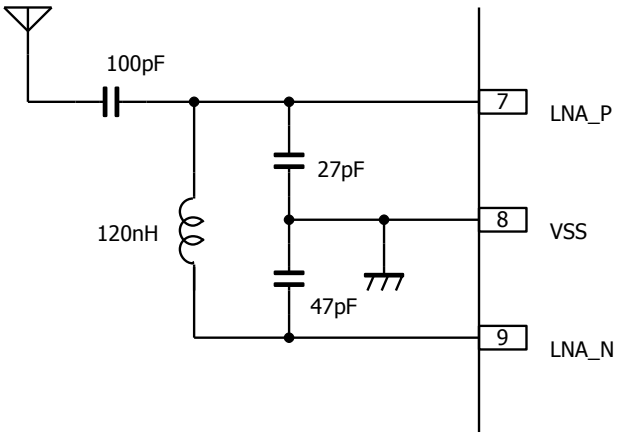
Example of applied circuit 2

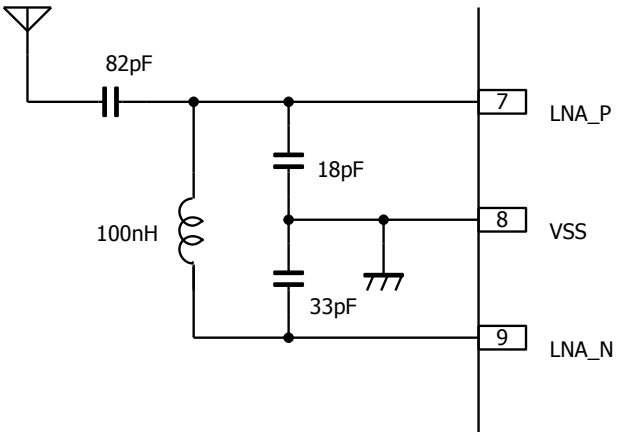


■RF-IN LC circuit value

1. JPN band (76MHz-90MHz)
   Input : C=100pF, L=120nH
   7PIN-GND : C=27pF
   9PIN-GND : C=47pF

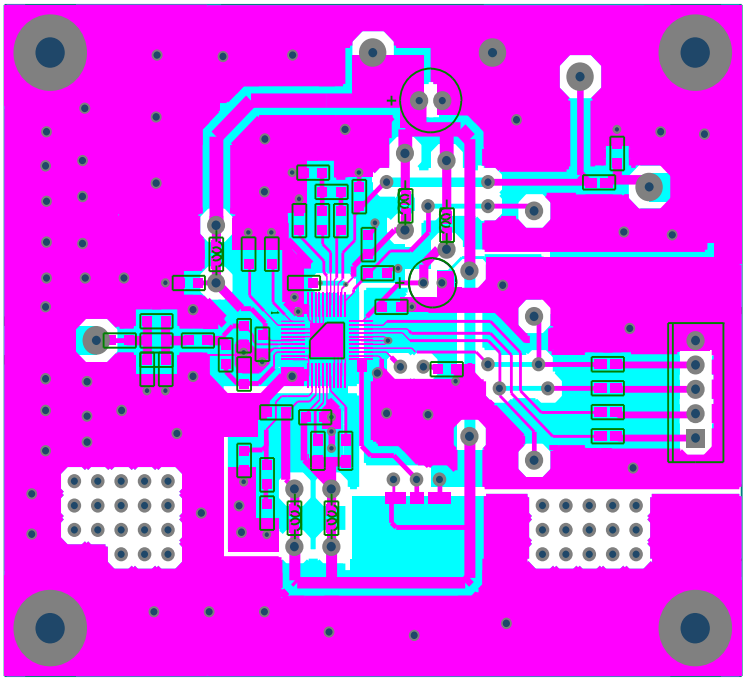
2. US band (88MHz-108MHz)
   Input : C=82pF, L=100nH
   7PIN-GND : C=18pF
   9PIN-GND : C=33pF



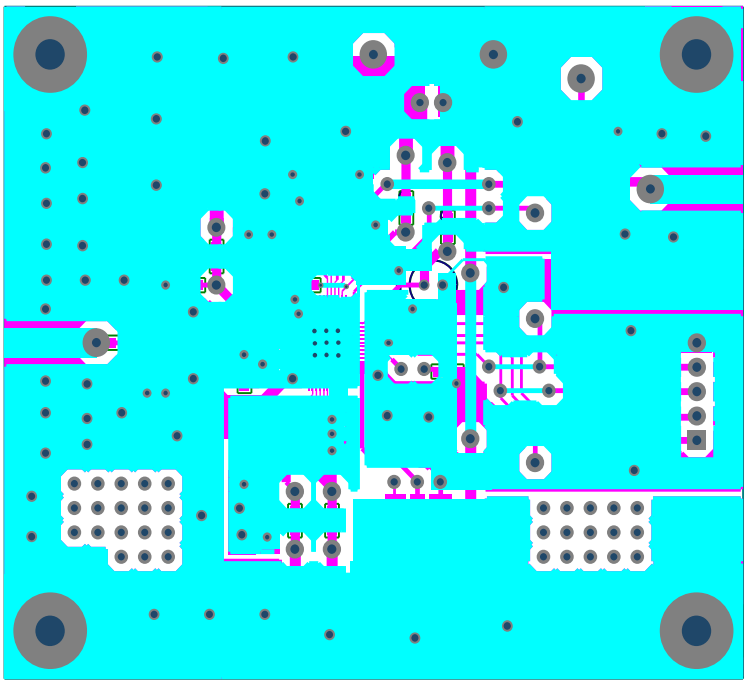


Board pattern layout guide:

Top View (component side）



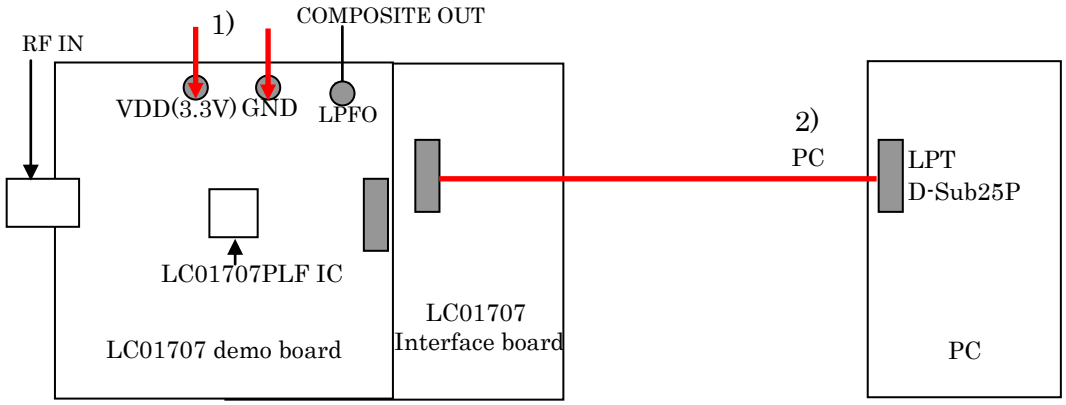
BOTTOM view (back side)



LC01707PLF controller manual:

1. How to connection

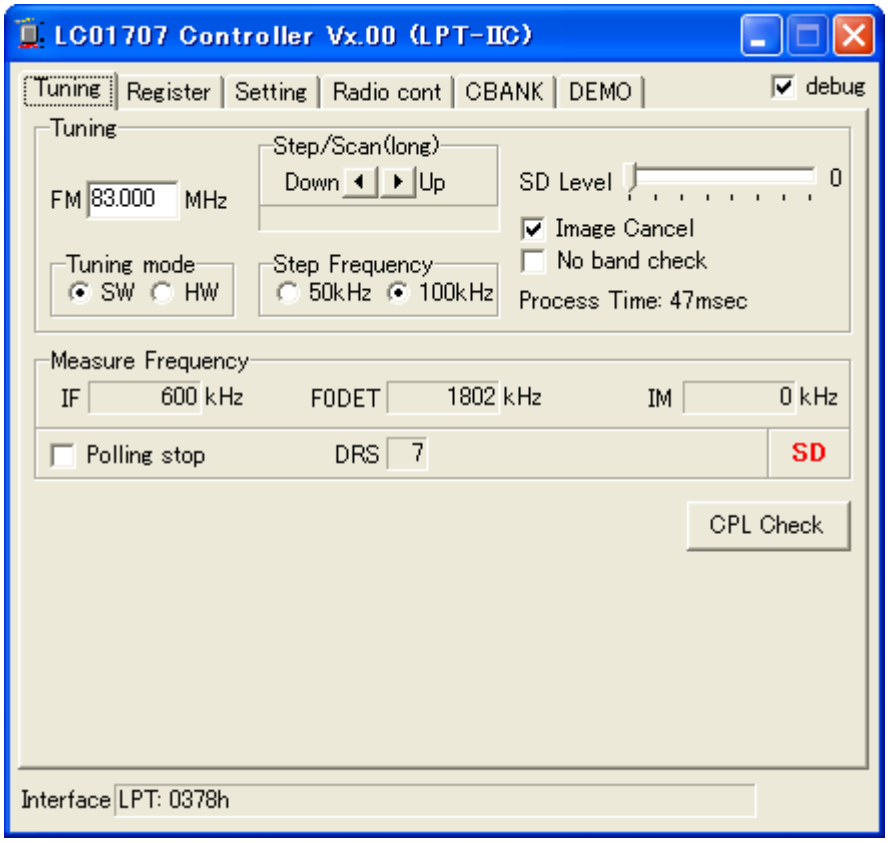
1) Power Supply voltage of 3.3V
2) Connected to an exclusive cable between parallel port and interface boards



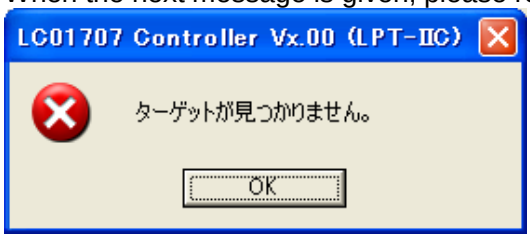
2. How to start of controller

•Defrost an LC01707ControllerVxXX.zip file

•Double-click LC01707Controller.exe file
When normalcy works, a [Tuning] screen opens.



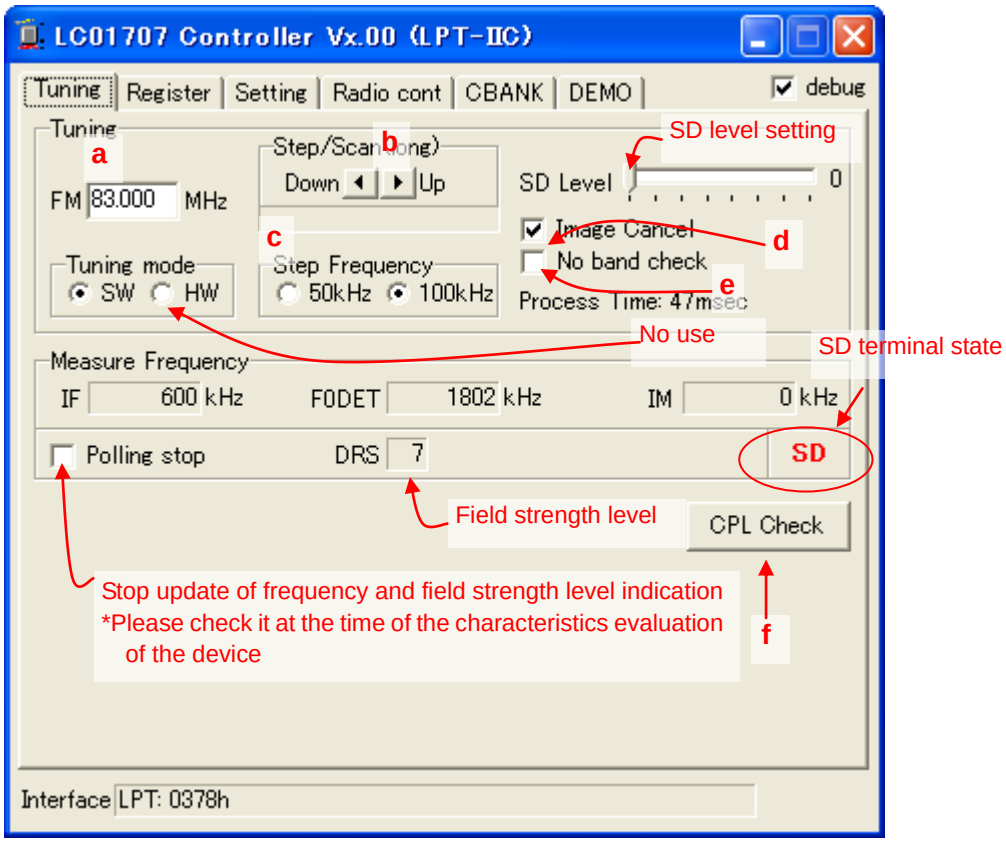
When the next message is given, please reconfirm connection and power supply.



3. Description of all parts

- [Tuning] tab

Frequency setting and confirmation are possible.



a. Tuning
It input frequency and am tuned up with the enter key

b. Step/Scan
Short push : 1step tuning Long push : scan tuning

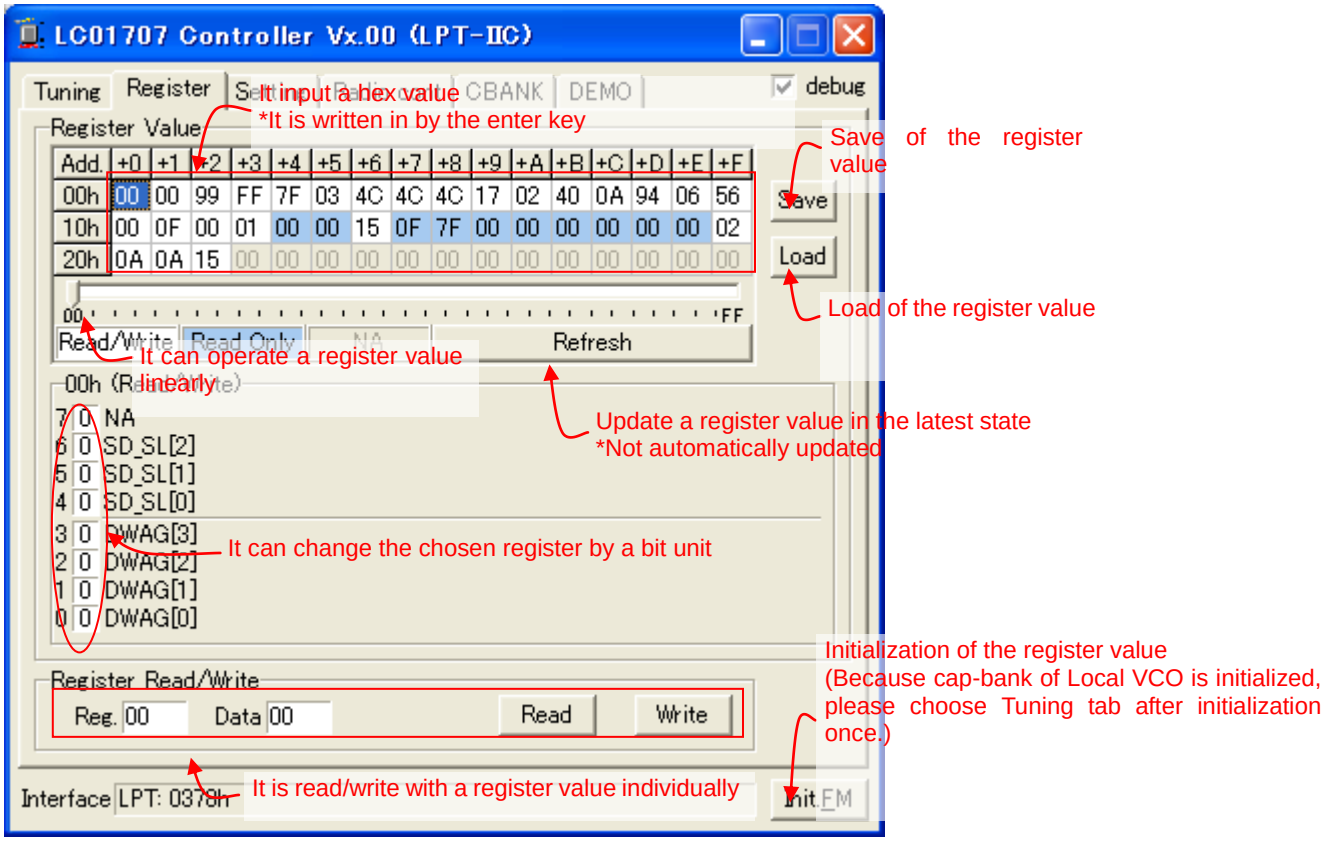
c. Step Frequency
Choose step frequency
*The step frequency of the Reg.02h(DFSEL) setting is 50kHz fixation

d. Image detection change ON-OFF check box
No check . . . Automatically image detection OFF
Check . . . Automatically image detection ON

e. Reception band limitation ON-OFF check box
No check (Normal) . . . Reception Band is 76MHz – 90MHz
Check (For Debugging) . . . The reception frequency range becomes same as VCO movement range

f. CPL Check button
You can confirm a CP terminal voltage form IIC by clicking it

• [Register] tab
Direct read/write can do a register value



4. How to end of controller

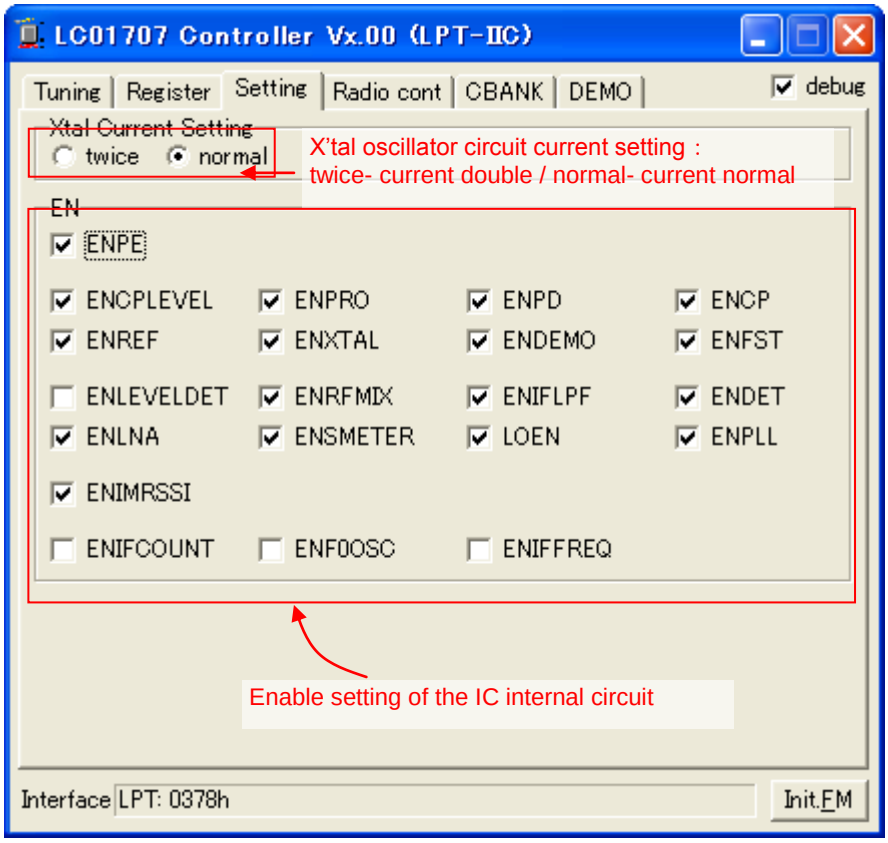
Please click ☒ button of the window top right corner

5. How to un-installation

Please delete the folder which you made with section 2.

6. Description of other tabs

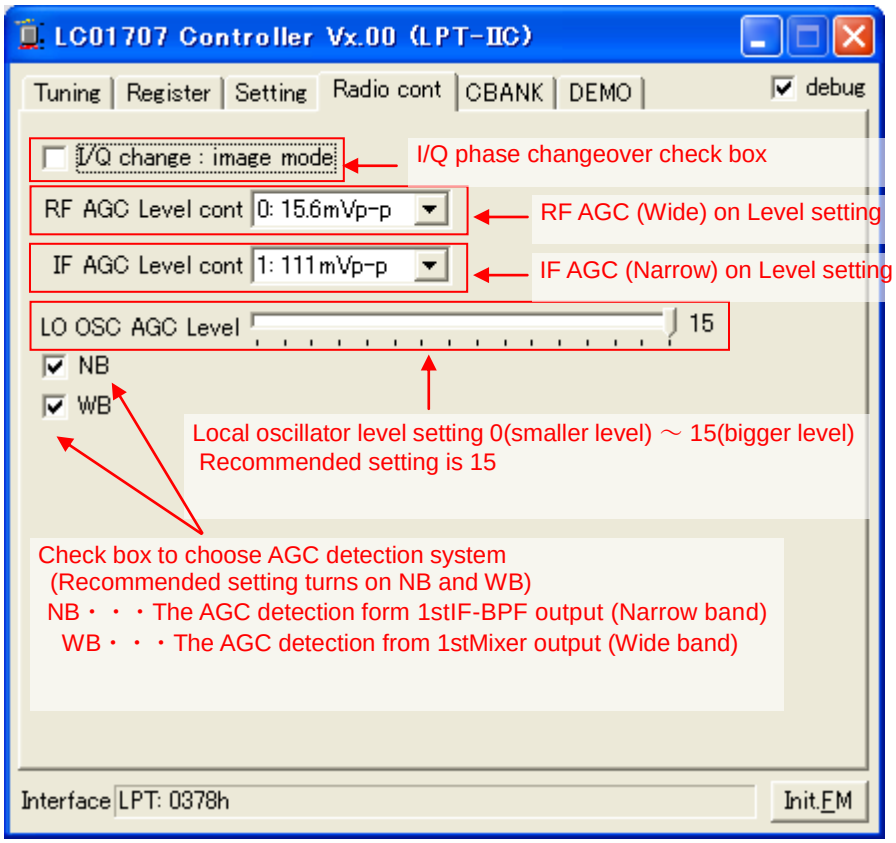
- [Setting] tab



About IC internal circuit enable setting

- ENPE . . . Whole circuit enable
- ENCPLEVEL . . . Charge pump level comparator enable
- ENPRO . . . Program counter enable
- ENPD . . . Phase comparator enable
- ENCP . . . Charge pump enable
- ENREF . . . Signal meter enable
- ENXTAL . . . X'tal oscillator enable
- ENDEMO . . . Demodulator enable
- ENFST . . . BPF and IF-AGC block enable
- ENLEVELDET . . . No use (OFF)
- ENRFMIX . . . RF-Mixer enable
- ENIFLPF . . . IF-LPF enable
- ENDET . . . Wide-AGC and Narrow-AGC enable
- ENLNA . . . LNA block enable
- ENSMETER . . . Reference counter enable
- LOEN . . . Local oscillator enable
- ENPLL . . . PLL block enable
- ENIMRSSI . . . X'tal oscillator circuit current setting enable
- ENIFCOUNT . . . Analog block frequency counter enable (IF counter), only at the time of scan
- ENF0OSC . . . f0 detection oscillator circuit enable, only at the time of setup and initial tuning
- ENIFFREQ . . . Logic block reference clock enable

• [Radio cont] tab

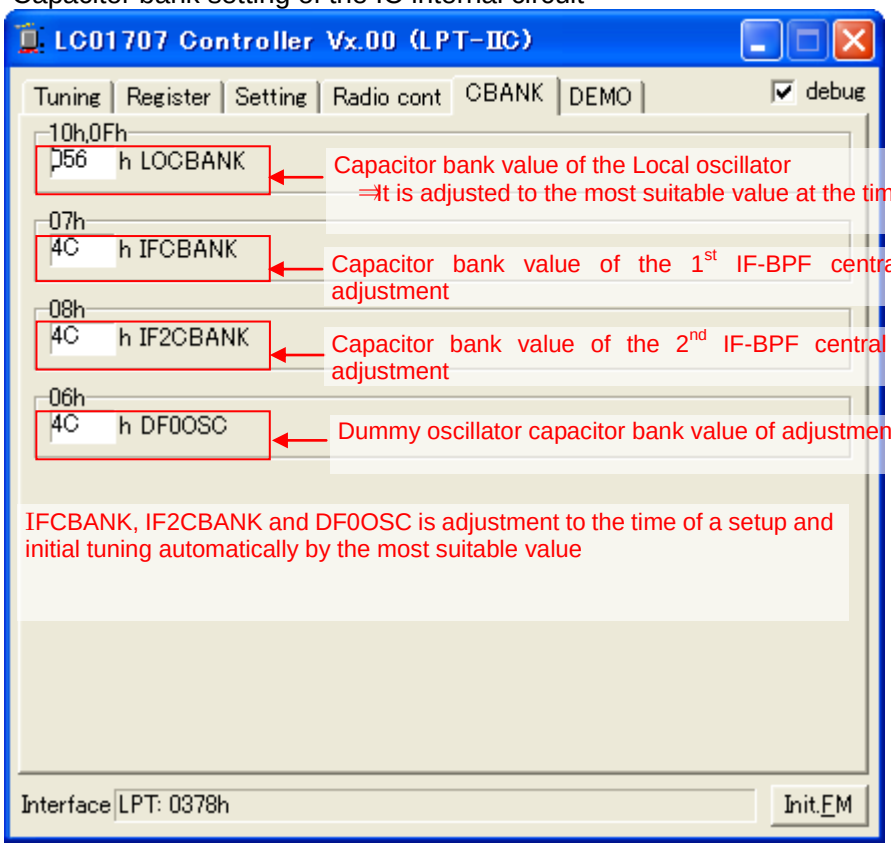


I/Q phase changeover check box . . . No check : Upper reception,
Check : When an imege frequency exists, it change to the Lower reception

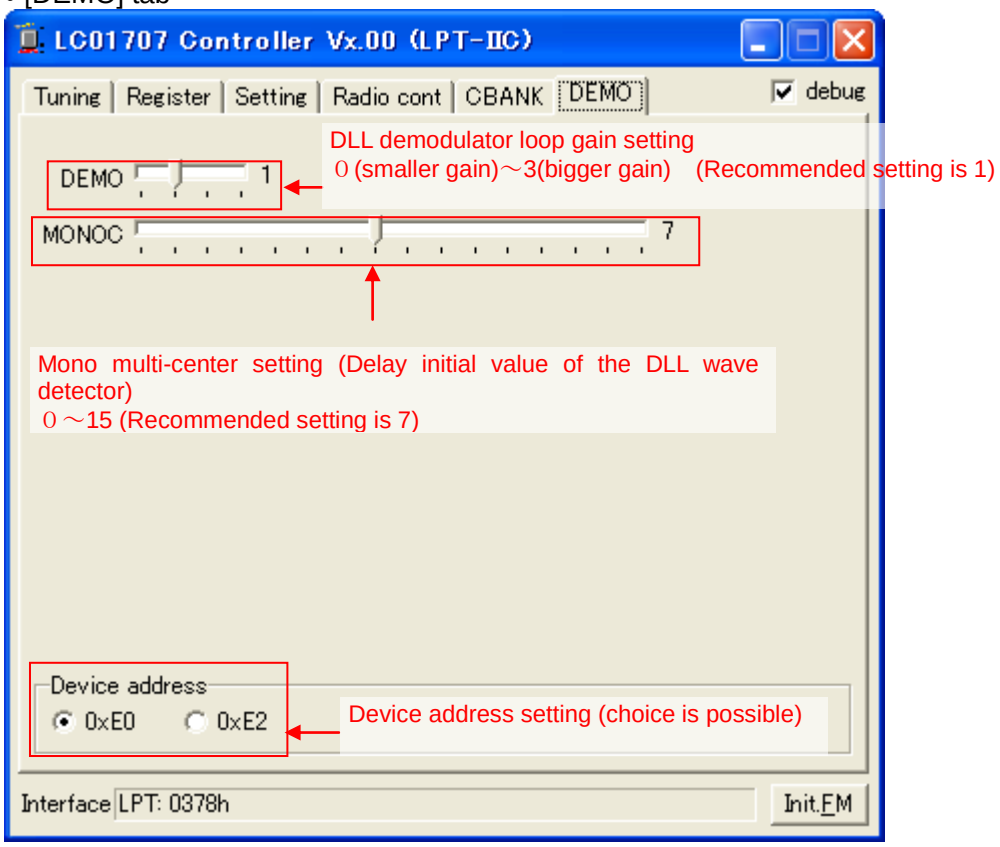
Please refer to Page 7 for the detailed movement of I/Q phase changeover check box.

• [CBANK] tab

Capacitor bank setting of the IC internal circuit



• [DEMO] tab



7. About an image detection change

The function of the image detection Upper/Lower change ON/OFF check box of Screen 1 is as follows.

When you checked it . . .

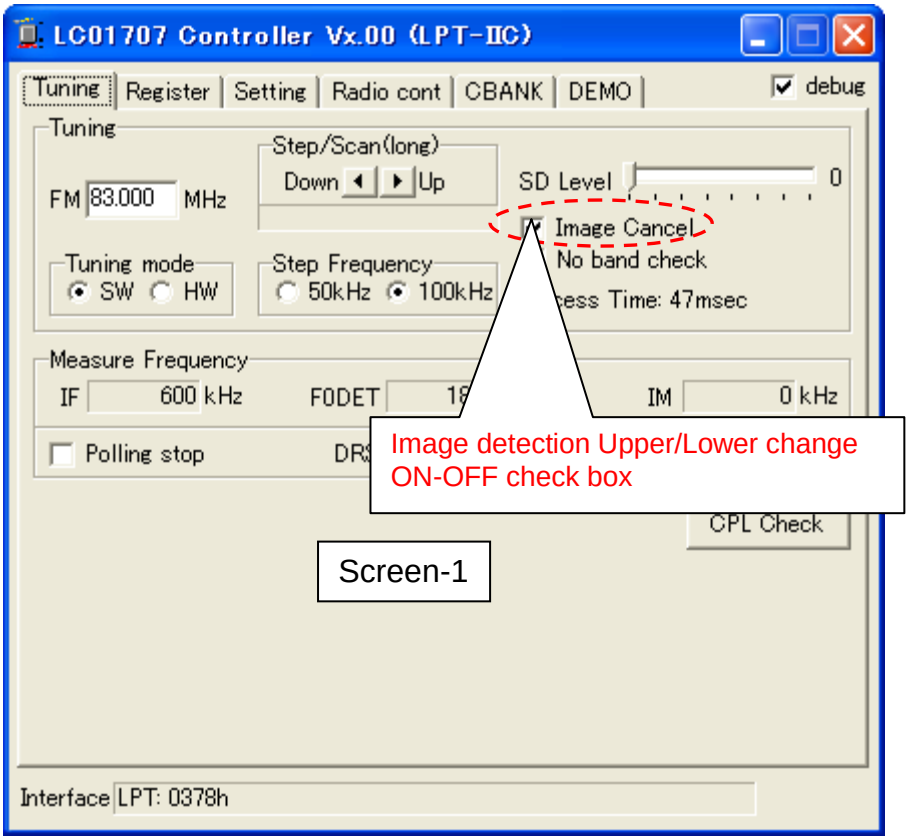
When an image detection function is ON, a Local oscillation changes to Upper or Lower automatically according to an image disturbance situation.

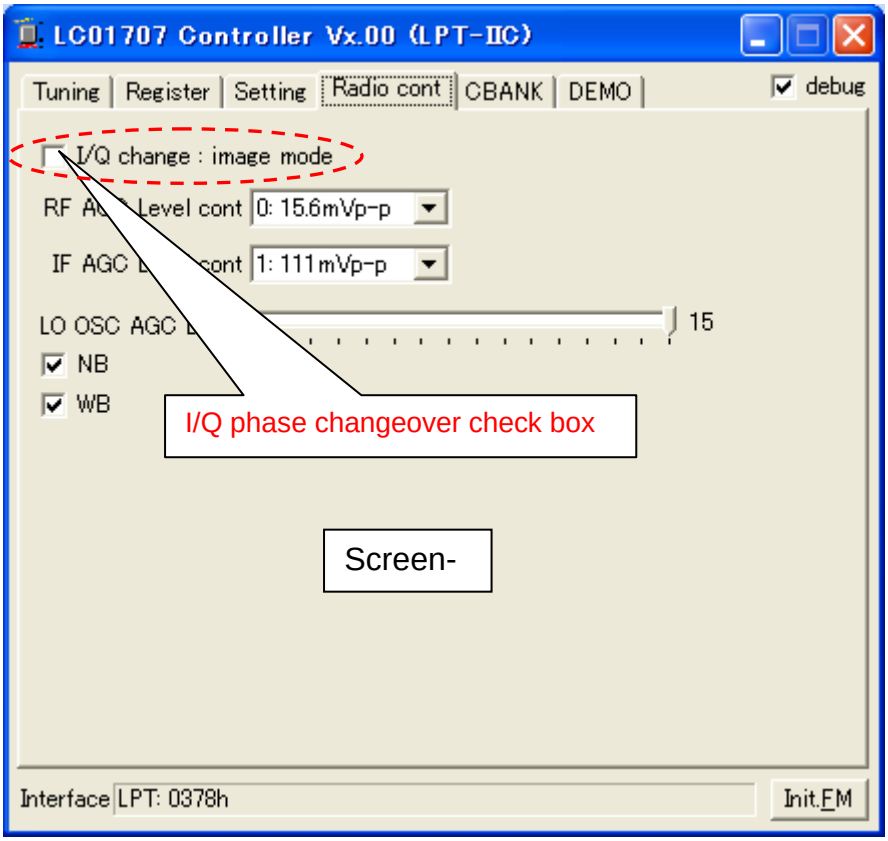
When there is no check . . .

An image detection function is turned off, and is not concerned with the existence of image disturbance, but usually becomes Upper reception.

When changing to Lower reception compulsorily, if the I/Q change check box of Screen 2 is turned on and it changes to the Tuning screen of Screen 1, it will not be concerned with the existence of image disturbance, but will become Lower reception.

If the I/Q change check box of Screen 2 is unchecked and it changes to the Tuning screen of Screen 1 also when changing from Lower reception to Upper reception, it will not be concerned with the existence of image disturbance, but will become Upper reception.




LC01707 Controller Vx.00 (LPT-IIC)
Tuning
Register
Setting
Radio cont
CBANK
DEMO
debug
I/Q change : image mode
Level cont
0: 15.6mVp-p
1: 111mVp-p
15
NB
WB
I/Q phase changeover check box
Screen-
Interface
LPT: 0378h
Init.FM

Communication specification:

Communication specifications are indicated as below:
Serial Interface (I^2C-bus);

Sending and receiving data through I^2C-bus that consists of two bus lines of a serial data line (SDA) and a serial clock line (SCL). This bus enables 8-bit bi-directional serial data to transmit at the maximum speed of 400kbits (fast mode). This is not compatible with Hs mode.

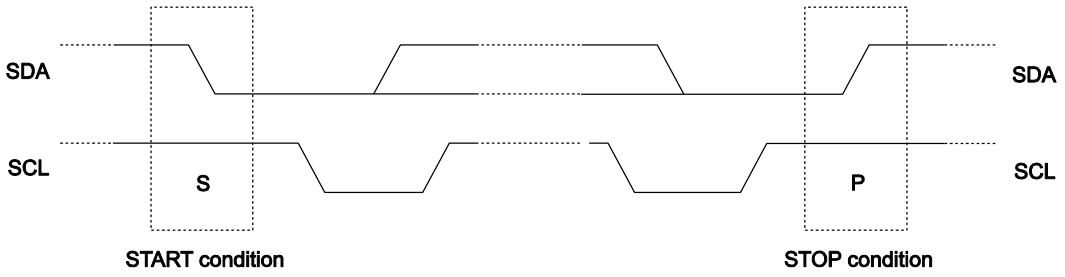
Terms used in I^2C

The following terms are used in I^2C

Terms	Description
Transmitter	Device to send data to the bus
Receiver	Device to receive from the bus
Master	Device to start data transmission, generate signal, and terminate data transmission
Slave	Device of which address is designated master

[Start] and [Stop] conditions

[Start] condition is required at the start of data communication and [Stop] condition at the end of data communication. The condition in which the SDA line changes from [H] to [L] with SCL at [H] is called the [Start] condition. The condition in which the SDA line changes from [L] to [H] with SCL at [H] is called the [Start] condition.

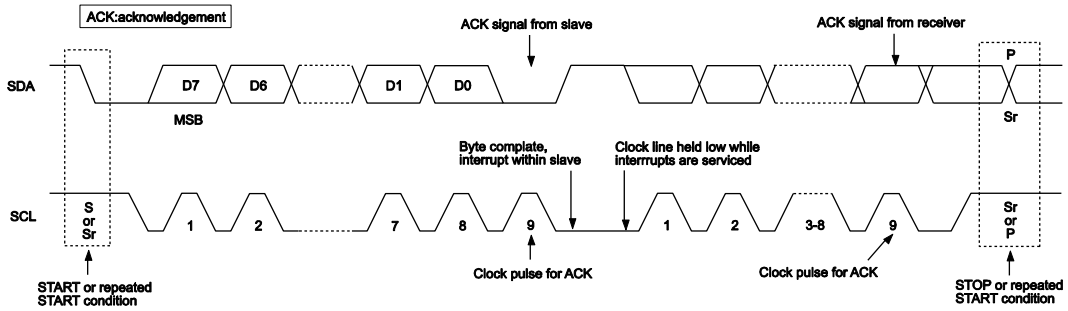


Data transmission

The length of each byte which is output to SDA line is always 8 bits. An acknowledge bit is needed after each byte. Data is transmitted sequentially from the most significant bit (MSB).

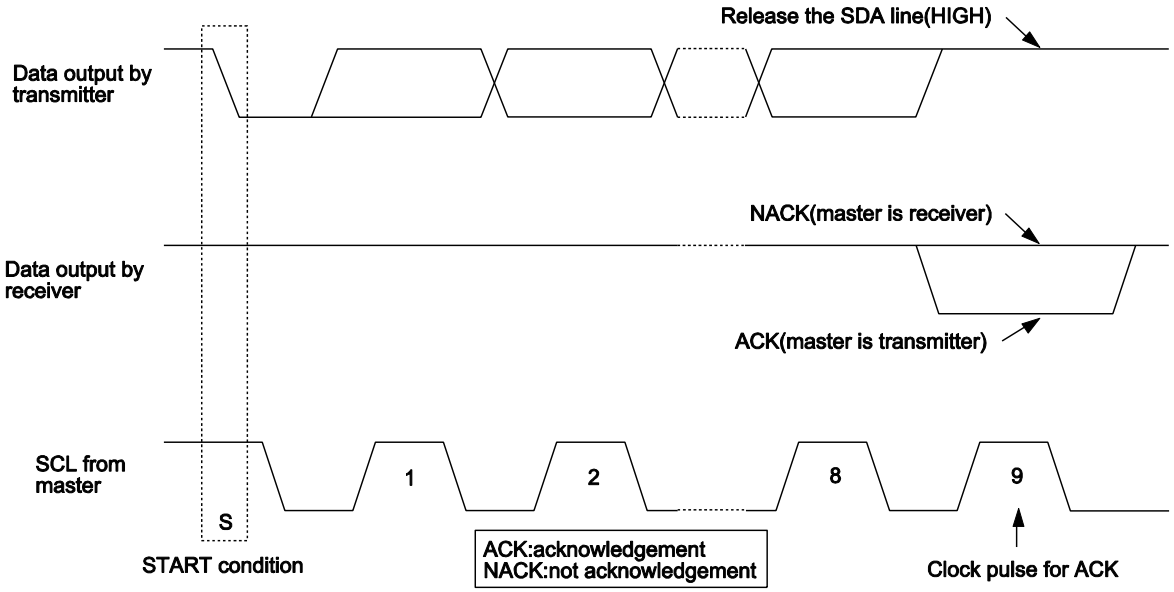
During the data transfer, the slave address is transmitted after the [Start] condition (S).

Data transfer is always ended by the [Stop] condition (P) generated by the master.



Acknowledge (Receive acknowledge)

When the master generates the acknowledge clock pulse, the transmitter opens the SDA line. (SDA line enters the [H] state.) When the acknowledge clock pulse is in the [H] state, the receiver sets the SDA line to [L] each time it receives one byte (eight bits) data. When the master works as a receiver, the master informs the slave of the end of data by omitting acknowledge at the end of data sent from the slave.

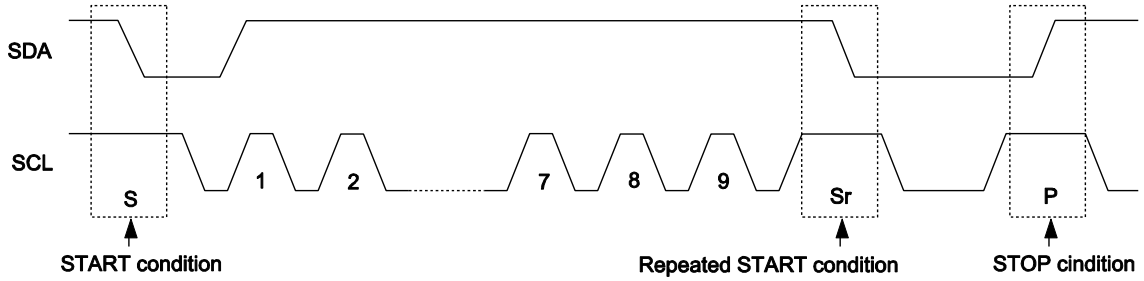


Software reset

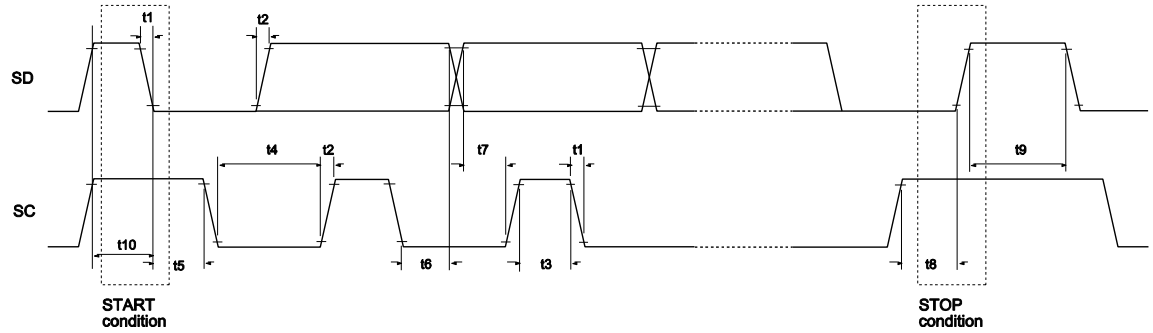
If the communication is interrupted (microcomputer reset, etc.), it is possible to communicate normally by entering the below signals and resetting the CPU in software.

*These signal timings restore the communication after its interruption. The register setting is never reset.

*Software reset command is incompatible with I^2C-bus format.



Electrical specification and timing for I/O stages



Bus line characteristics

Characteristic	Symbol	FAST-MODE		unit	Example at SCL = 100kHz
		min	max		
SCL clock frequency	fSCL		400	kHz	100
Fall time of SDA and SCL	t1	20+0.1Cb	300	ns	
Rise time of SDA and SCL	t2	20+0.1Cb	300	ns	
SCL “H” time	t3	0.6		μs	3
SCL “L” time	t4	1.3		μs	7
[Start] condition holding time	t5	0.6		μs	10
Data holding time for I^2C bus device	t6	0.3		μs	
Data setup time	t7	0.1		μs	3
[Stop] condition setup time	t8	0.6		μs	10
Bus free time between [Stop] and [Start]	t9	1.3		μs	20
[Start] condition setup time	t10	0.6		μs	
Bus line capacitive load	Cb		400	pF	

Serial interface voltage level V_{DD}: Communication bus voltage

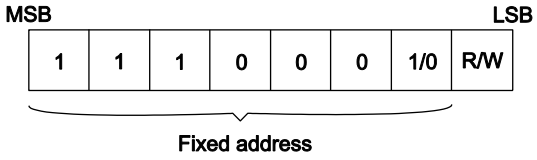
Characteristic	min	max	unit
High level input voltage	$0.7V_{DD}$	V_{DD}	V
Low level input voltage	0.0	$0.3V_{DD}$	V
High level output voltage (open drain)	V_{DD} *2		V
Low level output voltage (open drain)	0.0	$0.2V_{DD}$	V

*2: Output impedance of open drain becomes high at the high level output voltage.
Output voltage equals to V_{DD} (voltage =V_{DD}) since drain is pulled up to V_{DD}.

Definition of each bit

1) Slave address

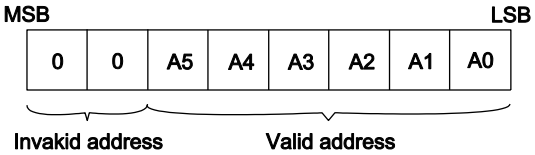
The slave address consists of seven-bit fixed address "1110000" or "1110001", which is unique to a chip, and the eighth-bit data direction bit(R/W). Sending (writing) is processed when the data direction bit is"0", and receiving (reading) is processed when it is "1". The fixed address is set to "1110001" at DEVAR=1 and it is set to "1110000" at
DEVAR=0.



R/W	BIT
READ	1
WRITE	0

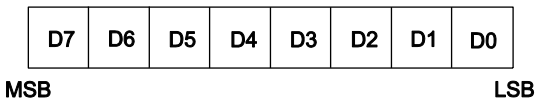
2) Register address

Since the total number of internal register is 34, 2-bit data set on the MSB side becomes invalid. 64 addresses are accepted 6 bits are used, but only 34 registers are used.



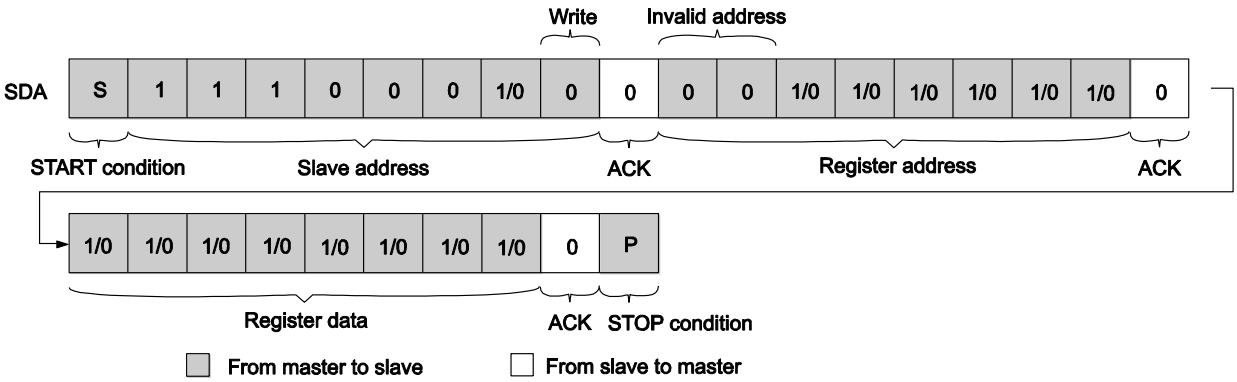
3) Register data

Each register data consists of eight bits.

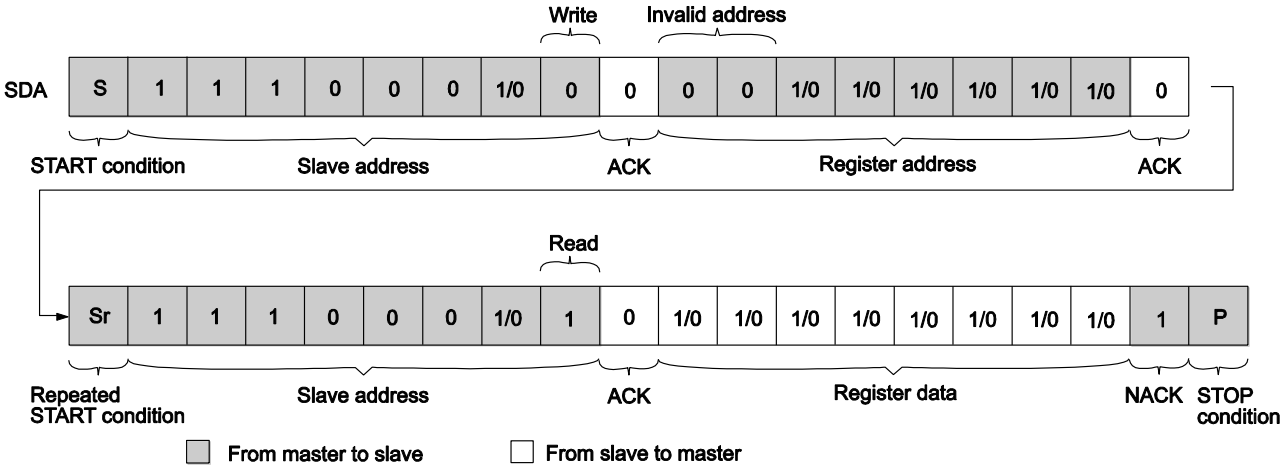


Command Format

1) Individual registers data writing



2) Individual registers data reading



SD pin specification

SD voltage level V_{DD}: supply voltage

item	min	max	unit
High level output voltage	V_{DD}-0.8	V_{DD}	V
Low level output voltage	0	0.4	V

Software development manual:

Index

Introduction

In this application note of LC01707PLF, the method of controlling the FM multiple Tuner IC, LC01707PLF which incorporates FM FE, IF,IF-Filter, PLL,FM-DEMO and LPF for car is described.

Chip Description

The configuration of LC01707PLF register is 35 x 8 bits. Transmission and reception to LC01707PLF chip is performed via IIC from a host microcomputer. (Refer to LC01707PLF data sheet about IIC specification.)

Also local oscillation signal for 1st MIX is made from VCO four times the frequency of the signal. 1st IF frequency is 1.2MHz and 2nd IF frequency is 600KHz.

POWER ON

Input into LC01707PLF chip in order of software reset and an initial-setting value after a power supply injection. The following is Register Map and initial data.

1-1. Register Map

Register Address	BIT	R/W	Bit name	Function
00h	7			Not use
	6	R/W	SD_SL[2]	Setting of SD level. (0:DRS0, 1:DRS1, 2:DRS2, 3:DRS3, 4:DRS4, 5:DRS5, 6:DRS6, 7:DRS7)
	5	R/W	SD_SL[1]	
	4	R/W	SD_SL[0]	
	3	R/W	DWAG[3]	Setting of wide band AGC level. (0:15.6mVp-p, 1:31.3mVp-p, 2:46.9mVp-p, 3:62.5mVp-p, 4:78.1mVp-p, 5:93.8mVp-p, 6:109.4mVp-p, 7:125.0mVp-p, 8:140.6mVp-p, 9:156.3mVp-p, 10:171.9mVp-p, 11:187.5mVp-p, 12:203.1mVp-p, 13:218.8mVp-p, 14:234.4mVp-p, 15:250mVp-p)
	2	R/W	DWAG[2]	
	1	R/W	DWAG[1]	
	0	R/W	DWAG[0]	
01h	7			Not use
	6			Not use
	5			Not use
	4			Not use
	3			Not use
	2			Not use
	1		IMSD_SL[1]	Not use
	0		IMSD_SL[0]	
02h	7	R/W	CLKIN	Xtal colpitts current source (1:normal, 0: twice)
	6	R/W	DLOCKSEL	LOCKDET selection of output wave (1: The number of times of comparison=6, 0: The number of times of comparison=3)
	5	R/W	DFSEL[1]	Selection of channel step (0:100kHz, 1 or 2:50kHz, 3:25kHz)
	4	R/W	DFSEL[0]	
	3	R/W	ENPE	Enable whole circuit (1:ON, 0:OFF)
	2	R/W	DNGA[2]	Setting of narrow band AGC level (0:35mVp-p,1:111mVp-p, 2:187mVp-p, 3:263mVp-p, 4:339mVp-p, 5:415mVp-p, 6:491mVp-p, 7:567mVp-p)
	1	R/W	DNGA[1]	
	0	R/W	DNGA[0]	
03h	7	R/W	ENCPLEVEL	Enable CP (charge pump) level comparator (1:ON, 0:OFF)
	6	R/W	DENPRO	Enable program counter (1:ON, 0:OFF)
	5	R/W	DENPD	Enable phase comparator (1:ON, 0:OFF)
	4	R/W	DENCP	Enable CP circuit (1:ON, 0:OFF)
	3	R/W	DENREF	Enable S-meter circuit (1:ON, 0:OFF)
	2	R/W	DENXTAL	Enable X'tal circuit (1:ON, 0:OFF)
	1	R/W	DENDEMO	Enable demodulator circuit (1:ON, 0:OFF)
	0	R/W	ENFST	Enable complex BPF block and IF AGC block (1:ON, 0:OFF)
04h	7	R/W	DENLEVELDET	Enable Cap bank control circuit (1:ON, 0:OFF)
	6	R/W	ENRFMIX	Enable RF MIX circuit (1:ON, 0:OFF)
	5	R/W	ENIFLPF	Enable IF LPF block (1:ON, 0:OFF)
	4	R/W	ENDET	Enable W_AGC, N_AGC block (1:ON, 0:OFF)
	3	R/W	ENLNA	Enable LNA circuit (1:ON, 0:OFF)
	2	R/W	DENSMETER	Enable reference counter (1:ON, 0:OFF)
	1	R/W	DLOEN	Enable local oscillator (1:ON, 0:OFF)
	0	R/W	DENPLL	Enable PLL block (1:ON, 0:OFF)

Register Address	BIT	R/W	Bit name	Function
05h	7			Not use
	6			Not use
	5			Not use
	4			Not use
	3			Not use
	2			Not use
	1	R/W	DNBAGC	Setting of narrow band AGC detection (1:ON, 0:OFF)
	0	R/W	DWBAGC	setting wide band AGC detection (1:ON, 0:OFF)
06h	7	R/W	DF0OSC[7]	Capacitor bank value Adjustment of oscillator frequency for setting of reference time constant
	6	R/W	DF0OSC[6]	
	5	R/W	DF0OSC[5]	
	4	R/W	DF0OSC[4]	
	3	R/W	DF0OSC[3]	
	2	R/W	DF0OSC[2]	
	1	R/W	DF0OSC[1]	
	0	R/W	DF0OSC[0]	
07h	7	R/W	DBPFO[7]	Capacitor bank value Complex BPF F0 adjustment
	6	R/W	DBPFO[6]	
	5	R/W	DBPFO[5]	
	4	R/W	DBPFO[4]	
	3	R/W	DBPFO[3]	
	2	R/W	DBPFO[2]	
	1	R/W	DBPFO[1]	
	0	R/W	DBPFO[0]	
08h	7	R/W	D2BPF[7]	Capacitor bank value 2^{nd} IF BPF F0 adjustment
	6	R/W	D2BPF[6]	
	5	R/W	D2BPF[5]	
	4	R/W	D2BPF[4]	
	3	R/W	D2BPF[3]	
	2	R/W	D2BPF[2]	
	1	R/W	D2BPF[1]	
	0	R/W	D2BPF[0]	
09h	7			Not use
	6			Not use
	5	R/W	DDEMOG[1]	Setting of DLL demodulator loop gain
	4	R/W	DDEMOG[0]	
	3	R/W	DMONOC[3]	Setting of mono-multi center
	2	R/W	DMONOC[2]	
	1	R/W	DMONOC[1]	
	0	R/W	DMONOC[0]	

Register Address	BIT	R/W	Bit name	Function
0Ah	7			Not use
	6			Not use
	5			Not use
	4			Not use
	3			Not use
	2			Not use
	1	R/W	ENIMRSSI	Setting of Xtal colpitts source follower transistor size (1:Normal size, 0: Twice size)
	0	R/W	DIQC	Switching of Complex BPF injection (0:upper, 1:lower)
0Bh	7			Not use
	6	R/W	DBL[6]	Adjustment of IQ balance
	5	R/W	DBL[5]	
	4	R/W	DBL[4]	
	3	R/W	DBL[3]	
	2	R/W	DBL[2]	
	1	R/W	DBL[1]	
	0	R/W	DBL[0]	
0Ch	7			Not use
	6			Not use
	5			Not use
	4			Not use
	3	R/W	DCP1REF[3]	Setting of charge pump output current value 0:0mA, 1:0.1mA, 2:0.2mA, 3:0.3mA, 4,0.4mA, 5:0.5mA, 6:0.6mA 7:0.7mA, 8:0.8mA, 9:0.9mA, A:1mA, B:1.1mA, C:1.2mA, D:Not use, E:Not use F:Not use
	2	R/W	DCP1REF[2]	
	1	R/W	DCP1REF[1]	
	0	R/W	DCP1REF[0]	
0Dh	7	R/W	DPCNT_L[7]	Dividing frequency N value(Lower 8bits) * Refer 2-3 for details
	6	R/W	DPCNT_L[6]	
	5	R/W	DPCNT_L[5]	
	4	R/W	DPCNT_L[4]	
	3	R/W	DPCNT_L[3]	
	2	R/W	DPCNT_L[2]	
	1	R/W	DPCNT_L[1]	
	0	R/W	DPCNT_L[0]	
0Eh	7	R/W	DPCNT_H[7]	Dividing frequency N value (Upper 8bits) * Refer 2-3 for details
	6	R/W	DPCNT_H[6]	
	5	R/W	DPCNT_H[5]	
	4	R/W	DPCNT_H[4]	
	3	R/W	DPCNT_H[3]	
	2	R/W	DPCNT_H[2]	
	1	R/W	DPCNT_H[1]	
	0	R/W	DPCNT_H[0]	

Register Address	BIT	R/W	Bit name	Function
0Fh	7	R/W	DCBANK_L[7]	Setting of local oscillator capacitor bank
	6	R/W	DCBANK_L[6]	
	5	R/W	DCBANK_L[5]	
	4	R/W	DCBANK_L[4]	
	3	R/W	DCBANK_L[3]	
	2	R/W	DCBANK_L[2]	
	1	R/W	DCBANK_L[1]	
	0	R/W	DCBANK_L[0]	
10h	7			Not use
	6			Not use
	5			Not use
	4			Not use
	3			Not use
	2			Not use
	1			Not use
	0	R/W	DCBANK_H[8]	Setting of local oscillator capacitor bank
11h	7			Not use
	6			Not use
	5			Not use
	4		DCBEN	Not use
	3	R/W	DLOALC[3]	Setting of oscillation level of local oscillator
	2	R/W	DLOALC[2]	
	1	R/W	DLOALC[1]	
	0	R/W	DLOALC[0]	
12h	7			Not use
	6	R/W	DENIFCOUNT	Enable frequency counter (analog block) (1:ON, 0:OFF)
	5	R/W	DENF0OSC	Enable F0 detection oscillator circuit (1:ON, 0:OFF)
	4	R/W	DENIFFREQ	Enable reference clock of logic part (1:ON, 0:OFF)
	3			Not use
	2	R/W	DSCTCOUNT[2]	Switching of count frequency 0:Not use, 1:IF frequency, 2: pre-scaler frequency, 3: pre-scaler frequency, 4:f0 detection oscillatory frequency , 5: f0 detection oscillatory frequency, 6: Not use, 7:IF frequency
	1	R/W	DSCTCOUNT[1]	
	0	R/W	DSCTCOUNT[0]	
13h	7			Not use
	6			Not use
	5			Not use
	4			Not use
	3			Not use
	2	R/W	CTE	Count start trigger (1:ON, becomes 0 by the automatic operation)
	1	R/W	GT[1]	Switching of frequency counter gate time (0:4msec, 1:8msec, 2:32msec, 3:64msec)
	0	R/W	GT[0]	

Register Address	BIT	R/W	Bit name	Function
14h	7	R	LOFQ_L[7]	LO_COUNT value (Lower 8bits)
	6	R	LOFQ_L[6]	
	5	R	LOFQ_L[5]	
	4	R	LOFQ_L[4]	
	3	R	LOFQ_L[3]	
	2	R	LOFQ_L[2]	
	1	R	LOFQ_L[1]	
	0	R	LOFQ_L[0]	
15h	7	R	LOFQ_H[7]	LO_COUNT value (Upper 8bits)
	6	R	LOFQ_H[6]	
	5	R	LOFQ_H[5]	
	4	R	LOFQ_H[4]	
	3	R	LOFQ_H[3]	
	2	R	LOFQ_H[2]	
	1	R	LOFQ_H[1]	
	0	R	LOFQ_H[0]	
16h	7			Not use
	6			Not use
	5		COUNTSEL	Not use
	4		LOCKDETSEL	Not use
	3		LOCKDET_DIG	Not use
	2	R/W	LOCKDET	LOCK detection (1:LOCK, 0:UNLOCK)
	1	R/W	PHLEVEL[1]	Detection of charge pump voltage level (0: less than 0.5V, 1:0.5V-2.8V, 2: not use, 3: more than 2.8V)
	0	R/W	PHLEVEL[0]	
17h	7			Not use
	6			Not use
	5			Not use
	4			Not use
	3	R	IMRSSI[3]	Reset detection circuit (0:reset , 1:reset release)
	2	R	IMRSSI[2]	
	1	R	IMRSSI[1]	
	0	R	IMRSSI[0]	
18h	7			Not use
	6	R	DRS[6]	S-meter detection level
	5	R	DRS[5]	
	4	R	DRS[4]	
	3	R	DRS[3]	
	2	R	DRS[2]	
	1	R	DRS[1]	
	0	R	DRS[0]	

Register Address	BIT	R/W	Bit name	Function
19h	7	R	IFCOUNT_L[7]	IF count value (Lower 8bits)
	6	R	IFCOUNT_L[6]	2^{nd} IF frequency measurement result
	5	R	IFCOUNT_L[5]	
	4	R	IFCOUNT_L[4]	
	3	R	IFCOUNT_L[3]	
	2	R	IFCOUNT_L[2]	
	1	R	IFCOUNT_L[1]	
	0	R	IFCOUNT_L[0]	
1Ah	7	R	IFCOUNT_H[7]	IF count value (Upper 8bits)
	6	R	IFCOUNT_H[6]	
	5	R	IFCOUNT_H[5]	
	4	R	IFCOUNT_H[4]	
	3	R	IFCOUNT_H[3]	
	2	R	IFCOUNT_H[2]	
	1	R	IFCOUNT_H[1]	
	0	R	IFCOUNT_H[0]	
1Bh	7	R	IMCOUNT_L[7]	Not use
	6	R	IMCOUNT_L[6]	
	5	R	IMCOUNT_L[5]	
	4	R	IMCOUNT_L[4]	
	3	R	IMCOUNT_L[3]	
	2	R	IMCOUNT_L[2]	
	1	R	IMCOUNT_L[1]	
	0	R	IMCOUNT_L[0]	
1Ch	7	R	IMCOUNT_H[7]	Not use
	6	R	IMCOUNT_H[6]	
	5	R	IMCOUNT_H[5]	
	4	R	IMCOUNT_H[4]	
	3	R	IMCOUNT_H[3]	
	2	R	IMCOUNT_H[2]	
	1	R	IMCOUNT_H[1]	
	0	R	IMCOUNT_H[0]	
1Dh	7	R	F0_L[7]	F0 count value (Lower 8bits)
	6	R	F0_L[6]	
	5	R	F0_L[5]	
	4	R	F0_L[4]	
	3	R	F0_L[3]	
	2	R	F0_L[2]	
	1	R	F0_L[1]	
	0	R	F0_L[0]	

Register Address	BIT	R/W	Bit name	Function
1Eh	7	R	F0_H[7]	F0 count value (Upper 8bits)
	6	R	F0_H[6]	
	5	R	F0_H[5]	
	4	R	F0_H[4]	
	3	R	F0_H[3]	
	2	R	F0_H[2]	
	1	R	F0_H[1]	
	0	R	F0_H[0]	
1Fh	7			Not use
	6			Not use
	5			Not use
	4			Not use
	3			Not use
	2	R/W	DOUTSEL	TEST register
	1	R/W	DCNTEST	TEST register
	0	R/W	DOUTTEST	TEST register
20h	7			Not use
	6	R/W	ERR2	Local Oscillator capacitor bank control error flag 2
	5	R/W	ERR1	Local Oscillator capacitor bank control error flag 1
	4	R/W	DCOSEL2	Switching of Local Oscillator capacitor bank value (1: capacitor bank control, 0:I2C input value)
	3	R/W	DCOSEL1	Switching of Local Oscillator capacitor bank control /Compensation processing after successive comparison (1:On. 0: Off)
	2	R/W	DCOSEL0	Switching of Local Oscillator capacitor bank control (Micro adjustment processing (1:On, 0: Off)
	1	R/W	DWAITSEL[1]	Waiting time for the check of PLL operation after adjustment of Local Oscillator capacitor bank (0:0.2msec, 1:0.4msec, 2:0.8usec, 3:1.6msec)
	0	R/W	DWAITSEL[0]	
21h	7			Not use
	6			Not use
	5	R/W	DENINT	Register for TEST
	4	R/W	MASLSEL	Register for TEST
	3	R/W	LOSEL	Register for TEST
	2	R/W	INTPH	Register for TEST
	1	R/W	INTIM	Register for TEST
	0	R/W	INTLO	Register for TEST
22h	7	R/W	TESTSEL[2]	Register for TEST
	6	R/W	TESTSEL[1]	
	5	R/W	TESTSEL[0]	
	4	R/W	DSW	PLL loop filter ON/OFF(1:ON 0:OFF)
	3	R/W	TIMESEL2[1]	Setting of lock of correcting circuit of Local Oscillator
	2	R/W	TIMESEL2[0]	capacitor bank control (0:0.2msec, 1:0.4msec, 2:0.8msec, 3:1.6msec)
	1	R/W	TIMESEL[1]	Setting of lock of successive comparison control operation of Local Oscillator capacitor bank control
	0	R/W	TIMESEL[0]	(0:10usec, 1:20usec, 2:40usec, 3:80usec)

1-2. Initial Setting

*Transmit data in order in the table.

Register Address	BIT	Bit name	Binary value	Hex value	Memo
00h	7		0	00h	Not use
	6	SD_SL[2]	0		Setting of SD level
	5	SD_SL[1]	0		
	4	SD_SL[0]	0		
	3	DWAG[3]	0		Setting of wide band AGC detection level
	2	DWAG[2]	0		
	1	DWAG[1]	0		
	0	DWAG[0]	0		
01h	7		0	00h	Not use
	6		0		Not use
	5		0		Not use
	4		0		Not use
	3		0		Not use
	2		0		Not use
	1	IMSD_SL[1]	0		Not use
	0	IMSD_SL[0]	0		
02h	7	CLKIN	0	06h	Setting of Xtal colpitts current
	6	DLOCKSEL	0		Switching of LOCKDET output wave
	5	DFSEL[1]	0		Switching of channel step
	4	DFSEL[0]	0		
	3	ENPE	0		Enable whole
	2	DNGA[2]	1		Setting of narrow band AGC level
	1	DNGA[1]	1		
	0	DNGA[0]	0		
05h	7		0	03h	Not use
	6		0		Not use
	5		0		Not use
	4		0		Not use
	3		0		Not use
	2		0		Not use
	1	DNBAGC	1		Switching of narrow band AGC
	0	DWBAGC	1		Switching of wide band AGC
06h	7	DF0OSC[7]	1	80h	Capacitor bank value
	6	DF0OSC[6]	0		
	5	DF0OSC[5]	0		
	4	DF0OSC[4]	0		
	3	DF0OSC[3]	0		
	2	DF0OSC[2]	0		
	1	DF0OSC[1]	0		
	0	DF0OSC[0]	0		

Register address	BIT	Bit name	Binary value	Hex value	Memo
07h	7	DBPFO[7]	1	80h	Capacitor bank value
	6	DBPFO[6]	0		
	5	DBPFO[5]	0		
	4	DBPFO[4]	0		
	3	DBPFO[3]	0		
	2	DBPFO[2]	0		
	1	DBPFO[1]	0		
	0	DBPFO[0]	0		
08h	7	D2BPF[7]	1	80h	Capacitor bank value
	6	D2BPF[6]	0		
	5	D2BPF[5]	0		
	4	D2BPF[4]	0		
	3	D2BPF[3]	0		
	2	D2BPF[2]	0		
	1	D2BPF[1]	0		
	0	D2BPF[0]	0		
09h	7		0	17h	Not use
	6		0		Not use
	5	DDEMOG[1]	0		Setting of DLL demodulator loop gain
	4	DDEMOG[0]	1		
	3	DMONOC[3]	0		Setting of mono-multi center
	2	DMONOC[2]	1		
	1	DMONOC[1]	1		
	0	DMONOC[0]	1		
0Ah	7		0	00h	Not use
	6		0		Not use
	5		0		Not use
	4		0		Not use
	3		0		Not use
	2		0		Not use
	1	ENIMRSSI	0		Setting of Xtal colpitts source follower transistor
	0	DIQC	0		Switching of Complex BPF injection
0Bh	7		0	40h	Not use
	6	DBL[6]	1		Setting of IQ balance
	5	DBL[5]	0		
	4	DBL[4]	0		
	3	DBL[3]	0		
	2	DBL[2]	0		
	1	DBL[1]	0		
	0	DBL[0]	0		

Register address	BIT	Bit name	Binary value	Hex value	Memo
0Ch	7		0	0Ah	Not use
	6		0		Not use
	5		0		Not use
	4		0		Not use
	3	DCP1REF[3]	1		Setting of charge pump output current value
	2	DCP1REF[2]	0		
	1	DCP1REF[1]	1		
	0	DCP1REF[0]	0		
0Fh	7	DCBANK_L[7]	0	00h	Setting of Local Oscillator capacitor bank
	6	DCBANK_L[6]	0		
	5	DCBANK_L[5]	0		
	4	DCBANK_L[4]	0		
	3	DCBANK_L[3]	0		
	2	DCBANK_L[2]	0		
	1	DCBANK_L[1]	0		
	0	DCBANK_L[0]	0		
10h	7		0	01h	Not use
	6		0		Not use
	5		0		Not use
	4		0		Not use
	3		0		Not use
	2		0		Not use
	1		0		Not use
	0	DCBANK_H[8]	1		Setting of Local Oscillator capacitor bank
11h	7		0	0Fh	Not use
	6		0		Not use
	5		0		Not use
	4	DCBEN	0		Not use
	3	DLOALC[3]	1		Setting of Local Oscillator oscillation level
	2	DLOALC[2]	1		
	1	DLOALC[1]	1		
	0	DLOALC[0]	1		
1Fh	7		0	02h	Not use
	6		0		Not use
	5		0		Not use
	4		0		Not use
	3		0		Not use
	2	DOUTSEL	0		TEST register
	1	DCNTEST	1		TEST register
	0	DOUTTEST	0		TEST register

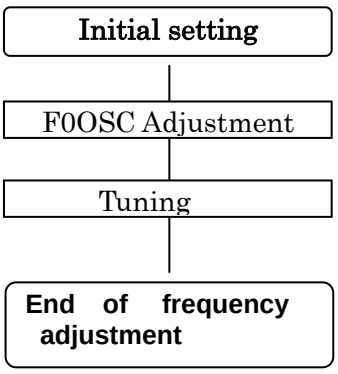
Register address	BIT	Bit name	Binary value	Hex value	Memo
20h	7		0	0Ah	Not use
	6	ERR2	0		Local Oscillator capacitor bank control error flag 2
	5	ERR1	0		Local Oscillator capacitor bank control error flag 1
	4	DCOSEL2	0		Switching of Local Oscillator capacitor bank value
	3	DCOSEL1	1		Switching of Local Oscillator capacitor bank control
	2	DCOSEL0	0		Switching of Local Oscillator capacitor bank control (Micro adjustment)
	1	DWAITSEL[1]	1		Waiting time for the check of PLL operation after adjustment of Local Oscillator capacitor bank
	0	DWAITSEL[0]	0		
21h	7		0	0Ah	Not use
	6		0		Not use
	5	DENINT	0		Register for TEST
	4	MASKSEL	0		
	3	LOSEL	1		
	2	INTPH	0		
	1	INTIM	1		
	0	INTLO	0		
02h	7	CLKIN	1	99h	Setting of Xtal colpitts current
	6	DLOCKSEL	0		Switching of LOCKDET output wave
	5	DFSEL[1]	0		Switching of channel step
	4	DFSEL[0]	1		
	3	ENPE	1		Enable whole
	2	DNGA[2]	0		Setting of narrow band AGC level
	1	DNGA[1]	0		
	0	DNGA[0]	1		
03h	7	ENCPLEVEL	1	FFh	Enable
	6	DENPRO	1		Enable
	5	DENPD	1		Enable
	4	DENCP	1		Enable
	3	DENREF	1		Enable
	2	DENXTAL	1		Enable
	1	DENDEMO	1		Enable
	0	ENFST	1		Enable
04h	7	DENLEVELDET	0	7Fh	Enable
	6	ENRFMIX	1		Enable
	5	ENIFLPF	1		Enable
	4	ENDET	1		Enable
	3	ENLNA	1		Enable
	2	DENSMETER	1		Enable
	1	DLOEN	1		Enable
	0	DENPLL	1		Enable

Register address	BIT	Bit name	Binary value	Hex value	Memo
0Ah	7		0	02h	Not use
	6		0		Not use
	5		0		Not use
	4		0		Not use
	3		0		Not use
	2		0		Not use
	1	ENIMRSSI	1		Setting of Xtal colpitts source follower transistor
	0	DIQC	0		Switching of complex BPF injection
12h	7		0	00h	Not use
	6	DENIFCOUNT	0		Enable frequency counter
	5	DENF0OSC	0		Enable F0 oscillator circuit
	4	DENIFFREQ	0		Enable reference clock of logic part
	3		0		Not use
	2	DSCTCOUNT[2]	0		Switching of count frequency
	1	DSCTCOUNT[1]	0		
	0	DSCTCOUNT[0]	0		
13h	7		0	01h	Not use
	6		0		Not use
	5		0		Not use
	4		0		Not use
	3		0		Not use
	2	CTE	0		Count start trigger
	1	GT[1]	0		Switching of gate time
	0	GT[0]	1		
16h	7		0	10h	Not use
	6		0		Not use
	5	COUNTSEL	0		Not use
	4	LOCKDETSEL	1		Not use
	3	LOCKDET_DIG	0		Not use
	2	LOCKDET	0		LOCK detection
	1	PHLEVEL[1]	0		Detection of CP output level
	0	PHLEVEL[0]	0		
22h	7	TESTSEL[2]	0	15h	Register for TEST
	6	TESTSEL[1]	0		
	5	TESTSEL[0]	0		
	4	DSW	1		ON/OFF of PLL loop filter
	3	TIMESEL2[1]	0		Setting of lock of correcting circuit of Local Oscillator capacitor bank control
	2	TIMESEL2[0]	1		
	1	TIMESEL[1]	0		Setting of lock of successive comparison control operation of Local Oscillator
	0	TIMESEL[0]	1		capacitor bank control

*It may be reference value. Set it voluntarily.*Refer to register map for a detailed function.

2-1. Tuning Method

The following shows the flow chart from Initialization to Tuning.

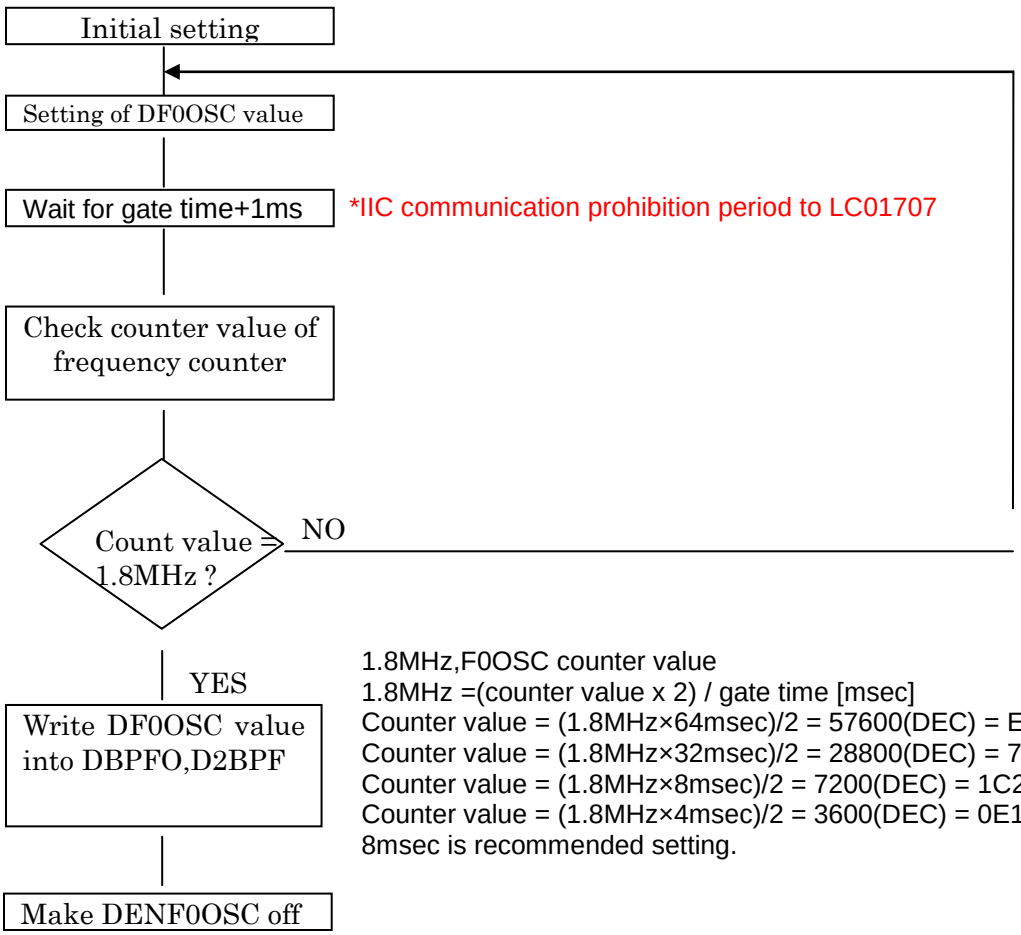


The frequency adjustment is done according to the procedure named Initial setting -> F0OSC Adjustment -> Tuning.
Refer to 2-2 (F0OSC Adjustment), 2-3, 2-4 for details of each flow.

2-2. F0OSC Adjustment

The adjustment of F0OSC oscillatory frequency is done to set the capacitor bank value of complex BPF and 2nd IF BPF.
F0OSC means replica oscillation circuit of complex BPF and 2nd IF filter.
By setting the capacitor bank value of complex BPF and 2nd IF BPF in the capacitor bank value which the F0OSC oscillatory frequency is adjusted to 1.8MHz, BPF frequency for 1st IF frequency 1.2MHz and 2nd IF frequency 600kHz can be adjusted.

Flow chart of F0 adjustment



1.8MHz,F0OSC counter value
1.8MHz =(counter value x 2) / gate time [msec]
Counter value = (1.8MHz×64msec)/2 = 57600(DEC) = E100h
Counter value = (1.8MHz×32msec)/2 = 28800(DEC) = 7080h
Counter value = (1.8MHz×8msec)/2 = 7200(DEC) = 1C20h
Counter value = (1.8MHz×4msec)/2 = 3600(DEC) = 0E10h
8msec is recommended setting.

Do the loop of the above-mentioned flow. Adjust capacitor bank value of DF0OSC by successive comparison control.

F0 adjustment Bit setting 1 (Frequency measurement)
* Transmit data in order in the table.

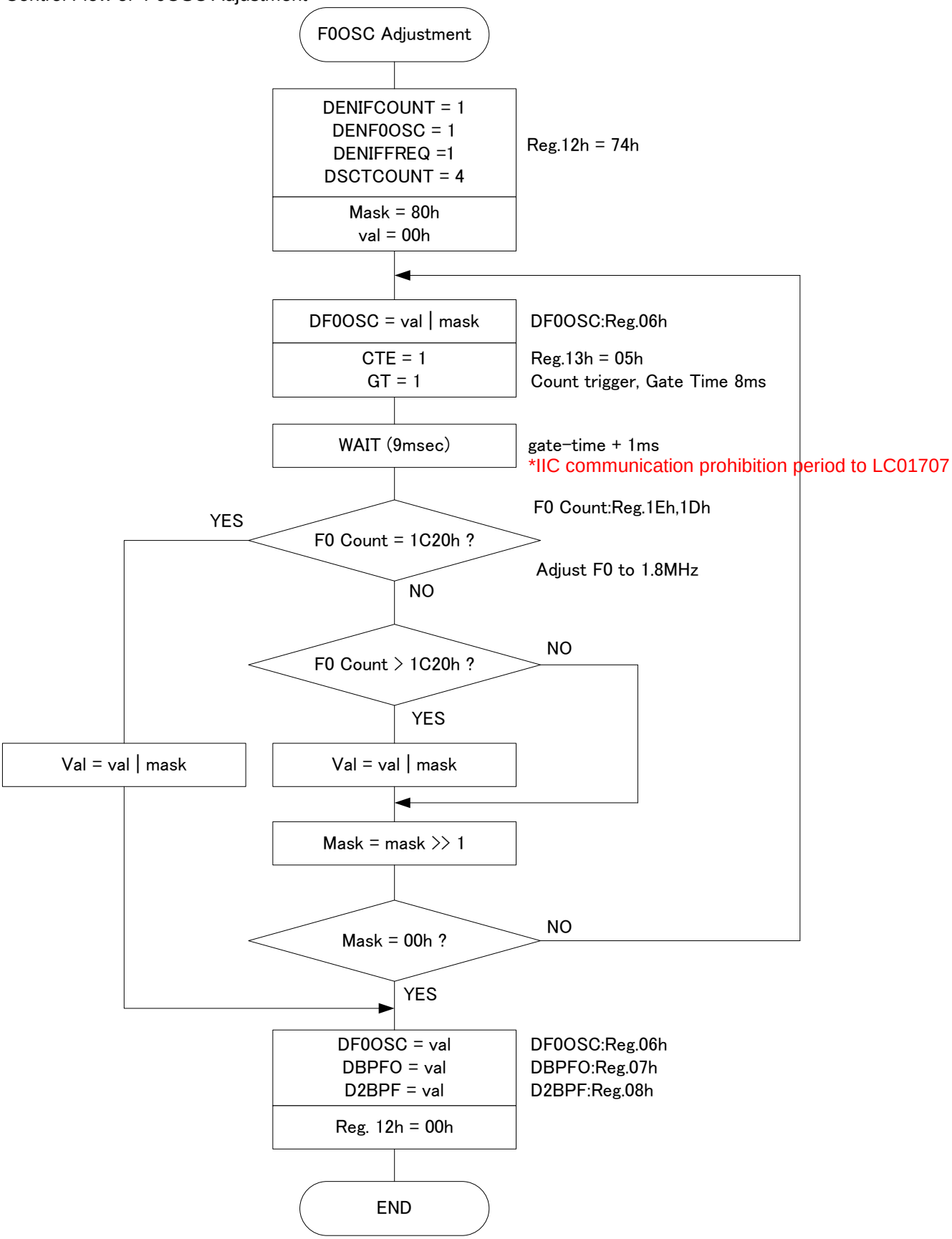
Register address	BIT	Bit name	Binary value	Hex value	Memo
12h	7		0	74h	Not use
	6	DENIFCOUNT	1		Enable(1:ON, 0:OFF)
	5	DENF0OSC	1		Enable (1:ON, 0:OFF)
	4	DENIFFREQ	1		Enable (1:ON, 0:OFF)
	3		0		Not use
	2	DSCTCOUNT	1		Switching of count frequency
	1		0		
	0		0		
13h	7		0	05h	Not use
	6		0		Not use
	5		0		Not use
	4		0		Not use
	3		0		Not use
	2	CTE	1		Count start trigger
	1	GT[1]	0		Switching of gate time (8msec)
	0	GT[0]	1		

After transmit data into 12h and 13h, wait for gate time + 1ms. Repeat until F0 frequency counter value can be adjusted.

Bit setting 2 after OSC F0 Adjustment (Transmit data of DBPFO,D2BPF)
* Transmit data in order in the table.

Register address	BIT	Bit name	Binary value	Hex value	Memo
07h	7	DBPFO	*	**h	Write the vale of 06h (DF0OSC)
	6		*		
	5		*		
	4		*		
	3		*		
	2		*		
	1		*		
	0		*		
08h	7	D2BPF	*	**h	Write the value of 06h (DF0OSC)
	6		*		
	5		*		
	4		*		
	3		*		
	2		*		
	1		*		
	0		*		
12h	7		0	00h	Not use
	6	DENIFCOUNT	0		Enable (1:ON, 0:OFF)
	5	DENF0OSC	0		Enable (1:ON, 0:OFF)
	4	DENIFFREQ	0		Enable (1:ON, 0:OFF)
	3		0		Not use
	2	DSCTCOUNT	0		Switching of count frequency
	1		0		
	0		0		

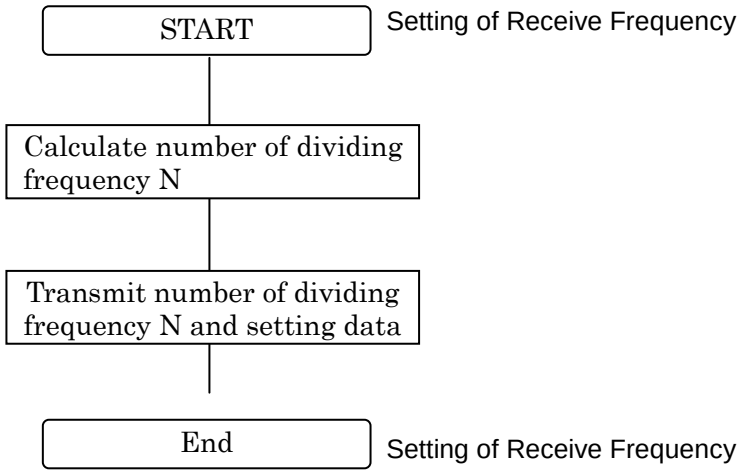
Control Flow of F0OSC Adjustment



2-3. Setting of Receive Frequency

When the frequency is set, and changed, frequency is converted into PLL data. Converted PLL data is called number of dividing frequency N. Number of dividing frequency N is 16 bits length.

By setting of number of dividing frequency N, phase comparison frequency which is input in phase comparator, is determined.



Number of dividing frequency N for receive frequency is calculated by the following formula.

Number of dividing frequency N (PCNT[15:0])=((4 X receive frequency)±(4 X 1st IF frequency))/(4 X channel step frequency)
* 1st frequency is 1.2MHz.

Example) In case of setting to channel step 25kHz, FM 100MHz (The interior of LC01707PLF : local oscillation 400MHz for 1st MIX, phase comparison frequency 100kHz)

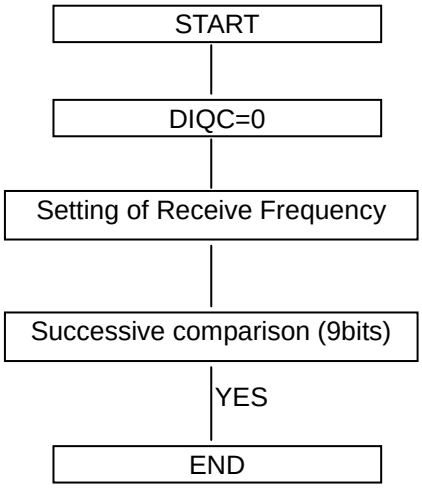
When upper is set (0Ah, DIQC=0)
(100MHz+1.2MHz)/(25kHz)=4048(0FD0h)
Supplementation (because of four time oscillation in the interior of LC01707)
(400MHz+4.8MHz)/(100kHz)=4048(0FD0h)

When lower is set (0Ah, DIQC=1)
(100MHz-1.2MHz)/(25kHz)=3952(0F70h)
Supplementation (because of four time oscillation in the interior of LC01707)
(400MHz-4.8MHz)/(100kHz)=3952(0F70h)
Number of dividing frequency N is set in 2-4, 2-5 CBANK Adjustment.

2-4. CBANK Adjustment (Software Tuning)

The control of capacitor bank of local oscillation for 1st MIX is needed to do PLL lock at receive frequency after setting of receive frequency in 2-3 chapter.

After writing capacitor bank value of local oscillation for 1st MIX, read voltage level of CP, and then control the capacitor bank value by successive comparison. The control flow is as follows.



* Set all 9bits even for PHLEVEL[1:0]=01h for successive comparison.
* Refer 2-3 chapter for setting of Receive Frequency.

* Transmit data in order in the table.

Register address	BIT	Bit name	Binary value	Hex value	Memo
0Ah	7		0	02h	Not use
	6		0		Not use
	5		0		Not use
	4		0		Not use
	3		0		Not use
	2		0		Not use
	1	ENIMRSSI	1		Setting of Xtal colpitts source follower transistor size
	0	DIQC	0		Switching of Complex BPF injection
0Dh	7	DPCNT_L	*	**h	Number of dividing frequency N (Lower 8bits)
	6		*		
	5		*		
	4		*		
	3		*		
	2		*		
	1		*		
	0		*		
0Eh	7	DPCNT_H	*	**h	Number of dividing frequency N (Upper 8bits)
	6		*		
	5		*		
	4		*		
	3		*		
	2		*		
	1		*		
	0		*		

Due to the state of PHLEVEL[1:0], set DCBANK[8:0] as follows.(successive comparison)

Register address	BIT	Bit name	Binary value	Hex value	Memo
0Fh	7	DCBANK_L	0	00h	Setting of Local Oscillator capacitor bank (After check)
	6		0		
	5		0		
	4		0		
	3		0		
	2		0		
	1		0		
	0		0		
10h	7		0	00h	Not use
	6		0		Not use
	5		0		Not use
	4		0		Not use
	3		0		Not use
	2		0		Not use
	1		0		Not use
	0	DCBANK_H	0		Setting of Local Oscillator capacitor bank (After check)

Register address	BIT	Bit name	Binary value	Hex value	Memo
0Fh	7	DCBANK_L	*	**h	Setting of Local Oscillator capacitor bank (After check)
	6		*		
	5		*		
	4		*		
	3		*		
	2		*		
	1		*		
	0		*		
10h	7		0	0*h	Not use
	6		0		Not use
	5		0		Not use
	4		0		Not use
	3		0		Not use
	2		0		Not use
	1		0		Not use
	0	DCBANK_H	*		Setting of Local Oscillator capacitor bank (After check)

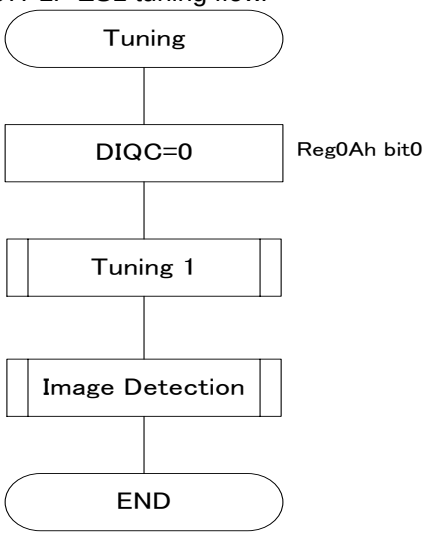
After transmitting data, wait for 1ms and read register 16h.

16h	7		0	1*h	Not use
	6		0		Not use
	5	COUNTSEL	0		Not use
	4	LOCKDETSEL	1		Not use
	3	LOCKDET_DIG	*		Not use
	2	LOCKDET	*		LOCK detection (1:LOCK,0:UNLOCK)
	1	PHLEVEL	*		Detection of CP output level
	0		*		

* Add successive comparison (which is the procedure which waits for 10ms after transmitting data) after normal procedure as flow to avoid error.
* When not set to PHLEVEL=01h, after retry flow to avoid error three times, judge that a device is poor.

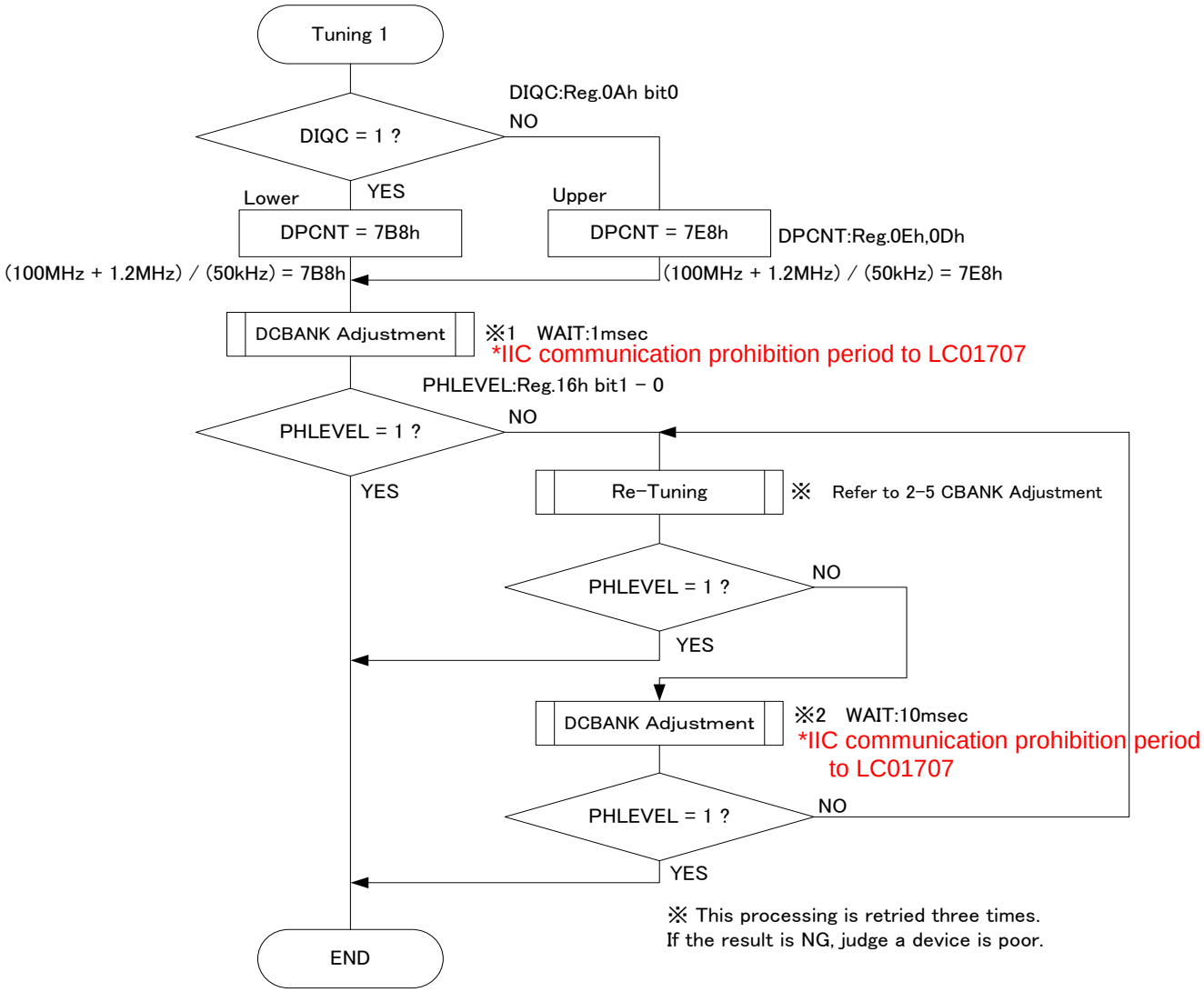
The flow of LC01707PLF control is as follows.

LC01707PLF ES1 tuning flow.

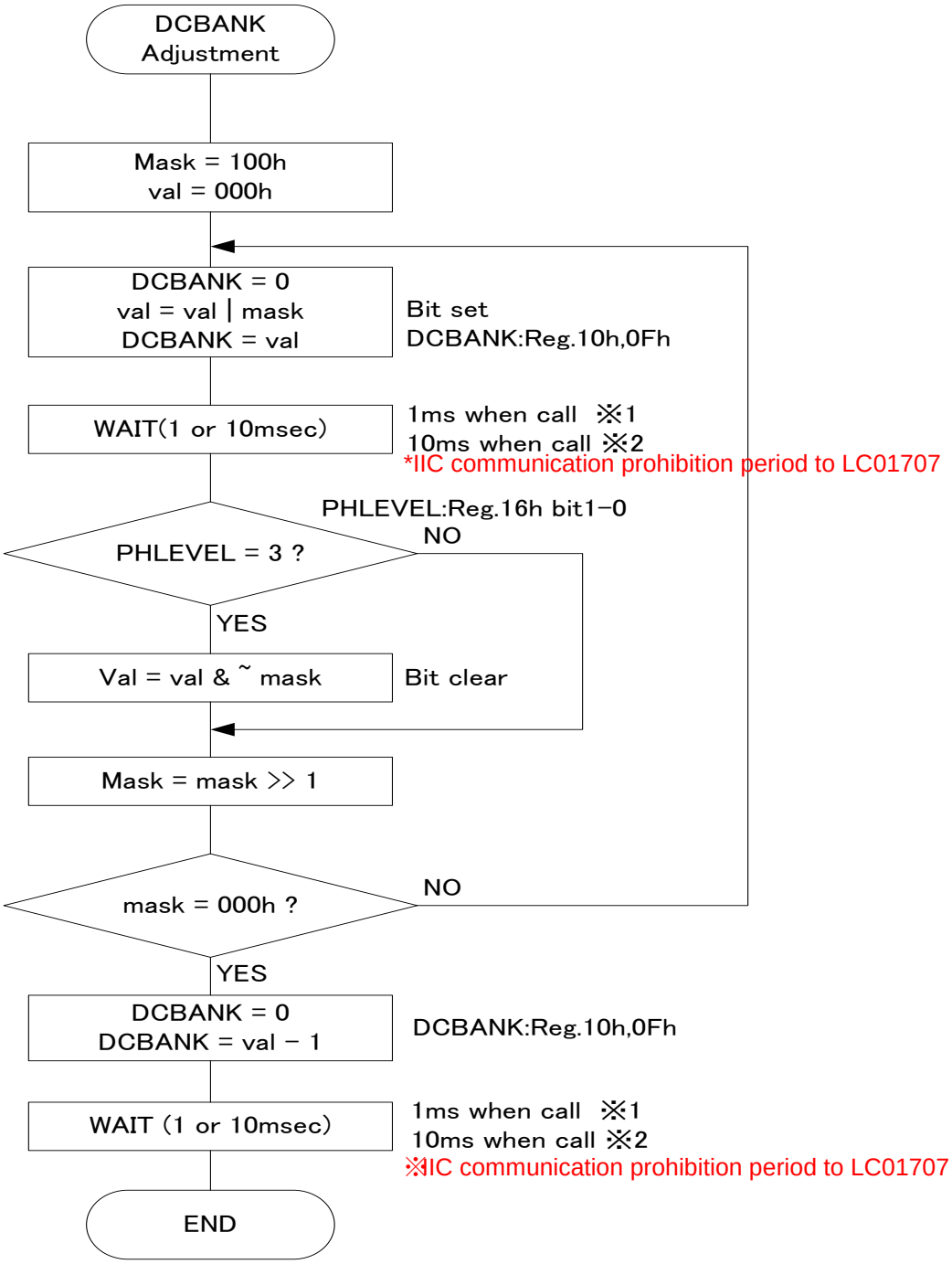


* As for image detection, refer to the flow in 2-6.

Tuning 1 Flow



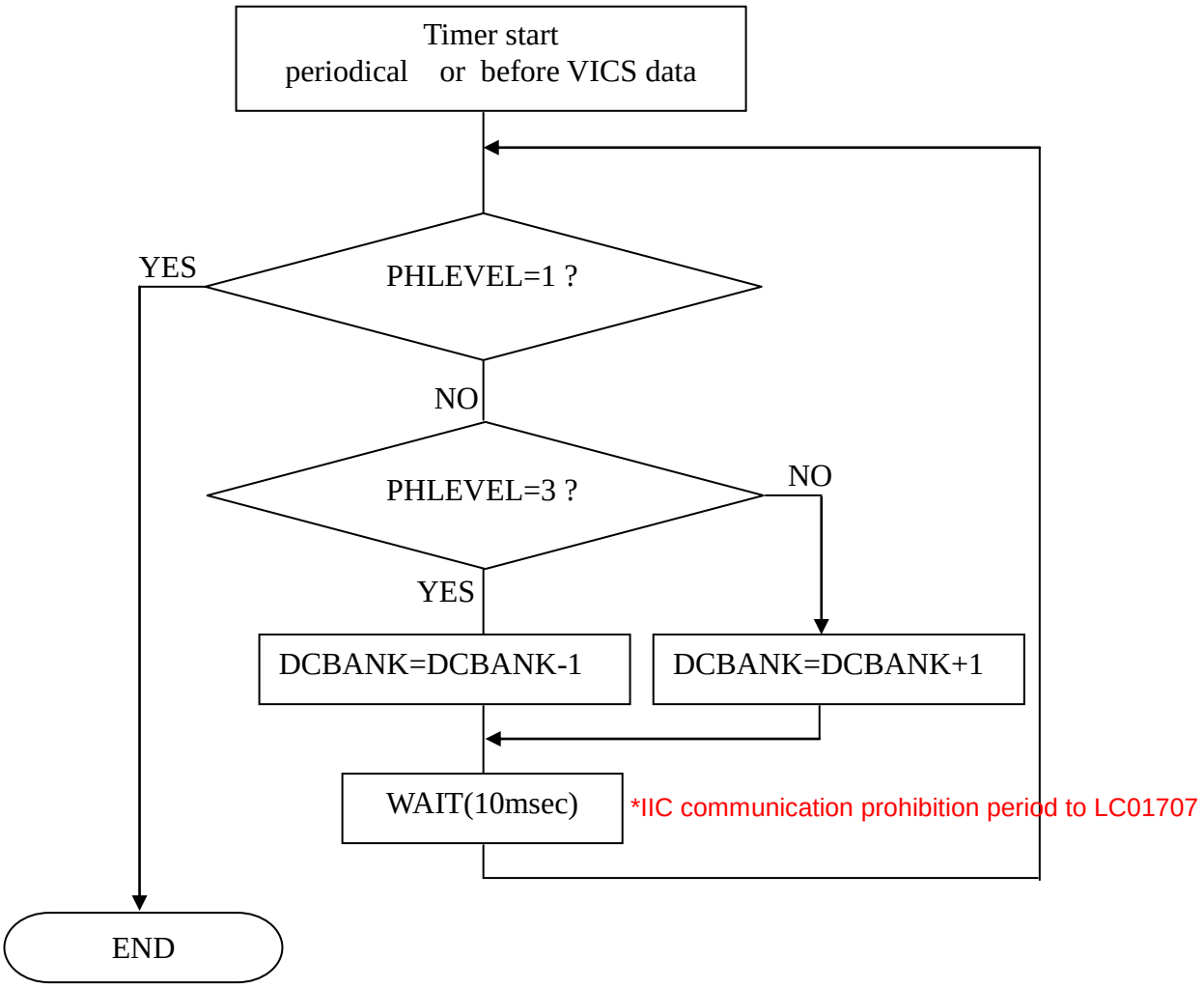
DCBANK Adjustment Flow



2-5. CBANK Adjustment (Re-tuning)

If the ambient temperature changes greatly after tuning in LC01707PLF, CP terminal voltage of PLL happens to drift to unexpected voltage which PLL can not be controlled (more than VFF-0.2V or less than GND+0.2V).
Two kinds of following flow is prepared in order to cope with this problem.

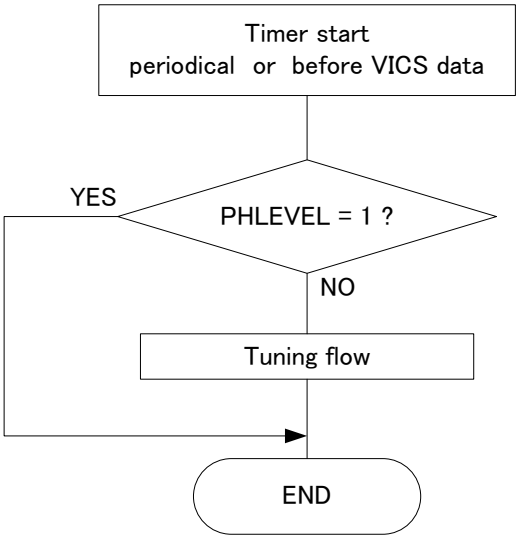
1) Re-tuning flow 1
CP terminal voltage should be monitored via IIC at regular intervals or before receiving VICS data.
The state of the voltage of the CP terminal is checked as three states of less than 0.5V(PHLEVEL=0), 0.5V-2.8V(PHLEVEL=1) or more than 2.8V(PHLEVEL=3) by checking PHLEVEL(16h) register which read at normal tuning flow via IIC .
Even at the time of usual tuning flow, by adjusting the capacitor bank value through this register, the voltage of CP terminal can be set to 0.5V-2.8V(PHLEVEL=1).
By adding the software which decrements Local Oscillator capacitor bank value, at the voltage of CP terminal is more than 2.8V (PHLEVEL=3), and increments the value at the voltage of CP terminal is less than 0.5V (PHLEVEL=0), the voltage of CP terminal can be kept the normal (PHLEVEL=1).



2) Re-Tuning flow 2

As well as the flow of 1), CP terminal voltage is monitored via IIC at regular intervals or before receiving VICS data.

By executing the tuning flow when the voltage of CP terminal is except 0.5V-2.8V(PHLEVEL=1), the voltage of CP terminal returns back to the normal.



About the merit and the demerit of each flow.

About the merit of flow 1).

When Re-Tuning is performed at a comparatively short interval, drift voltage of CP terminal is small since the amount of the temperature change is small. In that case, since adjustment frequency for increment and decrement of capacitor bank decreases, the adjustment time shortens comparatively.

About the demerit of flow 1).

If Re-Tuning is not performed for long time, drift voltage of CP terminal may be large. In that case, since adjustment frequency for increment and decrement of capacitor bank increases, the adjustment time becomes long.

About the merit of flow 2).

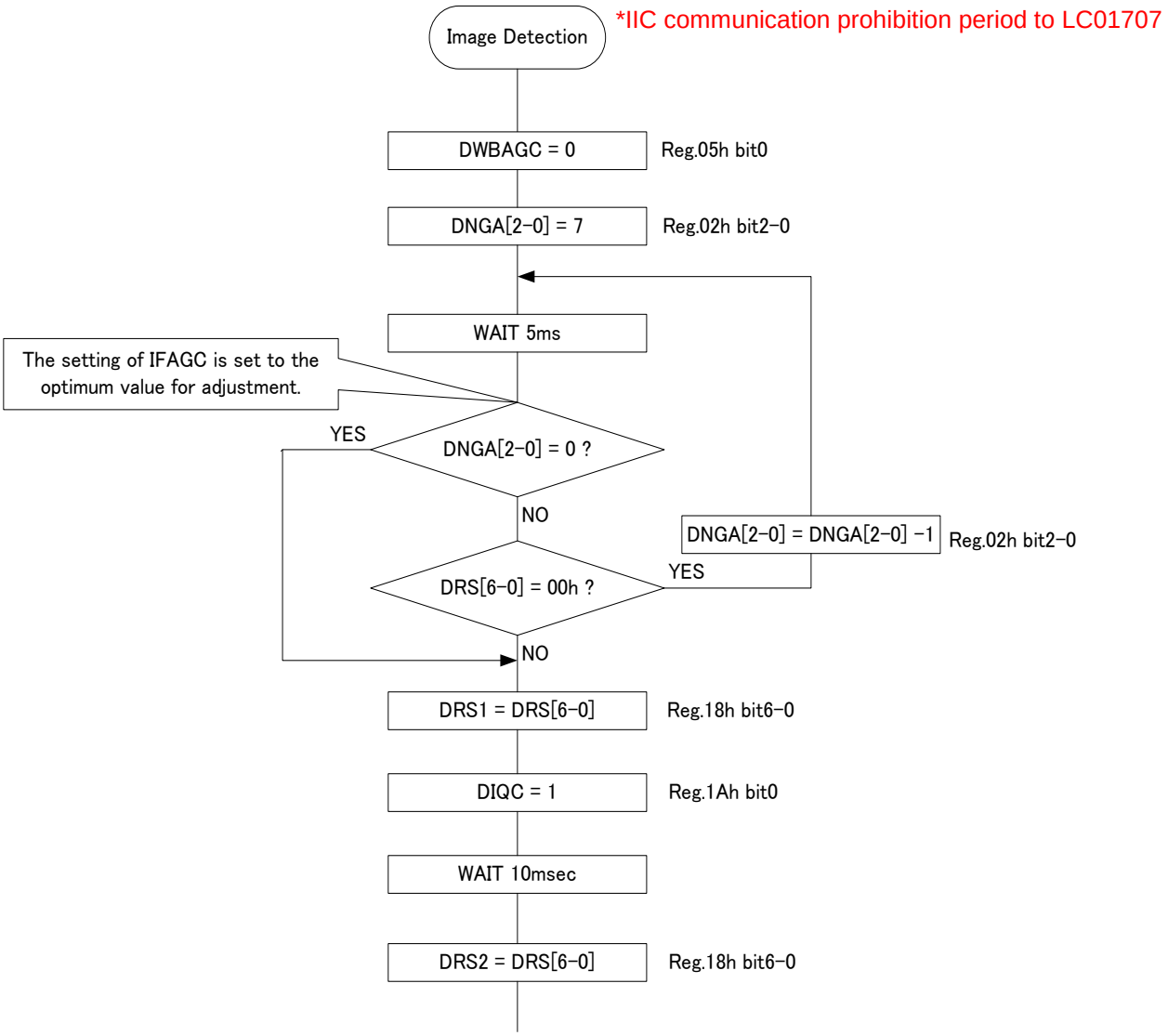
Even if re-tuning is not performed for a short term or long term, Re-Tuning flow will be ended for a certain period.

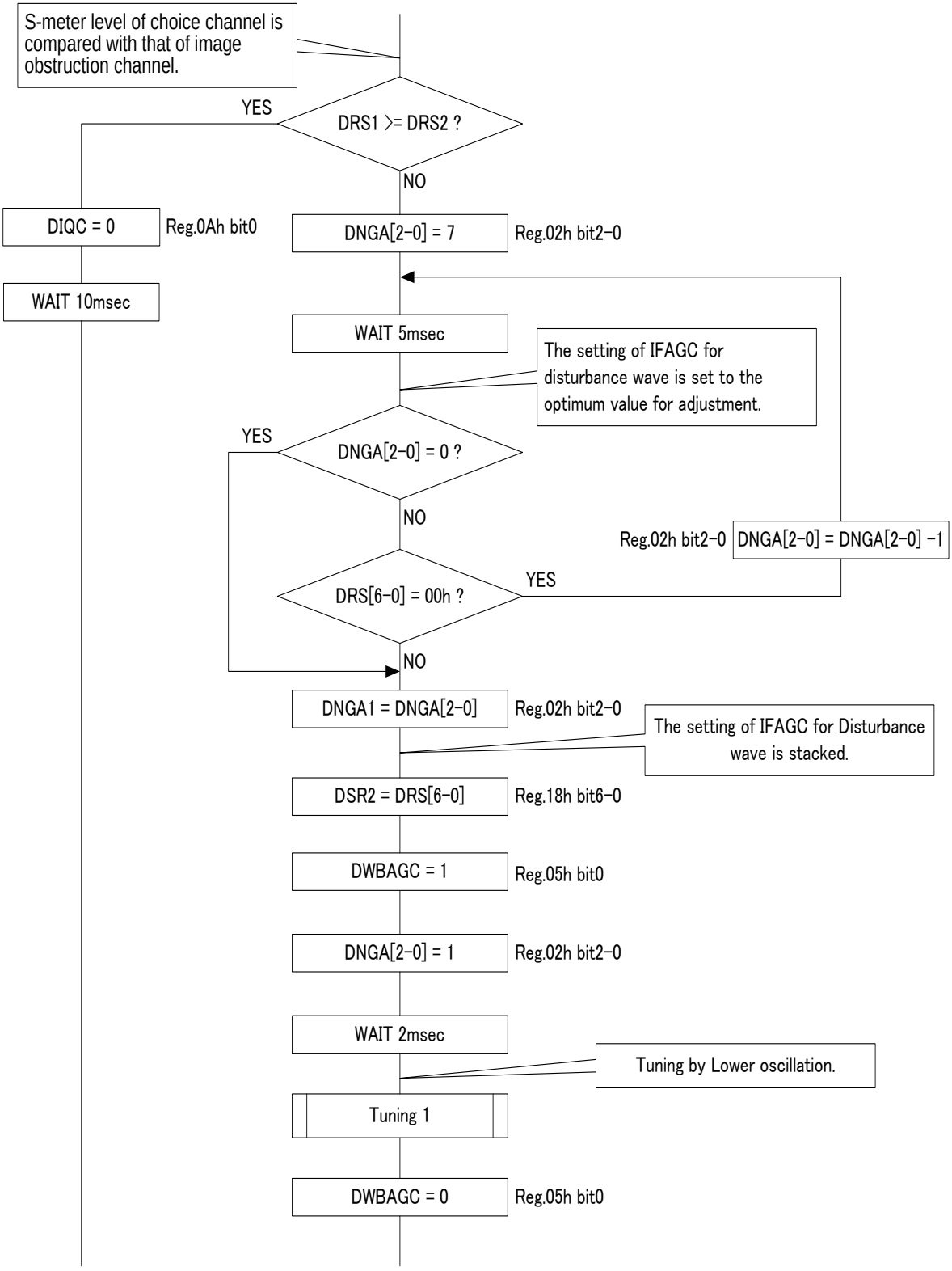
About the demerit of flow 2).

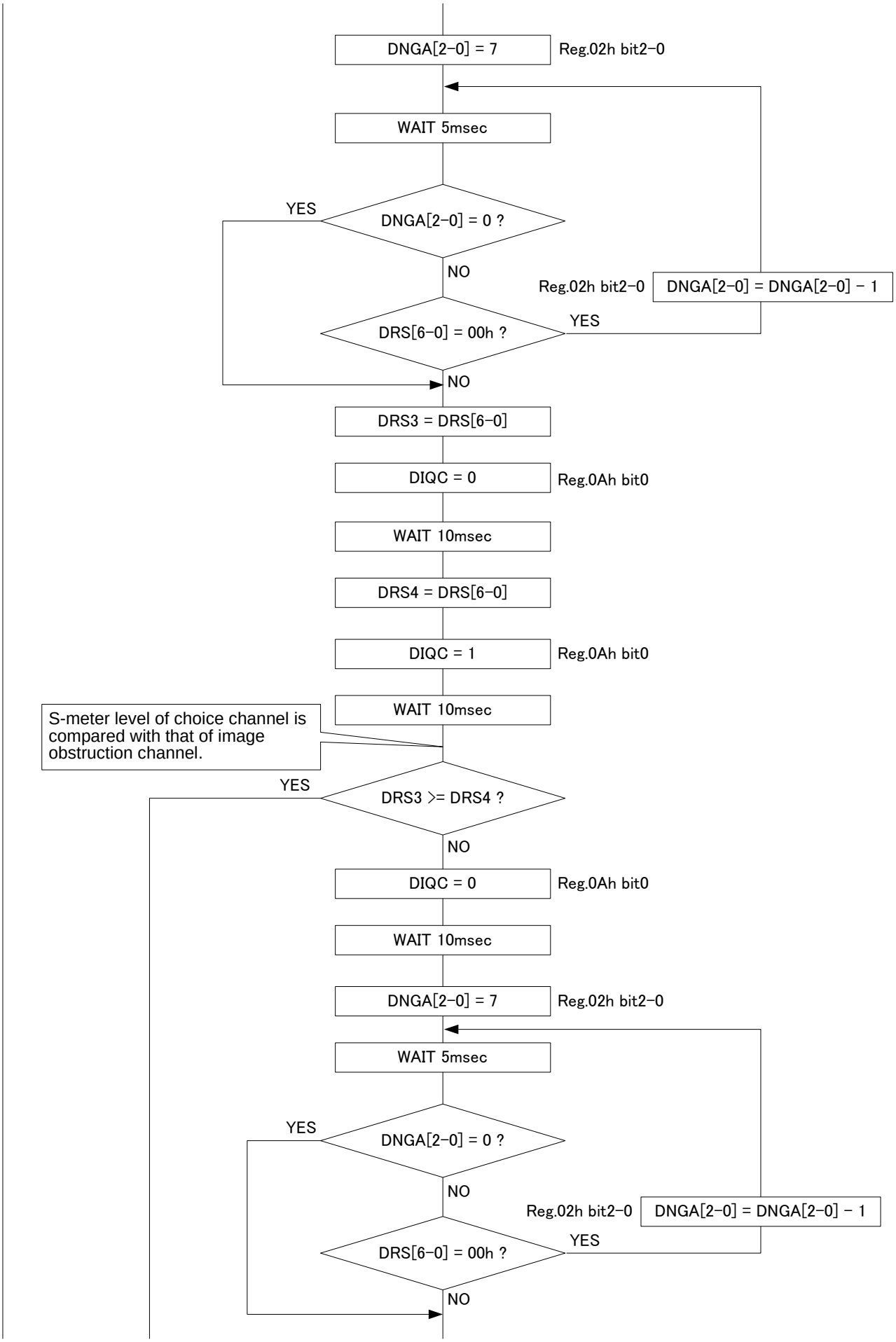
If Re-Tuning is performed at a comparatively short interval compared with flow of 1), the time required becomes long.

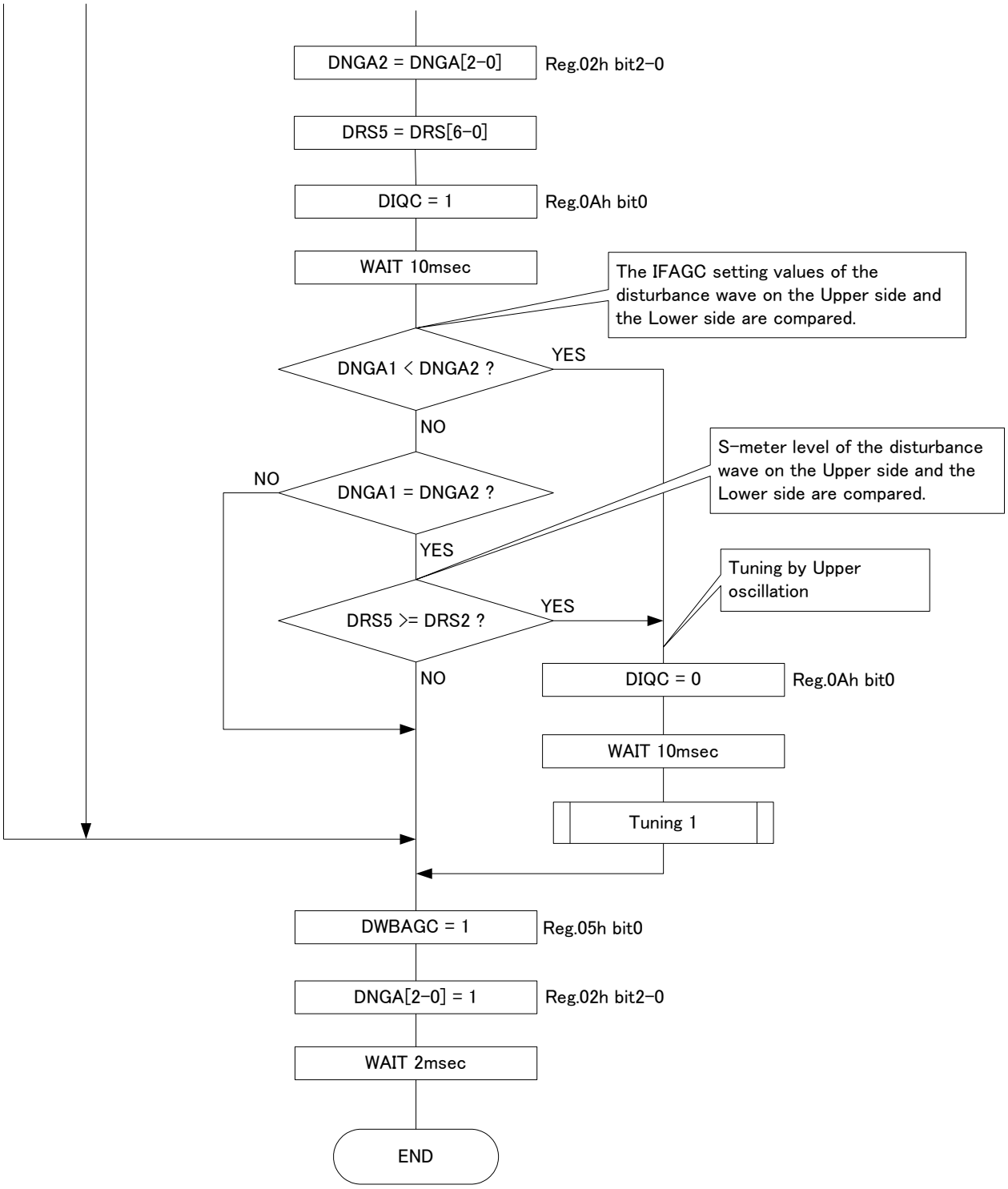
2-6. CBANK Adjustment (Flow to avoid image obstruction)

After tuning of Upper oscillation, the injection is changed and S-meter level of choice channel is compared with that of image obstruction channel.
When S-meter level of choice channel is higher than that of image obstruction channel, it will end by the Upper oscillation tuning.
When S-meter level of choice channel is lower than that of image obstruction channel, after tuning Lower oscillation, the injection is changed and S-meter level of choice channel is compared with that of image obstruction channel.
As that result, when S-meter level of choice channel is higher than that of image obstruction channel, it will end by the Lower oscillation tuning.
When S-meter level of image obstruction channel is higher than that of choice channel both when Upper oscillation tuning and Lower oscillation tuning, it should be tuned in to small influence of the image obstruction.
Refer to the following flow for the details of processing procedure.




S-meter level of choice channel is compared with that of image obstruction channel.
DRS1 >= DRS2 ?
YES
NO
DIQC = 0
Reg.0Ah bit0
WAIT 10msec
DNGA[2-0] = 7
Reg.02h bit2-0
WAIT 5msec
The setting of IFAGC for disturbance wave is set to the optimum value for adjustment.
DNGA[2-0] = 0 ?
YES
NO
Reg.02h bit2-0
DNGA[2-0] = DNGA[2-0] -1
DRS[6-0] = 00h ?
YES
NO
DNGA1 = DNGA[2-0]
Reg.02h bit2-0
The setting of IFAGC for Disturbance wave is stacked.
DSR2 = DRS[6-0]
Reg.18h bit6-0
DWBAGC = 1
Reg.05h bit0
DNGA[2-0] = 1
Reg.02h bit2-0
WAIT 2msec
Tuning by Lower oscillation.
Tuning 1
DWBAGC = 0
Reg.05h bit0


DNGA[2-0] = 7
Reg.02h bit2-0
WAIT 5msec
YES
DNGA[2-0] = 0 ?
NO
Reg.02h bit2-0
DNGA[2-0] = DNGA[2-0] - 1
DRS[6-0] = 00h ?
YES
NO
DRS3 = DRS[6-0]
DIQC = 0
Reg.0Ah bit0
WAIT 10msec
DRS4 = DRS[6-0]
DIQC = 1
Reg.0Ah bit0
WAIT 10msec
S-meter level of choice channel is compared with that of image obstruction channel.
YES
DRS3 >= DRS4 ?
NO
DIQC = 0
Reg.0Ah bit0
WAIT 10msec
DNGA[2-0] = 7
Reg.02h bit2-0
WAIT 5msec
YES
DNGA[2-0] = 0 ?
NO
Reg.02h bit2-0
DNGA[2-0] = DNGA[2-0] - 1
DRS[6-0] = 00h ?
YES
NO

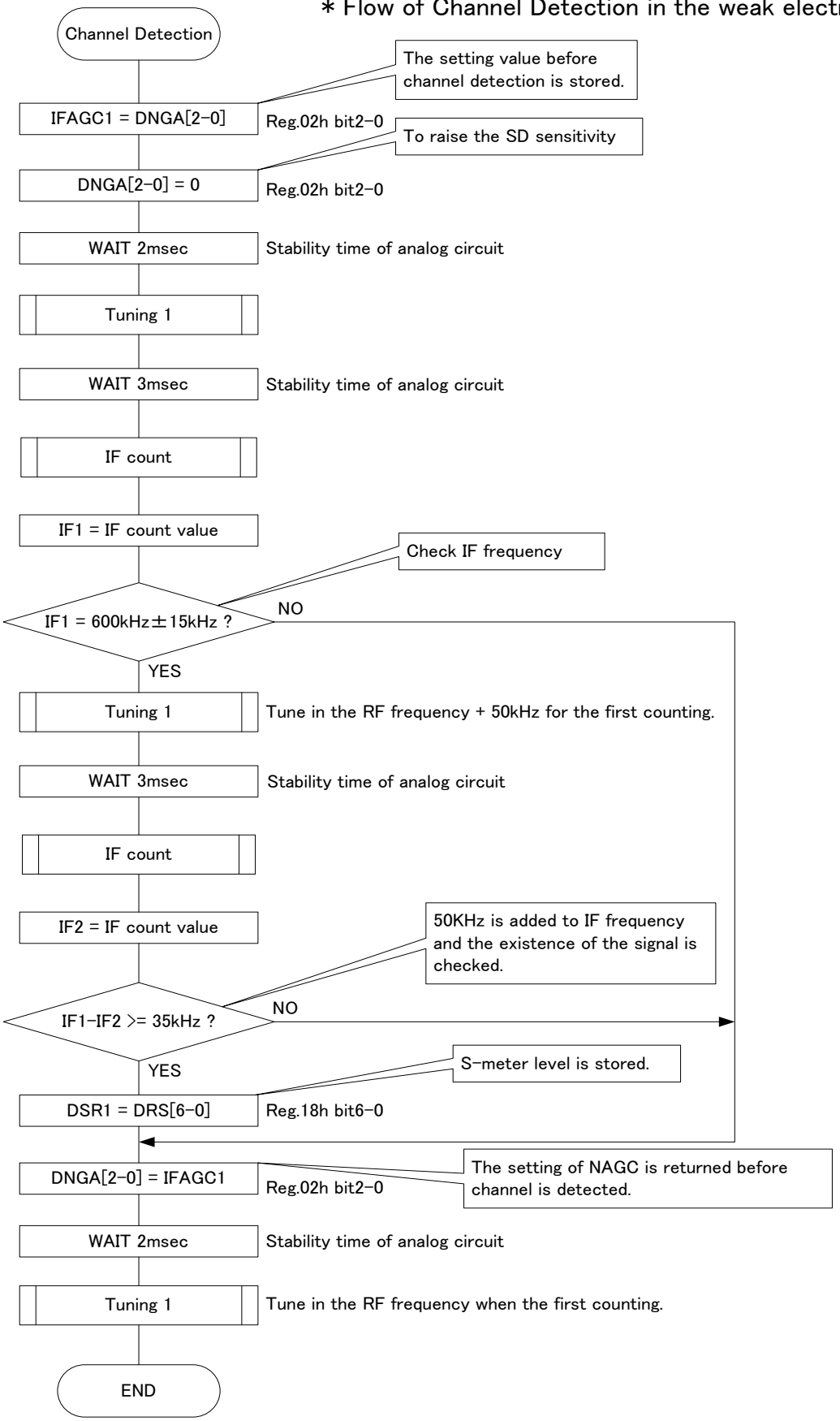

DNGA2 = DNGA[2-0]
Reg.02h bit2-0
DRS5 = DRS[6-0]
DIQC = 1
Reg.0Ah bit0
WAIT 10msec
The IFAGC setting values of the disturbance wave on the Upper side and the Lower side are compared.
DNGA1 < DNGA2 ?
YES
NO
S-meter level of the disturbance wave on the Upper side and the Lower side are compared.
NO
DNGA1 = DNGA2 ?
YES
Tuning by Upper oscillation
DRS5 >= DRS2 ?
YES
NO
DIQC = 0
Reg.0Ah bit0
WAIT 10msec
Tuning 1
DWBAGC = 1
Reg.05h bit0
DNGA[2-0] = 1
Reg.02h bit2-0
WAIT 2msec
END

2-7. Channel Detection

Channel Detection in the weak electric field is possible by IF frequency count in LC01707PLF.
After tuning in the first, IF frequency is counted, it is confirmed whether IF frequency is 600KHz±15KHz or less.
And then if IF frequency is 600kHz±15kHz or less, +50kHz of IF frequency is shifted, and tuning is performed again.
After re-tuning, IF frequency is counted. And when the difference before the re-tuning and after the re-tuning is 35kHz or more, Channel Detection is completed.
Additionally, refer to following flow about details.

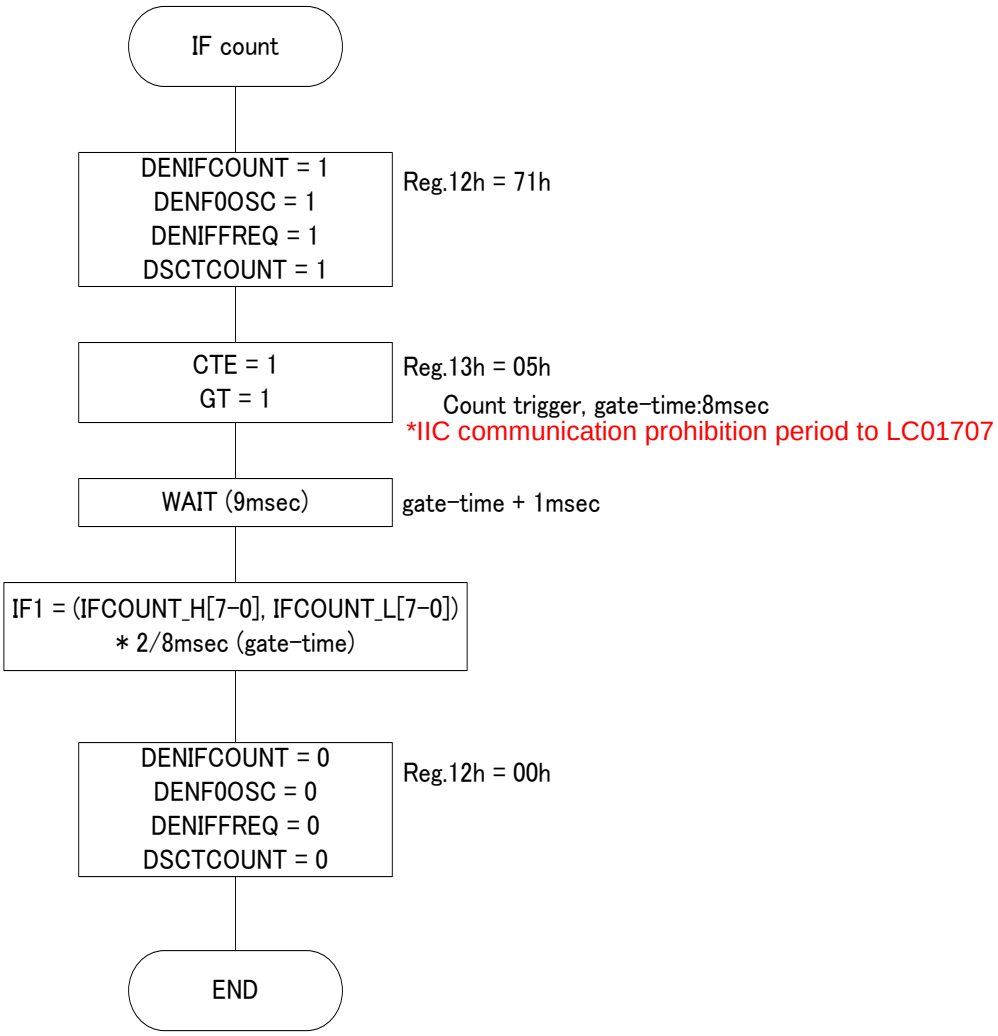
Channel Detection Flow of LC01707PLF

＊ Flow of Channel Detection in the weak electric field



＊

Refer to P27 of 2-4 CBANK Adjustment (Software Tuning) for tuning 1.



* Refer to 3-1 Frequency Counter

3-1. Frequency Counter

In LC01707PLF it is possible to count the frequency of IF and F0OSC. Frequency counter is showed in flow of F0 adjustment in 2-2 for count of frequency of F0OSC. The measurement procedure of the frequency is described to the following.

IF frequency measurement

* Transmit data in order in the table.

Register address	BIT	Bit name	Binary value	Hex value	Memo
12h	7		0	71h	Not use
	6	DENIFCOUNT	1		Enable(1:ON, 0:OFF)
	5	DENF0OSC	1		Enable(1:ON, 0:OFF)
	4	DENIFFREQ	1		Enable (1:ON, 0:OFF)
	3		0		Not use
	2	DSCTCOUNT	0		Selection of count frequency (IFCOUNT)
	1		0		
	0		1		
13h	7		0	05h	Not use
	6		0		Not use
	5		0		Not use
	4		0		Not use
	3		0		Not use
	2	CTE	1		Count start trigger
	1	GT[1]	0		Selection of gate time (8msec)
	0	GT[0]	1		

After transmitting data, read register 19h (IFCOUNT_L) and register 1Ah (IFCOUNT_H) after waiting for the time of 9ms (=gate time (8ms) + 1ms). The calculation of the frequency is as follows.

(COUNT value × 2) / gate time (8msec) = Measurement frequency

Example) In case of IF frequency 600kHz

(2400×2)/8msec=600kHz -> COUNT value is 2400 (decimal).

After acquisition of the count data, write 00h into 12h.

12h	7		0	00h	Not use
	6	DENIFCOUNT	0		Enable (1:ON, 0:OFF)
	5	DENF0OSC	0		Enable (1:ON, 0:OFF)
	4	DENIFFREQ	0		Enable (1:ON, 0:OFF)
	3		0		Not use
	2	DSCTCOUNT	0		Selection of gate time
	1		0		
	0		0		

F0OSC frequency measurement
* Transmit data in order in the table.

Register address	BIT	Bit name	Binary value	Hex value	Memo
12h	7		0	74h	Not use
	6	DENIFCOUNT	1		Enable (1:ON, 0:OFF)
	5	DENF0OSC	1		Enable (1:ON, 0:OFF)
	4	DENIFFREQ	1		Enable (1:ON, 0:OFF)
	3		0		Not use
	2	DSCTCOUNT	1		Selection of count frequency (f0 detection of oscillation frequency)
	1		0		
	0		0		
13h	7		0	05h	Not use
	6		0		Not use
	5		0		Not use
	4		0		Not use
	3		0		Not use
	2	CTE	1		Count start trigger
	1	GT[1]	0		Selection of gate time (8msec)
	0	GT[0]	1		

After transmitting data, by reading register 1Dh (F0_L) and register 1Eh (F0_H) after waiting for the time of 9ms (=gate time (8msec) + 1msec), acquire count data. The calculation of the frequency is similar to the calculating formula of the IF frequency. Use 8msec both for IF and F0OSC for gate time.

After acquisition of the count data, write 00h into 12h.

12h	7		0	00h	Not use
	6	DENIFCOUNT	0		Enable (1:ON,0:OFF)
	5	DENF0OSC	0		Enable (1:ON,0:OFF)
	4	DENIFFREQ	0		Enable (1:ON,0:OFF)
	3		0		Not use
	2	DSCTCOUNT	0		Selection of count frequency
	1		0		
	0		0		