Data Sheet
March 1997

m i c r o e l e c t r o n i c s   g r o u p

Lucent Technologies
Bell Labs Innovations

LB1011 General-Purpose SLIC

Features

- Basic SLIC function at a low cost
- High ac impedance characteristics for balanced-line, differential-mode, voice-band signals
- Full internal lightning surge-protection up to 4 A
- dc voltage drops can be adjusted to accommodate different peak signal levels

Description

The LB1011AB integrated circuit is an electronic SLIC that supplies a controlled dc current to the TIP/RING pair of a telephone system. The SLIC circuitry presents a low impedance to dc currents, while presenting a high impedance to ac signals. The LB1011AB is integrated as two complementary chips to supply dc currents of both positive and negative polarities to either balanced or unbalanced lines. In the balanced-line application, this device helps suppress undesirable common-mode signals.
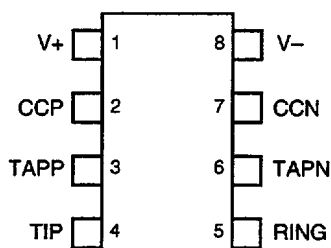
The LB1011AB is available in an 8-pin DIP.

Description (continued)
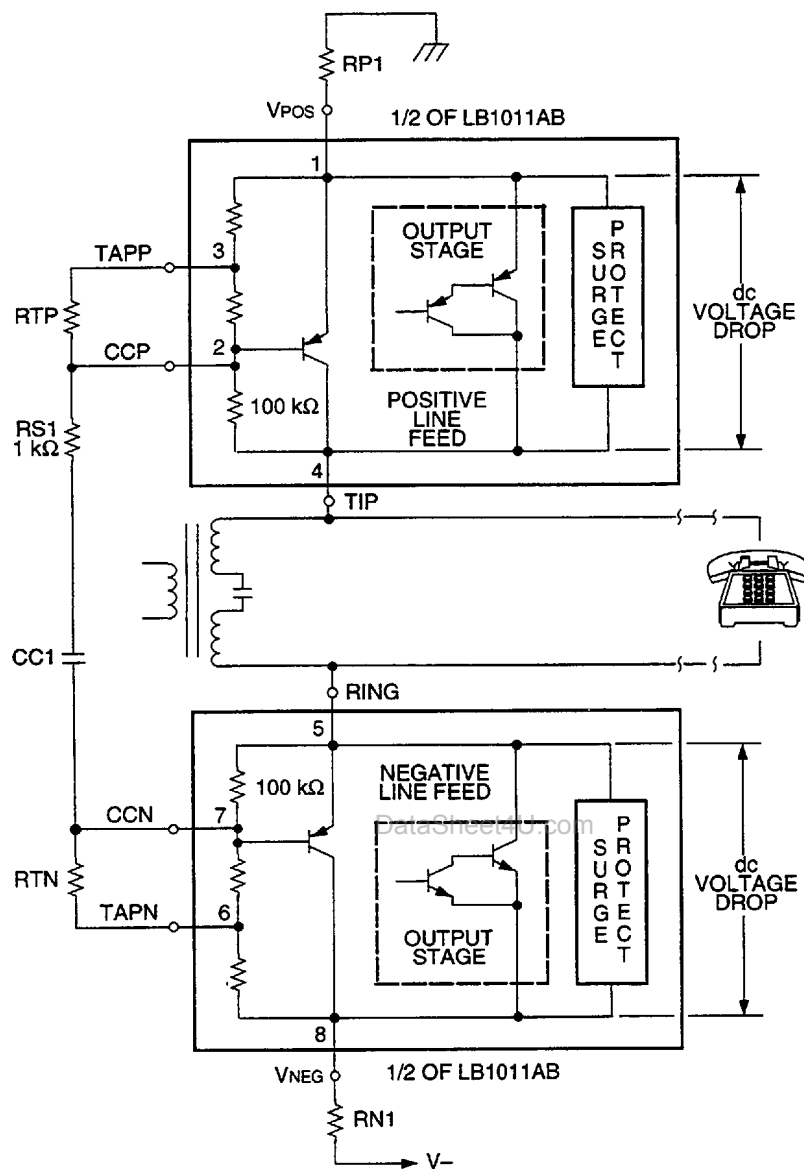
12-1862 (C)

Figure 1. Block Diagram

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Pin Information

12-1868.e (C)

Figure 2. Pin Diagram

Table 1. Pin Descriptions

Pin	Symbol	Type	Name/Description
1	V+	—	**Positive Power Supply.** This pin connects to the most positive external power supply (in some cases this may ground) through an external resistor. This external resistor is a factor in determining the amount of current which will be supplied by the positive line feed output.
2	CCP	—	**Cross-Coupling (Positive).** A capacitor between this pin and pin 7 (for balanced-line configuration) creates a high ac impedance between TIP and RING. Since full TIP-to-RING voltage appears across these pins, it is recommended that a 1.0 kΩ resistor be placed in series with the cross-coupling capacitor for surge protection purposes. Unbalanced-line applications should connect the cross-coupling capacitor to ground so that the common-mode impedance of the output is greatly increased.
3	TAPP	—	**Resistor Tap (Positive).** These terminals are used to adjust the dc voltage drops across the negative line feed. The nominal dc voltage drop is 3 V when no resistor is connected between pins 2 and 3 or pins 6 and 7. A short circuit between these pin combinations will produce voltage drops varying between 3 V and 4 V. A higher dc voltage drop (greater than 3 V) may be desirable for higher operating temperatures or when the peak value of the ac signal exceeds 2.5 V.
4	TIP	O	**Positive Line Feed.** This pin is the output of the Positive Line Feed.
5	RING	O	**Negative Line Feed.** This pin is the output of the Negative Line Feed.
6	TAPN	—	**Resistor Tap (Negative).** This pin is used to adjust the dc voltage drops across the Positive Line Feed. The nominal dc voltage drop is 3 V when no resistor is connected between pins 2 and 3 or pins 6 and 7. A short circuit between these pin combinations will produce voltage drops varying between 3 V and 4 V. A higher dc voltage drop (greater than 3 V) may be desirable for higher operating temperatures or when the peak value of the ac signal exceeds 2.5 V.
7	CCN	—	**Cross-Coupling (Negative).** A capacitor between this pin and pin 2 (for balanced-line configuration) creates a high ac impedance between TIP and RING. Since full TIP-to-RING voltage appears across these pins, it is recommended that a 1.0 kΩ resistor be placed in series with the cross-coupling capacitor for surge protection purposes. Unbalanced-line applications should connect the cross-coupling capacitor to ground so that the common-mode impedance of the output is greatly increased.
8	V–	—	**Negative Power Supply.** This pin connects to the most negative external power supply through an external resistor. This external resistor is a factor in determining the amount of current which will be supplied by the negative line feed output.

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Absolute Maximum Ratings (At 25 °C)

Stresses in excess of Absolute Maximum Ratings can cause permanent damage to the device. These are absolute stress ratings only. Functional operation of the device is not implied at these or any other conditions in excess of those given in the operational sections of the data sheet. Exposure to Absolute Maximum Ratings for extended periods can adversely affect device reliability.

| Parameter	Symbol	Min	Max	Unit
Ambient Operating Temperature	T_A	−20	70	°C
Storage Temperature	T_{stg}	−40	125	°C
Pin Soldering Temperature (t = 15 s max.)	—	—	300	°C
Current, Positive Line Feed (V_{POS} to TIP)	—	—	200	mA
Current, Negative Line Feed (RING to V_{NEG})	—	—	200	mA
Voltage, Positive Line Feed (V_{POS} to TIP; see Figure 3.)	—	—	4.85	V
Voltage, Negative Line Feed (RING to V_{NEG}; see Figure 3.)	—	—	4.00	V

Electrical Characteristics

T_A = 25 °C, unless otherwise specified. Minimum and maximum values are testing requirements. Typical values are characteristics of the device and are the result of engineering evaluations. Typical values are for information only and are not part of the testing requirements.

Table 2. Electrical Characteristics

Parameter	Test Conditions	Min	Typ	Max	Unit
dc Voltage Drop, Positive Line Feed	Figure 3	2.50	3.00	3.50	V
dc Voltage Drop, Negative Line Feed	Figure 3	−2.50	−3.00	−3.50	V
dc Voltage Drop, Positive Line Feed (high-level mode)	Figure 3 Connect pin 2 to 3	3.75	4.30	4.85	V
dc Voltage Drop, Negative Line Feed (high-level mode)	Figure 3 Connect pin 6 to 7	−3.60	−3.80	−4.00	V
Shunt Impedance	Figure 4	18	—	—	kΩ
Shunt Impedance (high-level mode)	Figure 4 Connect pin 2 to 3 and 6 to 7	18	—	—	kΩ
Longitudinal Balance	Figure 5	55	—	—	dB
Longitudinal Balance (high-level mode)	Figure 5 Connect pin 2 to 3 and 6 to 7	55	—	—	dB
Distortion	Figure 6	—	—	2.0	%
Distortion (high-level mode)	Figure 5 Connect pin 2 to 3 and 6 to 7	—	—	2.0	%
Base-to-Emitter Voltage; Positive Line Feed	Figure 7 I_{POS} = 50 mA	1.0	—	2.0	V
Base-to-Emitter Voltage Change; Positive Line Feed	Figure 7; ΔV = (V @ 100 mA) minus (V @ 50 mA)	25	—	250	mV
Base-to-Emitter Voltage; Negative Line Feed	Figure 7 I_{NEG} = 50 mA	1.0	—	2.0	V
Base-to-Emitter Voltage Change; Negative Line Feed	Figure 7; ΔV = (V @ 100 mA) minus (V @ 50 mA)	25	—	250	mV

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Electrical Characteristics (continued)

Table 2. Electrical Characteristics (continued)

Parameter	Test Conditions	Min	Typ	Max	Unit
SLIC, Total Voltage	Figure 8; I_{BF} = 50 mA	5.0	—	6.8	V
Change in Total Voltage	Figure 8; ΔV = (V @ 100 mA) minus (V @ 50 mA)	−400	—	600	mV
SLIC, Total Voltage (high-level mode)	Figure 8; I_{BF} = 50 mA Connect pin 2 to 3 and 6 to 7	7.2	—	9.4	V
Change in Total Voltage (high-level mode)	Figure 8; ΔV = (V @ 100 mA) minus (V @ 50 mA) Connect pin 2 to 3 and 6 to 7	−400	—	600	mV
Line/Supply Voltage: Positive Line Feed Negative Line Feed	Figure 9; I_T = 200 mA — —	— —	— —	1.4 1.4	V V
PNPN Breakdown Voltage: Positive Line Feed Negative Line Feed	Figure 9; I_T = 35 mA Pins 2 and 1 connected Pins 7 and 8 connected	8.0 8.0	— —	10 10	V V
PNPN Breakdown Voltage: Positive Line Feed Negative Line Feed	Figure 9; I_T = 200 mA Pins 2 and 1 connected Pins 7 and 8 connected	2.0 2.0	— —	5.0 5.0	V V

12-1863 (C)
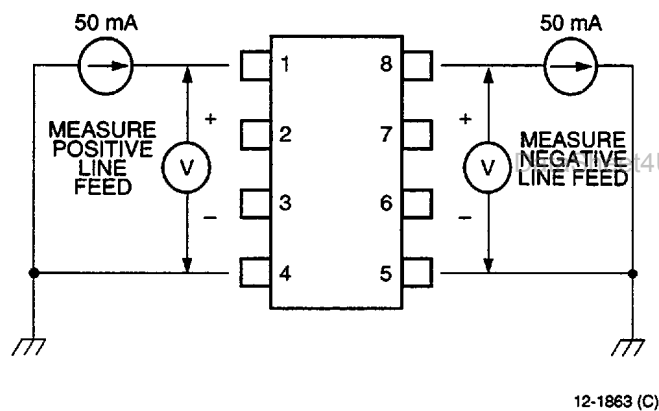
Figure 3. dc Voltage Drop Test Circuit

12-1864 (C)
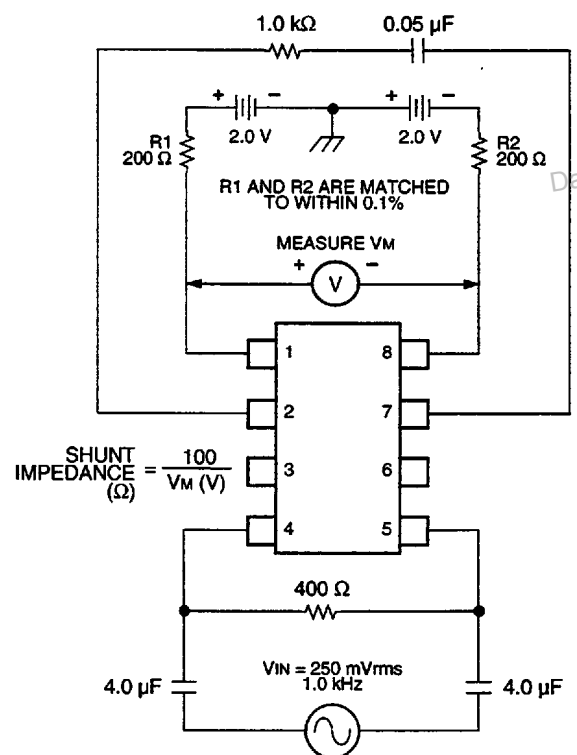
Notes:
R1 and R2 are matched to within 0.1%.

All power supply rails should be bypassed, as close as possible to the appropriate pin, with capacitors of 0.1 μF or greater.

Shunt impedance (in Ω) = $\dfrac{100}{V_M \text{ (in V)}}$.

Figure 4. Shunt Test Circuit

Electrical Characteristics (continued)

12-1865 (C)
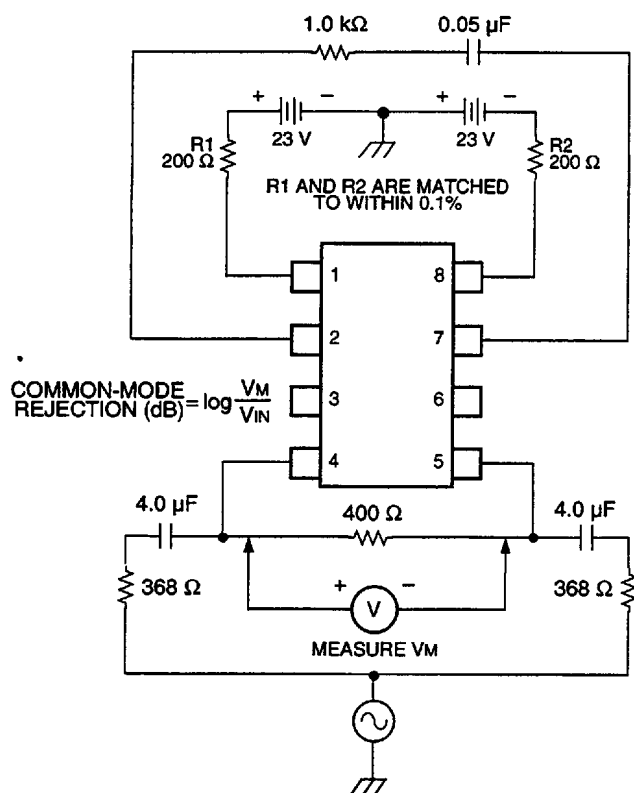
Notes:
All power supply rails should be bypassed, as close as possible to the appropriate pin, with capacitors of 0.1 µF or greater.

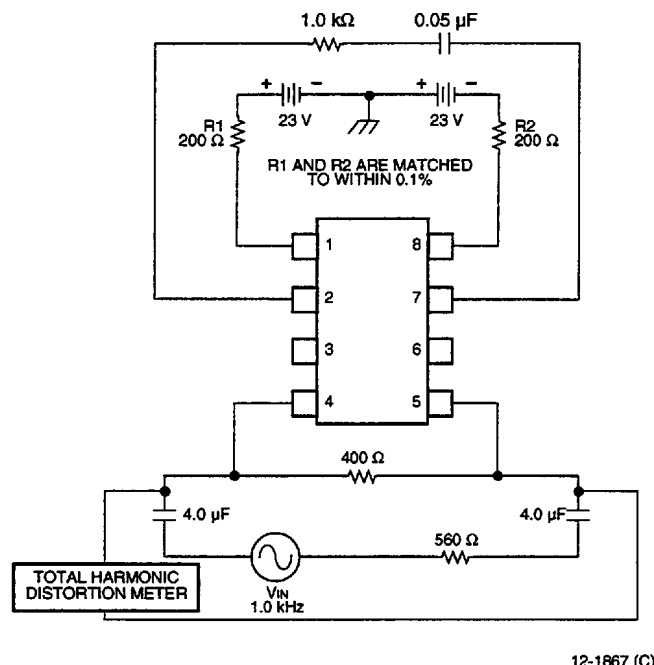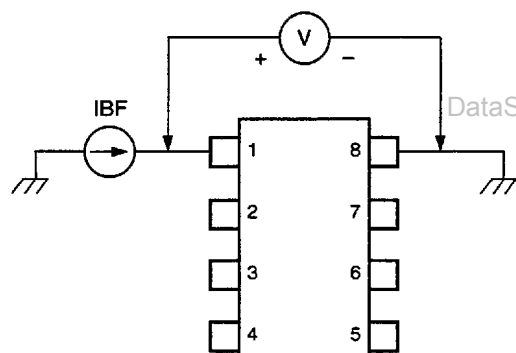Longitudinal balance (in dB) $= 20 \cdot \log\dfrac{V_M}{V_{IN}}$, $V_{IN} = 250$ mVrms 1 kHz.

Figure 5. Longitudinal Balance Test Circuit

12-1866 (C)
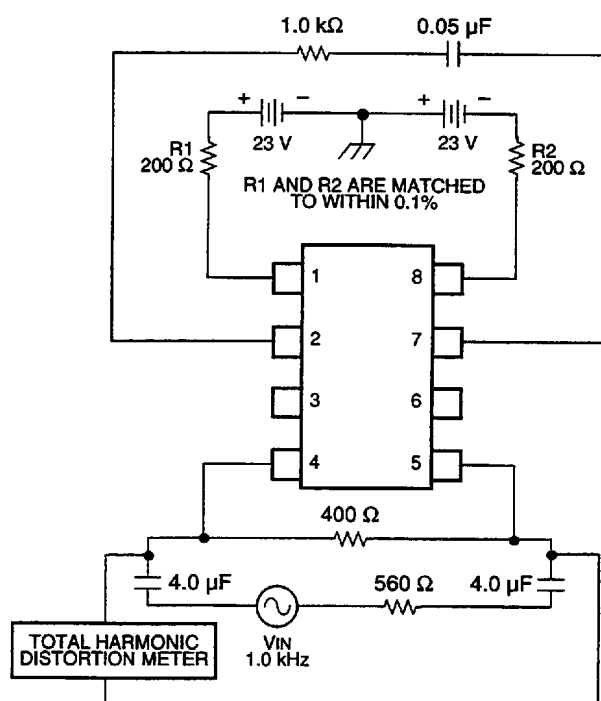
Note: All power supply rails should be bypassed, as close as possible to the appropriate pin, with capacitors of 0.1 µF or greater.

Figure 6. Distortion Test Circuit

Electrical Characteristics (continued)

12-1867 (C)

Figure 7. Base-to-Emitter Voltage Test Circuit

12-1868 (C)

Figure 8. SLIC Total Voltage Test Circuit
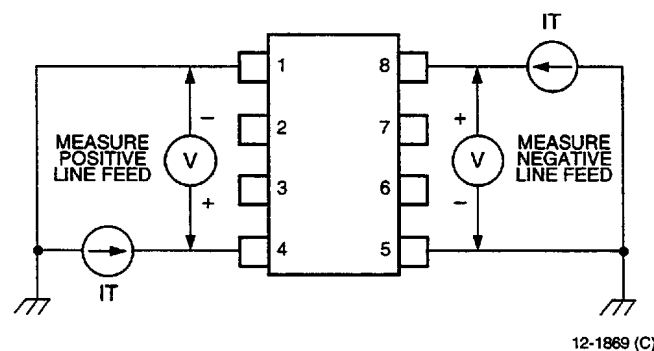
12-1869 (C)

Figure 9. Line/Supply Voltage Test Circuit

Surge Protection Characteristics

Internal surge protection circuitry, in conjunction with external resistors, provides protection against forward voltage surges. Reverse surges are dissipated through

large internal diodes bridged across each line feed section. Forward surge protection consists of a PNPN composite device. This PNPN composite device can withstand surges as shown in Figure 10. It has a break-over point (V_{BO}) of approximately 9 V, as shown in Figure 11. After breakover, the output is clamped at less than 2 V as long as the surge source supplies more than 150 mA. When the surge source drops below 150 mA, the PNPN device recovers and normal operations resume.
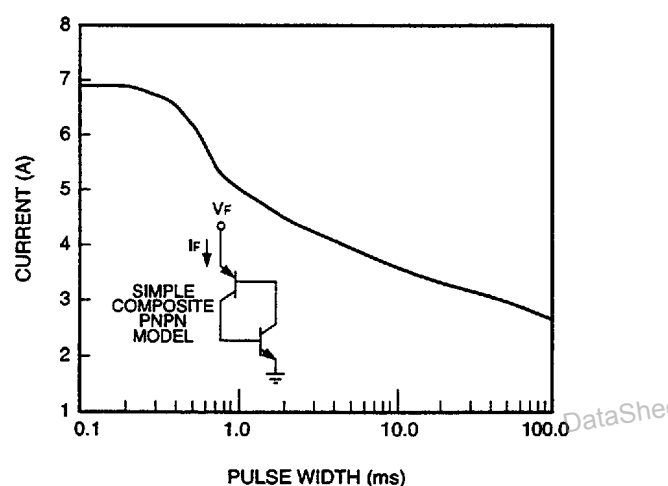
12-1872 (C)

Figure 10. Maximum Applied Forward Surge Limits (PNPN Composite Device)
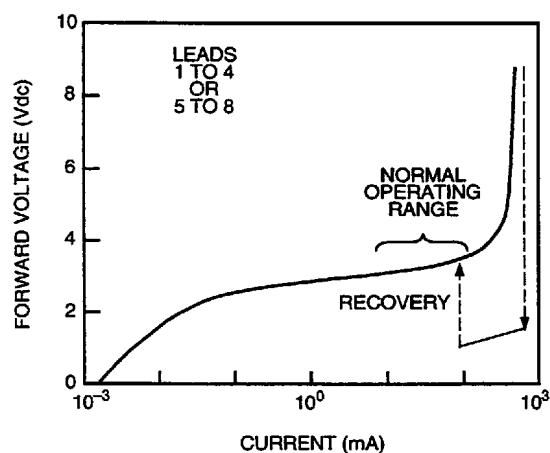
12-1873 (C)

Figure 11. Typical Voltage vs. Current (PNPN Composite Device)

Applying the LB1011AB

Theory of Operation

The LB1011AB will supply dc current to a telephone subscriber line without interfering with the ac signals on that line. This circuit has a constant dc voltage drop and is provided with surge protection. It has been integrated as two complementary chips to supply direct current to a balanced line or a current of either polarity to an unbalanced line. In the balanced-line mode, this circuit helps suppress common-mode signals. Connections for the balanced-line operation are outlined in Figure 1. This document describes some of the more important parameters of the SLIC function and component selection.

Referring to Figure 1, each LB1011AB stage feeding the line is a Darlington connection. The Darlington is driven by an amplifier whose input is a tap on a voltage divider. This input part of the circuits is designed to maintain a relatively constant dc voltage across each half of the device. The tap connections permit an external resistor (RTP, RTN) to raise the voltage drop across each half of the device from 3 V to 4 V. Such an increase can be desirable to reduce distortion at low operating temperatures or at peak signal voltages exceeding 2.5 V.

Since the dc voltage across the device is relatively constant, the current supplied to the line is controlled by the supply voltage, the external resistors to the supply, and the resistance shunting the line. For ac signals, however, the bases of the TAP transistors in each of the circuits are capacitively coupled together. Differential signals on the line do not disturb virtual ac ground at the center of this connection so both circuits act as constant-current sources thereby presenting a high-shunt impedance on the line. This cross coupling does not affect feedback for longitudinal signals, so for common-mode noises, the two circuits act as low-impedance paths to ground through the resistors connected to the supply voltages.

Component Selection

Feed Resistors

Feed resistor RP1 and RN1 are chosen to set the loop current. The loop current is given by:

$$I_{LOOP} = \frac{V_{BAT} - 2 \cdot V_{DC}}{R_{LOOP} + (RP1 + RN1)}$$

Here, V_{DC} is the typical drop across each half-circuit of the SLIC. For normal signal-level applications, the values for the LB1011AB device are 3 V. R_{LOOP} is the resistance of the twisted pair, neglecting the drop across the telephone set. Knowing the range of these parameters, the feed resistors can then be selected to provide the desired range of loop current. For this example, 370 Ω is chosen to limit the short-circuit loop current to 57 mA with a 48 V battery. Figure 12 shows the resulting dc characteristics.
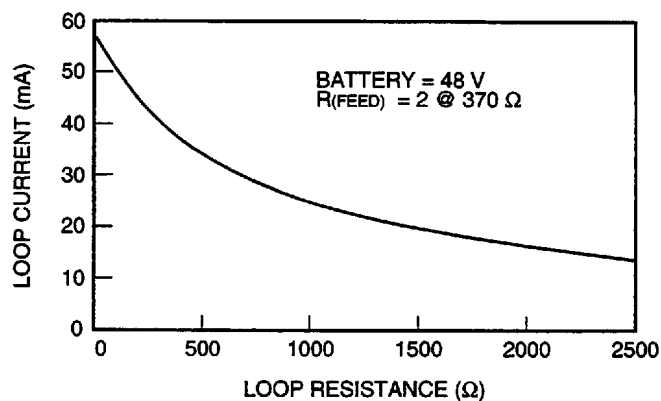
12-1855 (C)

Figure 12. Feed Current vs. Loop Resistance

A major consideration concerning feed resistor selection is common-mode rejection, also known as longitudinal balance. When two feed resistors are well matched, the circuit provides excellent rejection of common-mode loop signals. This relationship for a typical device is outlined in Figure 13.
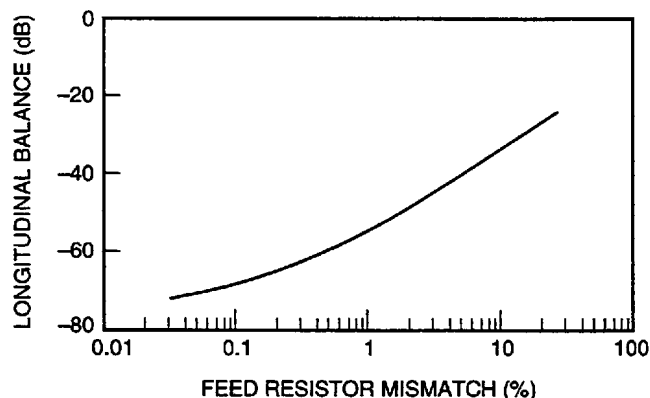

12-1856 (C)

Figure 13. Longitudinal Balance vs. Feed Resistor Mismatch

Applying the LB1011AB

Cross-Coupling Capacitor

The cross-coupling capacitor (C_{c1}) is used to provide the high ac impedance between the TIP and RING pins (4 and 5 respectively). In most applications, a 47 nF capacitor results in a very good performance. Higher values can be used to increase the ac impedance at lower frequencies, providing better return loss. The use of a 1 kΩ resistor in series with C_{c1} is recommended for surge protection purposes. Figure 14 illustrates the impedance as a function of frequency.
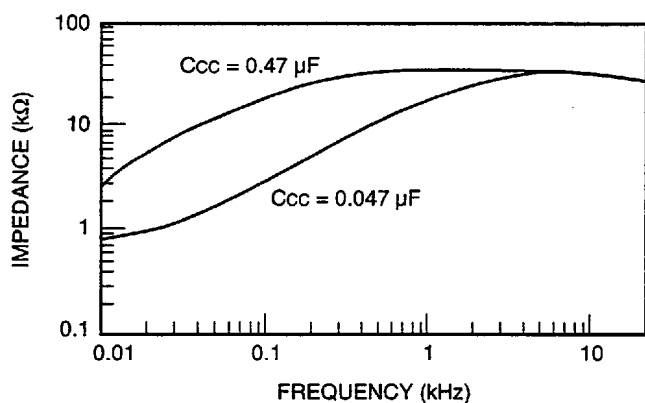
12-1857 (C)

Figure 14. Shunt Impedance vs. Frequency

Performance Highlights

Longitudinal Balance

When applied with well-matched feed resistors, the LB1011AB device provides excellent common-mode rejection, typically exceeding −55 dB over the entire voice band. The frequency dependence is shown in Figure 15.
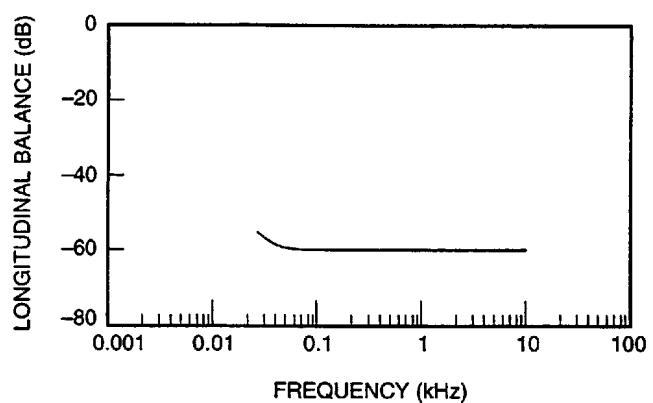
12-1858 (C)

Figure 15. Longitudinal Balance vs. Frequency

Performance Highlights (continued)

Return Loss

Referring to Figure 16, the return loss is defined as:

$$\text{Return Loss} = -20 \bullet \log \frac{Z - Z_{REF}}{Z + Z_{REF}}$$

where Z_{REF} is 600 Ω, and Z is the impedance of Z_{REF} in parallel with pins 4 and 5 of the LB1011AB. The performance is shown in Figure 17.

12-1859 (C)
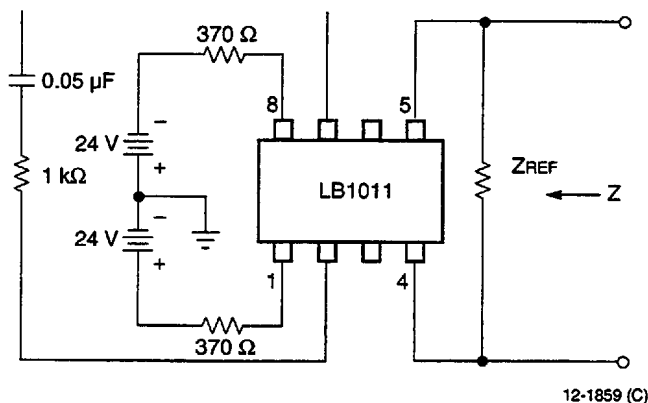
Figure 16. Return Loss Test Circuit

12-1860 (C)

Figure 17. Return Loss vs. Frequency

Distortion

By shorting pins 2 to 3 and 6 to 7, the nominal voltage drop across each half of the device is increased by 1 V, which increases the undistorted peak level. Figure 18 shows the typical distortion characteristics for both options over a broad range of line current.

12-1861 (C)

Figure 18. LB1011AB Distortion vs. Signal Level

Outline Diagram

Controlling dimensions are in millimeters.

8-Pin DIP

PIN #1 IDENTIFIER ZONE

SEATING PLANE

0.38 MIN

2.54 TYP   0.023 MAX

W
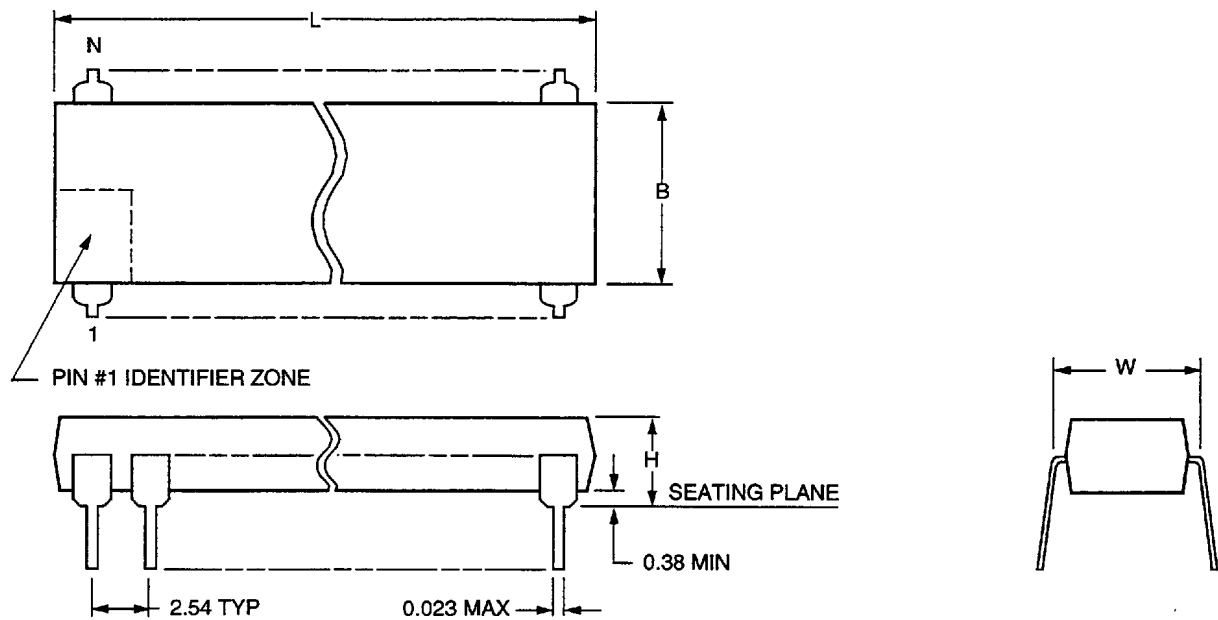
Package Description	Number of Pins (N)	Package Dimensions			
		Maximum Length (L)	Maximum Width Without Leads (B)	Maximum Width Including Leads (W)	Maximum Height Above Board (H)
PDIP3 (Plastic Dual-In-Line Package)	8	10.16	6.48	7.87	5.46

5-4410F

Ordering Information

Device Part No.	Description	Package	Comcode
LB1011AB	General-Purpose SLIC	8-Pin DIP	104208814

March 1997

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